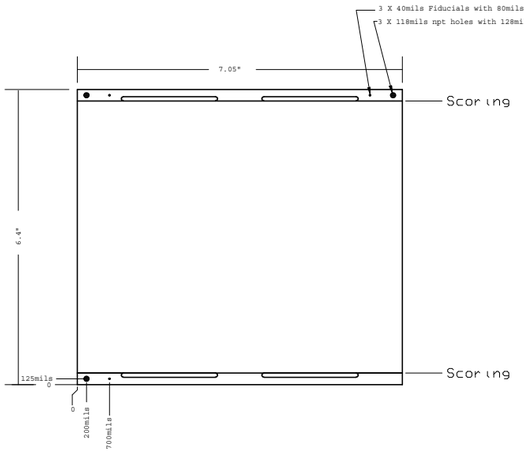
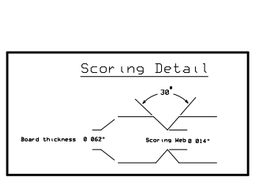
NOTES: (UNLESS OTHERWISE SPECIFIED)
THIS FAB SHOULD BE "RoHS COMPLIANT".

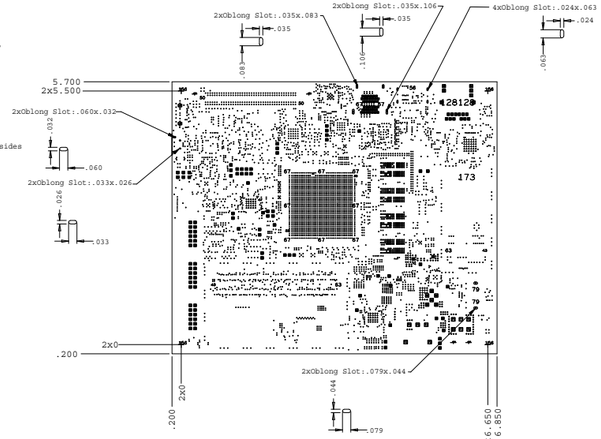
1. FABRICATE TO IPC-A-600, CURRENT REVISION
2. BOARD SHALL MEET THE INSPECTION CRITERIA OF
   a- ACCEPTABILITY AS PER IPC-A-600 (LATEST REVISION) CLASS II
   b- QUALIFICATION AND PERFORMANCE AS PER IPC-6012 (LATEST REVISION) CLASS II.
3. MATERIAL:ISOLA FR408HR (RoHS COMPLIANT MATERIAL) OR EQUIVALENT. GLASS TRANSITION TEMPERATURE MUST MEET OR EXCEED THE TEMPERATURE EXHIBITED WITH HIGH TEMPERATURE PROCESSES ASSOCIATED WITH LEAD FREE ASSEMBLY.
4. APPLY SOLDER MASK OVER BARE COPPER (SMOBC) IAW IPC-SM-840, BOTH SIDES, USING LPI, COLOR GREEN.
5. LPI SOLDER MASK TAIYO PSR4000 (RoHS COMPLIANT MATERIAL) OR EQUIVALENT WILL BE USED ON BOTH SIDES.
6. SOLDER MASK REGISTRATION TO BE WITHIN DIAMETRICAL TRUE POSITION OF + / - 0.002"WITH APPLICABLE HOLE / PAD.
7. FINISH: GOLD IMMERSION.
8. SILKSCREEN USING WHITE - HAVEN PC421 (NON-CONDUCTIVE OR EQUIVALENT RoHS COMPLIANT MATERIAL) BOTH SIDES DISTORTION OF SILKSCREEN IS ACCEPTABLE OVER TRACES. EPOXY INK ON SOLDER LANDS IS NOT ACCEPTABLE.
9. VENDOR LOGO AND DATE CODE TO BE MARKED SOLDER SIDE IN SILKSCREEN. MAXIMUM HEIGHT 0.12 INCHES.
10. 100% ELECTRICAL TEST REQUIRED FOR CONTINUITY. BOARD SHALL HAVE A UL-RATING OF 94V-0. UL SYMBOL AND RATING SHALL BE MARKED SOLDER SIDE IN SILKSCREEN.
11. REMOVE ALL UNUSED PADS FROM INTERNAL LAYERS.
12. 274X GERBER/ODB++ USED FOR FAB MUST BE VERIFIED AGAINST THE PROVIDED IPC356 NETLIST. COPPER SLIVERS THAT ARE LESS THAN 0.003" IN WIDTH BETWEEN ANTI-PAD TO PLANE EDGE, ANTI-PAD TO SPLIT PLANE AND ANTI-PAD TO ANTI-PAD MUST BE REMOVED FROM THE MANUFACTURING ARTWORK. A NETLIST COMPARISON MUST BE PASSED WITH NO VIOLATION AFTER THE REMOVAL OF SLIVERS. ANY REQUIREMENT FOR SLIVER REMOVAL ABOVE OR EQUAL TO THE 0.003" COPPER WIDTH MUST BE ADDRESSED AND APPROVED IN WRITING BY SUPPLIER.
13. VIAS ARE SUPPOSED TO BE DIRECTLY CONNECTED TO RESPECTIVE PLANE.
14. FOR IMPEDANCE CONTROL DETAILS REFER TO STACK-UP DOCUMENT INCLUDED ZCU106_HR408BUILD.pdf DATA.
15. VIA IN PAD TECHNOLOGY USED:
    VIA FILL IS REQUIRED: THIS IS A VIA IN PAD JOB. ALL VIA IN PAD LOCATIONS,LISTED IN "VIA_EPOXY_TOP" AND "VIA_EPOXY_BOT"MUST BE COMPLETELY FILLED" WITH PETERS PP-2795 OR EQUIVALENT 100% SOLIDS FILL MATERIAL, PLANARIZED, AND PLATED OVER WITH" COPPER AND SURFACE FINISH.
16. ALL VIA DRILLS LISTED IN "VIA_PLUG_TOP AND VIA_PLUG_BOT" MUST BE PLUGGED AND COVERED WITH SOLDER MASK.
17. PCB VENDOR IS ALLOWED TO ADD COPPER THIEVING TO ALL INTERNAL SIGNALS LAYERS. DISTANCE FROM EXISTING FEATURES MUST BE 100 MILS MINIMUM.
18. INTENTIONAL SHORT: SEE HW-Z1-ZCU104_REVC_SHORTS_LIST.DOC

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
B	PROTOTYPE	08/30/17	
B	PROTOTYPE	08/30/17	
C	PROTOTYPE	11/27/17	
1.0	PROTOTYPE	02/10/18	
01	PROTOTYPE	02/08/18	

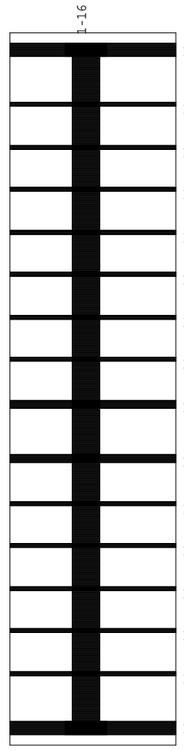




Array size X = 7.05" Y = 6.4"
Rail area 250mils including routing tab



DRILL CHART: TOP to BOTTOM ALL UNITS ARE IN MILS					
FIGURE	FHS	TOLERANCE	PLATED	QTY	ADDITIONAL
•	8.0	+0.0/-8.0	PLATED	473	
•	9.0	+0.0/-9.0	PLATED	1456	
•	10.0	+0.0/-10.0	PLATED	3132	
•	12.0	+0.0/-12.0	PLATED	239	
*	22.0	+3.0/-3.0	PLATED	38	
*	35.0	+3.0/-3.0	PLATED	12	
*	40.0	+3.0/-3.0	PLATED	98	
*	48.0	+3.0/-3.0	PLATED	6	
*	50.0	+3.0/-3.0	PLATED	5	
*	62.0	+3.0/-3.0	PLATED	2	
*	71.0	+3.0/-3.0	PLATED	6	
*	73.0	+3.0/-3.0	PLATED	5	
*	106.0	+3.0/-3.0	PLATED	2	
*	125.0	+3.0/-3.0	PLATED	2	
*	156.0	+3.0/-3.0	PLATED	4	
*	33.0	+2.0/-2.0	NON-PLATED	2	
*	40.0	+2.0/-2.0	NON-PLATED	2	
*	43.0	+2.0/-2.0	NON-PLATED	2	
*	50.0	+2.0/-2.0	NON-PLATED	2	
*	56.0	+2.0/-2.0	NON-PLATED	1	
*	63.0	+2.0/-2.0	NON-PLATED	2	
*	67.0	+2.0/-2.0	NON-PLATED	10	
*	79.0	+2.0/-2.0	NON-PLATED	2	
*	128.0	+2.0/-2.0	NON-PLATED	2	
*	173.0	+2.0/-2.0	NON-PLATED	1	
•	33.0x26.0	+4.0/-4.0	PLATED	2	
•	60.0x32.0	+4.0/-4.0	PLATED	2	
•	63.0x24.0	+4.0/-4.0	PLATED	4	
•	79.0x44.0	+4.0/-4.0	PLATED	2	
•	83.0x35.0	+4.0/-4.0	PLATED	2	
•	106.0x35.0	+4.0/-4.0	PLATED	2	
TOTAL HOLES: 5520					



DESIGN CROSS SECTION CHART
TOTAL THICKNESS 61.19 MIL

TOTAL THICKNESS 61.19 MIL +/- 5 MIL (8%)

IMPEDANCE CHART

	SINGLE ENDED		EDGE-COUPLED DIFFERENTIAL		EDGE-COUPLED DIFFERENTIAL
	TRACE WIDTH	TARGET IMPEDANCE Z (OHMS)	TRACEWIDTH/AIRGAP	TARGET IMPEDANCE Z (OHMS)	TRACEWIDTH/AIRGAP	TARGET IMPEDANCE Z (OHMS)
TOP SIDE	11 MIL 10 MIL 8 MIL ~~11.5 MIL~~	36 39 50 ~~28~~	3.1 MIL/3 MIL 3.1 MIL/4.1 MIL 3.1 MIL/5.1 MIL 3.2 MIL/7.8 MIL 3.4 MIL/8.4 MIL	~~66~~ ~~72~~ ~~76~~ ~~86~~ ~~90~~ ~~100~~	~~4.4 MIL/3.1 MIL~~ ~~4.3 MIL/5 MIL~~ ~~5.2 MIL/7.8 MIL~~	~~66~~ ~~76~~ ~~100~~
LAYER 3	6.2 MIL 5.5 MIL 3.5 MIL	36 39 50	3 MIL/3 MIL 3.1 MIL/4.1 MIL 3.1 MIL/5.1 MIL 3.2 MIL/7.8 MIL 3.4 MIL/8.4 MIL	~~66~~ ~~72~~ ~~76~~ ~~86~~ ~~90~~ ~~100~~	~~4.4 MIL/3.1 MIL~~ ~~4.3 MIL/5 MIL~~ ~~5.2 MIL/7.8 MIL~~	~~66~~ ~~76~~ ~~100~~
LAYER 5	6.2 MIL 5.5 MIL 3.5 MIL	36 39 50	3 MIL/3 MIL 3.1 MIL/4.1 MIL 3.1 MIL/5.1 MIL 3.2 MIL/7.8 MIL 3.4 MIL/8.4 MIL	~~66~~ ~~72~~ ~~76~~ ~~86~~ ~~90~~ ~~100~~	~~4.4 MIL/3.1 MIL~~ ~~4.3 MIL/5 MIL~~ ~~5.2 MIL/7.8 MIL~~	~~66~~ ~~76~~ ~~100~~
LAYER 7	6.2 MIL 5.5 MIL 3.5 MIL	36 39 50	3 MIL/3 MIL 3.1 MIL/4.1 MIL 3.1 MIL/5.1 MIL 3.2 MIL/7.8 MIL 3.4 MIL/8.4 MIL	~~66~~ ~~72~~ ~~76~~ ~~86~~ ~~90~~ ~~100~~	~~4.4 MIL/3.1 MIL~~ ~~4.3 MIL/5 MIL~~ ~~5.2 MIL/7.8 MIL~~	~~66~~ ~~76~~ ~~100~~
LAYER 12	6.2 MIL 5.5 MIL 3.5 MIL	36 39 50	3 MIL/3 MIL 3.1 MIL/4.1 MIL 3.1 MIL/5.1 MIL 3.2 MIL/7.8 MIL 3.4 MIL/8.4 MIL	~~66~~ ~~72~~ ~~76~~ ~~86~~ ~~90~~ ~~100~~	~~4.4 MIL/3.1 MIL~~ ~~4.3 MIL/5 MIL~~ ~~5.2 MIL/7.8 MIL~~	~~66~~ ~~76~~ ~~100~~
LAYER 14	6.2 MIL 5.5 MIL 3.5 MIL	36 39 50	3 MIL/3 MIL 3.1 MIL/4.1 MIL 3.1 MIL/5.1 MIL 3.2 MIL/7.8 MIL 3.4 MIL/8.4 MIL	~~66~~ ~~72~~ ~~76~~ ~~86~~ ~~90~~ ~~100~~	~~4.4 MIL/3.1 MIL~~ ~~4.3 MIL/5 MIL~~ ~~5.2 MIL/7.8 MIL~~	~~66~~ ~~76~~ ~~100~~
BOTTOMD	11 MIL 10 MIL 8 MIL ~~11.5 MIL~~	36 39 50 ~~28~~	3.1 MIL/3 MIL 3.1 MIL/4.1 MIL 3.1 MIL/5.1 MIL 3.2 MIL/7.8 MIL 3.4 MIL/8.4 MIL	~~66~~ ~~72~~ ~~76~~ ~~86~~ ~~90~~ ~~100~~	~~4.4 MIL/3.1 MIL~~ ~~4.3 MIL/5 MIL~~ ~~5.2 MIL/7.8 MIL~~	~~66~~ ~~76~~ ~~100~~

CROSSED IMPEDANCE CALL OUTS DO NOT EXIST IN PROVIDED DATA. IGNORE THEM.

UNLESS OTHERWISE SPECIFIED	SIGNATURES		DATE
DIMENSIONS ARE IN INCHES	DRAWN	Rocket EMS	02-10-18
TOLERANCES ON;	CHECKED	Brian Forsse	
2 PL DECIMALS +/- .010	ENGRG	Brian Forsse	02-10-18
3 PL DECIMALS +/- .005	ISSUED		
ANGLES +			
FRACTIONS +			

XILINX.
2100 LOGIC DR.
SAN JOSE, CA 95124
HWCP - HARDWARE & CONFIGURATION PLATFORMS

FABRICATION DRAWING

HW-Z1-ZCU104

PCB,ROHS COMPLIANT

SIZE	FSCM NO	DWG NO	REV
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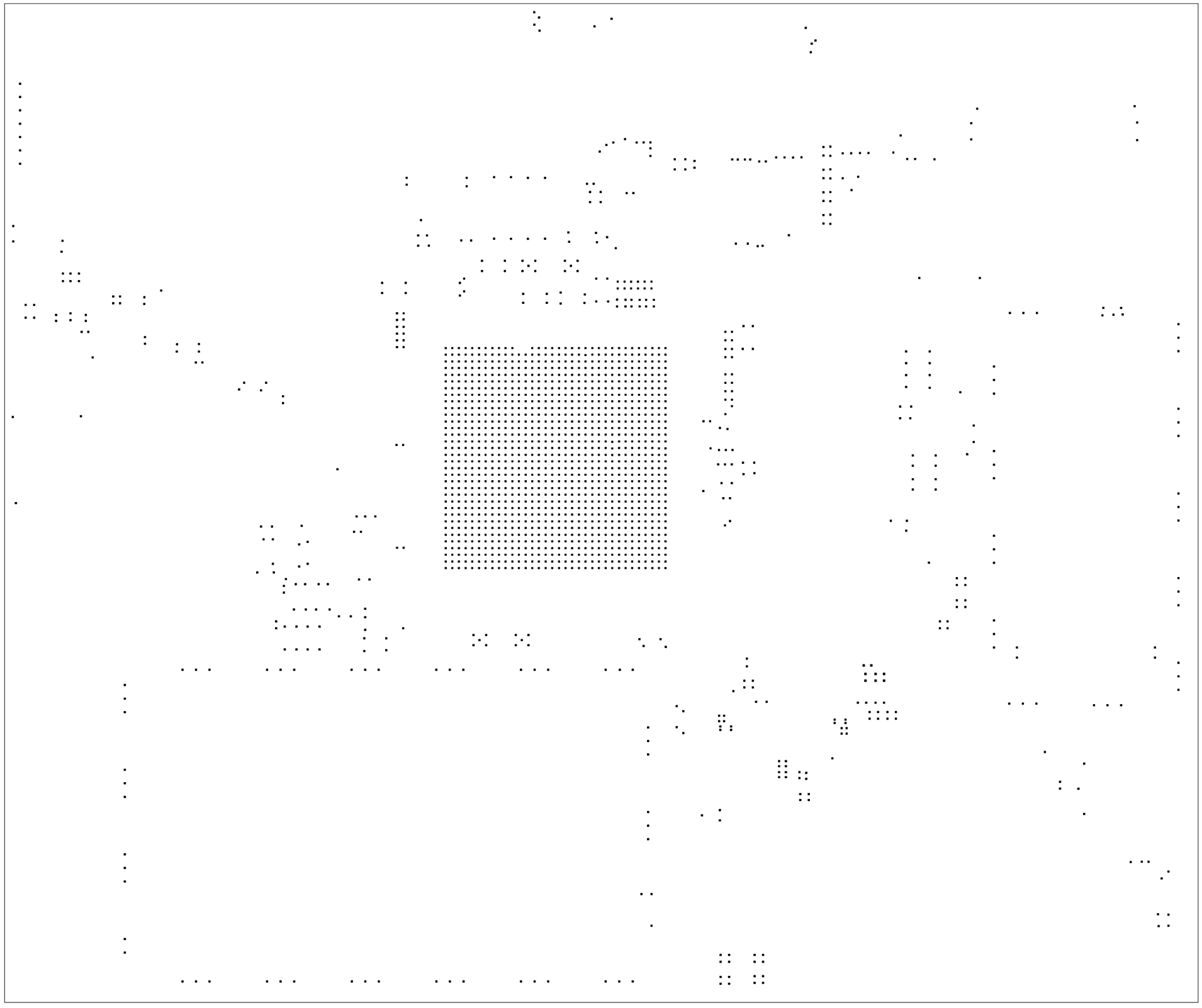
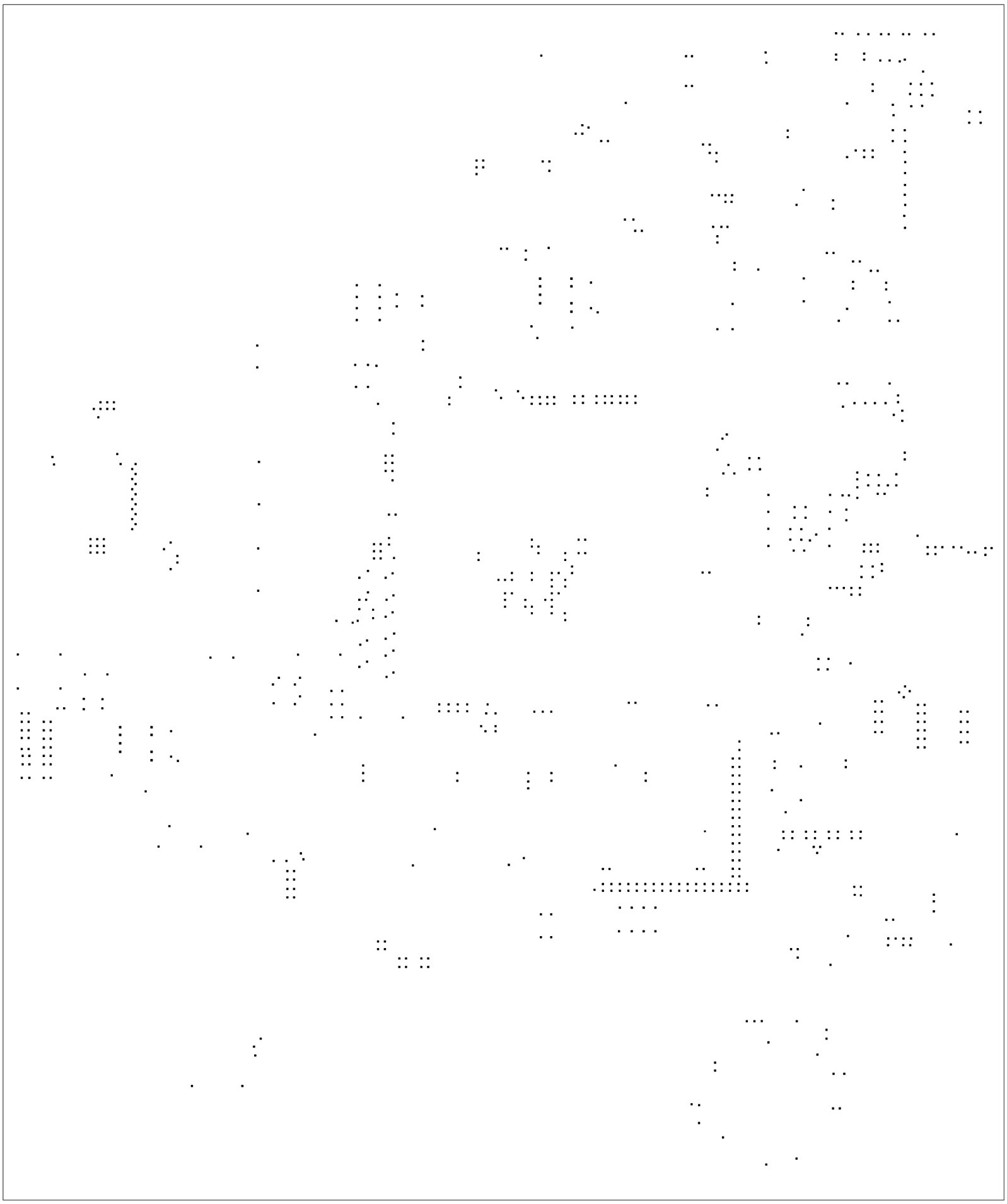
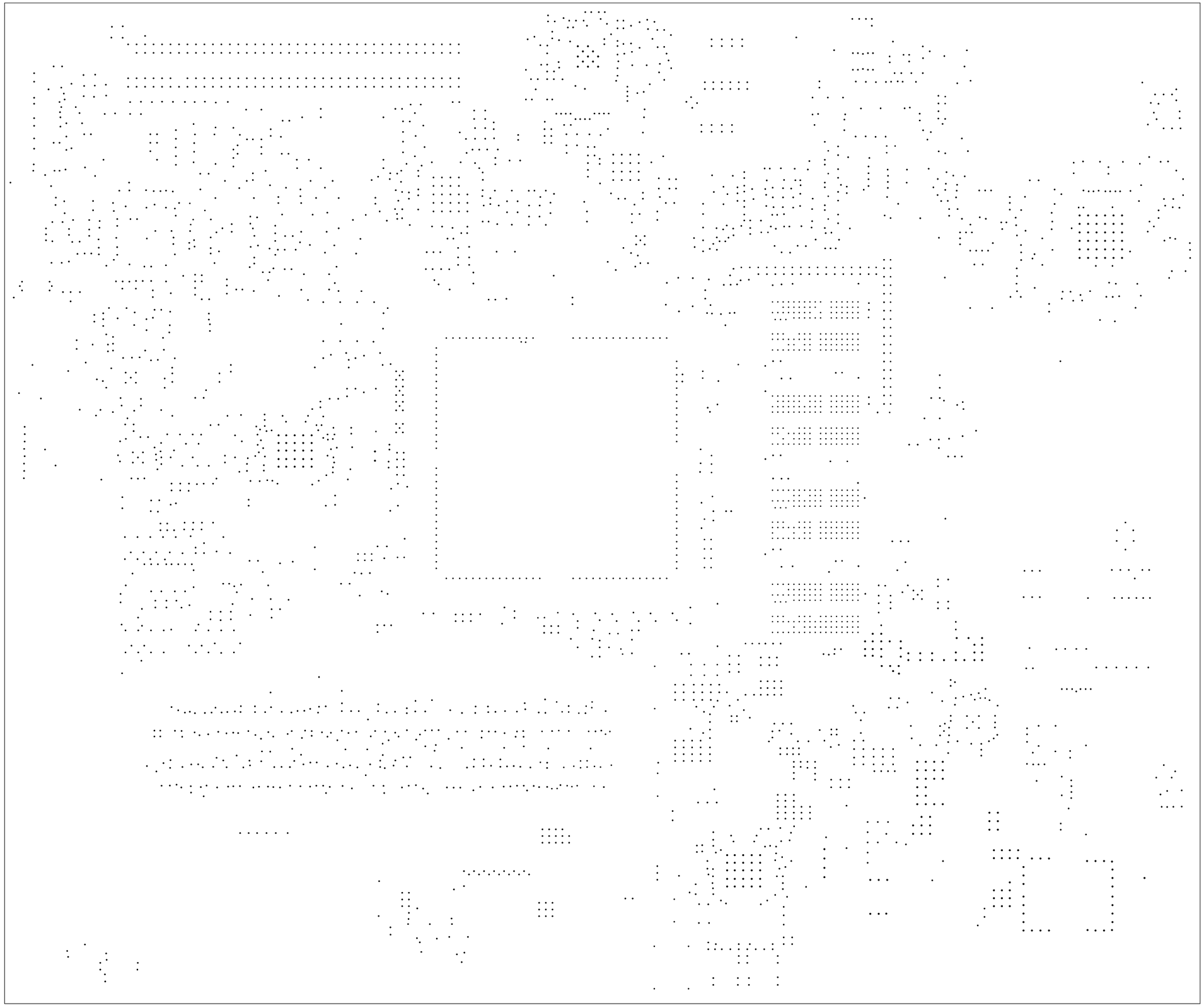
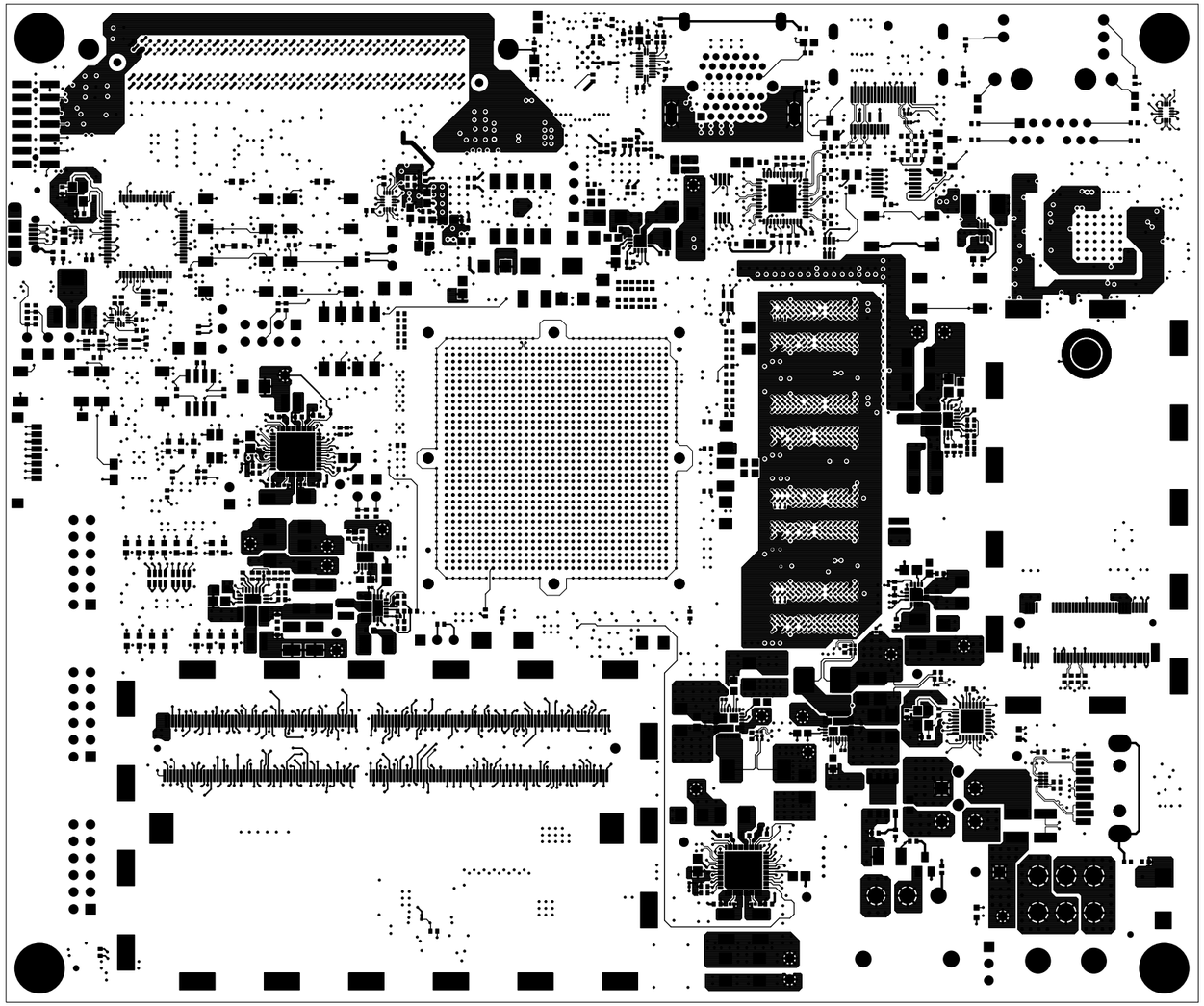
			VER: 1.0
SCALE NONE			SHEET 1 OF 1

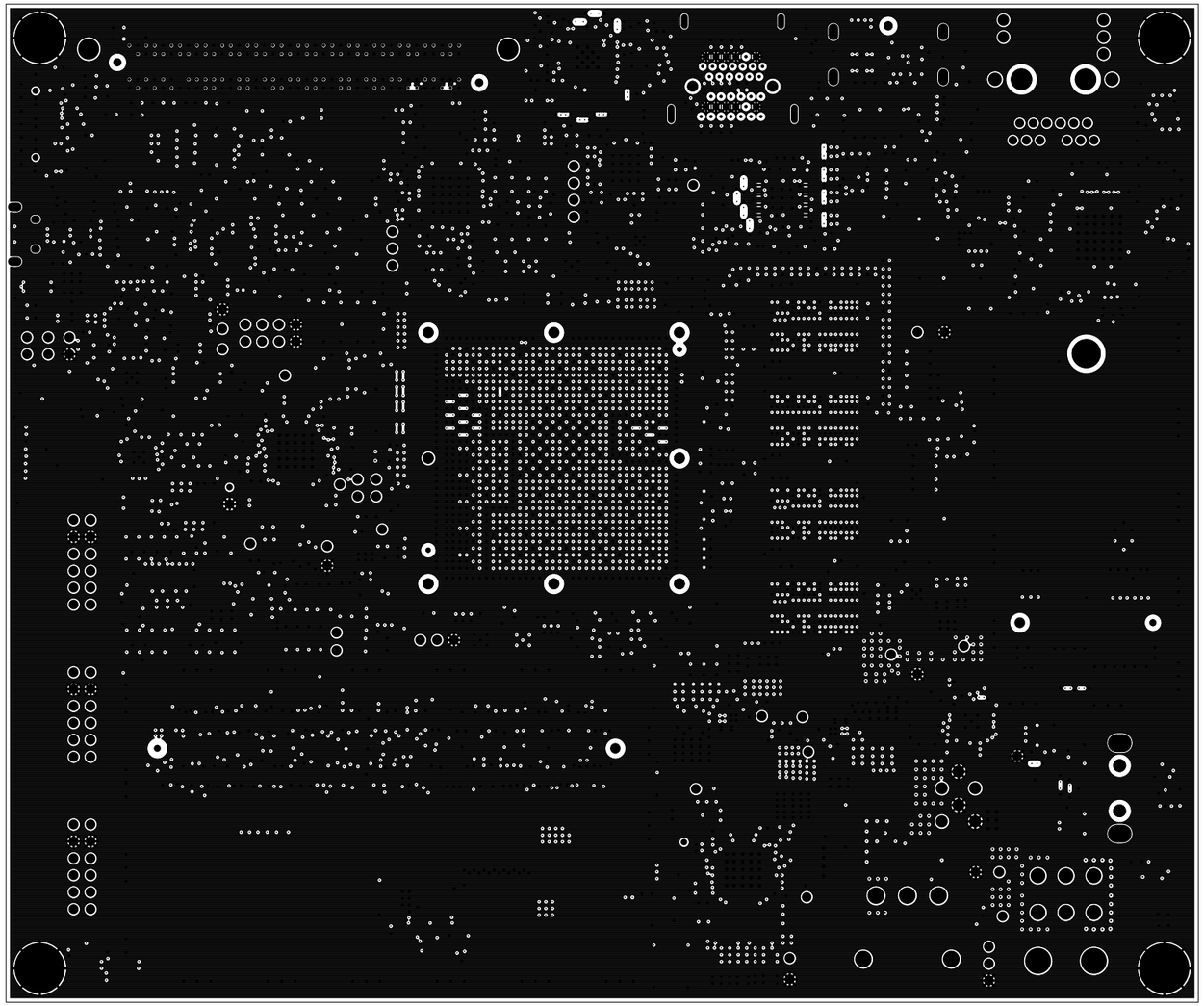




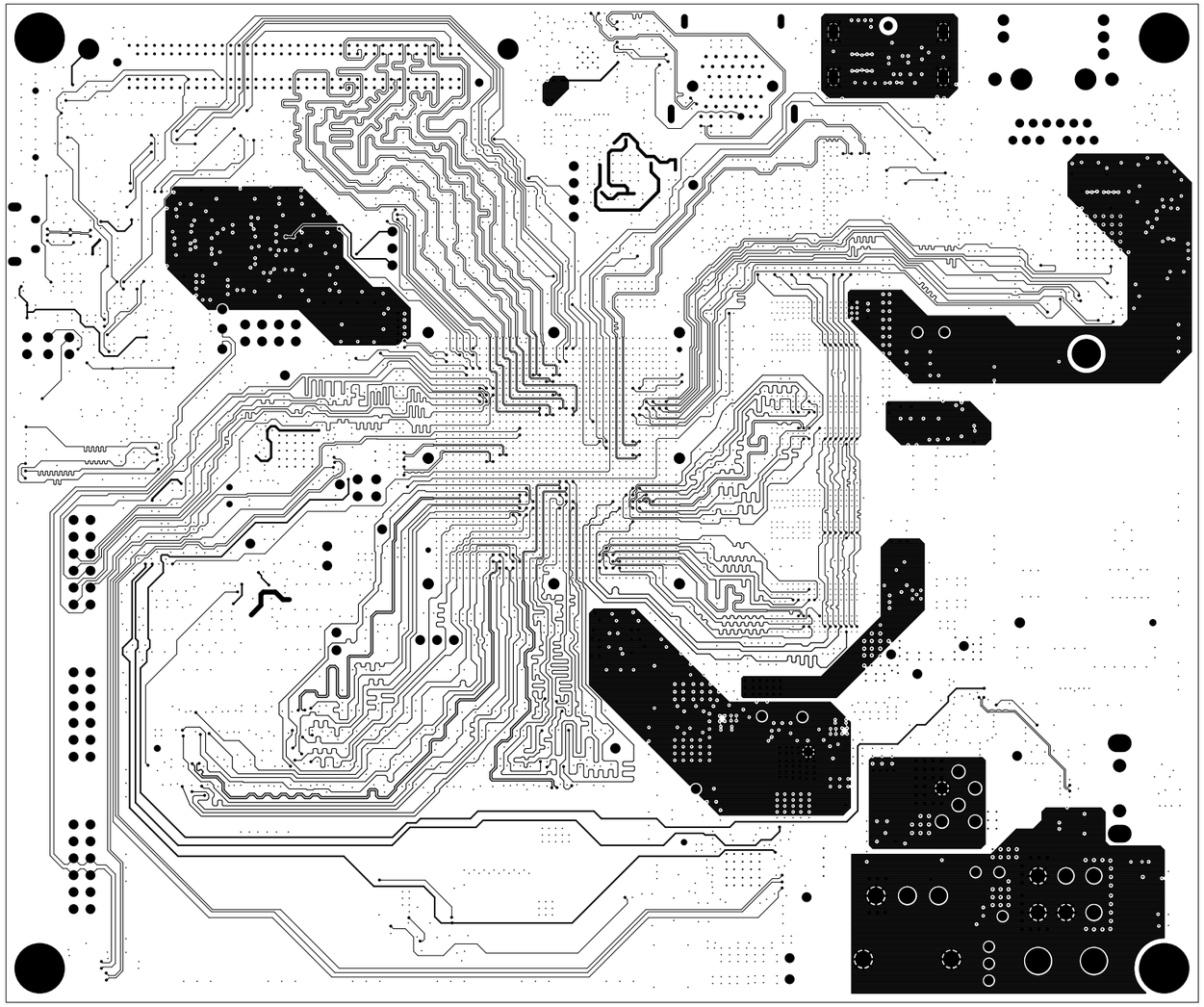




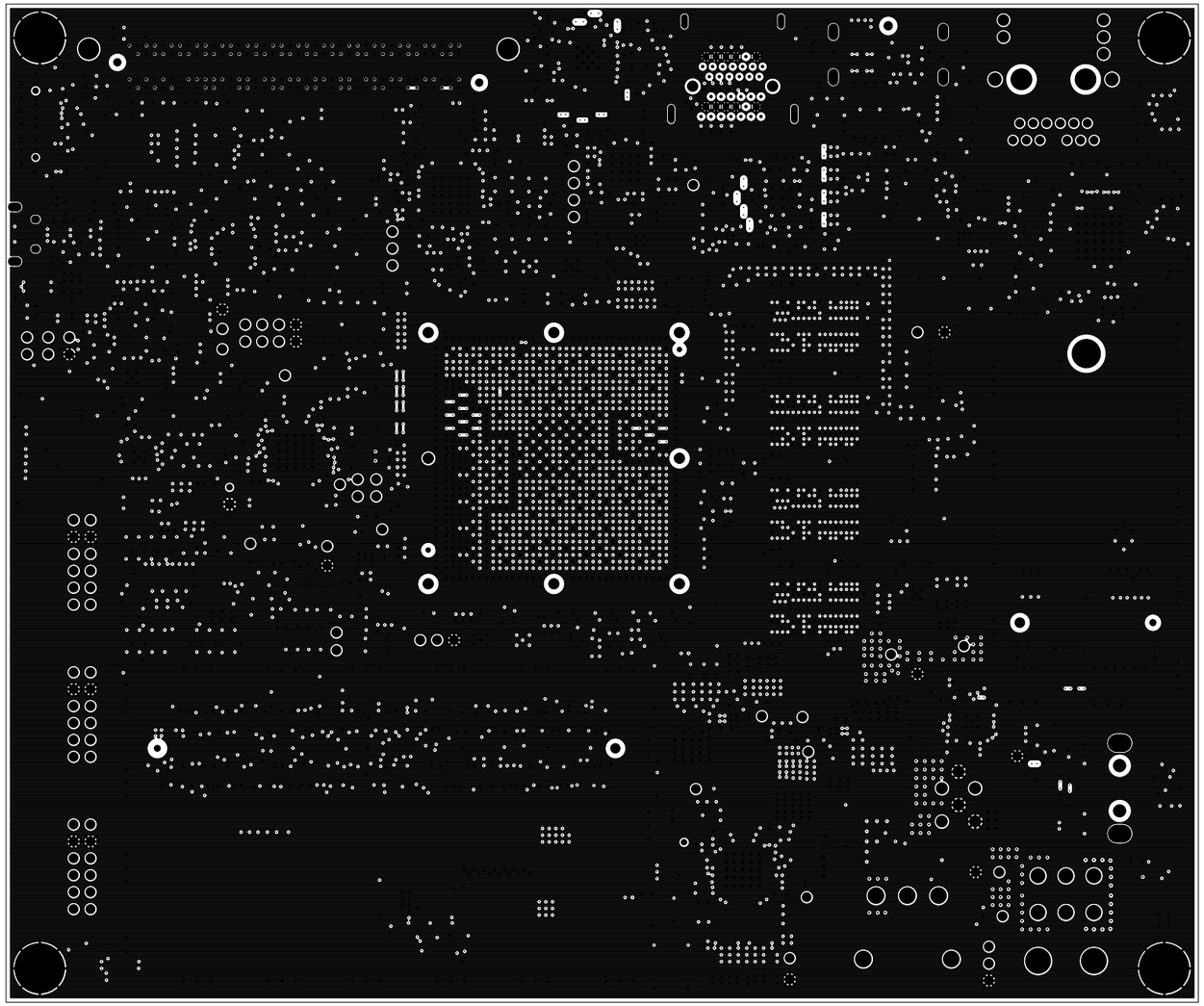
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 01 OF 22 LAYER: TOP	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 02 OF 22 LAYER: GND1	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 03 OF 22 LAYER: SIG1	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



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PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
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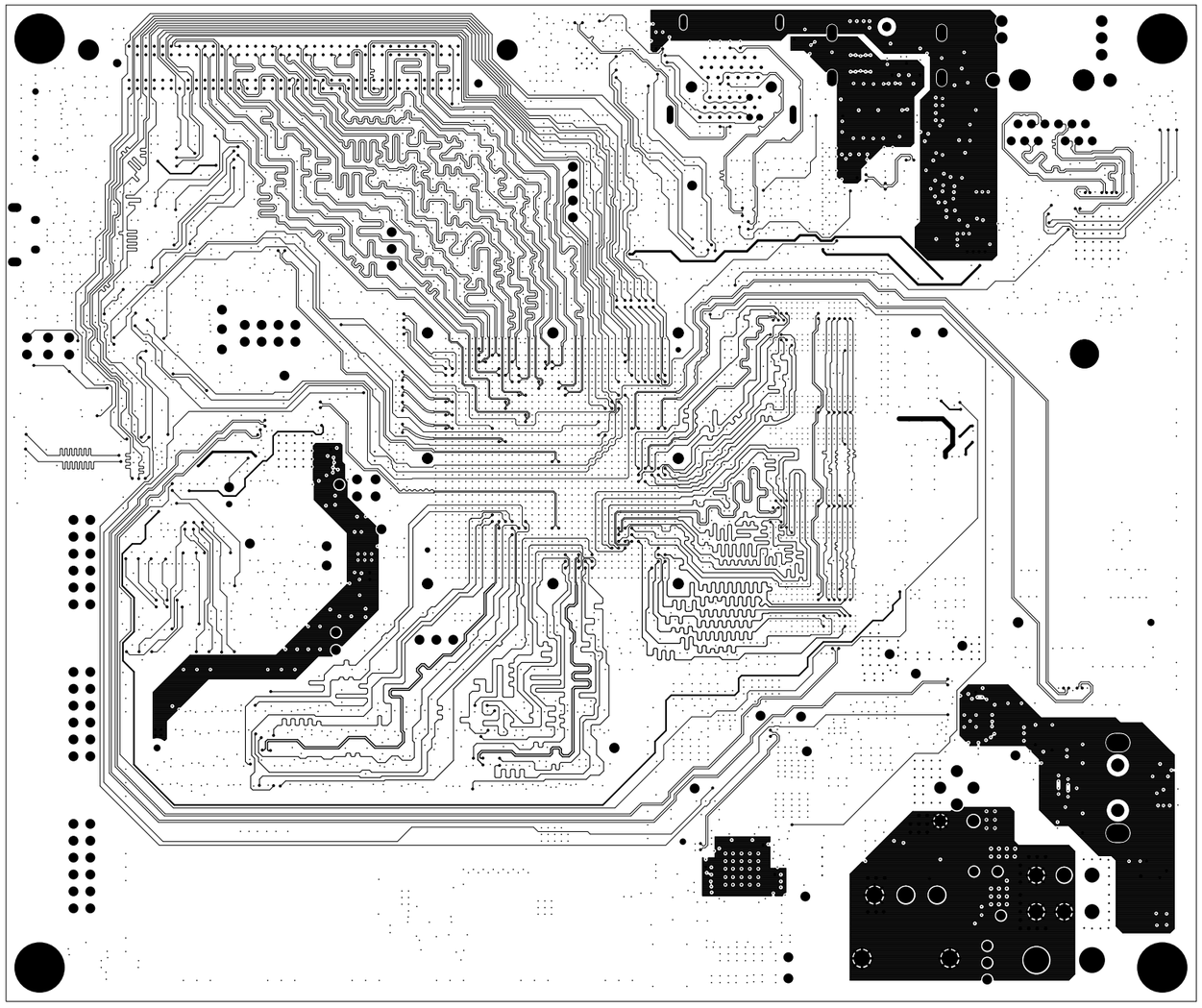

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PCB # 1280961	
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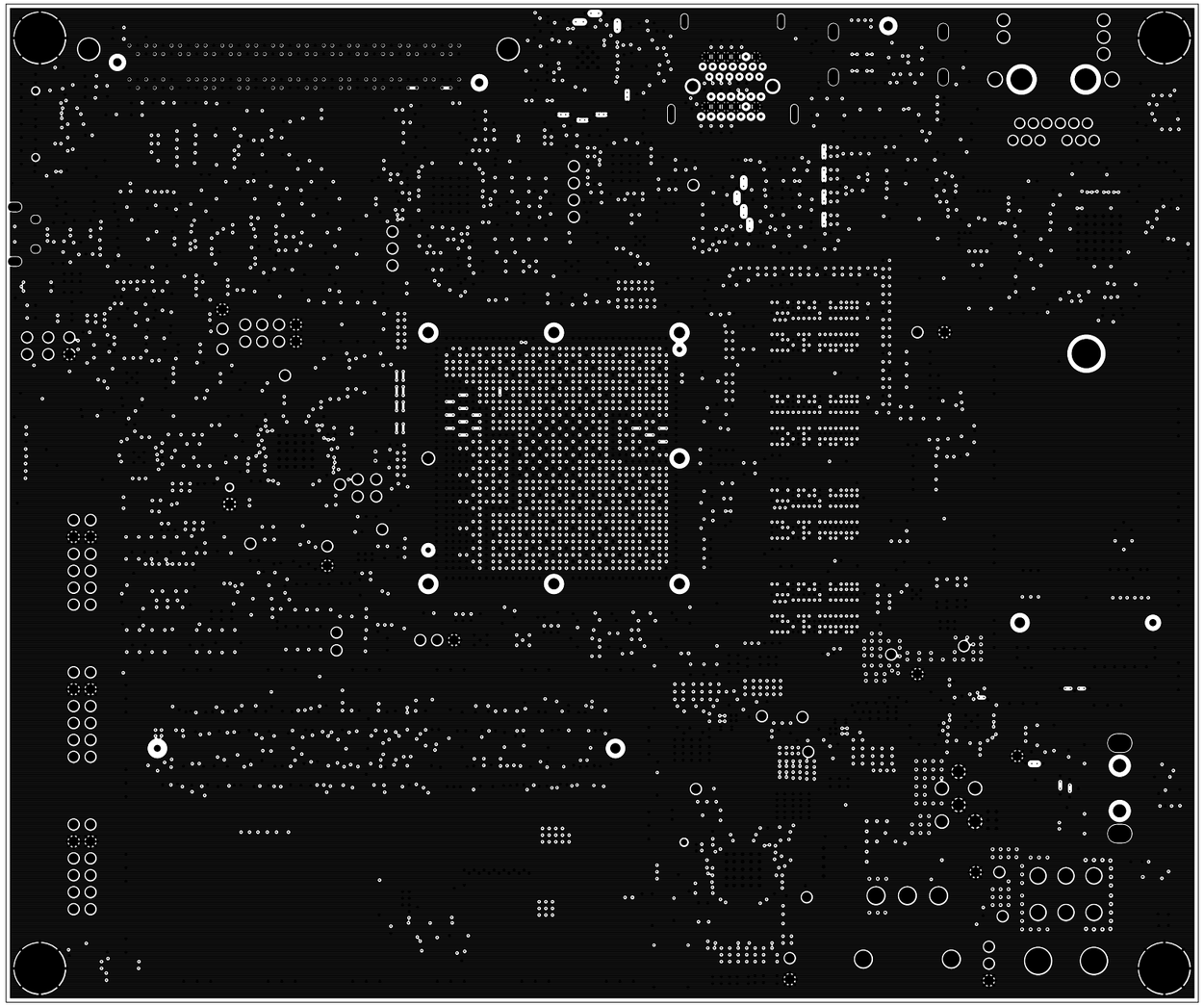

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PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
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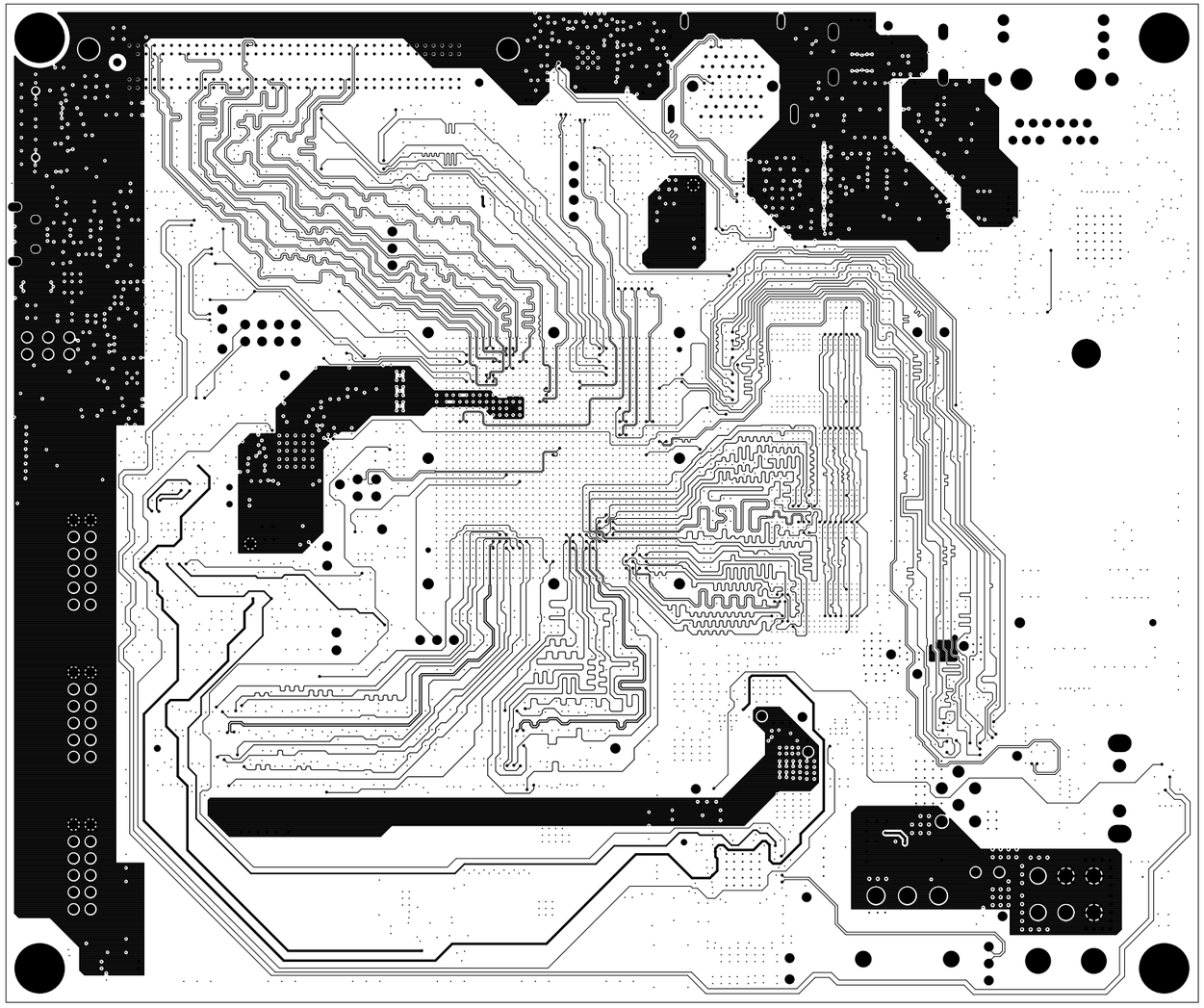

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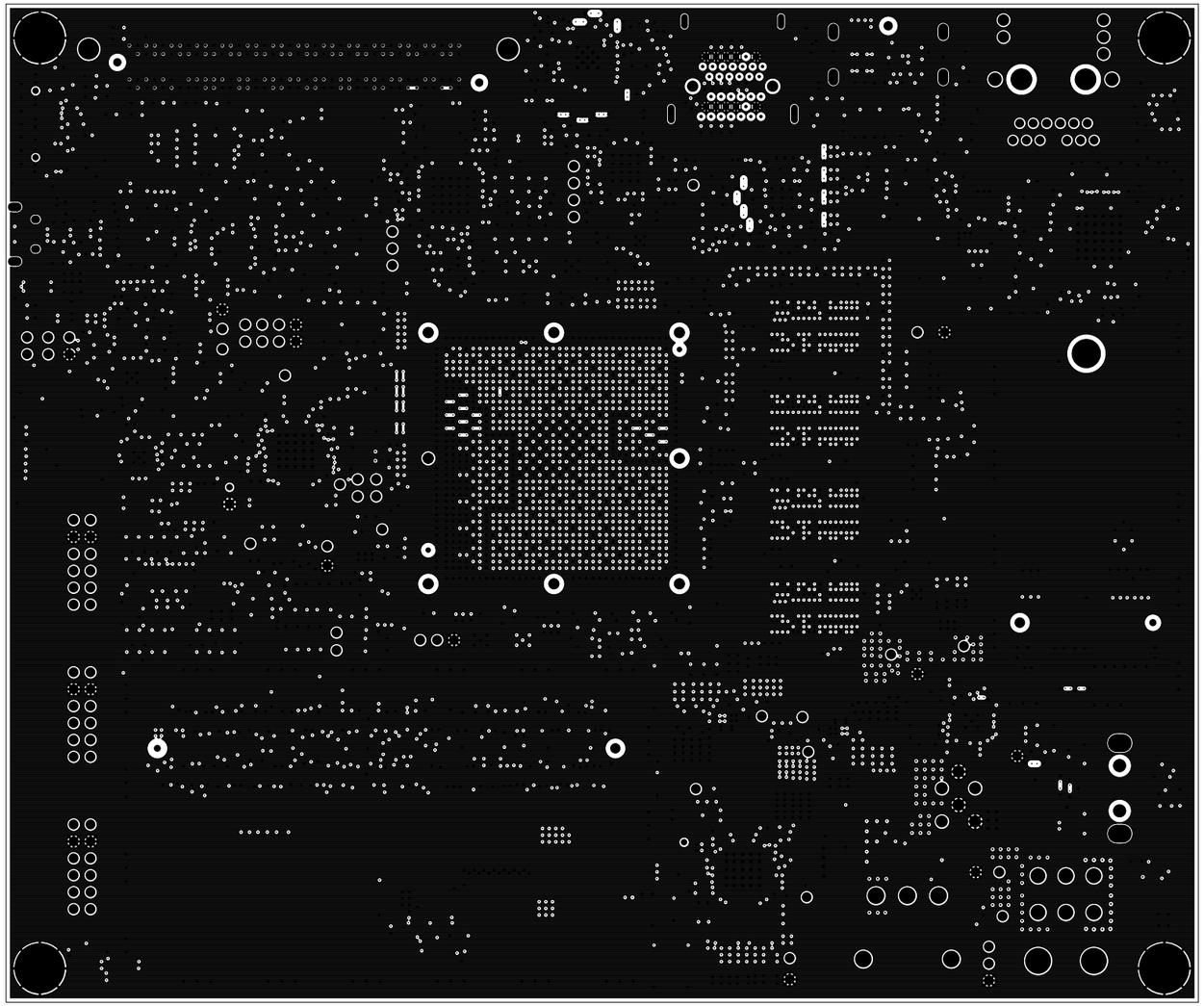
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 07 OF 22 LAYER: SIG3	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
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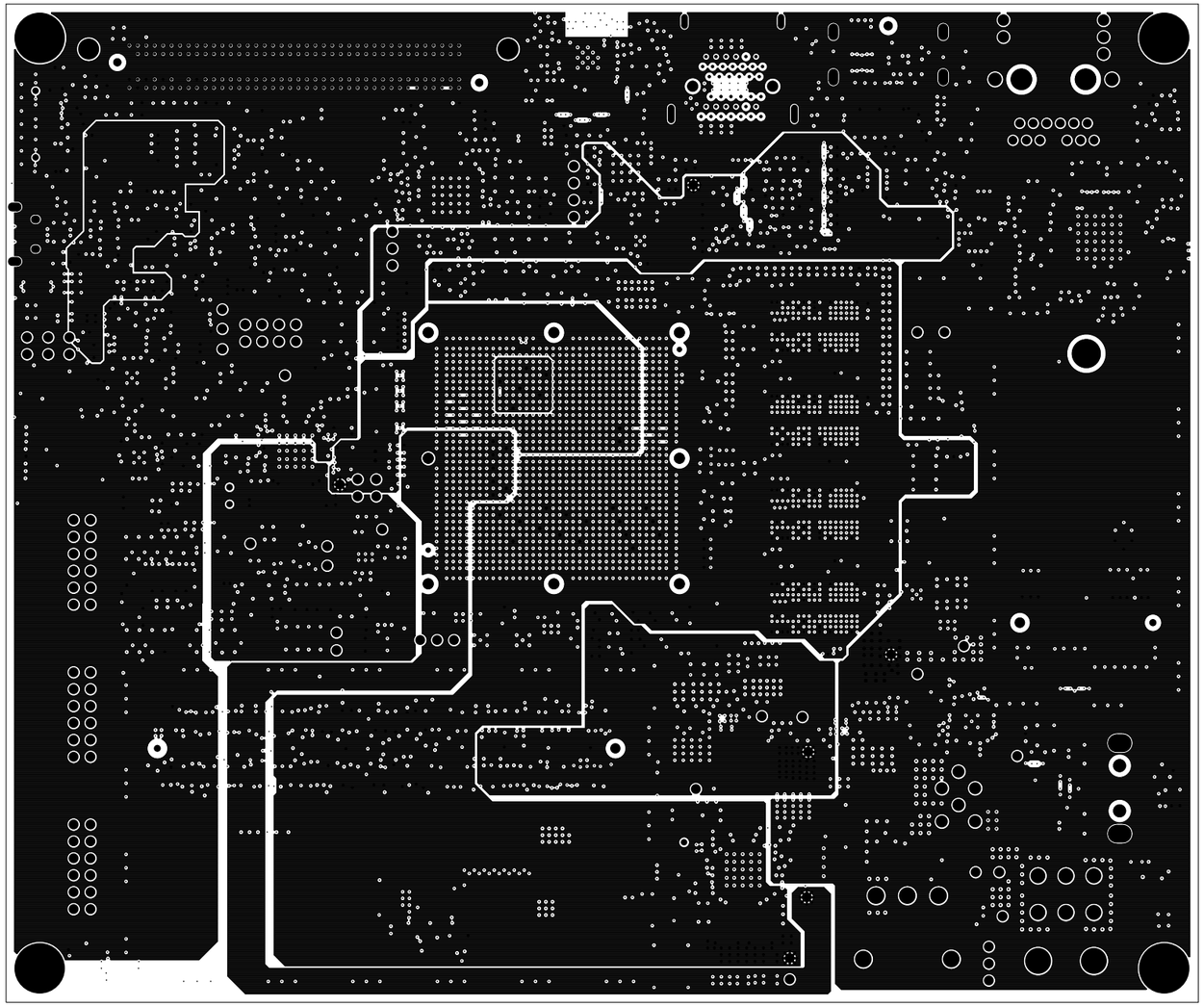

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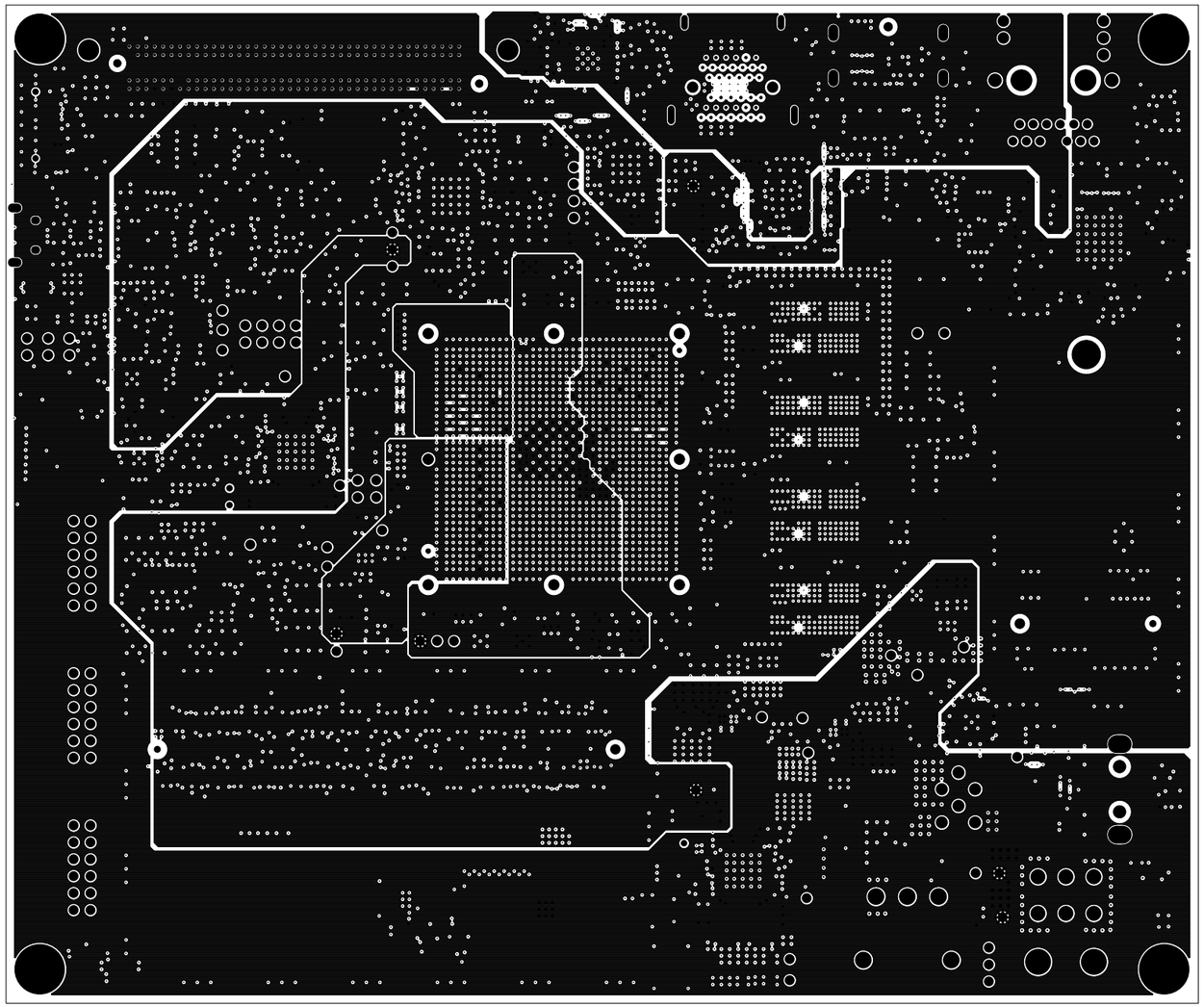
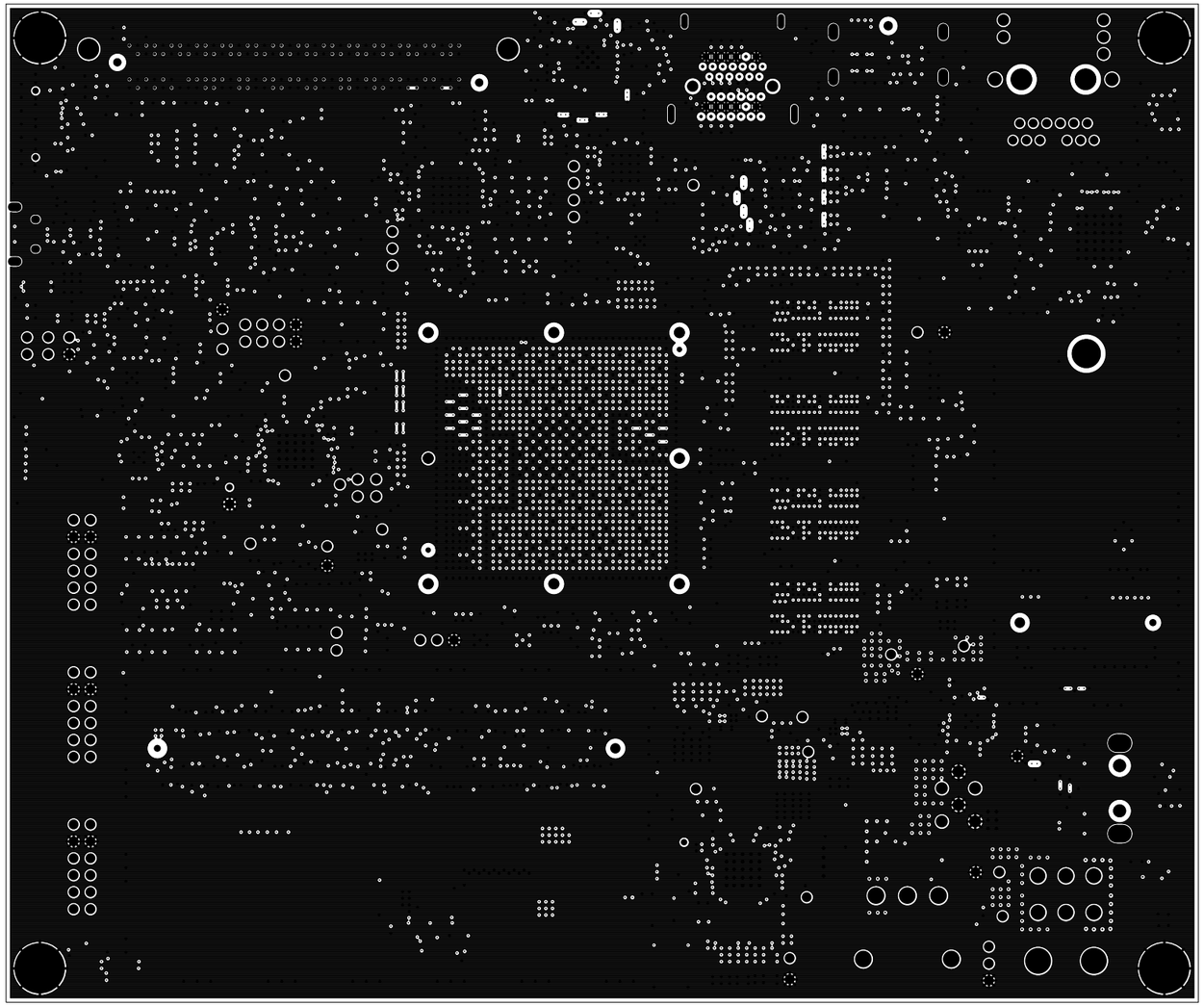
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 09 OF 22 LAYER: PWR1	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 10 OF 22 LAYER: PWR2	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



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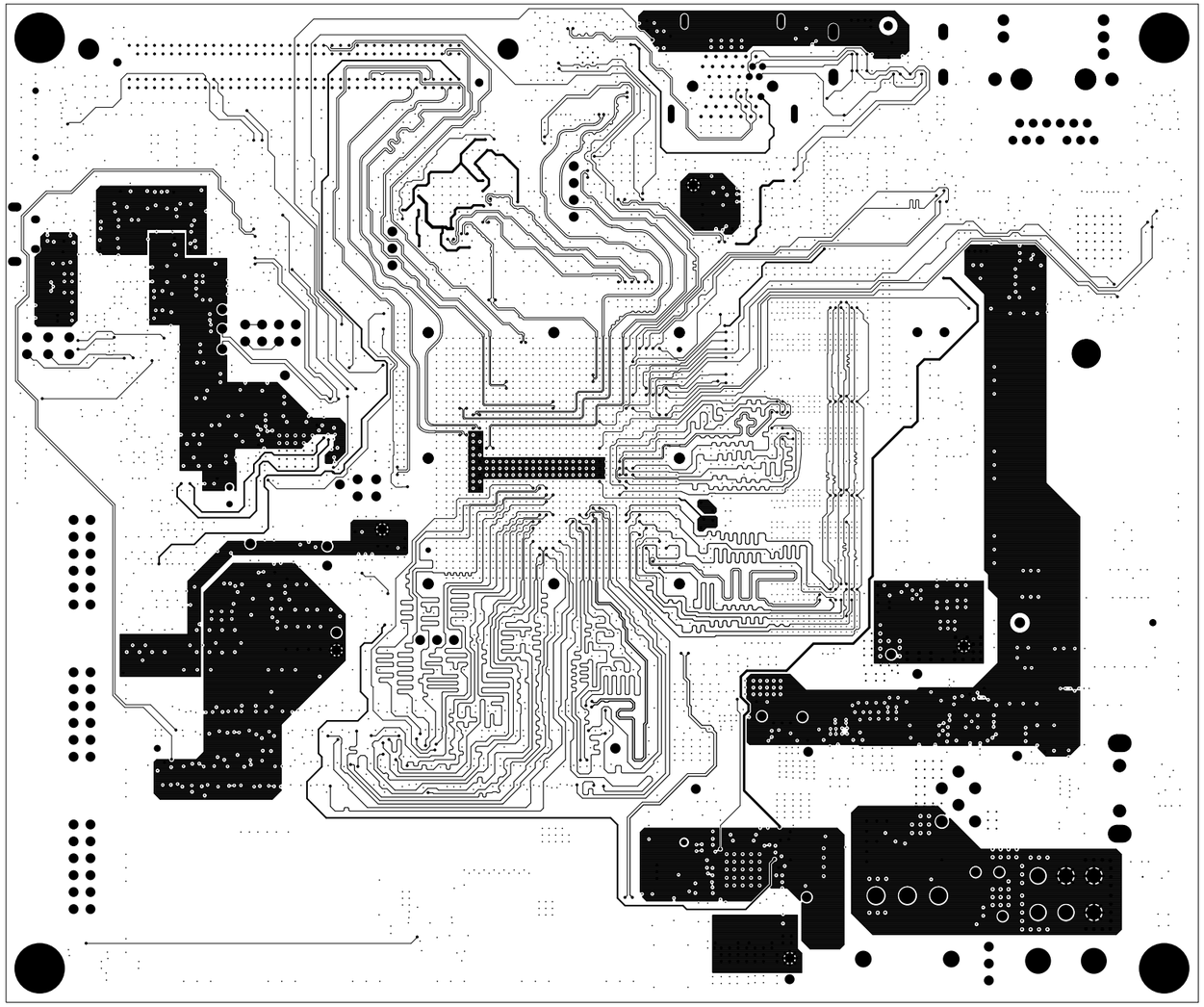
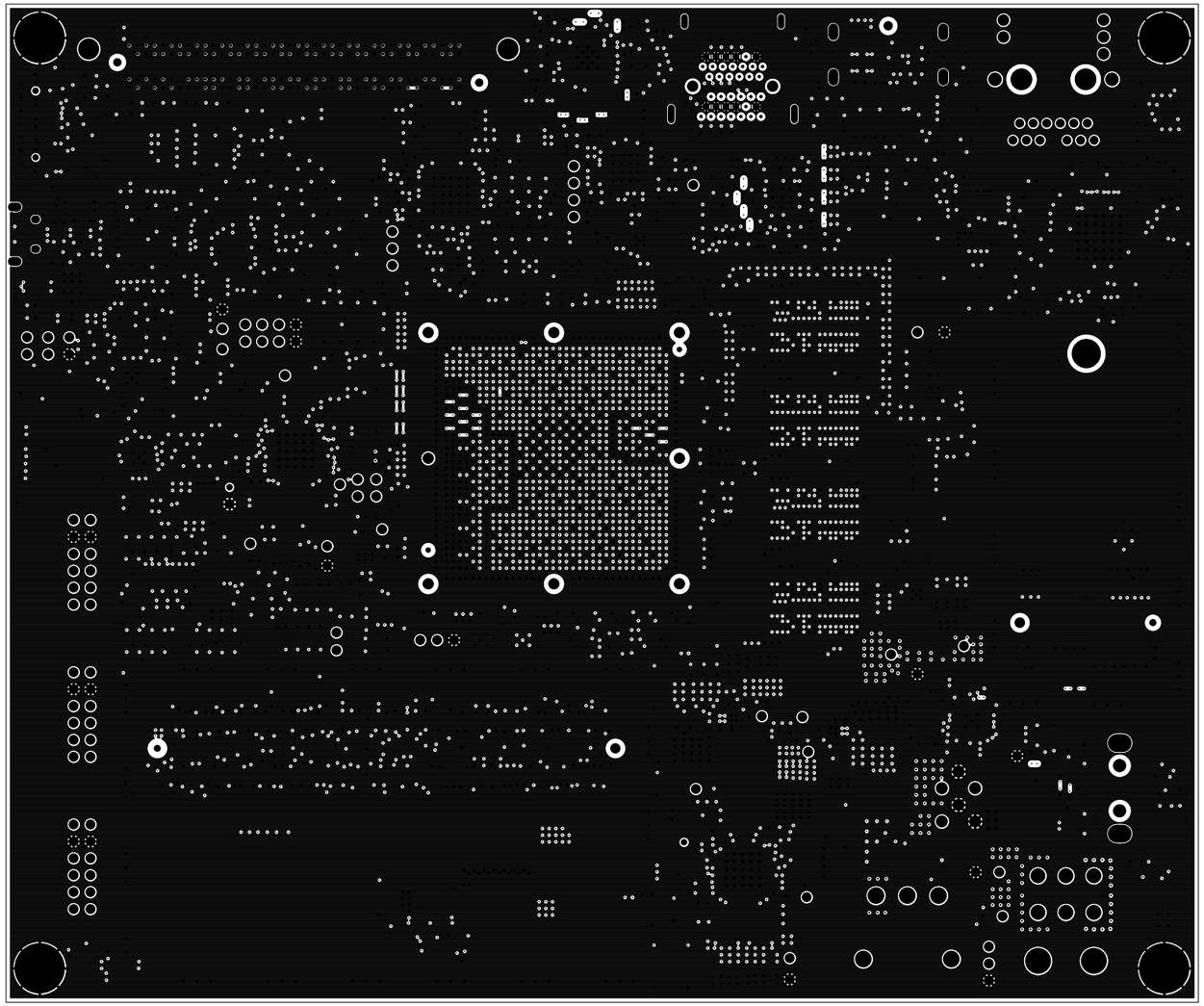
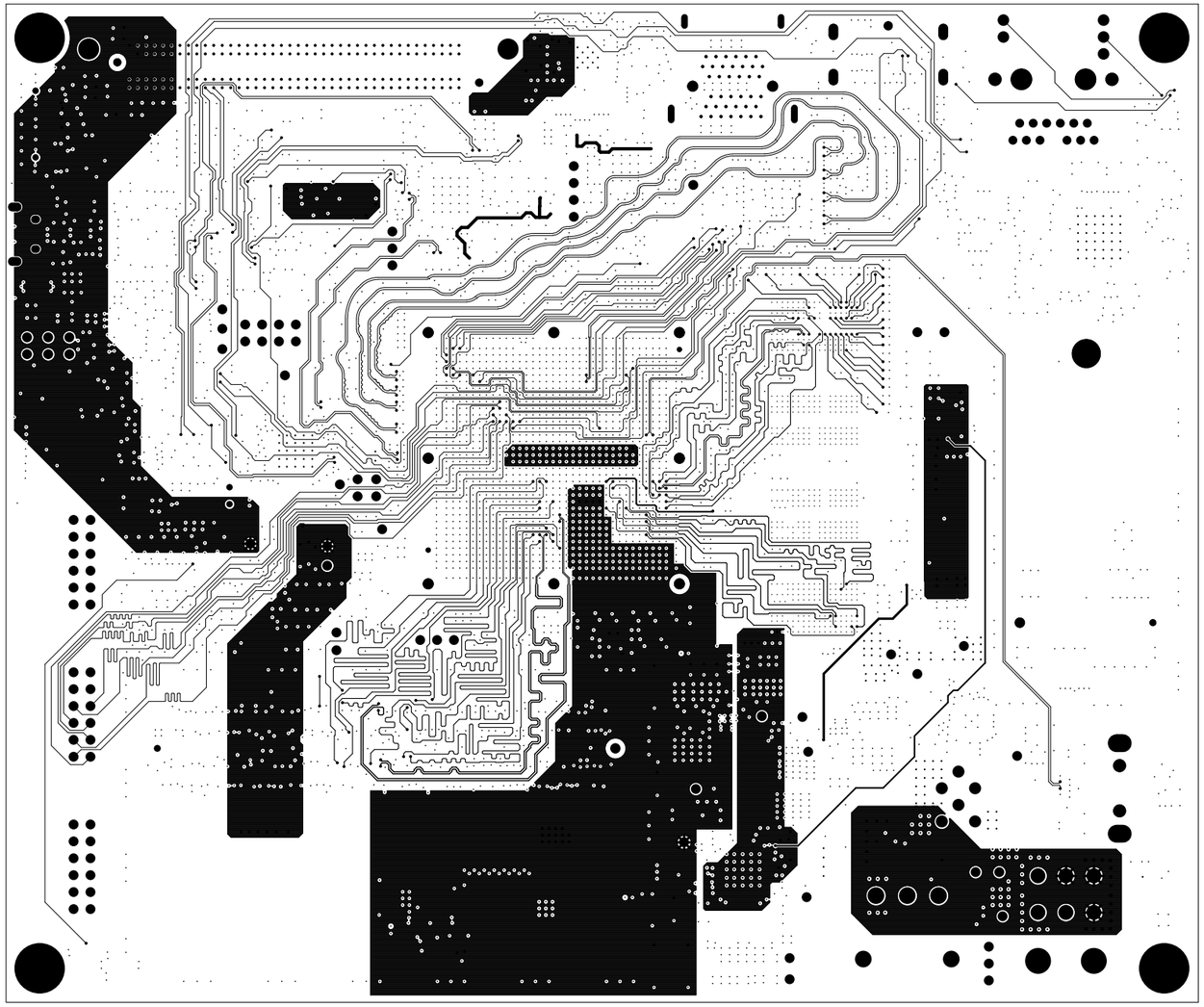
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 11 OF 22 LAYER: GND5	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



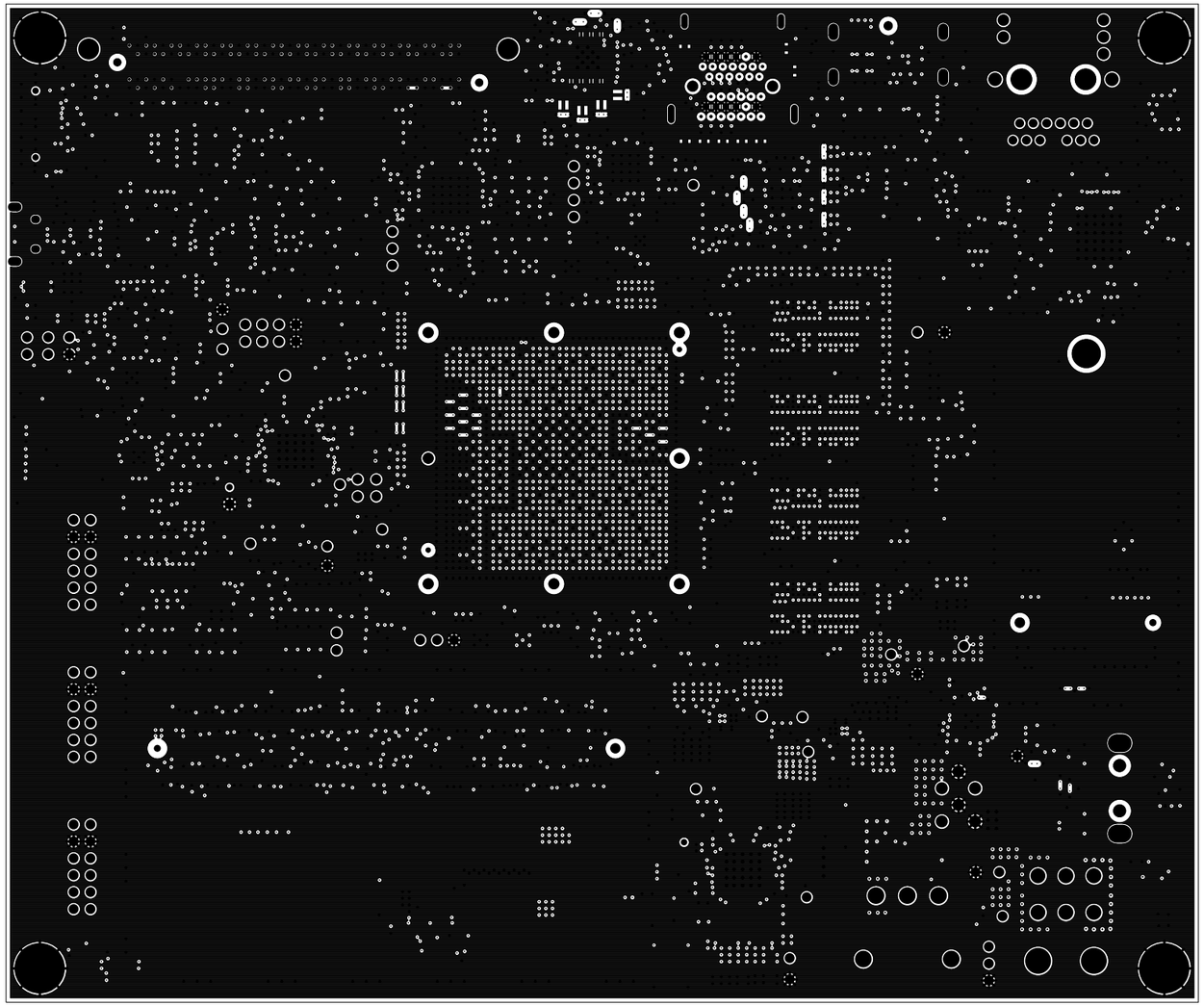
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 12 OF 22 LAYER: SIG4	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



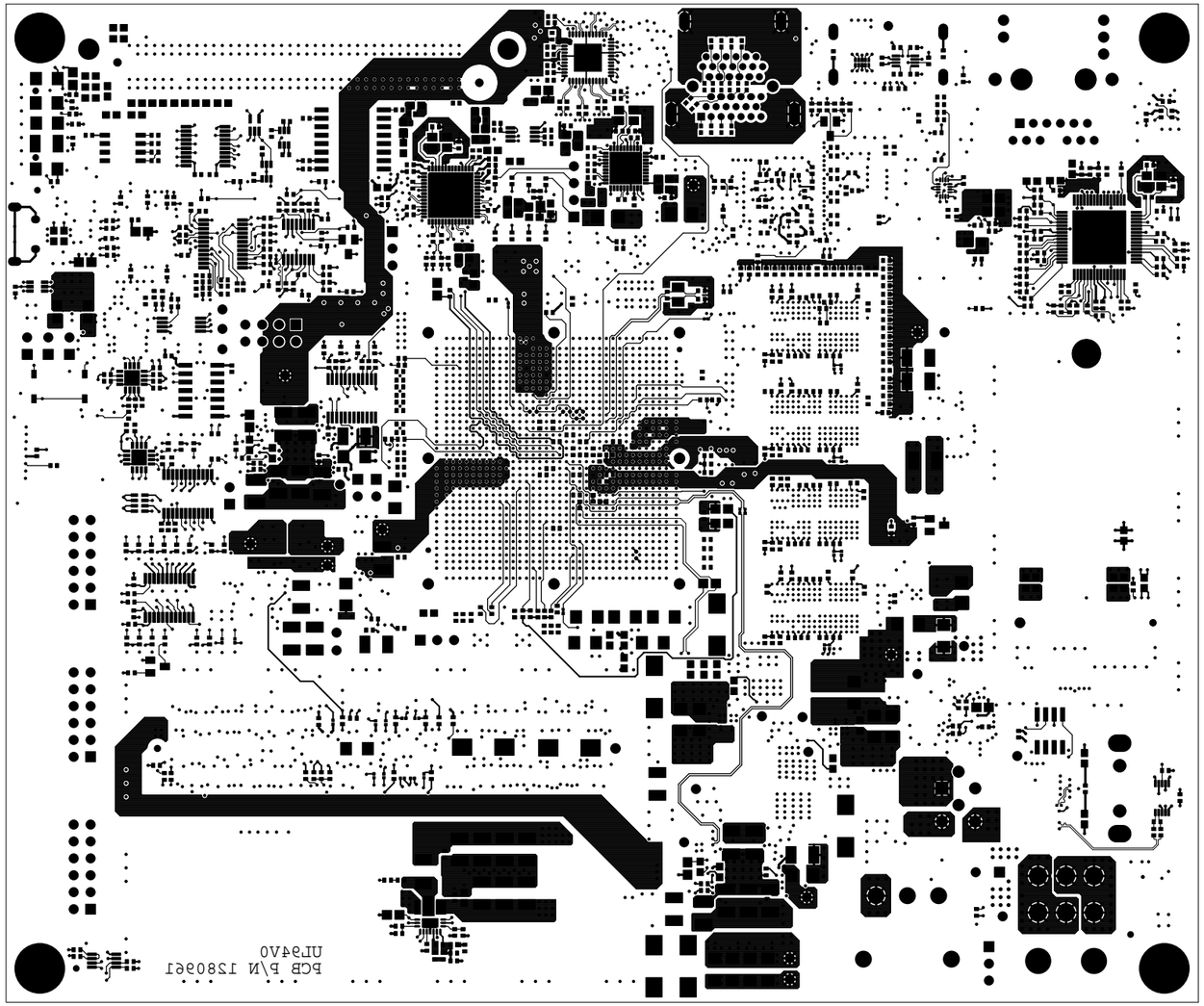
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 13 OF 22 LAYER: GND6	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



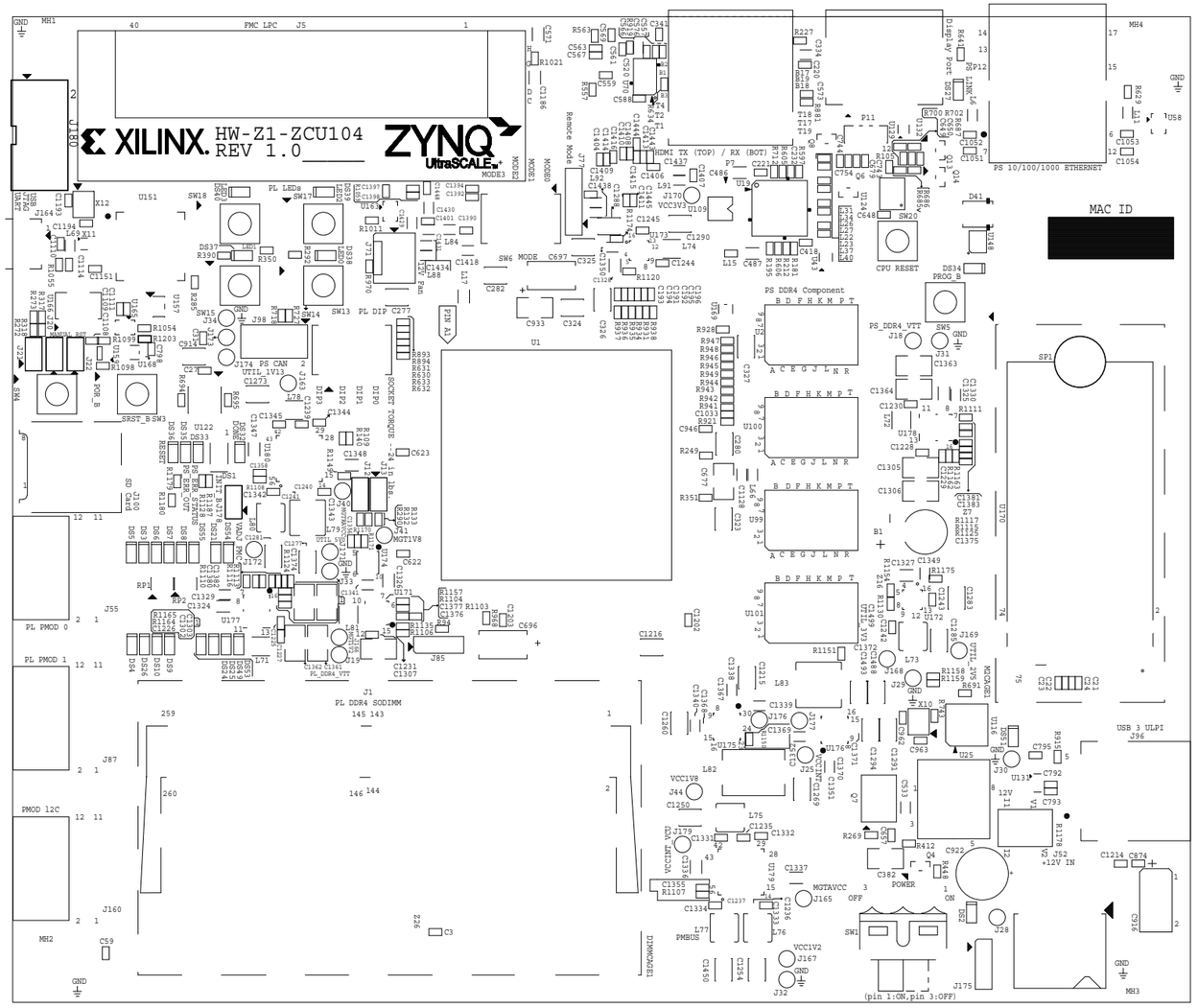
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 14 OF 22 LAYER: SIG5	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



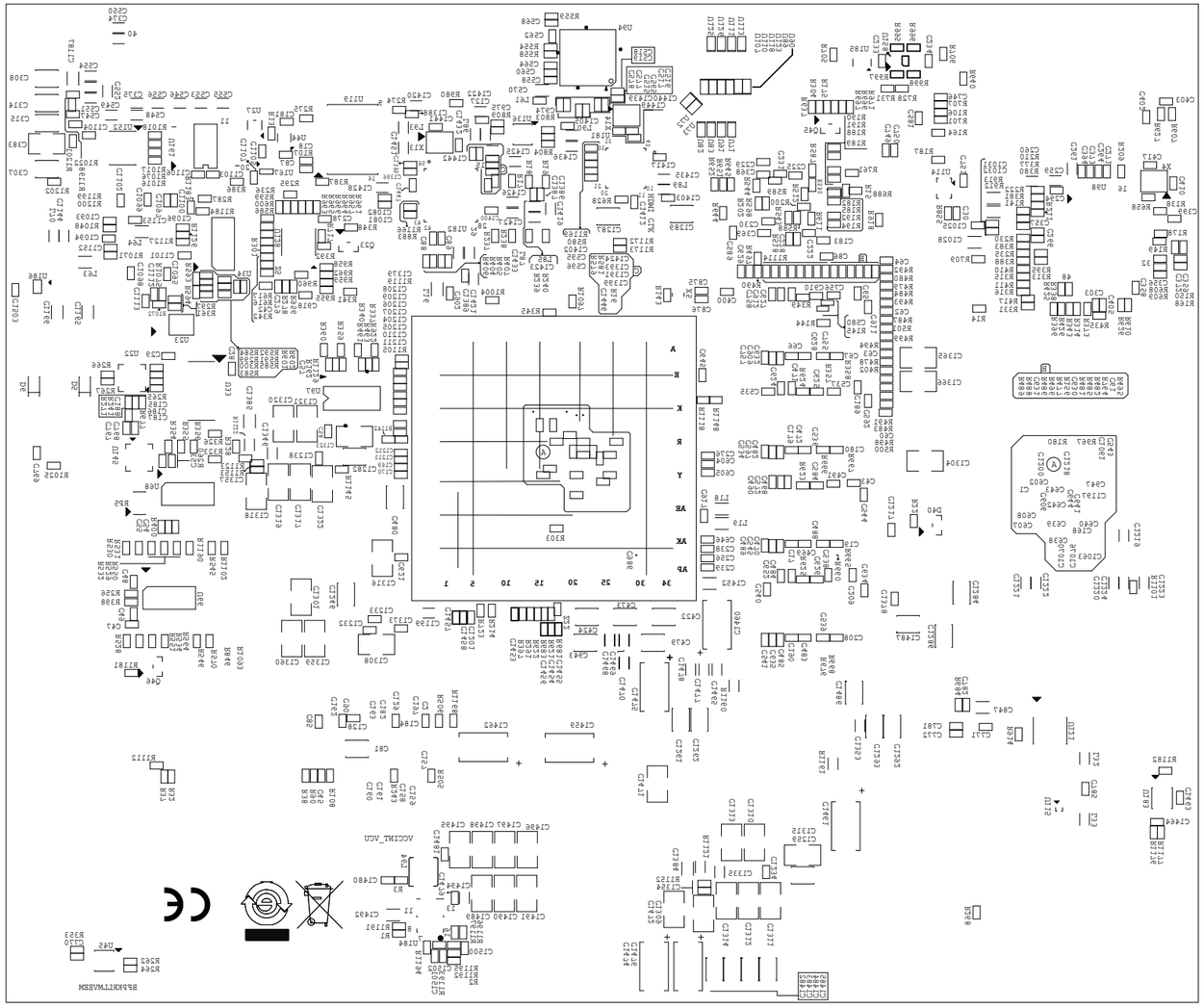
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 15 OF 22 LAYER: GND7	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



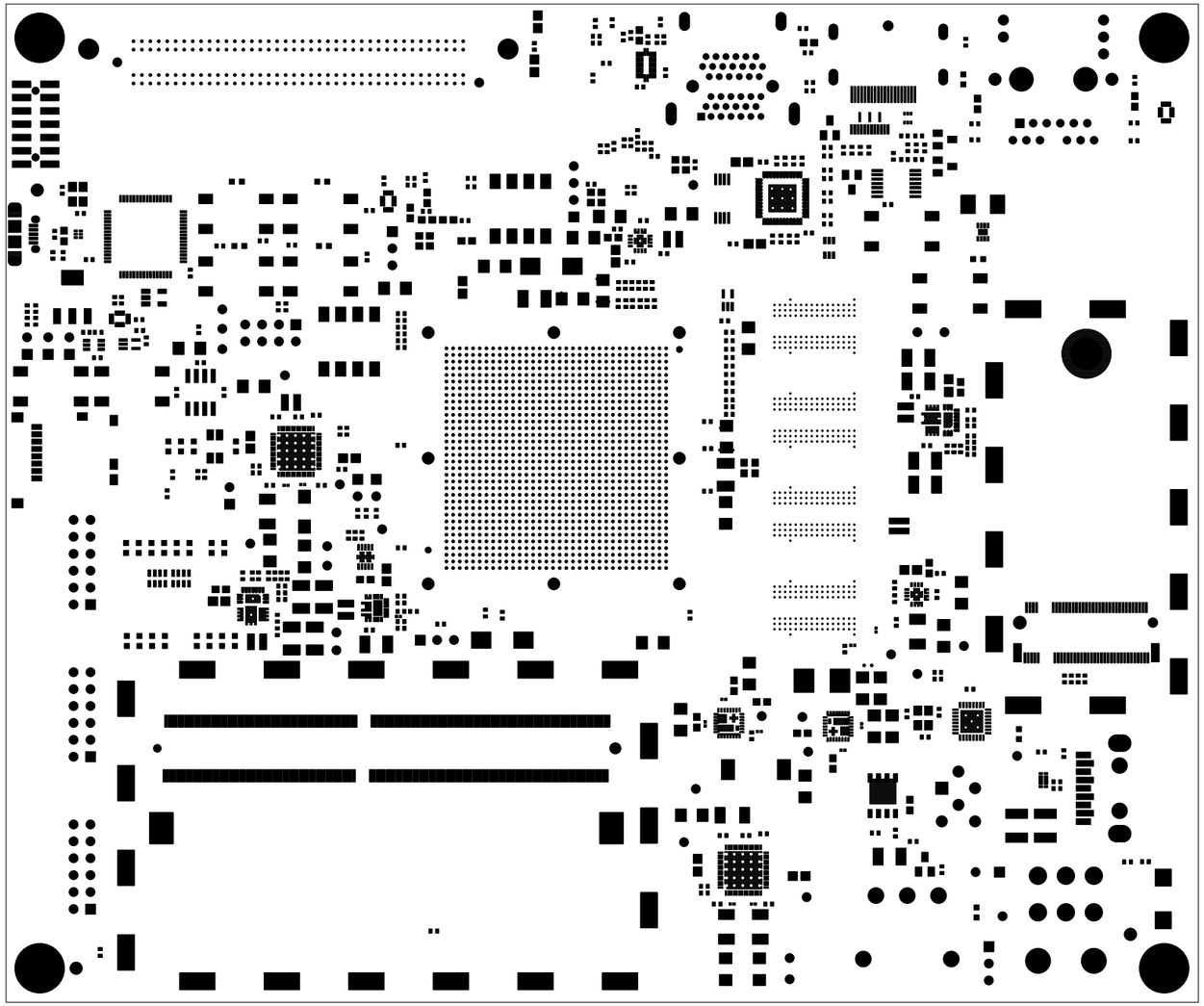
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 16 OF 22 LAYER: BOTTOM	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



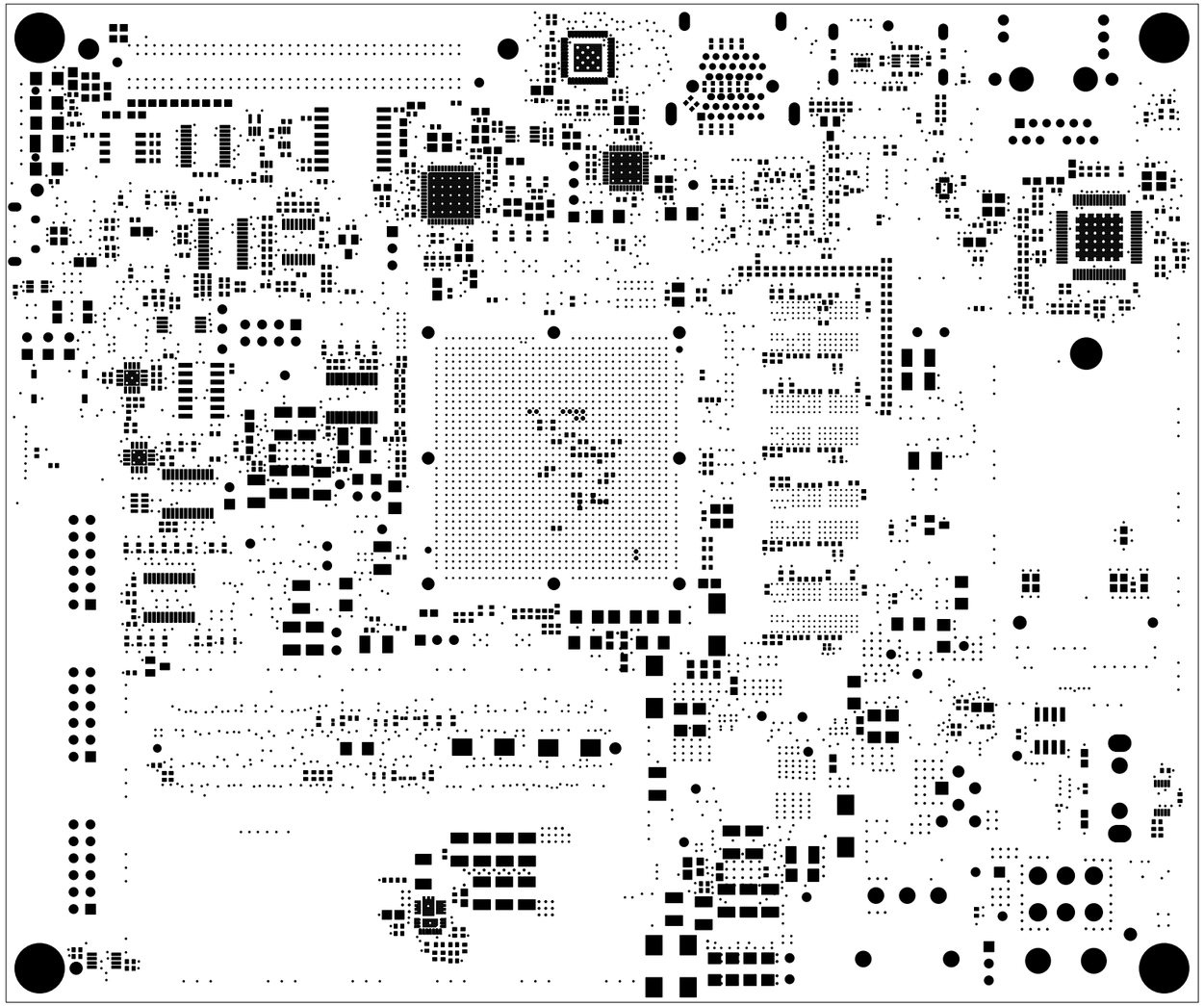
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 17 OF 22 LAYER: 17_SILK_TOP	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



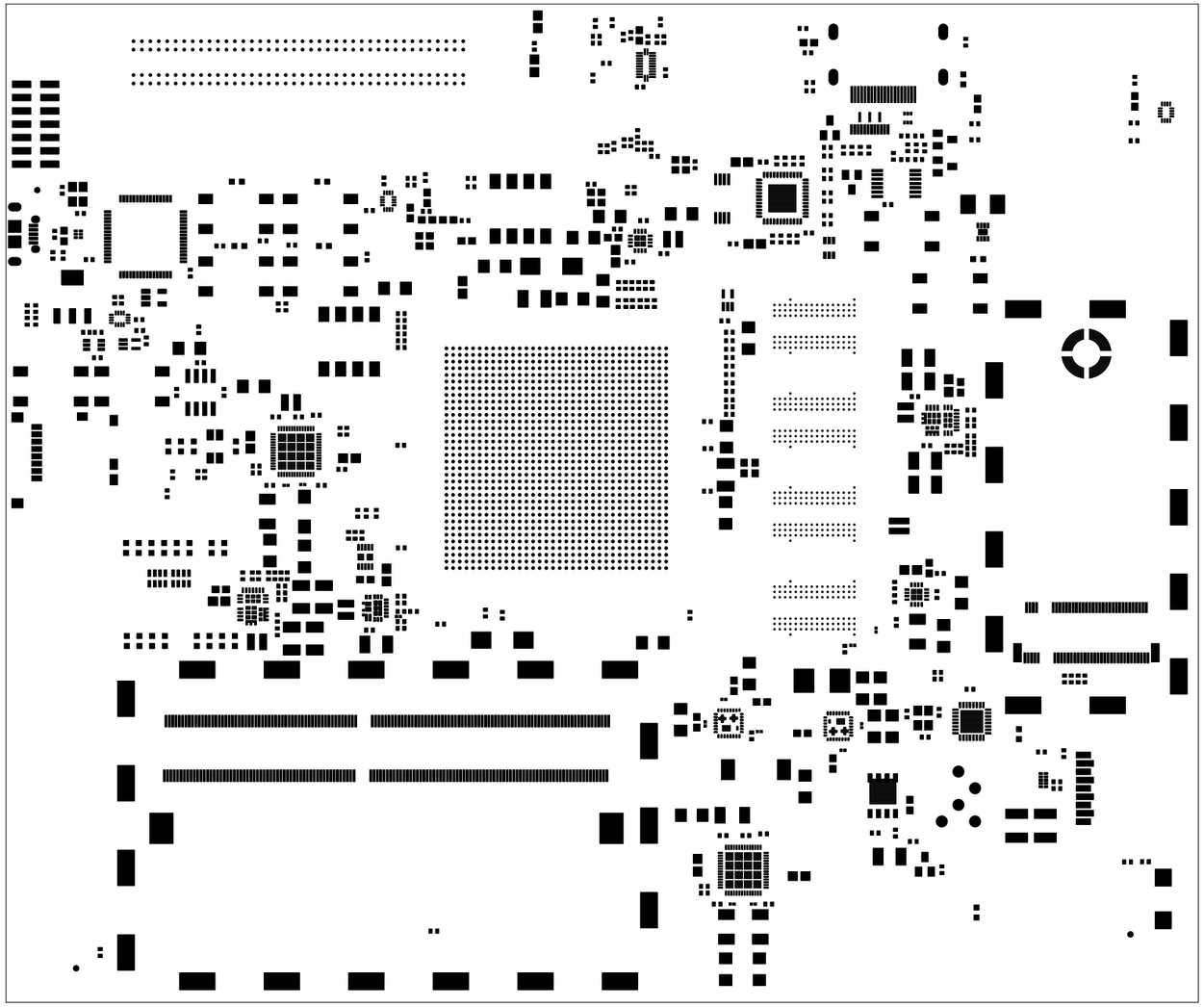
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 18 OF 22 LAYER:18_SILK_BOT	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



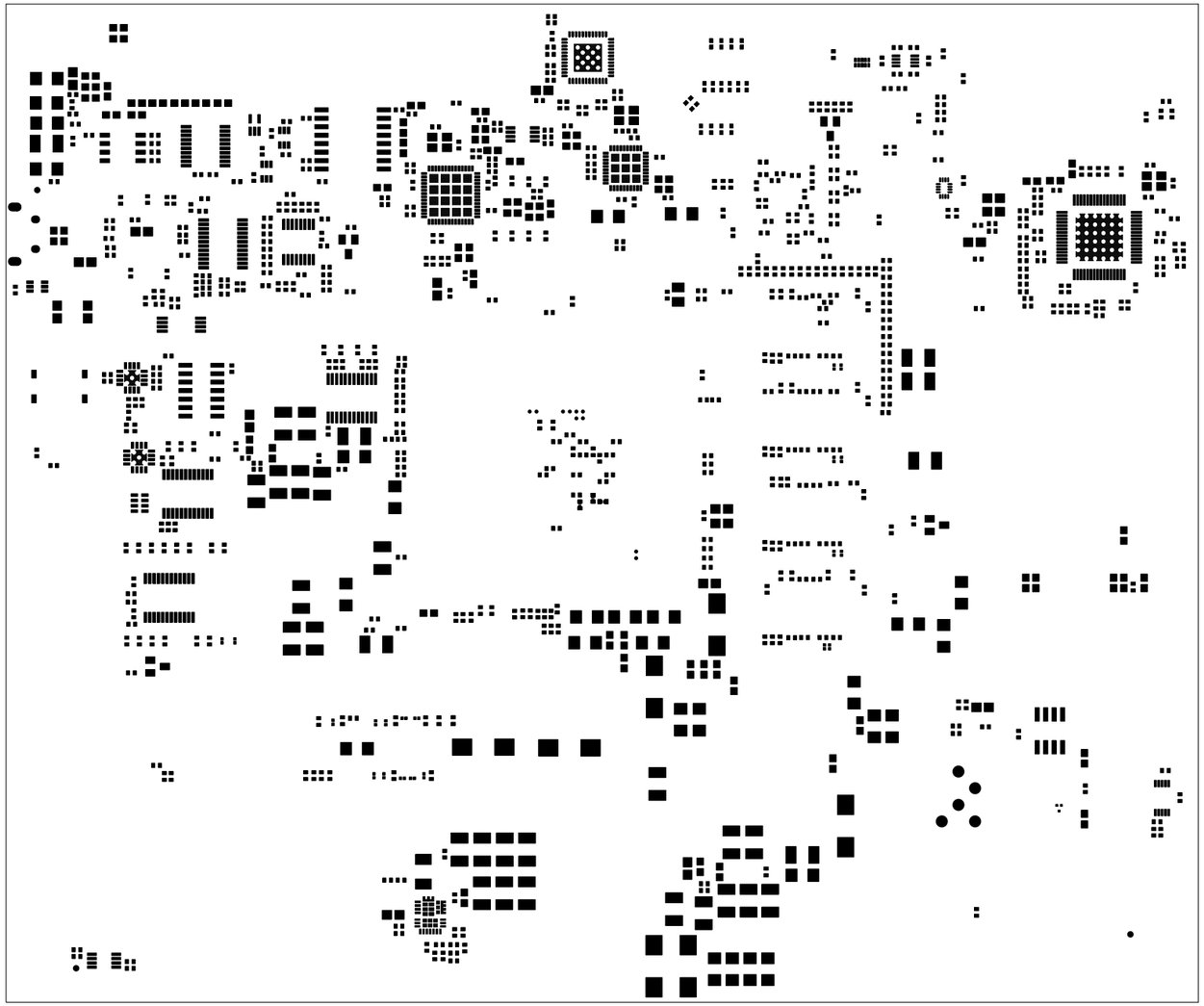
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 19 OF 22 LAYER: 19_SMASK_TOP	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



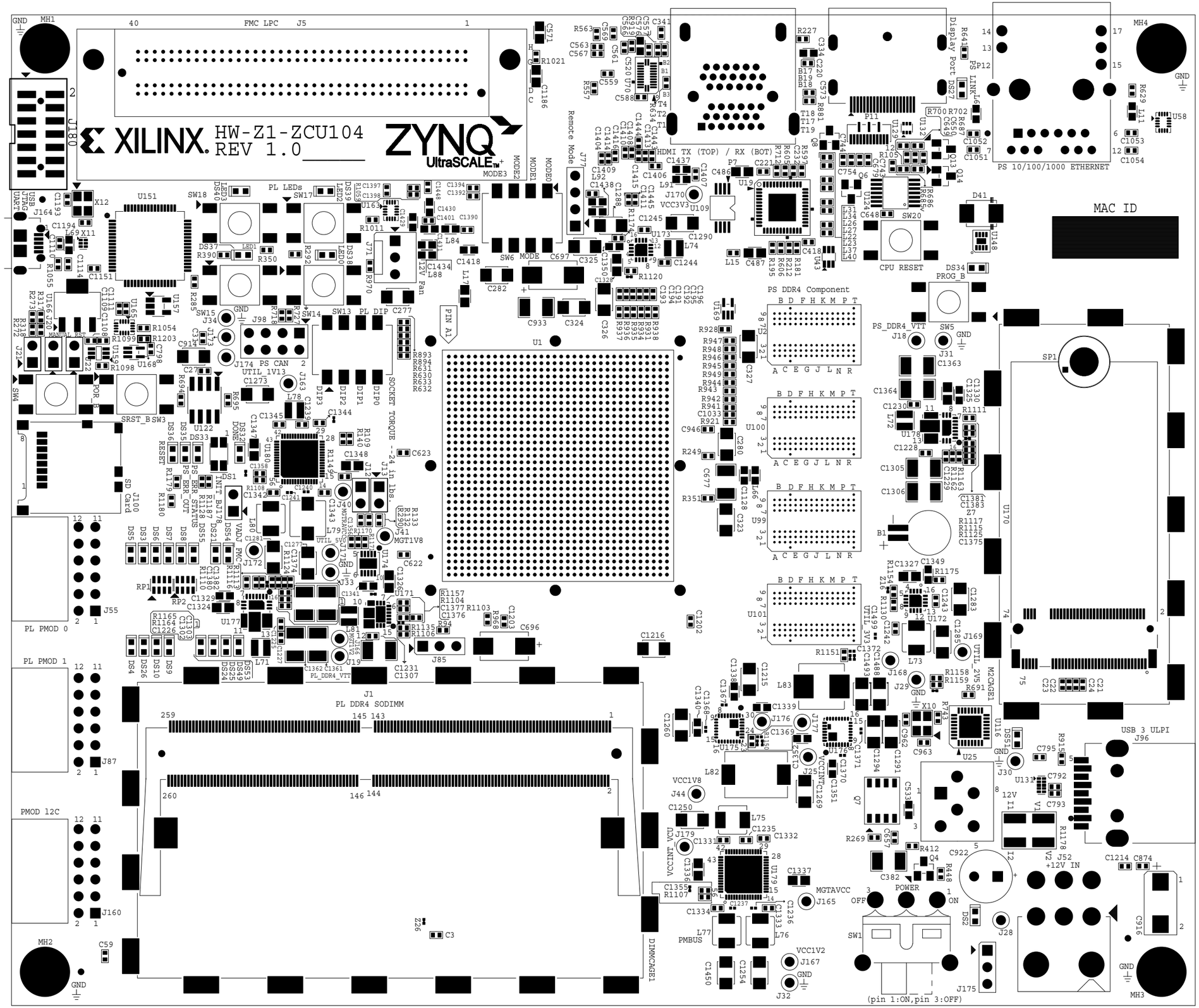
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 20 OF 22 LAYER:20_SMASK_BOT	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



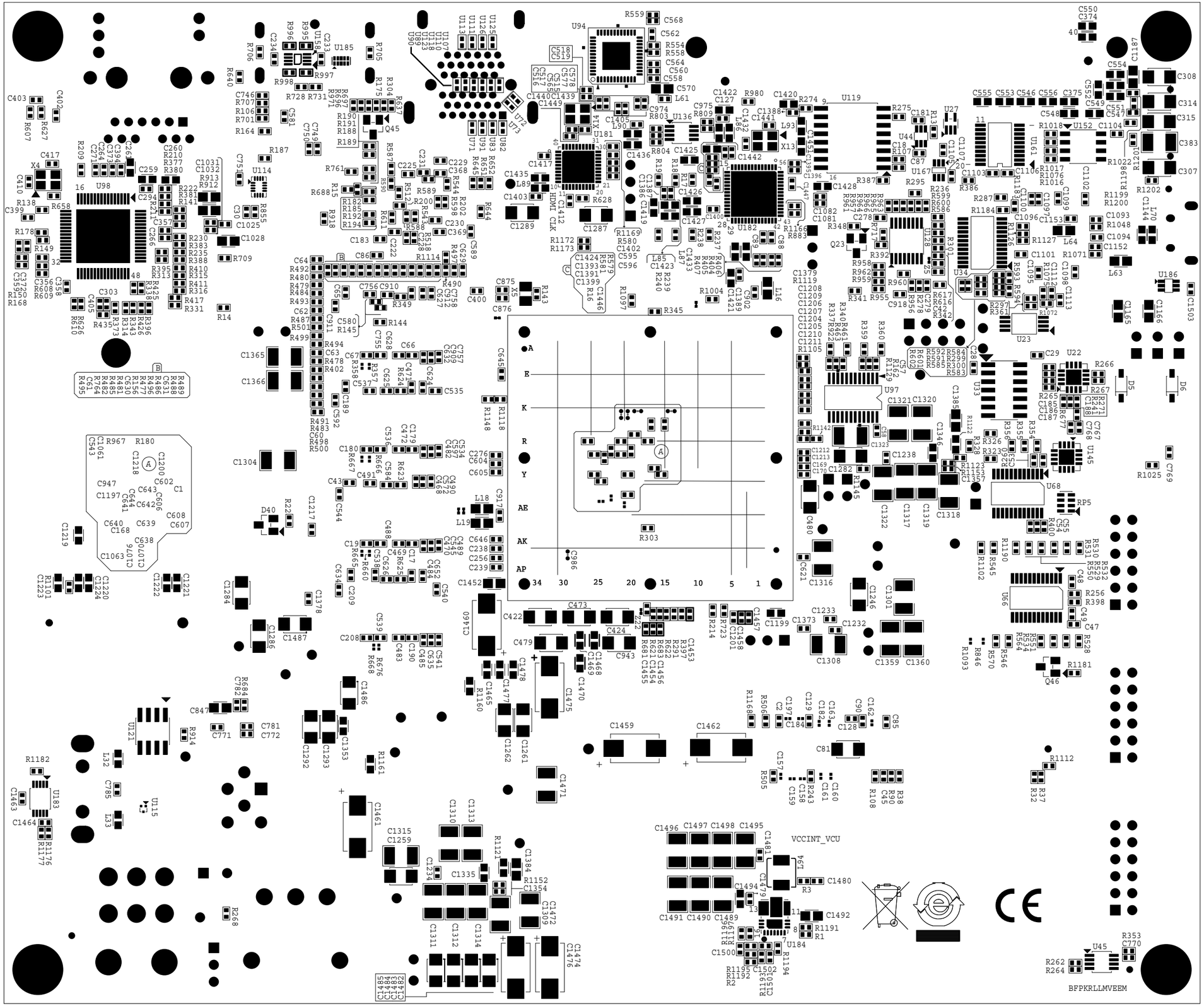
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 21 OF 22 LAYER: 21_PMASK_TOP	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU104	
PCB # 1280961	
Designed by Xilinx	DATE: 02/10/2018
SCAREY	PHONE:4088794451
SHEET 22 OF 22 LAYER:22_PMASK_BOT	XILINX DOC USE ONLY REVISION: 01 VERSION: 1.0



XILINX
HW-Z1-ZCU104
REV 1.0
ZYNQ
UltraSCALE
FMC LPC J5
PL LEDs
PS CAN
PL DIP
SOCKET TORQUE --24 in lbs.
PL PMOD 0
PL PMOD 1
PMOD 12C
J1
PL DDR4 SODIMM
DIMMCAGE1
PS DDR4 Component
HDMI TX (TOP) / RX (BOT)
PS 10/100/1000 ETHERNET
MAC ID
CPU RESET
PROG_B
USB 3 ULPI
J96
+12V IN
POWER
OFF
ON
(pin 1:ON,pin 3:OFF)
PMBUS
MGTAVCC
VCC1V8
VCC1V2
VCCINT
MGT1V8
MH1
MH2
MH3
MH4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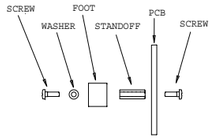
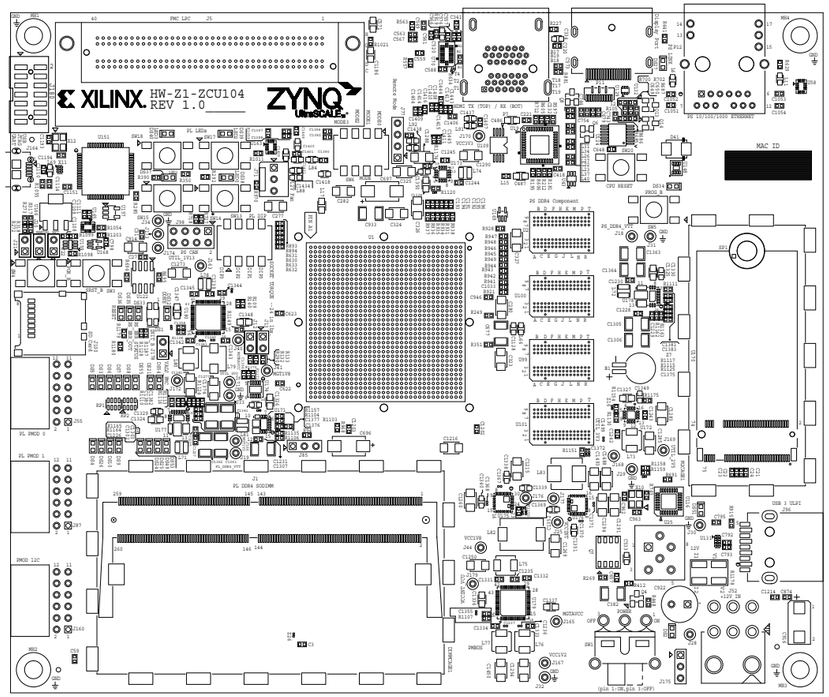
VCCINT_VCU
BFPKRLLMVEEM

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
B	PROTOTYPE	08/30/17	
B	PROTOTYPE	08/30/17	
C	PROTOTYPE	11/27/17	
1.0	PROTOTYPE	02/10/18	
01	PROTOTYPE	02/08/18	

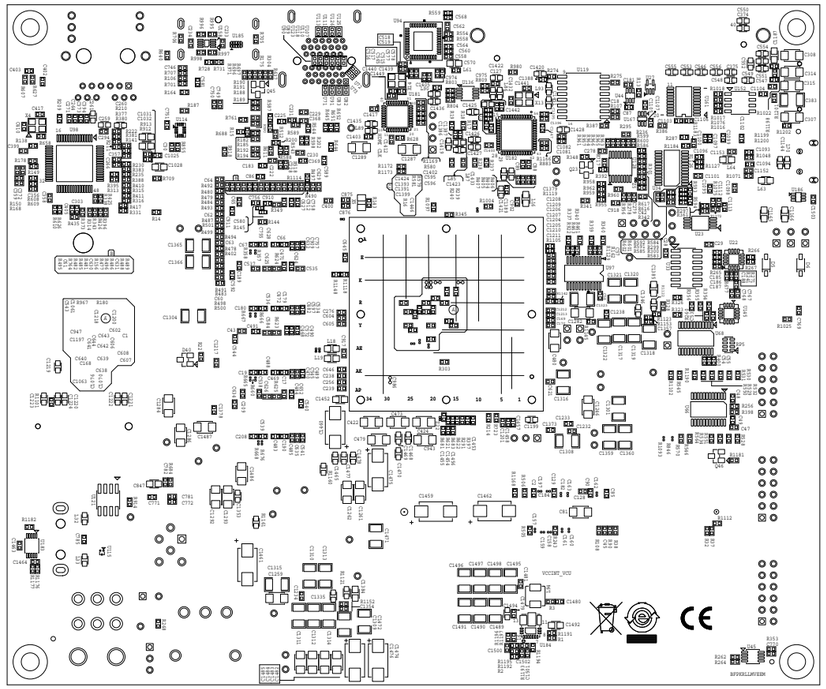
NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ASSEMBLE TO MEET INSPECTION CRITERIA OF IPC-A-610, CLASS 2, CURRENT REVISION.
2. BAG AND TAG (OR MARK CONTAINER) WITH PART NUMBER.
3. REFERENCE SCHEMATIC (OR AVL) FOR BILL OF MATERIALS.
4. ASSEMBLY SHOULD BE "ROHS" AND "LEAD FREE" COMPLIANT.
5. FAB IS BOUND TO USE "SAC305" SOLDER PASTE FOR COMPONENT ASSEMBLY.
6. (a) . VERIFY THAT THE SOLDER PASTE IS NOT APPLIED TO THE BGA PADS ON THE TOPSIDE.
   (b). VERIFY THAT SOLDER PASTE IS NOT APPLIED TO THE UN-POPULATED RESISTORS AND CAPACITORS UNDERNEATH U1.
   (c). MAXIMUM PASTE MASK STENCIL THICKNESS IN THE AREA OF MAXIMUM POWER SUPPLIES (eg HPQFN_19_A DEVICIES) MUST BE 4MILS MAX.
7. SERIAL NUMBER INSTRUCTIONS:-
   " FOLLOW THE XILINX SERIAL NUMBER CONVENTION. FOR EXAMPLE KCU105 REV A IS NUMBERED 1280723A001 TO 1280723A020, REV B SHOULD START AT 1280723C001 AND END AT 1280723C075" FOR REV C IT SHOULD START AT 1280723C001
8. DATASHEET SHOULD BE FOLLOWED FOR ALL HSMF-C155 DEVICES.





VIEWED FROM TOP SIDE



VIEWED FROM BOTTOM SIDE

UNLESS OTHERWISE SPECIFIED	SIGNATURES		DATE
DIMENSIONS ARE IN INCHES	DRAWN	Rocket EMS	02-10-18
TOLERANCES ON;	CHECKED	Brian Forsse	
2 PL DECIMALS +/- .010	ENGRG	Brian Forsse	02-10-18
3 PL DECIMALS +/- .005	ISSUED		
ANGLES +			
FRACTIONS +			

XILINX.
2100 LOGIC DR.
SAN JOSE, CA 95124
HWCP - HARDWARE & CONFIGURATION PLATFORMS

ASSEMBLY DRAWING

HW-Z1-ZCU104

SIZE	FSCM NO	DWG NO	REV: 01
D		0432057	VER: 1.0
SCALE NONE		SHEET 1 OF 1	