Performance optimization of power MOSFETs in SMT top-side-cooling packages by system design

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***Abstract*— This work presents easily applicable practices for optimizing the performance of power converters using discrete, top-side-cooled power packages. It demonstrates how parasitic elements in the power path can be minimized, using a full-bridge topology with novel Silicon-Carbide wide bandgap power semiconductors as an example. Furthermore, this paper explores two different methods for estimating power-loop inductances: one measurement based, and one simulation-based method. With the mismatch between the results being less than 10 percent, a total power-loop inductance of 7 nH (on average) could be achieved with the Silicon-Carbide second generation (G2) Power MOSFETs in Q-DPAK packages. Finally, suggestions for further optimization of the test board are offered. The recommendations and best practices outlined in this paper provide valuable insights for designers and developers of power conversion systems, facilitating faster design-in cycles for top-side-cooled power packages across various applications.**

Keywords—Power Electronics, Wide-Bandgap semiconductors, Silicon-Carbide, SMT, top-side-cooled packages, full-bridge topology, PCB layout, high power, Silicon Carbide, wide bandgap, optimization of electrical performance, best practice sharing.

I. INTRODUCTION

Reduced power-converter performance is significantly attributable to parasitic stray inductance in the converter's power-loops. Large parasitic stray inductances lead to a decline in switching speed, which is, in turn, a consequence of the reluctance exhibited by these parasitic elements. Moreover, the parasitic inductances contribute to unwanted energy accumulation within their magnetic fields in the power converter which cause elevated commutation losses and ultimately, limit the effective switching frequency of the power converter. Consequently, the impact of the stray inductance of power-loops has been extensively researched in literature [1-11].

This paper expands upon this research, focusing on top-side-cooled surface-mount-technology (SMT) packages, which offer a promising solution for enhanced thermal and high-class electrical performance. This work highlights the design process's degrees of freedom and their impact on electrical performance, specifically stray inductance, switching behavior, and voltage overshoots, using an optimized test board. Chapter II presents an overview of the test board and its fundamental underlying concepts, such as the power plane concept and the placement of the Q-DPAK top-side-cooled power packages. Chapter III explores the magnetic field compensation, a promising approach for minimizing the power-loop inductance. This chapter therefore displays the influence of geometrical factors given by the printed circuit board (PCB) design. Results show that excellent switching performance can be achieved by applying the magnetic field reduction principle, as demonstrated by the latest 750 V Silicon-Carbide (SiC) G2 automotive power switches in industry-standard top-side-cooled SMT packages (Q-DPAK). Subsequently, the power-loop inductance of the board is determined via two distinct methods: an experimental extraction of the stray inductance and a simulation of the stray inductances with a 3D FEM simulation. These two methods deliver closely aligned results, with the 3D FEM simulation offering deeper insights into board parasitics, including current distribution within the power-loops.

II. DESCRIPTION OF EVAL BOARD

The test vehicle used for this research is shown in **Fig. 1**. The board utilizes four latest-generation SiC power MOSFETs "AIMDQ75R016M2H" with 16 mΩ on-channel resistance, a rated voltage of 750 V and automotive qualification (AEC-Q101). This second generation of Infineon's SiC MOSFET technology offers industry leading figure-of-merits, which show their full benefit when these switches are used in low-parasitic environments.

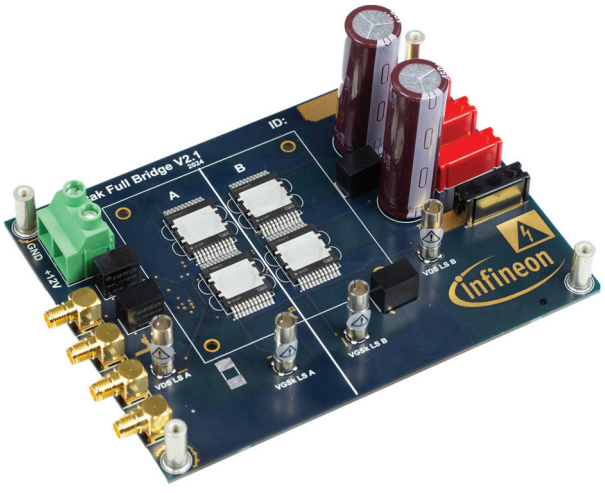

Fig. 1. Image of the full-bridge test PCB used for research (top-view)

Especially worth mentioning is, that the Silicon Carbide technology from Infineon is fully capable to be safely turned-off with 0 V while also enabling second-source compatibility by supporting negative turn-off voltages. This is enabled by a superior device design, an industry leading SiC technology together with an outstanding gate oxide. Nonetheless,

parasitic turn-on effects can still occur in designs with large parasitic contributions, since the high dv/dt from the drain-source node retains the potential to modulate the gate node via coupling capacitances caused by the PCB design. Parasitic turn-on, respectively turn-off events, can be identified by assessing the drain-to-source voltage (V_{ds}) waveform: in a well-designed power converter, the voltage across the MOSFET will show a monotonous transition during the commutation since the MOSFET remains in the desired state without suffering from uncontrolled switching events.

Each half-bridge (HB) has its own, dedicated MOSFET driver mounted on the bottom-side of the PCB, as illustrated in **Fig. 2**. Since these SiC MOSFETs have the outstanding property to support a zero-voltage turn-off, a gate driving voltage of +18 V and 0 V was taken into consideration. Consequently, the dual-channel MOSFET driver "2EDB9259Y" from Infineon Technologies was chosen to drive the "AIMDQ75R016M2H" SiC MOSFETs. The 2EDB9259Y is highly suitable, as it provides an undervoltage lockout level (UVLO) of 15 V, two fully isolated channels with short propagation delays, shot-through protection and a high common mode rejection ratio which is beneficial for the fast dv/dt of these novel wide-bandgap devices. The corresponding block diagram is presented in **Fig. 2**.

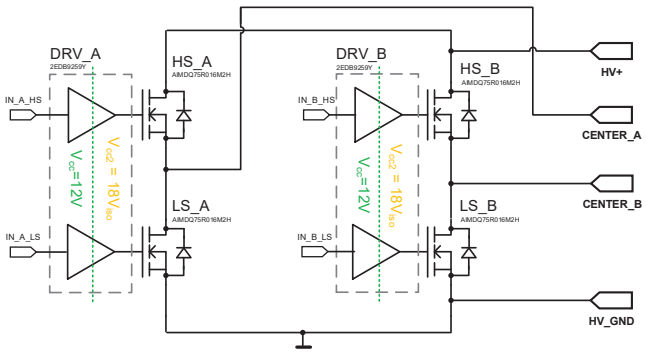

Fig. 2. Block diagramm of full-bridge EVAL board.

As **Fig. 3** shows, the test vehicle design deploys industry standard top-side-cooled SMT packages (Q-DPAK) on a standard four-layer PCB. The term "top-side-cooled" refers to SMT packages, which have the cooling pad exposed on the top-side of the power package – in contrary to "bottom-side cooled" packages, which incorporate the cooling pad on the bottom side. **Fig. 4** highlights these different concepts.

Top-side-cooled SMT power packages offer several advantages. Firstly, as SMT components, they are compatible with automated PCB assembly, eliminating the manual labor required for through-hole packages. Secondly, these packages inherently separate the thermal and electrical paths. This allows for efficient heat dissipation from the device's top surface, reducing system thermal resistance and minimizing the risk of thermal runaway without compromising electrical performance optimization.

However, designers used to utilize traditional through-hole packages may face challenges when using discrete top-side-cooled devices: the main concern is to achieve good electrical performance, while ensuring adequate isolation between high-voltage components and the cooling system while maintaining optimal thermal performance. This requires careful consideration of component placement, PCB layout, power plane design, selection of thermal interface materials and cooling system design (as **Fig. 3**, **Fig. 6** and **Fig. 7** show).

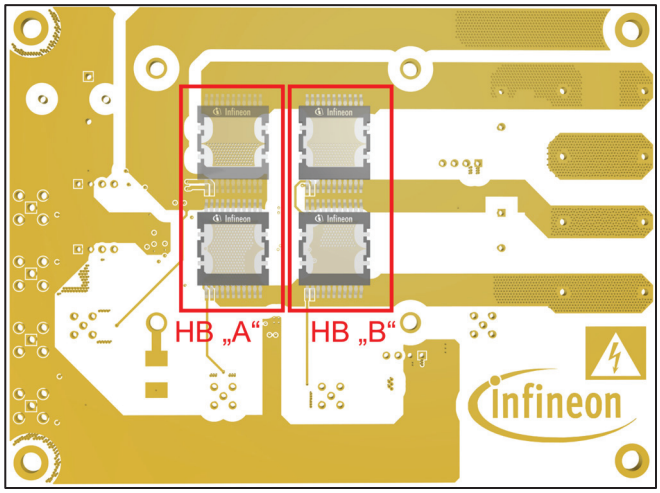

Fig. 3. Top-view of copper layer of test PCB with the Q-DPAK top-side-cooled power packages. The 3D package models are half-transparent to show the power-loop planes and vias below.

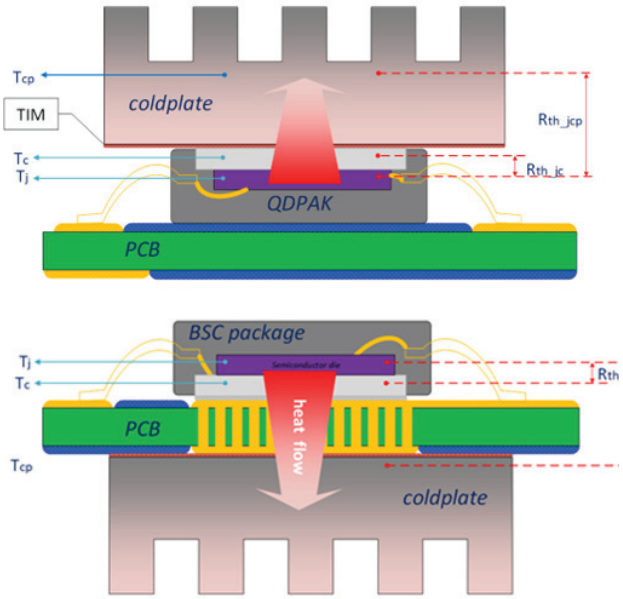

Fig. 4. Differences between discrete top- and bottom-side-cooled SMT power packges on PCB substrates. [12]

Continuous high-power operation necessitates a heatsink or cold plate, requiring careful consideration of mechanical constraints. To minimize mechanical stress on the PCB, a quadratic arrangement of power switches within a heatsink fixture array was selected. This design facilitates heatsink mounting for efficient power device cooling. The thermal interface between the Q-DPAK power package's exposed metal pads and the heatsink can be achieved using a gap pad or liquid gap filler. Notably, gap pads require significant compression to achieve optimal thermal performance, introducing substantial force into the system. The equidistant mounting holes minimize PCB mechanical strain and reduce board warpage, particularly in the absence of additional counteracting mechanical supports.

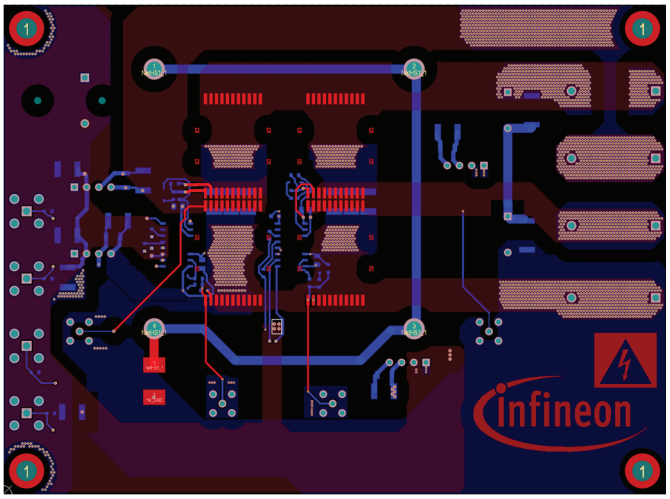

Fig. 5. PCB Layout: top-layer copper (red) and bottom-layer copper (blue) showing the fundamental power plane concept of this power converter. The two middle layers are hidden in this figure.

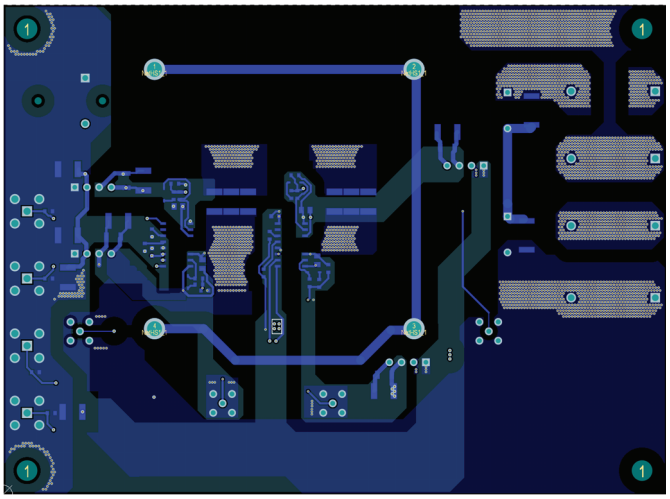

Fig. 6. PCB Layout: depiction of the bottom layer, illustrating critical signal traces and their respective ground planes in the third layer (light blue). These planes are utilized as a ground reference to minimize the effective stray inductance of each signal path and to enhanced signal integrity.

III. Performance Optimization at Board Level

A. Minimization of power-loop stray inductance

1) Theoretical considerations

The design objective for highly efficient power converters is to enable a fast commutation (i.e. high d*v*/d*t* and high d*i*/d*t*) while reducing ringing and overvoltage stress on the power MOSFETs. Especially wide-bandgap materials offer outstanding figure-of-merit values and can provide excellent switching performance as long as their environment allows for it. Therefore, it is imperative to optimize the physical layout of the PCB, i.e. reduction of the parasitic stray inductances among the different current paths, a reduced mid-point capacitance and low coupling capacitances between the different voltage domains.

For good power-loop performance, it is also necessary that the decoupling caps, which sustain the voltage on the DC link, offer a low-impedance connection to the power MOSFETs. This can be enabled by situating the decoupling capacitors as close as possible to the corresponding half-bridge switches. The design in this paper gives a reference of how to optimally position these capacitors just underneath the center-point of the half-bridge. Like this, the effective length of the power-loop can be reduced significantly (see **Fig. 7**).

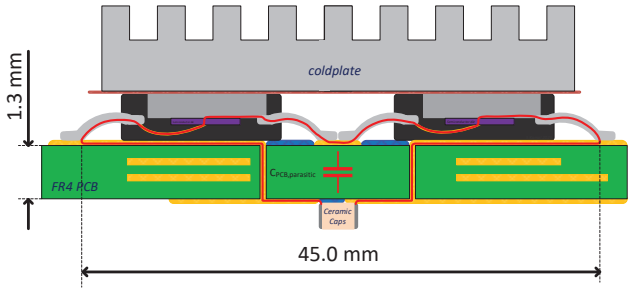

Fig. 7. Concept of power-loop comprising the two SiC MOSFETs in Q-DPAK on the top-side and the ceramic caps terminating the power-loop on the bottom side of the FR4 PCB.

Subsequently, the principle of magnetic field compensation is applied: this principle states, that the mutual inductance of a current path can be minimized by the superposition of the individual magnetic fields. Since the magnetic field created by the commutation current in the forward conductor has the same magnitude as the field of the reverse conductor, but with opposite direction, the total magnetic field could be lower than its individual contributors, depending on the geometrical dimensions of the conductor arrangements. Hence, the effective stray inductance of the power-loop depends mainly on the geometric circumstances and could be estimated as follows [3]:

$$L = \mu_0 l \frac{d}{w} \tag{1}$$

L describes the total inductance, μ0 being the magnetic permeability of vacuum, l represents the length of the conductors, w stands for the width of the conductors and d defines the distance between the conductors. **Fig. 8** shows the calculated stray inductance in dependency of the geometric mean distance of the copper planes according to **(1)**.

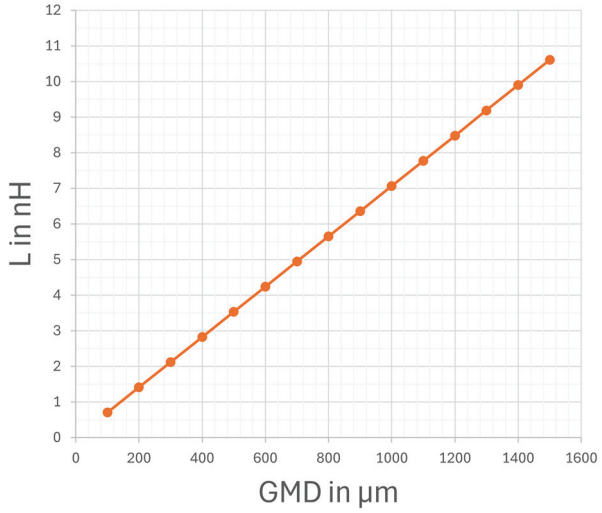

Fig. 8. Calculated inductance vs. the geometric mean distance between conductors.

Following (1) it becomes clear that also the energy stored in the magnetic field depends directly on the physical design of the PCB (2) [9]. **Equation 2** explains the relationship between magnetic field energy (E), inductance (L), current (I)

in dependency of μ0 and the dimensions of the PCB design: *l*, *d* and *w*.

$$E = \frac{1}{2} \cdot L \cdot I^2 = \frac{1}{2} \cdot \mu_0 l \frac{d}{w} \cdot I^2 \qquad (2)$$

In practice this calls for situating the forward- and the reverse current conductor as close as possible to each other and to terminate the power-loop with decoupling caps placed adjacent to the power MOSFETs. The power-loop implementation for SMT components is typically based upon either a horizontal or a vertical principle. The horizontal approach considers the decoupling caps being placed on the side of the PCB where the power MOSFETs reside, while the vertical concept places the decoupling caps on the opposite side allowing the current flowing in vertical direction.

This research is based on a vertical power-loop concept (see **Fig. 7**). The main advantages of this design concept are a higher utilization of the PCB space and that the component height of the decoupling caps can be arbitrary: it is not limited by the height of the power MOSFET packages, respectively the heatsink.

2) Experimental extraction of power-loop inductance

Upon completion of the power MOSFET turn-off switching transient, the drain-source voltage (V_{ds}) waveforms exhibit damped oscillations, indicative of parasitic inductance and capacitance interactions within the circuit. These oscillations are caused by the total parasitic capacitance in combination with the total stray inductance, with the magnitude damped by resistive components. Therefore, a series resonant network (consisting of a resistor *R* in series with an inductor *Lσ* and a capacitance *C*) can be assumed, where the period of the oscillation (*T*osc) is defined as:

$$T_{\mathrm{osc}} = 2\pi\sqrt{LC} \rightarrow L_{\sigma 1} = \frac{T_{\mathrm{osc}}^2}{4\pi^2 C} \qquad (3)$$

Further, the period of the oscillation (*T*osc) is determined via experimental measurements. The result of these measurements are display in **Fig. 9-12**. **Fig. 11** shows that the oscillation-period yields about 7.5 ns.

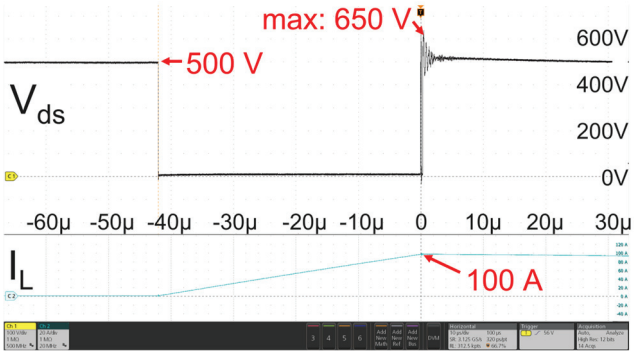

Fig. 9. Full view of the double pulse experiment: the black waveform (C1) shows the voltage accross drain and source (V_{ds}) on the low-side MOSFET AIMDQ75R016M2H in half-bridge "A", the turquoise curve (I_L) shows the current trough the inductor reaching ~ 100 A after 45 us (an aircoil with 200 uH was used as load).

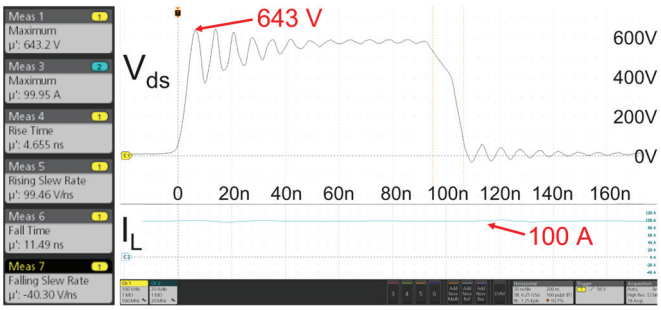

Fig. 10. Drain-to-Source voltage measurement of MOSFET AIMDQ75R016M2H positioned "LS_A" at V = 500 V and I = ~ 100 A with 0 V/+18 V gate driving; measurement taken directly on V_{DS} probing port: the V_{ds} voltage is rising montously in ~ 4.6 ns, attesting the absence of any parasitic re-turn-on.

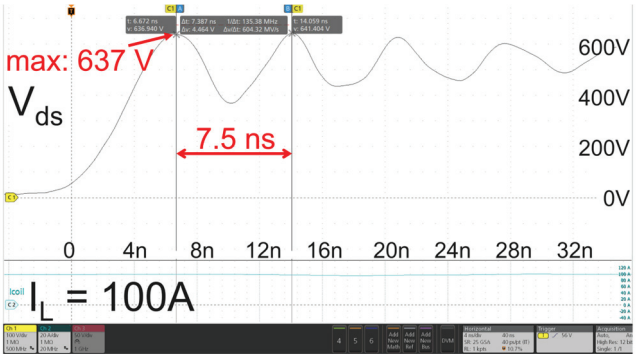

Fig. 11. Detail of V_{ds} measurement of MOSFET AIMDQ75R016M2H positioned "LS_A" at V = 500 V and I = ~ 100 A with 0 V/+18 V gate driving; measurement taken directly on V_{DS} probing port. The period of the V_{ds} oscillation is measured to determine the parasitic stray inductance of the power-loop.

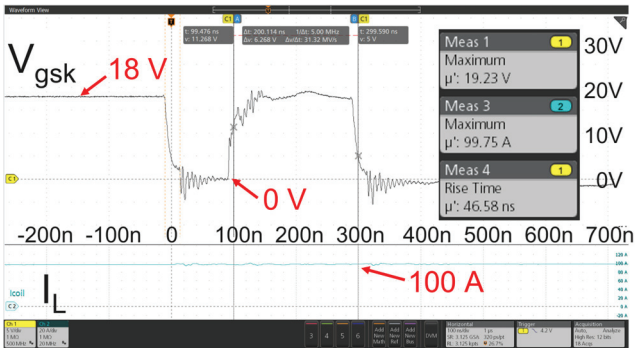

Fig. 12. A detailed image of the gate-to-kelvinsource (black waveform; C1) showing good controlability of the MOSFETs with uni-polar gate driving without pronounced gate ringing. The turquoise curve (I_L) shows the current trough the inductor reaching ~ 100 A after 40 μs (an aircoil with 200 μH was used as load).

Moreover, it can be assumed that the value of *C* is dominated by output capacitance (C_{oss}) of the power MOSFET. For the deployed AIMDQ75R016M2H the C_{oss} is about 195 pF at 500 V. This assumption is confirmed when the parasitic PCB capacitance is estimated as follows:

$$C_{\mathrm{PCB}} = \frac{\varepsilon_0 \varepsilon_r A}{d} = \frac{8.85 \cdot 10^{-12} \cdot 4.2\ \mathrm{F \cdot m^{-1}} \cdot 9 \cdot 10^{-5}\mathrm{m}^2}{1.6 \cdot 10^{-3}\mathrm{m}} = \sim 2\ \mathrm{pF} \qquad (4)$$

Adding 2 pF for the center-node of the half-bridge, finally the stray inductance $L_{\sigma 1}$ can be calculated by following (3):

$$L_{\sigma 1} = \frac{T_{osc}^2}{4\pi^2 C_{PCB}} = \frac{(7.5\text{ ns})^2}{4\pi^2 \cdot 197\text{ pF}} = \sim 7.2\text{ nH} \qquad (5)$$

3) Estimation of stray inductance via 3D FEM simulation

The parasitic inductances of the power-loop were extracted using a 3D FEM multi-physics parasitic extraction tool in addition to the experimental approaches. Therefore, the PCB was modeled in a 3D FEM simulation software. The underlying model assumes that a commutation current flows from the terminals of the decoupling caps to the power MOSFETs via the copper tracks of the PCB and back to the decoupling caps (see **Fig. 13**) while taking the actual layer stack-up (see **Fig. 14**) into consideration. Like this it is possible to extract the lumped stray inductance of the power-loops. Each half-bridge was analyzed individually to avoid any unintentional cross coupling between the different domains. The extracted results are displayed in **TABLE I.**

TABLE I. STRAY INDUCTANCE SIMULATION RESULTS

PCB domain	simulated stray inductance @100MHz
Power-loop of half-bridge "A"	6.84 nH
Power-loop of half-bridge "B"	7.09 nH

In addition, a current distribution simulation was performed. **Fig. 15** shows these results: the current distribution in "half-bridge A" along a plane on the top-side of the PCB at a source current of 60 A. It can be observed that the current distribution in the copper planes of the power-loop below the package is quite uniform. On the other hand, the vias, which are located below the Q-DPAK packages, exhibit a non-uniform current density: the first row of vias, which are located closer to the source, respectively to the drain leads, seem to carry the highest current. Their current density is approximately a decade higher compared to the remaining rows (**Fig. 15**). Interestingly, the first row of vias below the low-side MOSFET of half-bridge 'A' exhibits a current density of approximately 200 A/mm², while the remaining vias exhibit only a current density of approximately 100 A/mm².

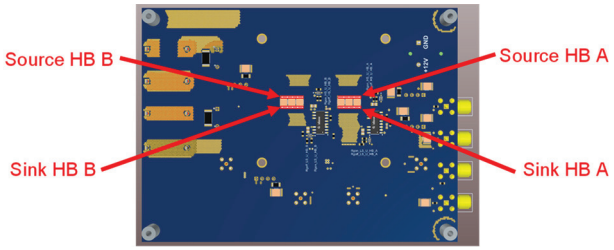

Fig. 13. Source and sink positions of the current for the stray inductance simulation.

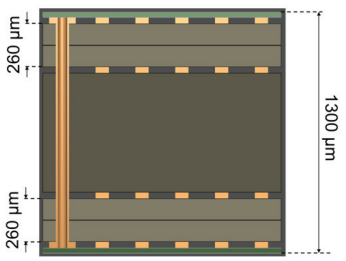

Fig. 14. PCB stackup: standard 4-layer FR4 with 35 µm copper layers.

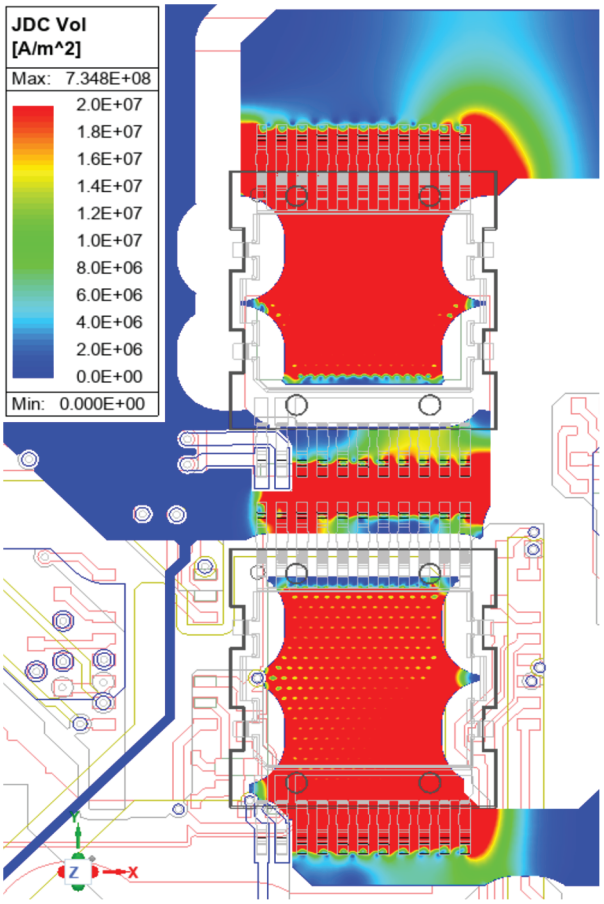

Fig. 15. Current density distribution in half-bridge "A" during 60 A commutation, evaluated at DC conditions.

B. *Minimization of parasitic capacitances*

Large coupling capacitances between the fast-switching nodes (exhibiting high d*v*/d*t* and high d*i*/d*t*) and the gate drive circuitry will cause larger displacement currents on the gate node, following the basic capacitor equation, where *Ig*(*t*) is the transient gate current, C_{rss} being the Reverse transfer capacitance of the power MOSFET, *C*par defines the total parasitic capacitance between the switching node and the gate drive circuitry, V_{ds} being the voltage from drain-to-source of the MOSFET and finally *t* being the transient time:

$$I_g(t) = \left(C_{rss} + C_{par}\right)\frac{dV_{ds}(t)}{dt} \qquad (6)$$

This effect can be partly mitigated by the gate driver if the connection from the driver to the MOSFET's gate exhibits low-impedance enabled by low external gate resistances and optimized gate loops, i.e. placing the MOSFET drives close to their respective power MOSFETs, utilizing the kelvin source connection and optimize the gate path routing by applying the strip-line principle – ideally with differential pair routing to enable matching impedances for the gate- and kelvin source connection. If a low parasitic capacitance between gate and drain node is not achievable, the large coupling could cause parasitic turn-on events, since the transient gate voltage rises above the devices' threshold with the effect that the channel of the power MOSFET turns on unwantedly. Large parasitic coupling capacitances will deteriorate the efficiency of any switching converter, since the stored parasitic energy stored in these parasitic capacitances will cause additional losses at commutation.

These two effects cause the necessity of reducing the coupling area via PCB design and to maximize the distance between critical nodes, as the basic definition of the capacitance indicates. **(4)**

This means in practical terms that the high side MOSFET must be placed as close as possible to the low side MOSFET to minimize the switching node area. Also, crossings of critical signals need to be avoided, respectively minimized, as much as possible. It could be beneficial to allow longer connections to walk-around critical areas and to maximize the distance between the nodes, for example, use thin tracks on the most outer layers PCB or even use SMT components to bridge critical signals in a 90-degree angle to minimize the overlapping copper area.

C. Considerations for mechnical integrity

Common heatsink attachments will introduce a force onto the PCB which could lead to mechanical stress in the PCB and hence in PCB warping. Although the test vehicle used for this experiment does not comprise a heatsink, the PCB is already enabled to house a heatsink. For this reason, a quadratic arrangement of the top-side-cooled power MOSFETs was implemented. This approach equalizes the forces along x- and y-directions due to the equidistant spacing of the heatsink fixtures and therefore minimizes the warpage even if a compression for gap-pads is required.

Nonetheless, if the gap-pad needs to be compressed further, a mechanical fixture to counteract the forces governed by the screws would be beneficial.

An additional solution to maintain a good mechanical integrity of the PCB while achieving good thermal performance could be to use a liquid gap-filler in between the heatsink instead of the typically used gap-pad. A liquid gap filler solution will decrease the necessity of compression forces and thus relax the mechanical constraints.

D. Discussion and further improvements

The PCB offers a clearance of 2.6 mm on the outer layers. This design requirement limits the flexibility of placing through vias and other components. If a lower clearance can be accepted, the power-loop could be build more densely and therefore the performance of the power-loops can be increased further.

The PCB, used as a research vehicle, exhibits numerous through-vias within the power-loop. While the large number of vias reduce the electrical resistance, they also increase the geometric mean distance and therefore potentially deteriorate the power-loop. The reason for this is simply that some current will flow in the outer vias additionally and hence increasing the geometric mean distance in comparison to a single row of vias, which is placed as close as possible to the switching node (while still fulfilling the required creepage distances).

The power-loop in this design is implemented to enable a vertical current flow, as **Fig. 7** shows. Another possibility would be to deploy a horizontal power-loop concept, as suggested by [1]. The big advantage of the horizontal power-loop is, that the geometric mean distances and hence the power-loop inductance is independent of the distances between the copper layers, or respectively, the thickness of the PCB. Nonetheless, practically the PCB thickness will not cause a significant impact for implementations similar to this test PCB since the horizontal dimension of the power-loop is about 45 mm, while the PCB thickness is only about 1.3 mm.

A further reduction of the power-loop inductance could be achieved by increasing the complexity of the PCB. The usage of buried- and blind vias will enable even tighter spacings and hence optimizing the distance between the conductive planes even further. Another approach would be to exploit all available copper layers in an “interleaving schema” as proposed in [9] while increasing the number of PCB layers further.

The advantage of these techniques is that the mutual inductance could be reduced further with the compromise of increased complexity resulting in higher PCB manufacturing costs.

IV. Conclusion

This paper presents the results of a performance optimization study conducted on a full-bridge board, a critical building block employed in a wide array of power converter topologies. However, these findings can be broadly applicable to general power converter design, independent of specific topologies or the choice of power devices.

The converter's improved performance is achieved by reducing key parasitic elements using optimized component placement and sophisticated PCB design techniques.

Especially the parasitic mutual inductance of the power-loop presents a significant impact on the switching speed of modern semiconductors. A careful design of the power-loop is recommended especially for wide-bandgap semiconductors (such as SiC or GaN devices) to exploit the benefits of the magnetic field compensation. This is showcased for novel automotive 750 V Silicon-Carbide power semiconductors in top-side-cooled power packages in a full-bridge topology, where the stray-inductance could be significantly reduced to 7 nH (on average). The different methods of the stray inductance characterization yielded results with high concordance with a relative deviation of less than 10 percent, whereas the method based on experimental results prove to be the most easy applicable while yielding viable results for further comparisons.

It is also noteworthy, that the vertical power-loop concept of this test-board exhibit a very low switch-node capacitance (about 2 pF) which is accountable to the top-side-cooled Q-DPAK power packages, since no thermal vias are needed for thermal management and thus, the effective area of the switch-node is minimized.

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