MOSFET With Lossless, High Precision Current Sensing in Motor Drive Applications

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Abstract

In motor drive inverters, the phase current must be measured to perform closed loop control. Cost-sensitive applications often use lower-accuracy, high-loss sensing technologies, such as resistive shunts, due to their low cost. Lossless, high accuracy technologies exist, but they typically target high-performance applications with fewer cost constraints. This paper discusses a new power device that integrates a power MOSFET with current sense technology and diagnostic functions into a single package. The lossless sensing provides significant thermal advantages and high measurement accuracy, making the device suitable for a wide range of motor control applications.

1 Introduction

Current sensing in cost-sensitive motor drives is typically realized with resistive shunts combined with analog signal acquisition circuits. The resistive shunt solution provides adequate current sensing accuracy at an attractive cost, but with increased power dissipation due to losses in the shunt. Since power losses increase with the square of the current, higher current levels necessitate costly thermal management approaches, in the design of the PCB and cooling system, to ensure sufficient overall reliability of the solution.

While lossless current sense solutions are available, such as Hall, AMR (Anisotropic Magneto Resistance), and Current Transformer [1], these solutions often come with a higher cost than resistive shunts, making them unacceptable for many applications. Conversely, current sensing utilizing the power MOSFET's $R_{DS,on}$, as proposed in [2], is a lossless and low-cost solution. This solution suffers from $R_{DS,on}$ variation over temperature of more than 100% of its nominal value [3], making it suitable only for applications with lower accuracy requirements.

The device discussed in this paper integrates a power MOSFET, current sense capability, and diagnostic features into a single PG-TISON package to realize a 'current sense MOSFET, also referred to as a CSFET, see Fig. 1. The current sense IC is based on a current-mirror approach where the sense output (IMON) is proportional to the drain-to-source current of the power MOSFET. The sensing technology is virtually lossless, and the sense signal interfaces directly to an analog-to-digital-converter (ADC) with only a few passive, low-cost external components, such as resistors and capacitors. The CSFET utilizes a chip-on-chip design, where the IC sits on top of the MOSFET, resulting in the same footprint and comparable $R_{DS,on}$ as that of a conventional power MOSFET without sensing capability.

The current sense IC and MOSFET are matched and optimized for current sensing accuracy. Combined with integrated real-time temperature and offset compensations, the current sensing accuracy across all operating conditions is superior to resistive shunts with analog signal acquisition circuits.

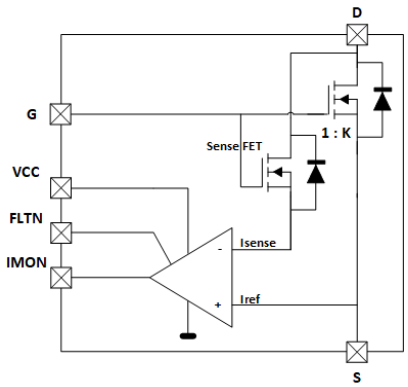


Fig. 1 CSFET device integrating a MOSFET with current sense and diagnostic capabilities.

2 Application of CSFET

A 3-phase motor drive, realized with three CSFET low-side devices and three conventional MOSFET high-side devices, is shown in Fig. 2. In terms of current sensing capability, the configuration is comparable to a shunt resistor placed between the source of the low-side MOSFET and GND.

IMON is a current-source output which is proportional to the MOSFET current. Current outputs typically provide better noise/EMI immunity than voltage outputs and can simplify PCB layout.

IMON is converted to a voltage, VIMON, and level-shifted for the ADC using a simple resistive divider which is supplied by the ADC reference. Overcurrent, overtemperature, and undervoltage faults are communicated on the FLTN pin that interfaces directly to the microcontroller with only a pull-up resistor needed.

For applications with high current requirements, devices can be seamlessly paralleled by shorting the current source IMON signals together to represent the sum of the current through the parallel power devices. The combined IMON signal is translated into a voltage with a single resistive divider. The open-drain FLTN pins can also be tied together, requiring only a single pull-up resistor on the combined FLTN signal.

The device supports bi-directional sensing with IMON valid when the gate is on. This is comparable to a resistive shunt sensing scheme where the current is also defined when the low-side gate is on.

An example of current sense with CSFET is shown in Fig. 3, where the top part of the figure shows positive current (into the motor) and the bottom part shows negative current (out of the motor). The IMON signal (blue) is reporting when the low-side gate signal (red) is on. When the low-side gate signal is off, the IMON signal settles at the mid-point voltage as defined by the resistive divider placed on the IMON signal.

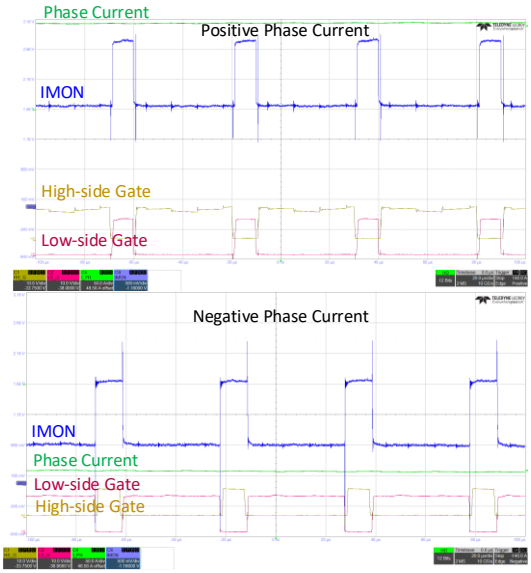


Fig. 3 Current sense with CSFET at 150A, 20kHz SVPWM.

3 Thermal Comparison

To experimentally investigate the value proposition of lossless current sensing, two 3-phase inverter boards were developed, see Fig. 4. As low-side devices, the red board on the left utilizes three 40 V / 0.9 mΩ CSFETs with integrated current sensing, from Infineon Technologies. The blue board utilizes three conventional MOSFETs as low-side devices and resistive shunts for current sensing. Except for the low-side power devices, the current sensing technology and minor layout modifications to accommodate shunts, the two

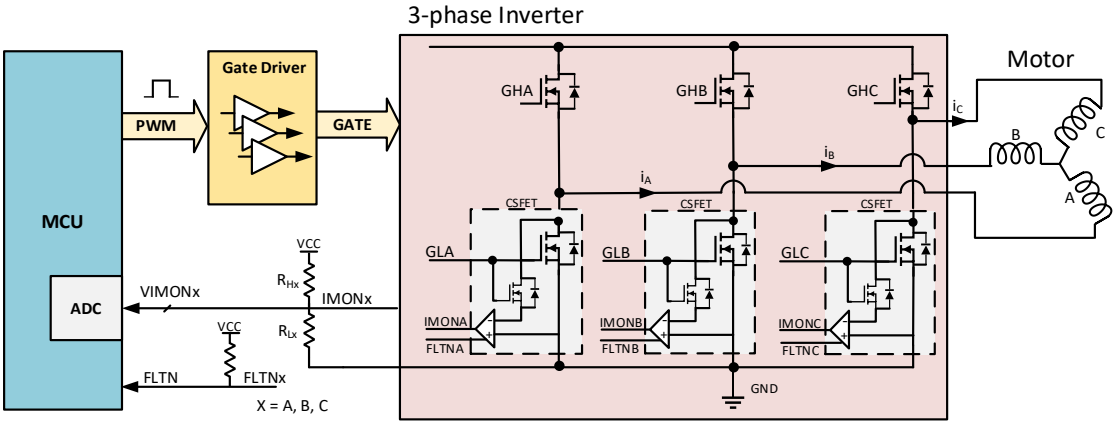


Fig. 2 A 3-phase motor drive with CSFETs as low-side devices for lossless low-side current sensing.

boards are identical. These setups enable a direct thermal comparison between the two solutions by driving an identical motor load, under identical operating conditions and with an identical control scheme. Any thermal difference can therefore be attributed to the current-sensing implementations and the low-side power devices.



Fig. 4 3-phase inverter boards used for thermal comparison of CSFET and resistive shunts.

The thermal comparison included four different configurations of low-side devices and shunts as summarized in Table 1. Configuration 1 is realized with the board on the left in Fig. 4. It features CSFET and its integrated current sense with no need for resistive shunts. Configuration 2-4 are all realized with the board on the right in Fig. 4 but with different combinations of MOSFETs and shunts. Configuration 2 has a low-side MOSFET with an $R_{DS,on}$ of 0.9 mΩ (same as the CSFET) and a resistive shunt of 300 μΩ for current sense. Configuration 3 utilizes the same low-side MOSFET as configuration 2 but with a smaller shunt resistor of 200 μΩ. Finally, configuration 4 utilizes a low-side MOSFET with an $R_{DS,on}$ of 0.7 mΩ and a shunt resistor of 200 μΩ. In terms of combined resistive losses, configurations 1 and 4 are comparable.

All configurations use the same conventional 0.7 mΩ $R_{DS,on}$ MOSFET as the high-side device.

Configuration	Low-side device	Resistive shunt
1	CSFET with 0.9 mΩ $R_{DS,on}$	No shunt
2	MOSFET with 0.9 mΩ $R_{DS,on}$	300 μΩ
3	MOSFET with 0.9 mΩ $R_{DS,on}$	200 μΩ
4	MOSFET with 0.7 mΩ $R_{DS,on}$	200 μΩ

Table 1 Configurations of low-side devices and resistive shunts used in thermal comparison.

The experimental setups were controlled using Space-Vector-Modulation (SVPWM), with a 20 kHz switching frequency and 1μs deadtime. While performing a sweep in motor phase current, key temperature locations (a. low-side MOSFET case, b. high-side MOSFET case, c. heatsink core d. PCB surface adjacent to a phase-leg) were monitored with a thermal camera, and their steady-state values were captured, as shown in Fig. 5.

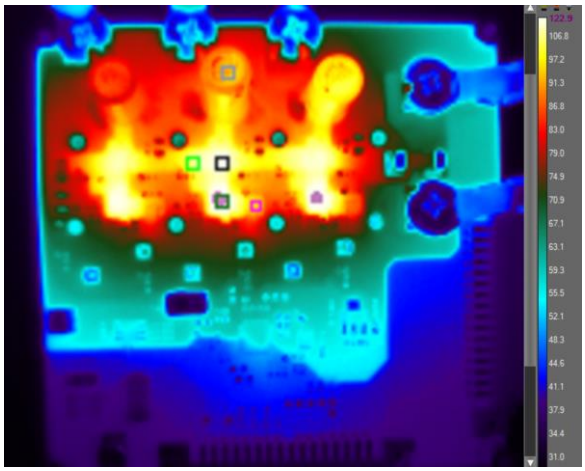


Fig. 5 Thermal imaging of 3-phase inverter board.

3.1 Switching Devices Thermal Results

The results of the low-side and high-side MOSFET thermal comparison are shown in Fig. 6 and Fig. 7, respectively. The plots show power device case-temperatures as a function of peak phase current. Across the current range, the CSFET-based inverter operates at lower device temperatures than all the resistive shunt configurations.

Comparing the CSFET configuration with the 0.9 mΩ MOSFET + 300 μΩ shunt, the low-side and high-side MOSFET temperatures are reduced by 18°C and 11°C, respectively, at a 150 A peak phase current.

This temperature reduction can improve inverter reliability or be traded for higher phase current at the same case-temperature. An 18°C temperature advantage on the CSFET board allows the inverter to drive approximately 10% higher current while maintaining the same device temperature.

Despite comparable resistive losses, it is noted that the CSFET inverter runs cooler than the 0.7 mΩ MOSFET + 200 μΩ shunt configuration across all observed temperatures.

Although all configurations use identical high-side devices, the high-side case-temperature is lowest with the CSFET approach because reduced total inverter loss means lower the heatsink temperature, which in turn reduces the temperature of the entire board.

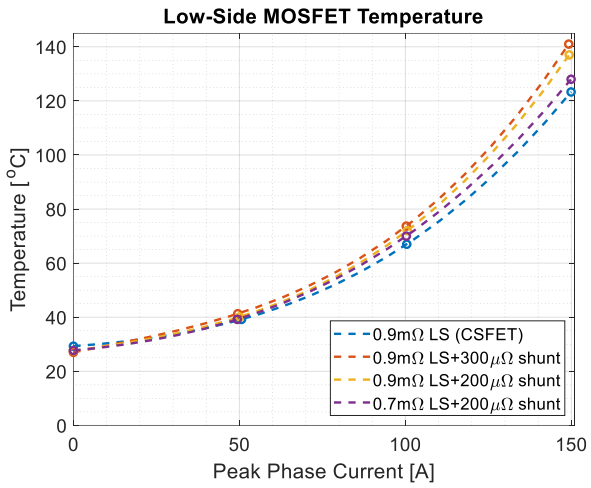


Fig. 6 Low-side MOSFET temperature comparison.

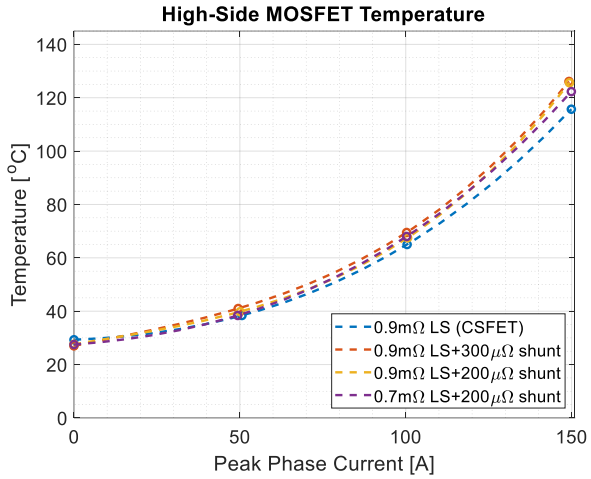


Fig. 7 High-side MOSFET temperature comparison.

3.2 Heatsink Thermal Results

Fig. 8 shows the core temperature of the heatsink mounted on the backside of the PCBs. Comparing the CSFET with the 0.9 mΩ MOSFET + 300 μΩ shunt, the heatsink temperature is reduced by approximately 9°C at a 150 A peak phase current.

The lower heatsink temperature allows the inverter to drive approximately 10% higher current while maintaining the same heatsink temperature.

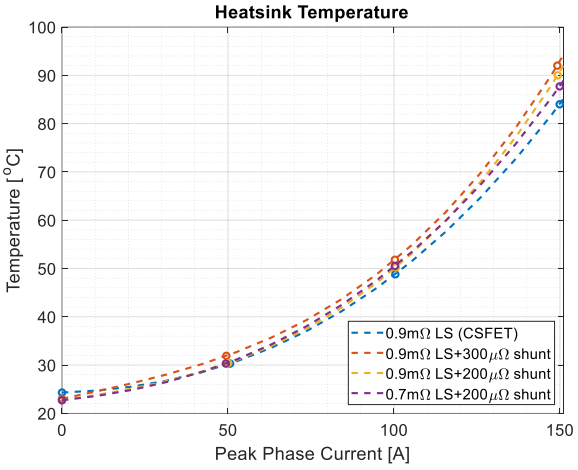


Fig. 8 Heatsink temperature comparison.

3.3 PCB Thermal Results

Fig. 9 shows the temperature of the PCB surface adjacent to the phase legs. Comparing the CSFET to the 0.9 mΩ MOSFET + 300 μΩ shunt, the PCB temperature is reduced by approximately 15°C (13%), at a 150 A peak phase current.

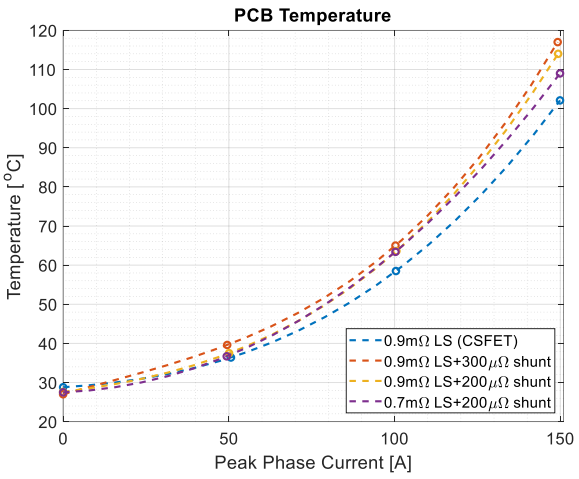


Fig. 9 PCB temperature comparison.

3.4 Analysis of Thermal Results

Table 2 summarizes a thermal comparison of the four configurations at 150 A peak phase current. The inverter using CSFETs shows significant improvement over the resistive shunts-based solutions, even when compared to a low-side implementation with a 0.7 mΩ $R_{DS,on}$ MOSFET.

Configuration	Temperature @ 150 A		
	MOSFET LS/HS [°C]	Heatsink [°C]	PCB [°C]
CSFET with 0.9 mΩ $R_{DS,on}$	123/115	84	102
MOSFET with 0.9 mΩ $R_{DS,on}$ + 300 μΩ shunt	141/126	93	117
MOSFET with 0.9 mΩ $R_{DS,on}$ + 200 μΩ shunt	137/125	90	114
MOSFET with 0.7 mΩ $R_{DS,on}$ + 200 μΩ shunt	128/122	88	109

Table 2 Summary of 3-phase inverter temperatures with different low-side and sense configurations.

Part of the thermal improvements can be attributed to the elimination of the losses in the resistive shunts (at 150 A peak, approximately 5 W power losses in the 300 μΩ resistive shunts and 3.3 W power losses in the 200 μΩ resistive shunts). However, the resistive losses alone are not enough to explain the thermal difference. This is confirmed by the 0.7 mΩ MOSFET + 200 μΩ shunt configuration. This configuration has the same total resistive losses as the CSFET inverter and yet it runs hotter across all measurement points.

A key factor is the PCB layout changes necessary to accommodate the mounting of the shunts on the surface of the PCB. The conventional low-side device has a shunt resistor placed between the source of the MOSFET and power ground as shown on the left side of Fig. 10. The “top” of the shunt and the source of the MOSFET connect to an isolated “island” that duplicates through the layers of the PCB. The island is kept small to minimize stray inductance and PCB size but it reduces the ability to conduct heat away from the low-side device.

The placement of this shunt resistor causes the source to be electrically and thermally separated from the ground plane which consequently results in reduced thermal dissipation capability. The CSFET solution connects the source of the low-side device directly to a large power ground plane which effectively transports heat away from the hot-spot and enhances heatsinking capability of the whole PCB.

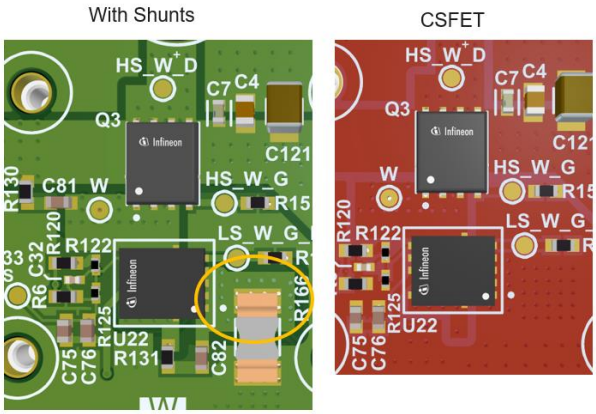


Fig. 10 Placement of resistive shunts creates an isolated island at the source of the low-side MOSFET.

4 Conclusion

The experiments presented in the paper demonstrate that the CSFET enables significant reduction in thermal stress, which can either improve reliability or increase output current capability without additional cooling. The compact integration of high-accuracy, lossless current sensing simplifies the design by eliminating the need for bulky, heat-generating shunt resistors and associated precision amplifier circuitry.

A comparison of four different configurations of low-side devices and sense technologies was used to demonstrate the thermal performance.

It was discussed how the CSFET enables optimized PCB layout that effectively dissipates heat away from the hot-spots. This characteristic was demonstrated by comparing the CSFET to a larger MOSFET, with lower $R_{DS,on}$. Even with equal resistive losses, the CSFET outperformed by operating at lower temperatures.

References

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[2] Rok Pajer, et al. "Evaluation of MOSFET RDSon Resistance for Current Measurement Purposes in Power Converter’s Applications", 2015 International Conference on Electrical Drives and Power Electronics (EDPE)

[3] Infineon Technologies, “ISC007N04NM6 OptiMOS™6 Power-Transistor, 40V Datasheet”, 2023