Ensuring the safe operation of MOSFETs in bidirectional protection power switch (BDPS) applications

Guidelines for battery protection against abnormal conditions

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Introduction

The global market for battery-powered applications is rapidly growing, including power tools, consumer robotics, light electric vehicles, and many others.

The evolution of switched-mode power supply (SMPS) topologies enables designers to ensure safe charging and discharging of the equipment's battery using bidirectional converters through the same terminal. However, to meet the safety requirements and prevent damage and failures, those SMPS need to be equipped with a protection switch. Uni- and bidirectional switches are widely used to charge/discharge and protect against various failures like in-rush current, overcurrent, short-circuit, reverse voltage, or over-and under-voltage.

In the following sections, we present the guidelines that can help designers to develop an appropriate unidirectional, or bidirectional direction protection switch circuit such that the MOSFETs are operating within their safe operating area.

What is a bidirectional power switch (BDPS), and how to realize it

A bidirectional switch is an active switch that has the ability to block the current in both directions. It offers effective protection against abnormal conditions like a short-circuit, reverse voltages, etc., that occur accidentally or due to manual errors in battery/SMPS terminals.

A BDPS can be realized by using two N- or P-channel FETs. N-channel FETs are preferred out of these two due to low $R_{DS(on)}$ and cost compared to P-channel FETs. Because of the body diode, a single MOSFET can pass or block the current in only one direction. The configurations shown below in Figure 1 are required to realize a BDPS.

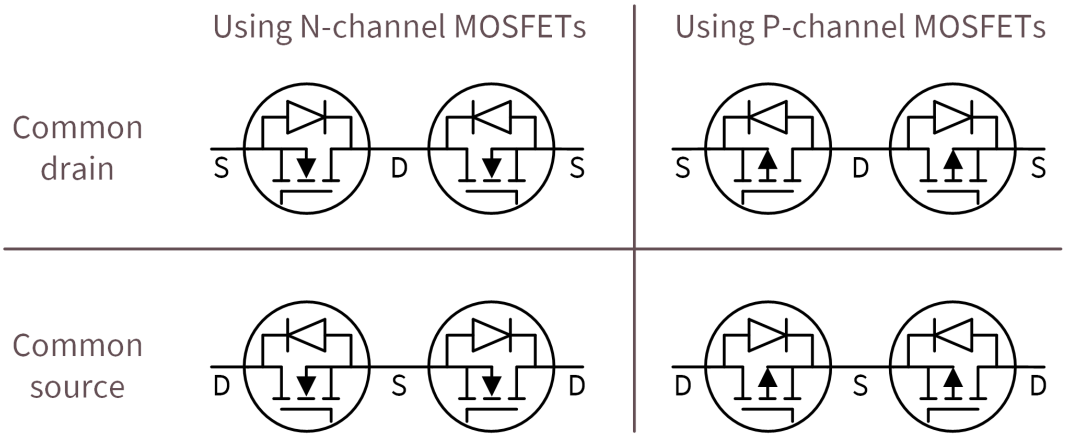

Figure 1. *BDPS configurations*

Selecting the proper MOSFET for a protection power switch

To enhance efficiency, battery backup duration, effective protection against failures, and to avoid the cost of thermal solutions, MOSFET selected for BDPS shall offer:

- Lower power dissipation
- Better thermal interface
- Avalanche-free operation
- Identical current sharing between parallel MOSFETs
- Proper and safe turn on/off operation

Considering the various parasitic effects, the MOSFETs used for BDPS ensure their safe operation in normal and abnormal cases that a certain application can expect. Below is the high-level schematic of a system with a battery, a load, and a BDPS. Additionally, various wires and parasitics are modeled. A worst-case scenario depicted in a short circuit event is analyzed to correctly select the type and amount of MOSFETs for the BDPS.

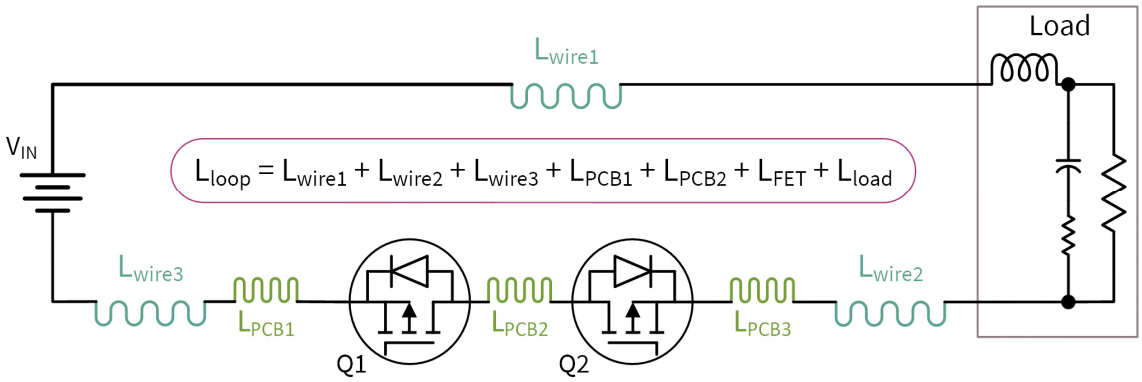

Figure 2. *MOSFETs topology as low-side BDPS*

Table 1. *Detailed design parameters assumed in this article to illustrate the MOSFET selection for BDPS*

Parameters	Variable	Value
Input voltage	V_{IN}	50 V
Continuous current	I_{cont}	50 A
Cable and parasitic inductance	L_{loop}	1.5 µH
Short-circuit current (*)	I_{SC}	100 A
Controller detection time or short circuit duration	t_{SC}	100 µs
Change in current during short circuit	dI/dt	7 A/µs
Maximum allowable temperature rise	T_{max}	90°C
Maximum Ambient temperature	T_{amb}	50°C

(*) Can be estimated from source/battery voltage and its impedance

Avalanche-free operation

Typically MOSFETs used as protection switches are programmed to turn on slowly to limit inrush current and turn off as fast as possible to protect against abnormal conditions (such as a short-

circuit or an overcharge etc.). During turn on/off, MOSFETs shall be operated within the safe limits as per chapter " Safe operation of MOSFETs."

The fast switching off of MOSFETs in the events like a short-circuit leads to high dI/dt currents through the loop inductance and induces high voltage (V_L = L*dI/dt). Eventually, this voltage adds to the drain voltage of the MOSFET (as shown in Figure 3), which could lead the MOSFET into avalanche. The maximum voltage across the MOSFET used in the protection switch can be calculated by Equation 1. To avoid MOSFET avalanching, the breakdown voltage of the selected MOSFET needs to be higher than the maximum voltage (V_{max}) calculated. In this case, IPT020N10N5, an OptiMOS™ 5 100V power MOSFET in TO-Leadless (TOLL) package, is selected.

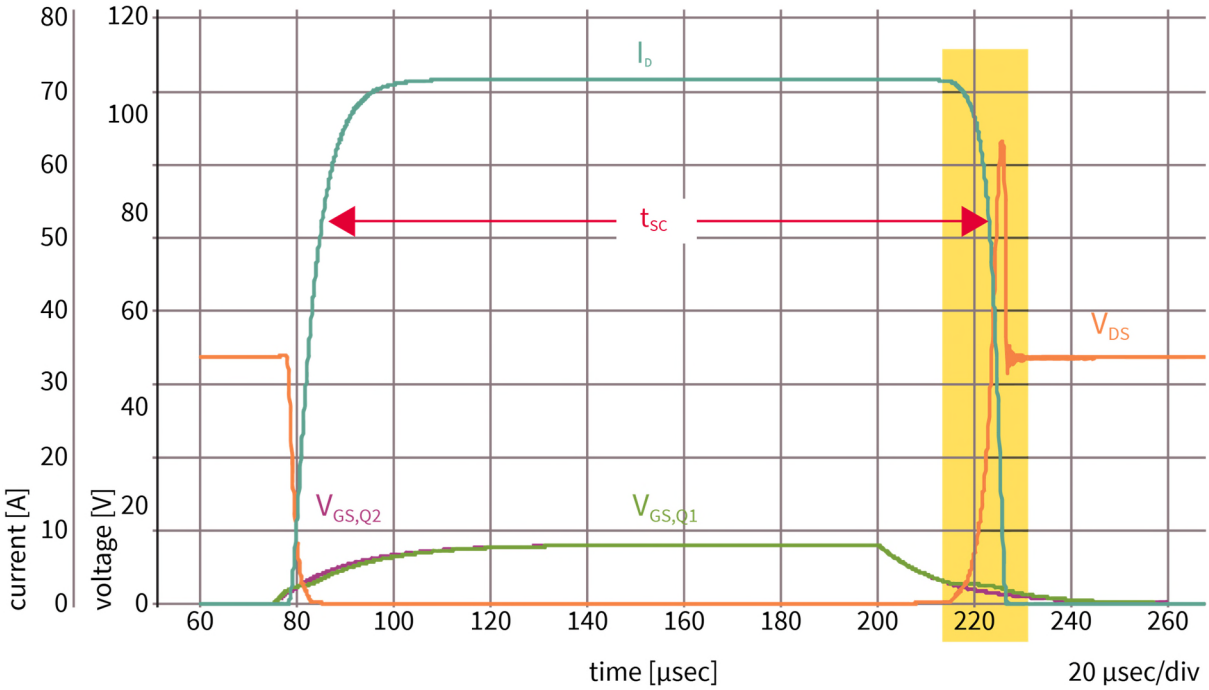

Figure 3. *Typical waveform during short-circuit*

$$V_{max} = V_{IN} + L_{Loop} \cdot \frac{dI}{dt} \text{ [V]} \qquad \textbf{Equation 1}$$

Design: $V_{max} = 50\text{ V} + (2 \cdot 1.5\text{ µH}) \cdot 7\frac{\text{A}}{\text{µs}} = 92\text{ V}$

Selected MOSFET: 100 V, 1.5 mΩ **(IPT020N10N5)**

Maximum current per MOSFET

Equation 2 calculates the maximum current ($I_{Allowed}$) that a MOSFET can carry at the maximum operating temperature allowed by each application.

$$I_{allowed} = \sqrt{\frac{T_{max} - T_{amb}}{R_{DS(on)@100°C} \cdot R_{thJA}}} \text{ [A]} \qquad \textbf{Equation 2}$$

Design: $I_{allowed} = \sqrt{\frac{90°C - 50°C}{2.16\text{ mΩ} \cdot 40°C/W}} = 21.5\text{ A}$

$R_{DS(on)@100°C} = 2.16\text{ mΩ}$ from device datasheet
$R_{thJA} = 40°C/W$ for device on PCB, 6 cm² cooling area

From Equation 2, it can be noted that a MOSFET with lower thermal resistance allows for higher current through it.

Infineon's MOSFET portfolio is available in different packages offering various thermal resistances. (Figure 4).

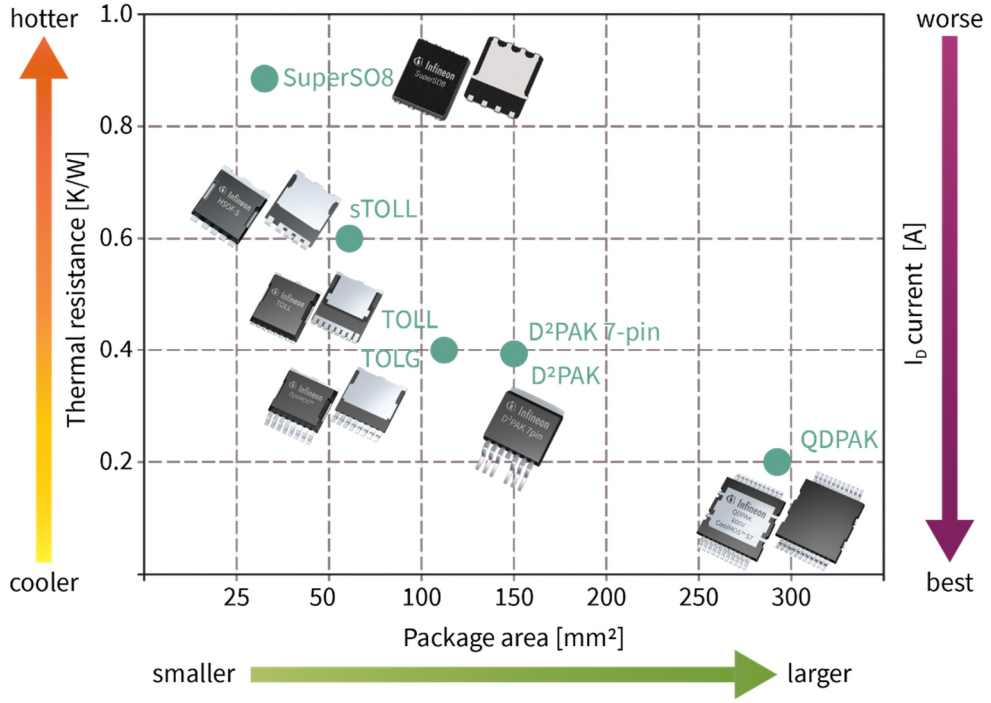

Figure 4. *MOSFET package area vs. thermal resistance vs. current*

Number of MOSFETs required in parallel

Typically, MOSFETs are paralleled for high-current applications to reduce losses and distribute temperature evenly on the PCB.

Equation (3) estimates the number of MOSFETs in parallel (N) that can achieve the desired operating temperature

$$N = I_L \cdot \sqrt{\frac{R_{DS(on)} \cdot R_{thJA}}{T_{max} - T_{amb}}} = \frac{I_{cont}}{I_{allowed}}$$ **Equation 3**

Design: $N = \frac{50\ A}{21.5\ A} = 2.33 \approx 3$ MOSFETs

The calculated value is rounded up to the next higher value. 3 MOSFETs are selected in parallel

MOSFETs have a positive temperature coefficient, meaning that $R_{DS(on)}$ increases with the device temperature.

Due to I^2R or conduction losses, the die temperature of the MOSFETs increases. But the temperature of the MOSFET with low $R_{DS(on)}$ shares a higher current, and its $R_{DS(on)}$ increases due to higher I^2R losses, resulting in a stable thermal state after a specific duration.

However, the MOSFET with the lowest $R_{DS(on)}$ is the hottest one, and it must be ensured that the temperature on this MOSFET shall be less than the operating temperature specified in its datasheet.

Power dissipation

Conduction or I^2R losses (P_{cond}) of a MOSFET is the lone contributor to the losses in a BDPS. MOSFETs best-suited for BDPS offer best-in-class low on-resistance ($R_{DS(on)}$). As discussed previously, the $R_{DS(on)}$ of the MOSFET increases with increasing temperature. For safe operation, MOSFETs are mainly operated below 100°C. Considering the $R_{DS(on)}$ of MOSFETs at 100°C, the conduction losses of the MOSFET can be calculated using Equation 4.

$$P_{\text{cond}} = \left(\frac{I_{\text{cont}}}{N}\right)^2 \cdot R_{\text{DS(on)@100°C}} \text{ [W]} \qquad \textbf{Equation 4}$$

$$\text{Design: } P_{\text{cond}} = \left(\frac{50\text{ A}}{3}\right)^2 \cdot 2.16\text{ m}\Omega = 0.6\text{ Watt}$$

Due to its more than 40 years of MOSFET experience and continuous package and technology innovation, Infineon can offer decreased $R_{DS(on)}$ values when moving from OptiMOS™ 3 to OptiMOS™ 5 in the same package to enable better performance in applications such as BDPS where low $R_{DS(on)}$ is critical.

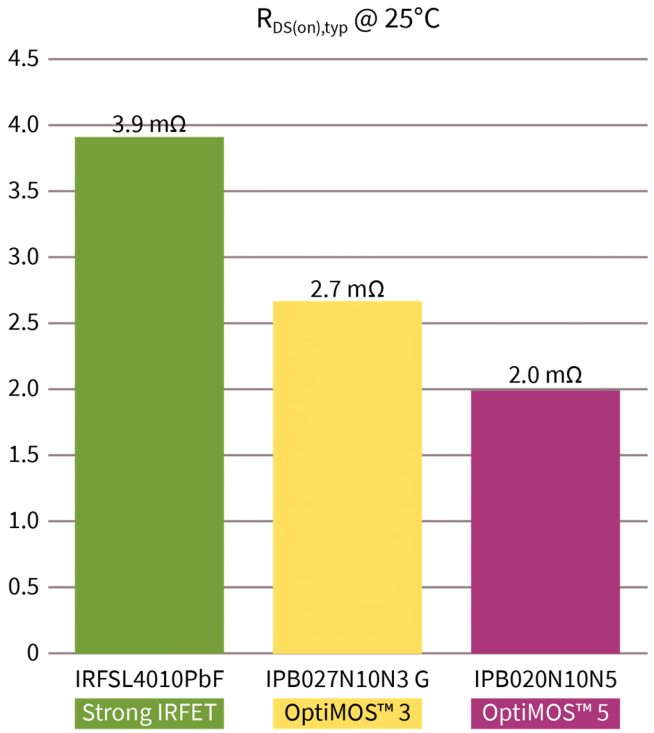

Figure 5. *$R_{DS(on)}$ improvement over Infineon MOSFET technologies and generations*

Temperature rise

The maximum allowable temperature rise on the device depends on the application area. Case temperature of the MOSFET is calculated from Equation 5.

$$T_{J_{FET}} = \left(\left(P_{cond} \cdot R_{thJA}\right) + T_{amb}\right)\ [°C] \qquad \textbf{Equation 5}$$

Design: $T_{J_{FET}} = (0.6\ W \cdot 40°\ C/W + 50°C)\ °C = 74°C$

$R_{thJA} = 40°\ C/W$ (from the datasheet of IPT020N10N5)

The estimated temperature on the MOSFET is below the maximum allowable temperature rise (T_{max}) on the devices (i.e., 95°C) and satisfies the design requirement.

Safe operation of MOSFETs

Usually, housekeeping ICs (such as battery monitoring ICs, comparator ICs, etc.) or controllers are employed to detect faults and control protection switches. These controllers need time to detect and respond to the faults. In the case of a short-circuit (as shown in Figure 3), MOSFETs shall withstand and shall not fail for such response periods (T_{sc}).

A slow turn-on of protection switches is mainly preferred to limit in-rush current and the fast turn-off to protect against faults. During this turn-on/off time, MOSFETs are subjected to pass through linear mode operation (highlighted by the yellow shaded region in Figure 3). Therefore, the MOSFETs selected as protection switches must be carefully analyzed for:

- Transient junction temperature rise
- Linear turn-on/off operation

Transient junction temperature

Short high-current pulses during a short-circuit period (T_{sc}) or short high-power dissipation during inrush current limiting period can create a hot spot on the MOSFET die. To ensure safe operation, the transient junction temperature of the MOSFET must below the silicon operating temperature specified in the device datasheet.

Equation 6 below uses the transient thermal impedance from the datasheet to estimate the junction temperature on the FET.

$$T_{JSC} = \left(\left(\frac{{I_{SC}}^2 \cdot R_{DS(on)}@100°C}{N} \cdot Z_{thJC1}\right) + T_{J_{FET}}\right)\ [°C] \qquad \textbf{Equation 6}$$

Design: $T_{JSC} = \left(\left(\frac{100\ A^2 \cdot 2.16\ m\Omega}{3} \cdot 0.04°C/W\right) + 85°C\right) = 85.3°C$

Z_{thJC1}: refer to Figure 6

Short circuit current of 100 A for 100 µs through MOSFET increase temperature by 0.3°C. At the end of short circuit event temperature rise of FET is 85.3°C

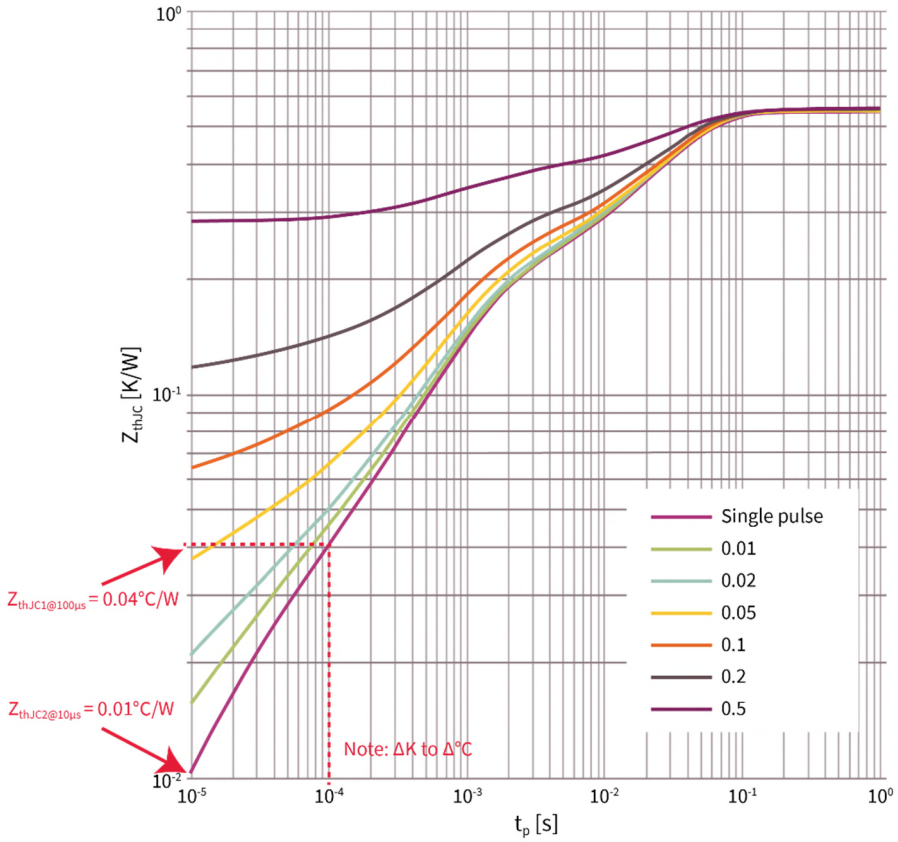

Figure 6. *IPT020N10N5 transient thermal impedance*

Linear turn on/off operation

During a turn-on/-off event, the MOSFET used as the protection switch accommodates linear mode operation. Under abnormal conditions such as a short-circuit, a safe design ensures a MOSFET operation within its safe operating area (SOA).

In MOSFETs datasheets, SOA boundaries are defined at a specific squared pulse duration. As explained in [1], the protection switch operates at certain dV/dt or dI/dt, which means that non-squared power pulses are applied during turn-on/off.

So, it is not possible to use the SOA chart from MOSFETs datasheets directly. Instead, in case of critical and abnormal conditions, one should perform the following calculation steps:

- **Step 1:** Calculate transient power dissipated

$$P(t) = V_{DS}(t) \cdot I_D(t) \text{ [W]} \qquad \textbf{Equation 7}$$

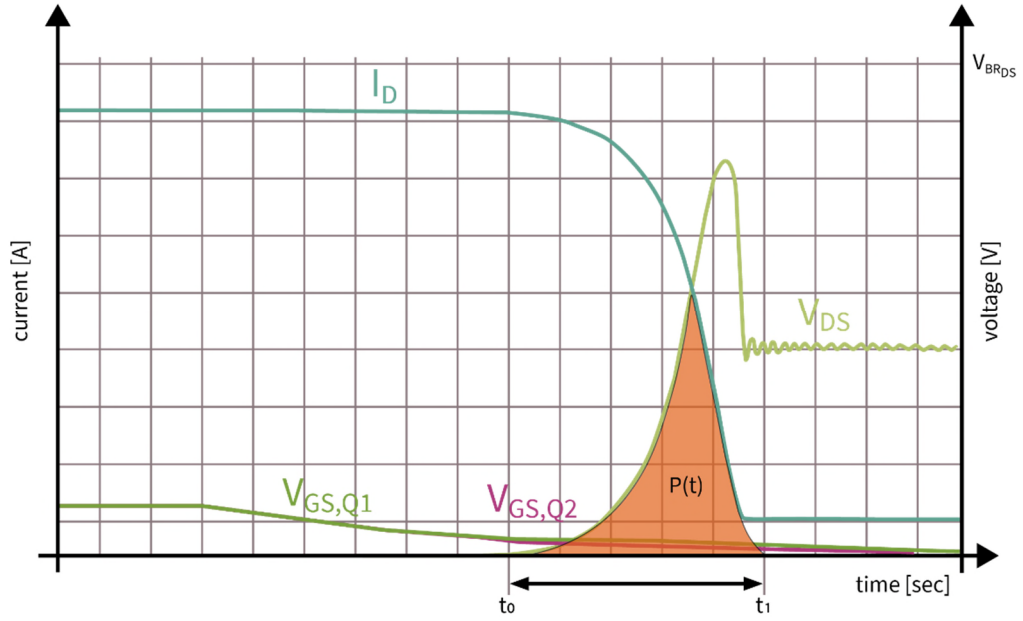

Figure 7. *$V_{DS}(t)$, $I_D(t)$, and $P_D(t)$ waveforms*

- **Step 2:** Integrate the power dissipated during turn on/off event to calculate dissipated energy

$$E = \int_{t_0}^{t_1} P(t)dt \ [\mathrm{J}] \qquad \textbf{Equation 8}$$

Design: $E = 15\ \mathrm{mJ}\ @\ \Delta t = 10\ \mu s$

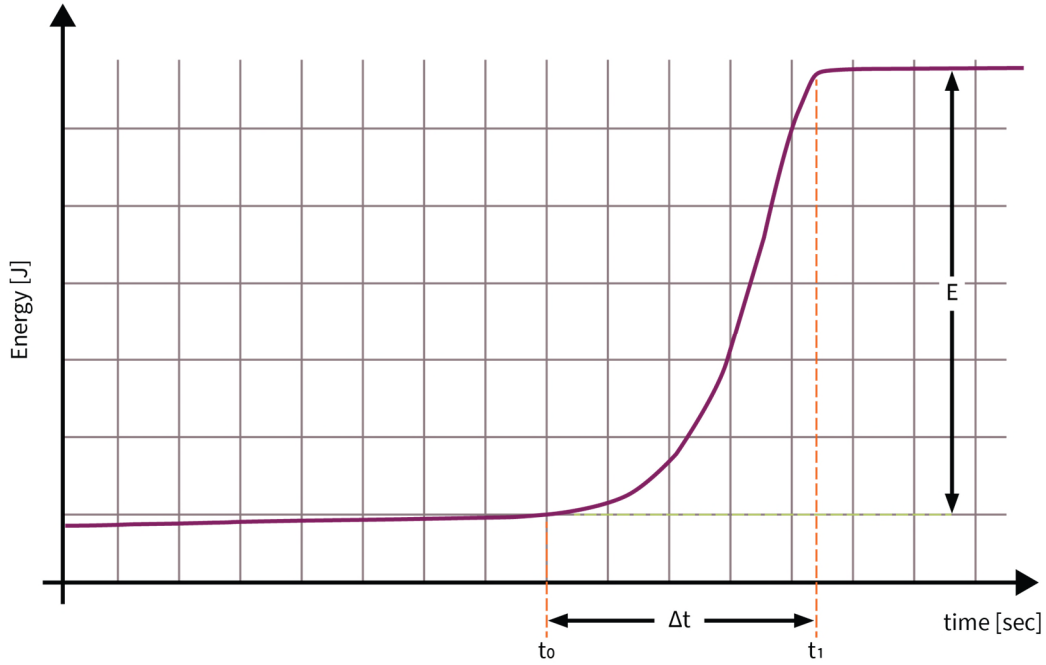

Figure 8. *Energy dissipation*