How to Properly Power FPGAs in Advanced Hybrid and Digital Phased Array Radars

Publication date: February 13, 2024
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Beamforming and beam-steering technologies used in military applications have seen significant advances, especially when coupled with the emergence of 5G communications and commercial space data communications. This progress led to the introduction of active electronically scanned array (AESA) and/or phased-array systems, which are now more affordable and available in full digital and/or hybrid configuration. The majority of

the active spectrum is now covered by these systems, making them suitable for use in radar, electronic warfare (EW), and various military communications systems.

Radar first transitioned from mechanically scanned to analog phased array in the 1970s primarily supporting military programs for tracking and fire control. These systems greatly enhanced the number of targets detected and tracked, showed greater resistance to blockers, reacted faster, and greatly reduced maintenance costs due to the reduction of mechanically steered parts.

The concept of a digital phased array, in which each element is controlled from an analog-to-digital (ADC) or digital-to-analog (DAC) pair, provides an order of magnitude better performance and operations across a larger part of the spectrum. Paired with powerful and configurable software, the technology is poised to displace most of the existing mechanically scanned and analog technologies due to its ability to perform digital beamforming/steering and direct digital sampling from each antenna element. Another major benefit is that losing a channel or antenna element has a negligible effect on system performance.

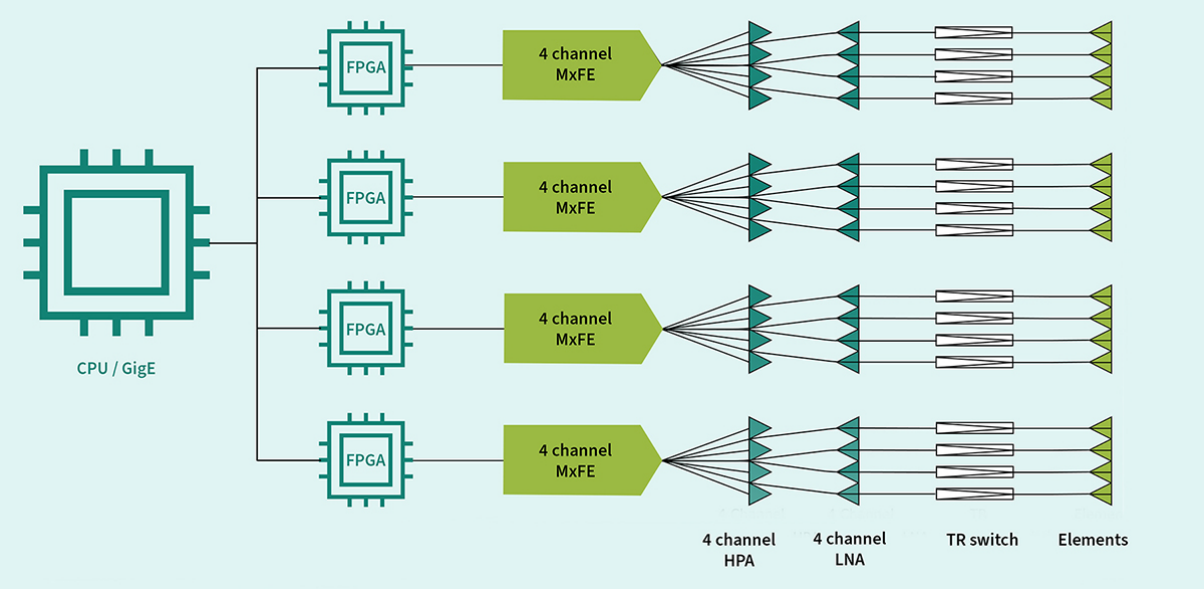

Figure 1: Digital phased array: MxFE, or multifunction front end, contains a number of ADC/DAC pairs.

Significant cost barriers, along with power and thermal constraints, strangled deployment of these systems due to expensive and power-hungry, ADCs and DACs paired with equally power-hungry and costly field-programmable gate arrays (FPGAs). While concerns also lingered around latency and bus design, efficiency losses in the amplification and gain stages worsened the problem.

Major semiconductor efficiency improvements over the last five years have also lowered cost barriers, enabling deployment of next-generation phased-array designs. The challenge still remains, however, about how to efficiently power these systems in a way that considers watts consumed and radiated, yet is mindful of size and geometry constraints.

There are various considerations and solutions for powering military and space FPGAs, ADCs, DACs and other digital assets in designs that require higher reliability than automotive, industrial or consumer. Whether it be on-orbit, on-wing, terrestrial, or in a munition, there are unique considerations to choosing a power solution that matches the robustness of the rest of the electronic design.

A compromise solution: hybrid phased array

The compromise solution was to use a hybrid phased array in which the FPGAs, ADCs and DACs (let's call them together "digitizers") were fewer and moved farther away from the antenna. The digitizers drove lower-power analog beamformer/beam-steering systems that in turn drove a sub-array. Gain could be inserted either before or after the beamformer, depending on the design. (Figure 2.)

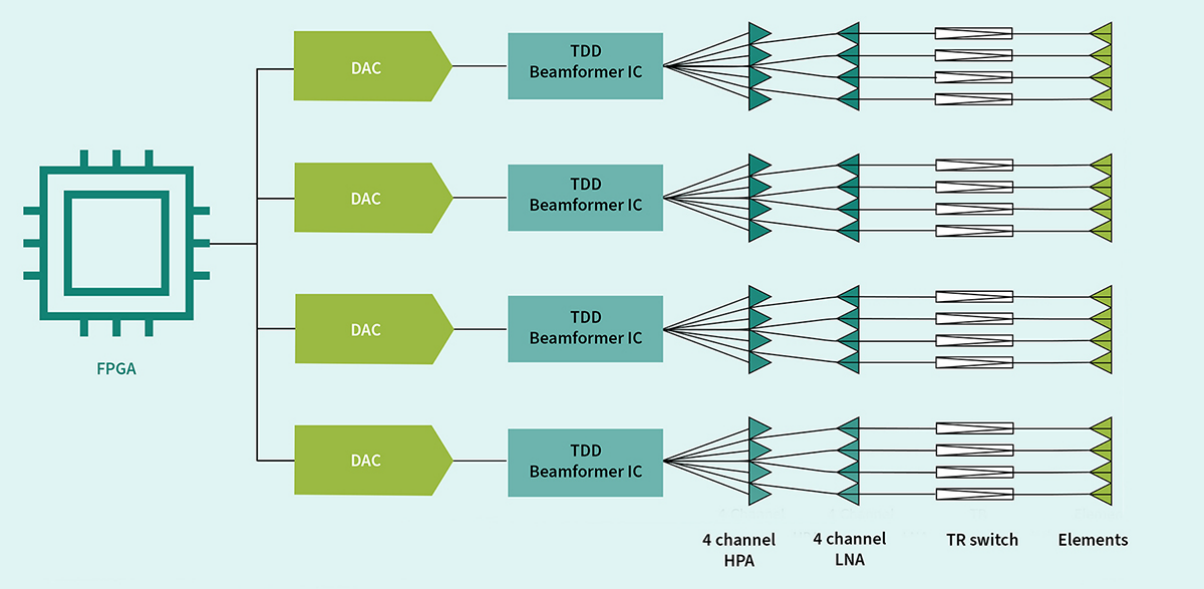

Figure 2: A diagram shows a hybrid phased array.

The primary drawbacks of this approach include redundant channel loss, spectrum reduction, and less array efficiency due to constraints driven by sub-array architecture. Advantages are less power consumption and reduced thermal concerns, lower cost, and the benefits of a mostly analog front end.

Over the last five years, we've seen significant improvements in power and thermal semiconductor efficiencies, with new competitors driving down prices to the point that next-generation phased-array systems are being deployed with a true digital architecture across many more applications and markets. But efficiently powering these systems remains a challenge given the watts consumed and wasted, and considers the size and geometry constraints due to the high density of electronics behind the antenna elements.

Of the key enablers of digital phased arrays (AESAs), let's focus on the FPGA that is a critical component of both digital and hybrid systems. FPGAs are chosen to perform extremely fast

calculations to support signal isolations, Fast Fourier Transforms (FFTs), and I/Q data extraction [in-phase (I) and quadrature (Q) elements] from systems that may be sampling 16 bits at 20 gigasamples per second (Gs/sec). When transmitting, the chain is reversed and the FPGA is also critical in calculations that form and steer the radio-frequency (RF) beams.

FPGAs require reliable sequenced power many times, consuming a high number of watts depending on duty cycle and active function. The three most important considerations in your power design for an FPGA in higher reliability applications are:

1. Maintaining voltage regulation on power rails: FPGA power rails have tight regulation requirements. The needs of these rails are progressively more challenging for newer FPGAs, where the target regulation and allowable tolerance are lower, while the load step transient increases.

2. Thermal management: Greater FPGA computing capability requires more power, a variable that adds more design complexity to prevent power-supply component temperatures from exceeding maximum limits. This reality is further exacerbated with FPGA trends, where the lower voltage-rail requirements generally lead to lower efficiency (i.e., greater power loss of the power converter) and the desire to keep the power-supply area small concentrates loss into a tighter space and increases temperature rise.

3. Proper power up and down: The addition of new features and computing capabilities of FPGAs increases the number of power rails needed. Some FPGAs offer different ways for power management, where the options are generally between reducing power-conversion size and count around the FPGA versus additional flexibility for power-saving modes. All of these rails have strict requirements, which include:

    - Sequencing, where some rails need to come up and be in regulation before others, and vice versa during power down
    - Power supply ramp, where the voltage rail needs to rise monotonically within a specified time

Powering FPGA and system level needs: point of load converters

To meet these requirements, point of load (PoL) converters are typically used, where a DC-DC converter is placed as close to the FPGA “load” as possible. There are many variations of PoL converters, all of which have benefits and limitations. The ideal solution depends on both the FPGA and system level requirement, so a focused design is recommended. If a focused design is not used, the performance will either be reduced, the size will be excessively large, or there will be a significant thermal management challenge. (Figure 3.)

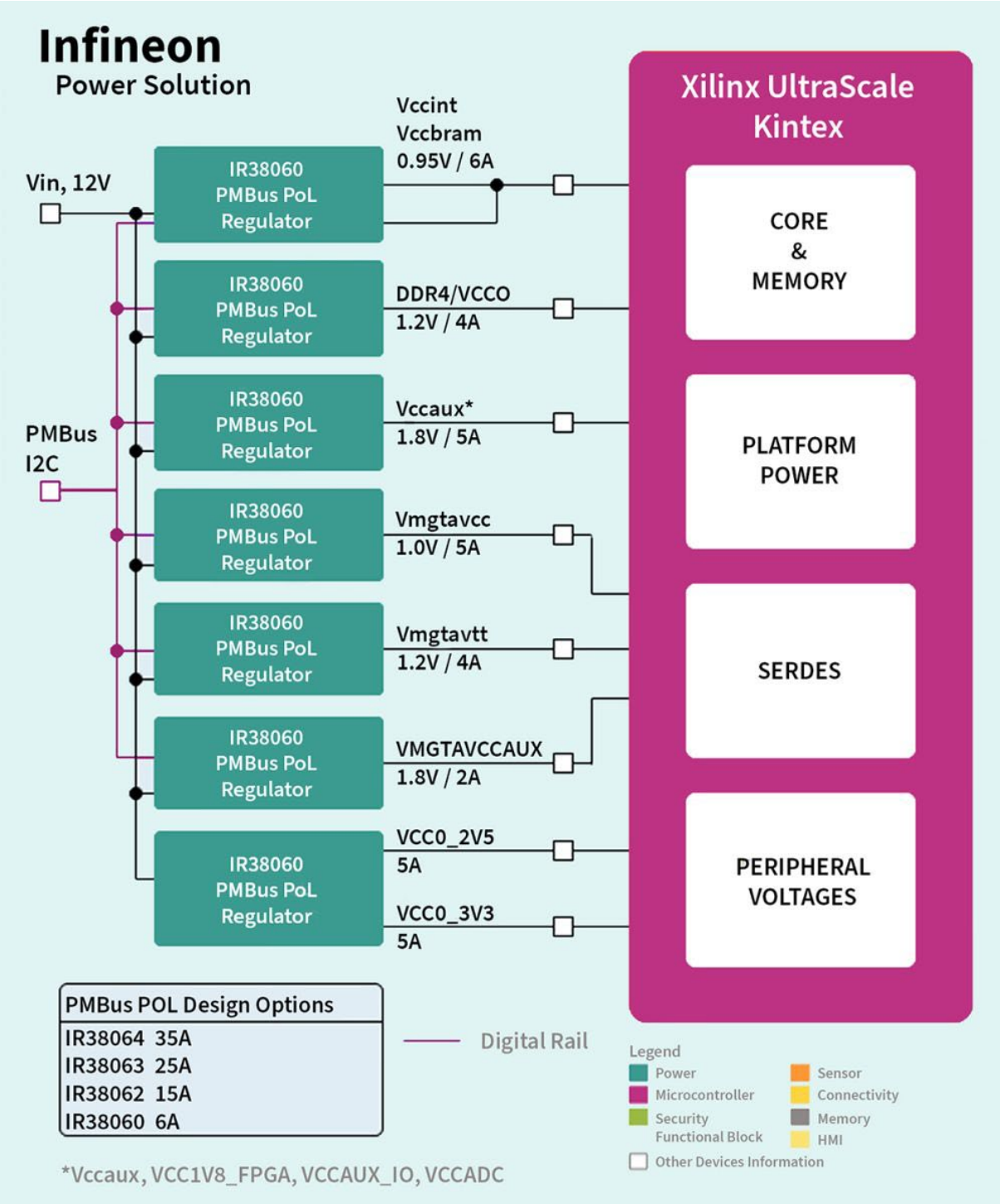

Figure 3: An Infineon power reference design for Xilinx Ultrascale Kintex FPGA.

To have the right solution to power an FPGA load, the following design considerations are recommended.

First, select a control topology that meets design requirements while balancing performance. For example, a controller can have voltage mode control, which is simple, works over a wide range, and has good immunity to noise, but it suffers from poor transient performance which requires

more output capacitors. It could alternately have current mode control, which improves transient performance and allows for reduction in output capacitors, along with inherent current protection to protect against fault events.

This comes at the expense of increased sensitivity to noise and more complex compensation design. It could additionally have constant on-time (COT) control, where it has the best transient performance possible, allowing for smallest output capacitance, but it requires variable switching frequency which can interfere with sensitive RF payloads.

Second, choose a power stage that works well. For loads that are 40 A or below, single-stage buck converters typically are the most common. There are many solutions that integrate the controller and power FETs [field-effect transistors] – referred to as integrated point of load (IPoL) – which simplify design and are small. For higher-current applications, multiphase operation becomes more popular since the parallel power stages reduce ripple current and allow for less output capacitance, increase efficiency by reducing peak current through any single component, improve transient performance, and spread out power losses over a larger area, therefore reducing peak temperature.

Third, pick a controller with the right level of programmability. Options can range from simple analog controllers, where parameters are either set at the factory or set with a resistor or capacitor on a pin, to fully digital controllers with communication protocols like PMBus where monitoring and control can enable a high degree of remote operation.

Can these power solutions handle it?

In conclusion, FPGAs play a critical role in digital and hybrid phased arrays. Starting up and powering these digital assets in military and space designs can be complex, especially with the higher levels of reliability needed in these applications. Choosing the right power solution to match the robustness of the FPGA and system is key. While the newest developments for AESA are advancing fast, designers can feel confident that there are power solutions already deployed and mature enough to support these systems.

Meet the authors



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