Extending EV charger lifetime under different charging strategies by advanced SiC power MOSFET packaging technology

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Abstract

The high-efficiency and high-power density of DC Electric Vehicles (EV) fast charger is enabled by SiC MOSFET power semiconductor technology with fast switching speed with low losses. On the other hand, an often overlook aspect in DC EV fast charger design is their operation lifetime. Due to the repetitive on/off cycle during charging operation, SiC MOSFET used in fast DC EV charger is under high mechanical stress, which will cause package fatigue and eventually lead to wear out failure. The problem is further exacerbated by certain charging strategies, e.g. pulse charging, that further increase mechanical stress on SiC power device during charging. Substantial derating of power device junction temperature is required to keep the power cycling (PC) lifetime of SiC MOSFET device to an acceptable level of just few years.

Latest advance in SiC MOSFET packaging technology is addressing this problem with significant PC lifetime improvement. Copper metallization and strengthened chip attach, collectively known as .XT technology, increase the PC lifetime of SiC MOSFET module by more than 22 times. This provide an unprecedented robust SiC MOSFET module that substantially extend the operation lifetime of fast DC EV charger even under the demanding charging profile of pulse charging.

Keywords: electric vehicles, EV charger, constant current-constant voltage, boost charging, multi-stage constant current, pulse charging, battery lifetime, SiC power MOSFET, power cycling lifetime, package, .XT technology

1. Introduction

The choice of battery charging strategy is often a trade-off amongst charging time, battery lifetime and charging efficiency. For example, use of higher charging current rate (C-rate) will reduce charging time, but also reduce battery lifetime and charging efficiency [1-2]. With public DC fast electric vehicles (EV) charger expected to perform over 20 charging cycles per day or 8000 cycles per year, the power cycling (PC) lifetime of power semiconductor used in DC fast EV charger becomes an issue due to wear out failure. EV charger power semiconductor lifetime is therefore an additional optimization trade-off factor in the choice of DC fast EV charging strategy. Such relationship, as shown in the dotted line in Fig.1, has not been adequately studied so far [3].

This paper will start with an overview of different charging strategies, followed by analysis of their implications to PC lifetime of SiC power MOSFET, and the application techniques to meet SiC power MOSFET PC lifetime requirement. PC lifetime improvement brought by recent advance in SiC MOSFET packaging technology known as .XT technology will be examined. The use of SiC MOSFET with .XT technology in different battery charging strategies to extend PC lifetime will be analysed and compared.

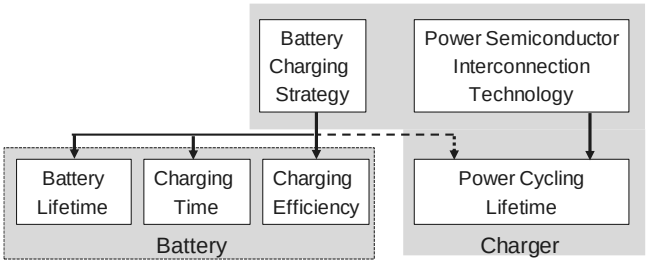

Fig.1 Battery charging strategy has direct impact on power semiconductor PC lifetime.

2. Evolution of battery charging strategies

Significant research efforts have been directed towards optimizing EV battery charging methodologies around charging time, battery lifetime and charging efficiency. Constant Current-Constant Voltage (CC-CV) method is a well-established technique for lithium-ion batteries, in which the battery is charged at a constant current I_O until it reaches a predetermined voltage V_{MAX}, after which the charging voltage is held constant while the charging current gradually decreases until the battery is fully charged. To charge EVs with higher battery pack capacities in shorter time, higher C-rate is needed, which will increase battery power loss and temperature, and reduce coulombic efficiency and battery lifetime. Other improved charging strategies, namely boost charging, multi-stage constant current charging (MSCC) and pulse charging are thus developed, as shown in Fig. 2.

Multi-stage constant current (MSCC) charging strategy (Fig. 2C), which uses two or more distinct stages of constant current charging with decreasing C-rates, was developed based on the principle that the lithium plating phenomenon, being one of the primary lifetime degradation mechanisms for Li ion batteries, is prominent at higher C-rates when the state-of-charge (SoC) is above 40%-50% [4], while at lower SoC the same C-rate has much less impact on lifetime.

MSCC takes benefit of this characteristics by applying higher C-rate initially to achieve faster charging, and gradually lowering the C-rate at higher

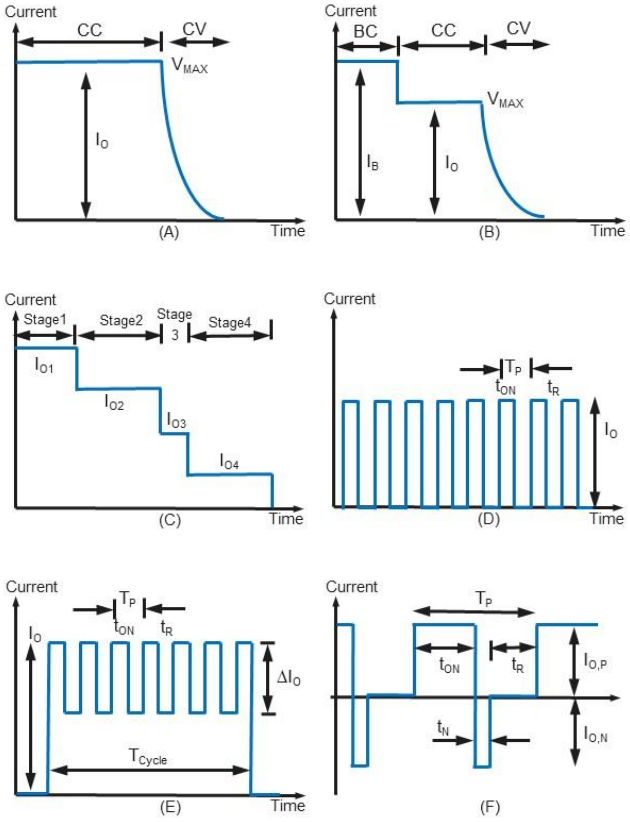

Fig. 2 Battery charging strategies. (A) Constant-current constant-voltage (CC-CV), (B)Boost charging, (C) Multi-stage constant current (MSCC), (D) Positive pulse charging, (E) Constant-current (CC) Pulse Charging, and (F) Negative Pulse Charging

SoC to reduce the capacity fade, and thus achieving an overall improvement of charging time and battery lifetime together, compared to conventional CC-CV method. Also, in MSCC the time-consuming constant voltage charging stage is not employed, and thus reduce charging time and the electrolyte oxidation process [5]. The charging profile parameters can be chosen to improve battery performance e.g. charging time, or lifetime independently or together.

The impact of CC-CV and MSCC charging strategies on power electronic converters in their utilization rate and charging efficiency have been studied in [6]. In [7], the impact of CC-CV and 5-stage MSCC (5MSCC) charging strategies on battery back and converter heatsink temperature rise has been experimentally studied, and it shows that the peak and average temperature rise of 5SMCC is higher than CC-CV, while it improves on charging time and charging efficiency.

Pulse charging was also developed to reduce charging time, improve battery lifetime and reduce temperature rise compared to CC-CV mode, In Positive Pulse Charging (PPC) mode shown in Fig. 2D, short current pulse t_{ON} interspersed with rest periods t_R are used to charge battery.

Constant current charging (CC) mode can be combined with pulse charging mode to become CC-Pulse Charging mode as shown in Fig. 2E, with current pulse amplitude ΔI_O set as a percentage of maximum charging current I_O.

In negative pulse charging (NPC) mode shown in Fig. 2F, short discharge periods t_N are also added to PPC. The rationale behind is that rest intervals allow for better diffusion of lithium ions within the battery electrodes, reducing concentration polarization and potentially enabling faster and more efficient charging than continuous high-current charging.

The benefits of PPC on battery lifetime improvement by slow down internal resistance increase over battery lifetime has been intensively studied, e.g. NMC Li ion batteries lifetime extension up to 60% for a specific PPC with low pulse frequency of 0.05Hz is shown in [8]. Many studies also claim various benefits of NPC on active material utilization and longer lifetime. However, the benefits of pulse charging are highly dependent on the battery chemistry and choice of pulse parameters includes amplitude, frequency and duty cycle. Optimal choice of these parameters is a complex optimization problem as they are often inter-dependent [9-13].

3. SiC MOSFET PC lifetime and .XT technology

Due to coefficients of thermal expansion (CTE) mismatch of the different materials within semiconductor package layers, when power semiconductors are used in applications with repeated load cycles, device junction temperature will cycle up and down, lead to continuous thermal stress, fatigue and eventual wear out failure to the package.

The power cycling (PC) failure lifetime of power semiconductors can be modelled by the Bayerer model (LESIT Model) [14]

$$N_f = A \cdot \Delta T_J^{\alpha 1} \cdot \exp[\alpha_2/(T_J+273)] \cdot t_{on}^{\alpha 3}$$

where:

N_f	Number of cycles to failure
A	Material-dependent constant
ΔT_J	Temperature Swing
T_J	Maximum junction temperature
t_{on}	Heating Time
α_1~α_3	Exponents for each parameter

PC lifetime is strongly influenced by ΔT_J and less influenced by T_J. PC lifetime of a particular product or technology is published by manufacturer as PC curve [15] or analytical model [16], based on test result with extrapolation.

With conventional power module interconnection technologies using soft solder and aluminum bond wires, the PC capability of SiC power module is lower than that of Si power module, due to the lifetime bottleneck failure mechanism changed from bond wire life-off to die attach solder delamination [17-18].

To improve PC lifetime of SiC power module, advanced interconnection technology combining copper front-side interconnection with diffusion soldering for die attach, known as the .XT technology

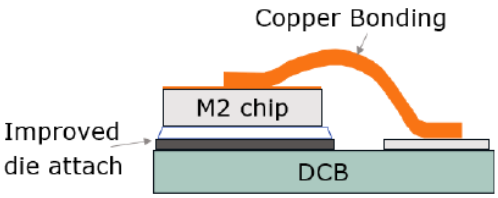

Fig. 3 The .XT technology for power semiconductor packaging consists of copper top-side metallization and improved die attach of diffusion soldering, increase SiC MOSFET PC lifetime by 22 times.

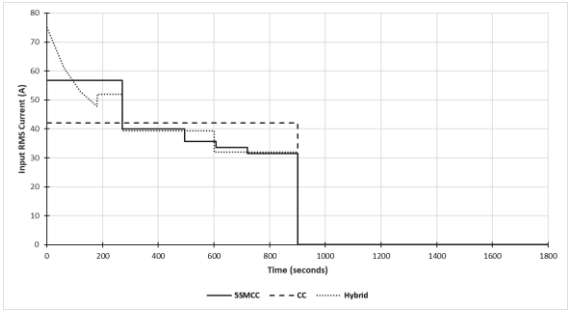

Fig. 4 Charging current profile of CC, 5MSCC, and MSCC+boost modes

(Fig. 3) is used [19-20]. With the high tensile strength in die-attach process, soldering degradation is not the weak link anymore, shifting the bottleneck back to bond wire [21-22]. Use of robust copper bond wire and chip metallization increase the PC capability by more than 22 times for the same ΔT_J [23].

4. SiC MOSFET PC lifetime in CC and MSCC modes

SiC MOSFET PC lifetime used in EV charger charging with a particular charging strategy can be estimated by using the rain-flow counting method [18], in which the complex mission profile is decomposed into a series of simple cycles, each characterized by its temperature swing (maximum and minimum) and mean temperature. Such power cycling lifetime calculation can be done manually using analytical PC lifetime model [16] or automatically using online lifetime simulation service [25].

In this section, PC lifetime of SiC MOSFET using conventional interconnection technology (Gen 1) in CC mode is simulated using lifetime simulation service as reference, to compare with different variants of MSCC, and also with .XT SiC MOSFET technology (Gen 2).

The charging current profiles of of CC, 5MSCC, and MSCC+boost modes are plotted together in Fig. 4 for comparison.

Gen 1 SiC MOSFET FF11MR12W2M1HP_B11 (1200 V, 11 mΩ) from Infineon is used in a 3-phase 2-level inverter bridge for PC lifetime evaluation with the inverter and charger operation parameters shown in Table 1.

Table 1 Inverter and charger operation parameters

Inverter conditions	
Modulation algorithm	SPWM
DC link voltage	800 V
Output frequency	50 Hz
Switching frequency	48 kHz
Modulation index	0.85
Power factor cos(ϕ)	-1
Output voltage	416 V

Charger operation		
Charging time	15	min
# charging	2	/hour
# active hour	12	/day
Cycle/day	24	
Cycle/yr	8760	

Thermal parameters

$R_{TH,JH}$	0.595 K/W
T_A	55.0 °C

$R_{TH,HA}$	0.4 K/W
$\tau_{TH,HA}$	120 s

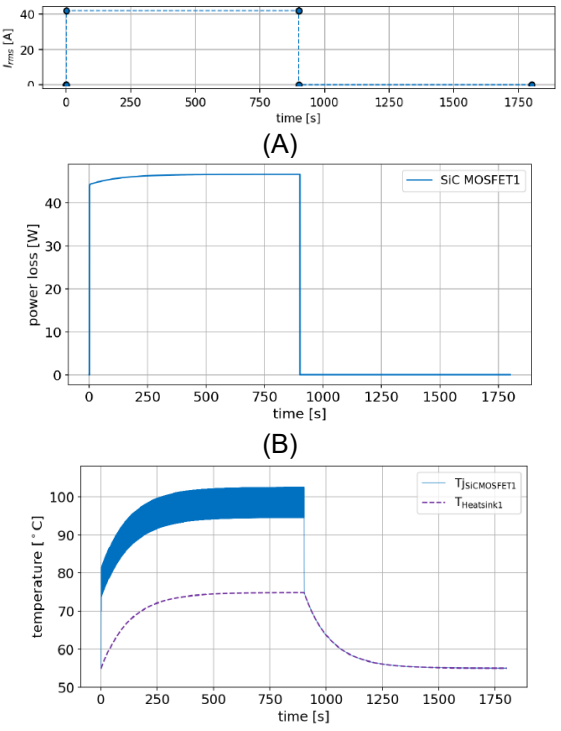

Fig. 5 (A) Charging current I_O, (B) SiC MOSFET power dissipation P_D and (C) SiC MOSFET junction temperature T_J in CC mode. ΔT_J = 47.5 K, PC lifetime =124800 cycles

(A) CC mode as reference

Charging current I_O, SiC MOSFET power dissipation P_D and junction temperature T_J in CC mode are shown in Fig.5. $T_{J,MAX}$ is 103°C and the PC lifetime by lifetime simulation is 124800 cycles. Note that the junction temperature T_J ripple in Figs. 5 - 7 is due to the AC input frequency. The low T_J ripple amplitude of around 10K will not affect SiC MOSFET lifetime.

(B) 5MSCC mode

In 5MSCC mode, the initial charging current I_O in stage 1 is set to 60A, higher than 40A in CC mode. I_O is reduced to below 40A in subsequent stages to extend battery lifetime.

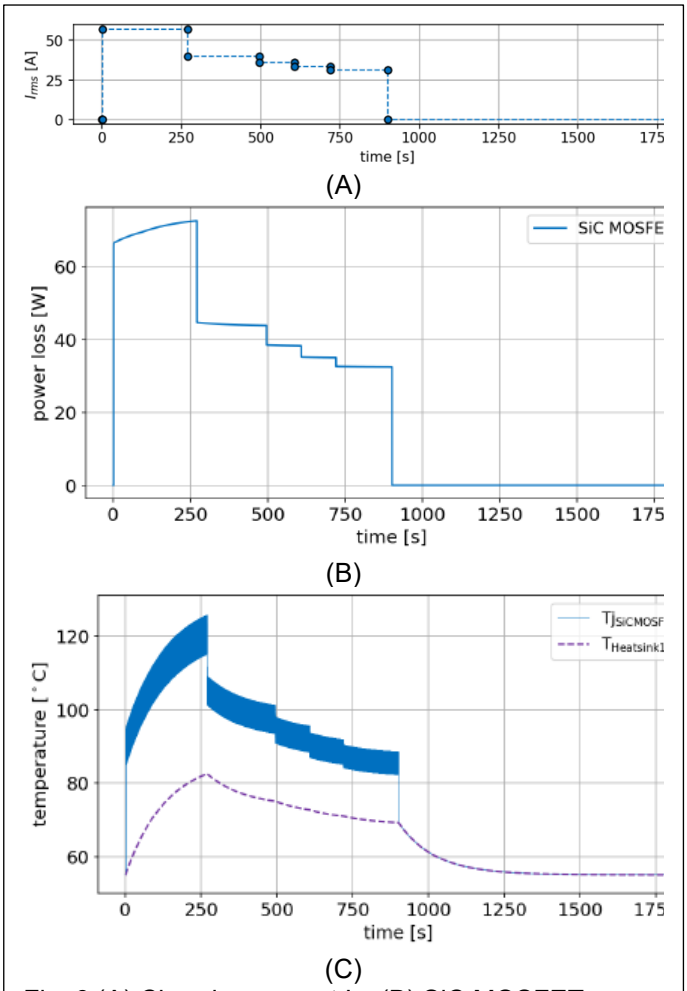

Fig. 6 (A) Charging current I_O, (B) SiC MOSFET power dissipation P_D and (C) SiC MOSFET temperature T_J in 5MSCC mode. ΔT_J = 70.7 K, PC lifetime = 22230 cycles

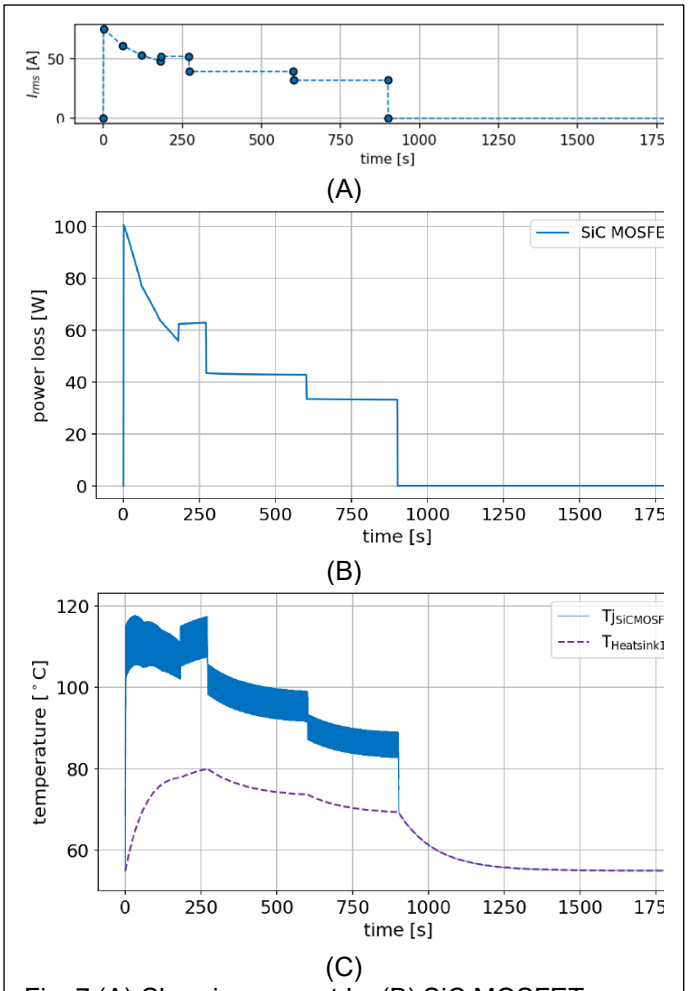

Fig. 7 (A) Charging current I_O, (B) SiC MOSFET power dissipation P_D and (C) SiC MOSFET junction temperature T_J in MSCC+boost mode. ΔT_J = 62.6 K, PC lifetime = 42230 cycles

Comparing SiC MOSFET PC lifetime in CC and 5MSCC modes:

- With ΔT_J increased from 47.5 K to 70.7 K, PC lifetime with 5MSCC mode is reduced to only 17.8% of that in CC mode, or about 2.5 years, which is too short for DC fast EV charger application.
- Changes of charging current I_O and T_J in subsequent charging stages, which do not increase T_J, do not affect PC lifetime.

(C) MSCC with initial current boost (MSCC+boost)

The charging current profile I_O, SiC MOSFET power dissipation P_D and SiC MOSFET junction temperature T_J in MSCC+boost mode are shown in Fig. 7.

In MSCC+boost mode, an initial charging current boost is added to MSCC when charging starts. The time constant of this initial current boost is set to be equal to the heatsink time constant $\tau_{TH,HA}$, to take advantage of time required for initial heatsink temperature rise, such that the maximum junction temperature is kept relatively constant at around 118 ºC during the first 260 seconds as shown in Fig.7C

The benefit of MSCC+boost approach is, while it offers the benefits of MSCC on overall improvement of both charging time and battery lifetime compared to CC mode, the initial current boost profile which matches with heatsink time constant will increase initial charging current I_O without increasing T_J for an extend period, thus maximize initial charging current without incurring extra PC lifetime penalty to SiC MOSFET, and allow a lower current in subsequent charging stages to further improve battery lifetime.

(D) Use of Gen 2 .XT SiC MOSFET

With Gen 2 .XT SiC MOSFET being used, the number of PC cycle will be increased by 22 times [23]. PC lifetime in MSCC+Boost mode will be increased to over 100 years at the same operation conditions. The extra lifetime offered by the .XT technology can be converted into higher output charging current by operating SiC MOSFET can at higher $T_{VJ,OP}$. Calculated from the PC lifetime model [16,23], the Gen 2 .XT SiC MOSFET can operate at $T_{VJ,OP}$ =159°C with PC lifetime of 10 years.

The PC lifetime and battery lifetime impact of SiC MOSFET in CC, 5MSCC, and MSCC+boost mode, using Gen 1 and Gen 2 .XT SiC MOSFET, are compared in Table 2 as

Table 2 Comparison of Gen 1 and Gen 2 .XT SiC MOSFET PC lifetime in CC, 5MSCC and MSCC+Boost modes

Mode	CC	5MSCC	MSCC+Boost	
SiC MOSFET	Gen 1	Gen 1	Gen 1	Gen 2 .XT
T_A (°C)	55	55	55	55
$T_{VJ,MAX}$ (°C)	103	128	118	159
ΔT_J (°C)	47.5	70.7	62.6	104
# PC cycle	124800	22230	42230	87600
PC lifetime*	14.2 yr	2.5 yr	4.8 yr	10 yr
Battery life time impact		Reduce charging current at end-of-charge improve battery lifetime over CC mode		

* Based on 24 charging cycle/day, equivalent to 8760 cycle/year

- MSCC+boost mode offers longer SiC MOSFET PC lifetime than 5MSCC mode (1.9x), and also improve battery lifetime over CC mode due to reduced charging current at end-of-charge, with the same charging time.
- Use of Gen 2 .XT SiC MOSFET improve both the output charging current ($T_{VJ,OP}$ increase from 118°C to 159°C) and SiC MOSFET PC lifetime (2.1x) in MSCC+Boost mode.

5. SiC MOSFET PC lifetime in CC-Pulse Charging mode

The following parameter choice, approximation and assumptions are made in order to simplify PC lifetime calculations:

- Charging pulse width T_P is chosen to be far shorter than heatsink time constant $\tau_{TH,HA}$, i.e. $T_P << \tau_{TH,HA}$, such that heatsink temperature T_H will remains constant within current pulse
- Using SiC MOSFET drain current I_D as proxy of charging current I_O. The relationship of I_D and I_O is not linear and depends on converter topology chosen. For example, in LLC topology commonly used in EV charger, due to presence of circulating current in I_D which is independent of I_O, the percentage change of I_D is higher than that of I_O.
- Only DC conduction loss of SiC MOSFET is considered.
- Temperature-dependency of $R_{DS(ON)}$ is modelled by excel curve-fitting, with coefficients bear no physical meaning

Infineon SiC MOSFET module of generation 1 (FF33MR12W1M1H_B11) and generation 2 (F4-8MXTR12C2M2_H11) are used for PC lifetime calculation with analytical model [15-16] under the following conditions:

Charger service operation parameters

Full cycle $t_{(ON)}$	15	min
Charge cycle	2	/hour
Charging hour	12	/day
Charge cycle	8760	/year

Pulse charging parameters

Pulse on time $t_{(ON)}$	10	sec
Pulse period T_P	20	sec
Ambient temp T_A	45	°C

SiC MOSFET $R_{DS(ON)}$ and thermal resistances $R_{TH,JH}$ and heatsink $R_{TH,HA}$ are summarized in following table

	Gen 1 (33mΩ)	Gen 2 .XT (8mΩ)	
	FF33MR12W1M1H_B11	F4-8MXTR12C2M2_H11	
$R_{DS(ON)}$	28.283 $e^{0.0051\ Tj}$	7.296 $e^{0.0049\ Tj}$	mΩ
$R_{TH,JH}$	1.54	0.59	K/W
$R_{TH,HA}$	0.8 (Forced-air cooling)		K/W
	0.1 (Liquid-cooling)		K/W

In CC-Pulse Charging mode, the number of PC lifetime cycle N_{CCPulC}, is given by

$$1/N_{CCPulC} = 1/N_{CC} + 1/N_{PulC}$$

where:

N_{CC} PC lifetime for constant current mode (charging envelope)

N_{PulC} PC lifetime for pulse charging

(A) Effect of cooling of PC lifetime

Pulse charging can be combined with constant-current charging to become constant-current (CC)-Pulse Charging mode. As charging pulse period is normally much shorter than the heatsink time constant, the heatsink temperature T_H can be assumed constant within pulse charging period. Therefore, ΔT_J during pulse charging period equals to ΔT_{JH}, which is determined by SiC MOSFET junction-to-heatsink thermal resistance R_{THJH} and power dissipation P_D only, and independent of heatsink thermal resistance R_{THHA}. On the other hand, ΔT_J for the entire charging cycle (the "charging envelope") equals to ΔT_{JA}, and is determined by SiC MOSFET R_{THJH}, R_{THHA} and power dissipation P_D. Therefore, the heatsink cooling approach will have different effects to ΔT_J of charging pulse (ΔT_{JH}) and charging cycle envelope (ΔT_{JA}) respectively. ΔT_J of charging pulse will have a higher influence on overall PC lifetime when heatsink thermal resistance R_{THHA} is low, e.g. in liquid cooling, therefore overall PC lifetime in pulse charging will be shorter with liquid cooling.

(B) With forced-air cooling

Gen 1 SiC MOSFET PC lifetime against pulse charging current amplitude ΔI_D as percentage of drain current I_D with $T_{VJ,OP,MAX}$ =125°C is shown in Fig. 8

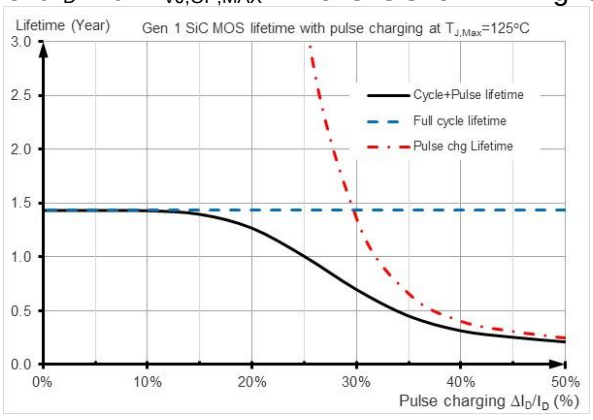

Fig. 8 SiC MOSFET PC lifetime against pulse charging current amplitude ΔI_D as percentage of drain current I_D with $T_{VJ,OP,MAX}$ =125°C.

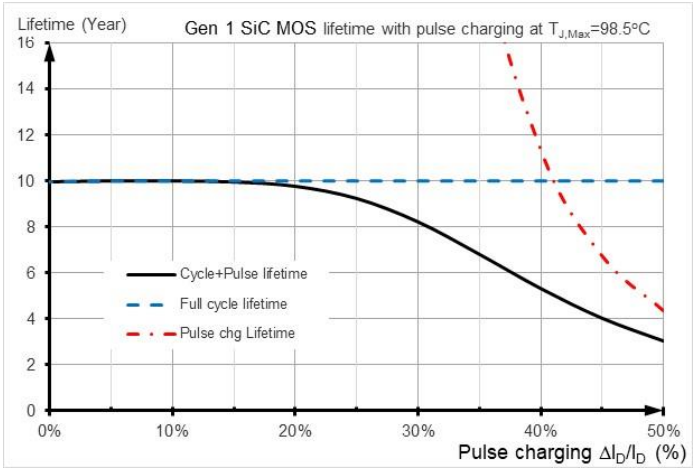

Fig. 9 By further derate $T_{VJ,OP,MAX}$ to 98.5°C, SiC MOSFET PC lifetime can be extended to over 10 years for pulse charging current amplitude ΔI_D from 0% up to 20% of drain current I_D

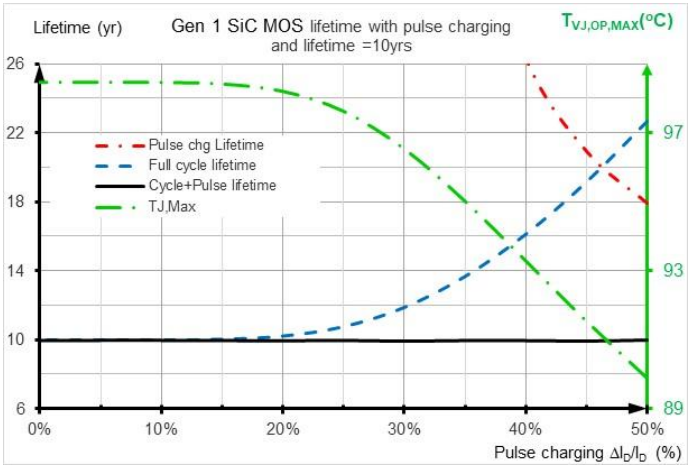

Fig. 10 Allowed maximum operation junction temperature $T_{VJ,OP,MAX}$ from 98.5°C to 89.9°C for pulse charging current amplitude ΔI_D from 0% to 50% of drain current I_D with SiC MOSFET PC lifetime set to always 10 years

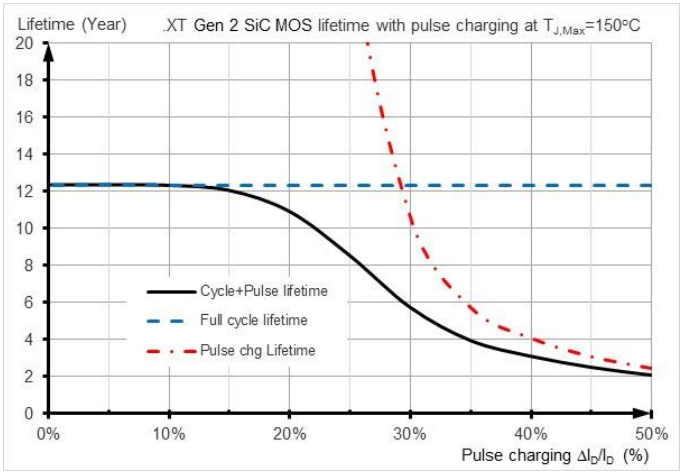

Fig. 11 Using Gen 2 SiC MOSFET with .XT technology, at $T_{VJ,OP}$ =150°C, SiC MOSFET PC lifetime can be extended to over 10 years for pulse charging current amplitude up to 22% of charging current

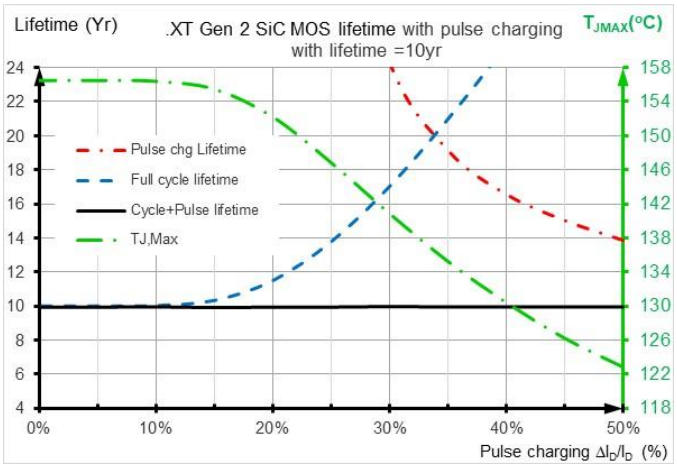

Fig. 12 Using Gen 2 SiC MOSFET with .XT technology and forced-air cooling, and SiC MOSFET PC lifetime set to 10 years, the allowed maximum operation junction temperature $T_{VJ,OP,MAX}$ changes from 157°C to 123°C with current amplitude ΔI_D from 0% to 50% of drain current I_D, in CC-pulse charging mode

(C) **With liquid cooling**

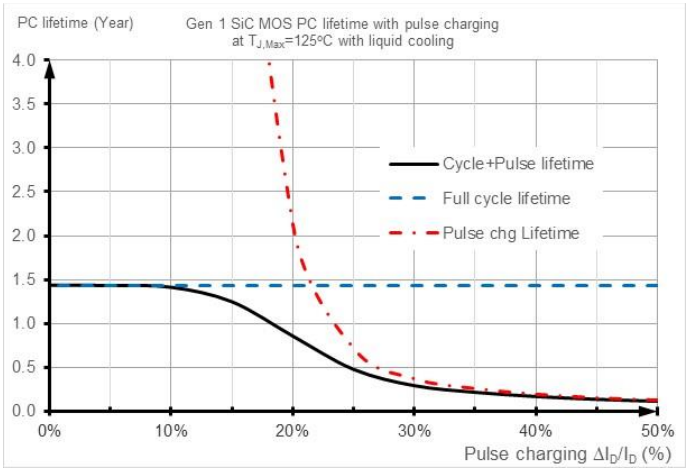

Fig. 13 SiC MOSFET PC lifetime against pulse charging current amplitude ΔI_D as percentage of drain current I_D with $T_{VJ,OP,MAX}$ =125°C and liquid cooling

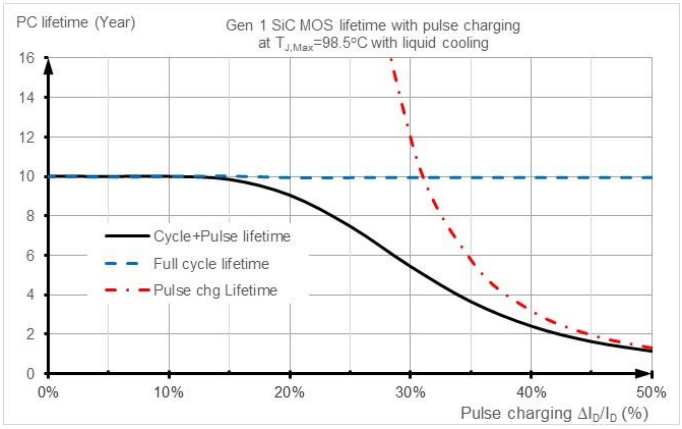

Fig. 14 By derate $T_{VJ,OP,MAX}$ to 98.5°C using liquid cooling, SiC MOSFET PC lifetime can be extended to over 10 years for pulse charging current amplitude ΔI_D up to 15% of drain current I_D

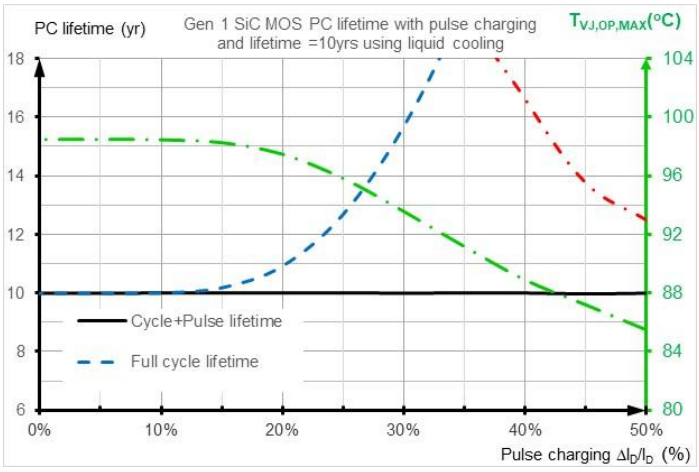

Fig. 15 With SiC MOSFET PC lifetime set to 10 years and using liquid cooling, the allowed maximum operation junction temperature $T_{VJ,OP,MAX}$ changes from 98.5°C to 85.5°C for pulse charging current amplitude ΔI_D from 0% to 50% of drain current I_D

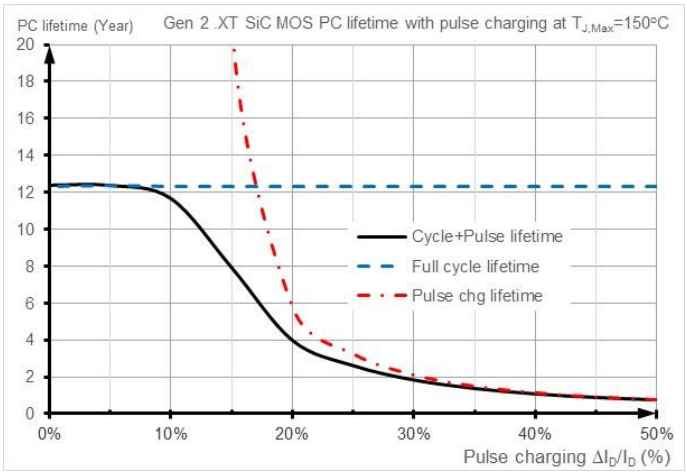

Fig. 16 Using Gen 2 SiC MOSFET with .XT technology, with $T_{VJ,OP,MAX}$ =150°C, SiC MOSFET PC lifetime can be extended to over 10 years for pulse charging current amplitude up to 12% of charging current with liquid cooling

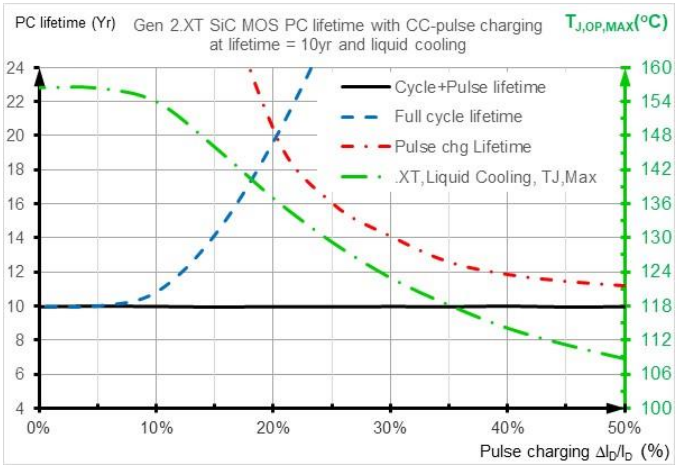

Fig. 17 Using Gen 2 SiC MOSFET with .XT technology and liquid cooling, and SiC MOSFET PC lifetime set to 10 years, the allowed maximum operation junction temperature $T_{VJ,OP,MAX}$ changes from 157°C to 123°C with current amplitude ΔI_D from 0% to 50% of drain current I_D for CC-pulse charging

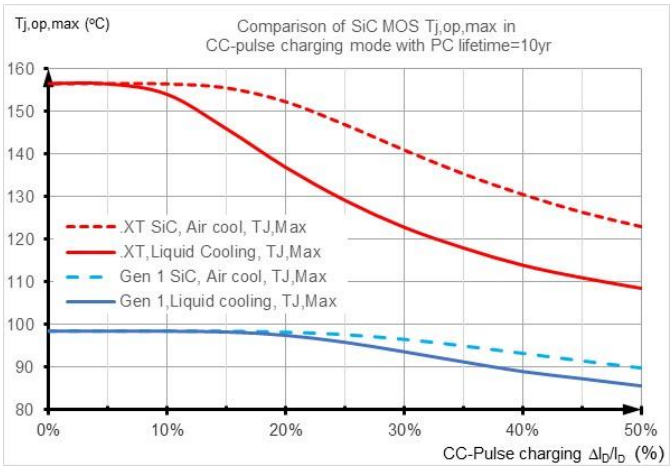

Fig. 18 Comparison of SiC MOSFET allowed maximum operation junction temperature $T_{VJ,OP,MAX}$ in CC-Pulse charging mode between Gen1 and Gen2 .XT SiC MOSFET using forced-air cooling and liquid cooling

6. SiC MOSFET PC lifetime in pulse charging mode

In pulse charging mode, current pulse with amplitude I_O and duty cycle of 50% are used to charge the battery. To compare the PC lifetime of SiC MOSFET in pulse charging mode with CC mode, a drain current $I_{D,10yrCC}$ is set as reference, at which the PC lifetime is 10 years in CC mode. PC lifetime in pulse charging mode is then calculated at different percentage of $I_{D,10yrCC}$ and compared with that in CC mode. Note that in the comparisons of pulse charging with CC mode,

- since the charging pulse has only 50% duty cycle, at the same charging current amplitude, the charging time has to be doubled in pulse charging mode compared to CC mode. If comparison has to be made with same charging time, charging current amplitude in pulse charging mode should be twice of that in CC mode,
- the reference drain current $I_{D,10yrCC}$ is different between SiC MOSFET gen 1 and gen 2 .XT due to the different maximum operation junction temperature $T_{VJ,MAX}$ and output current capability. Parameter for comparison between SiC MOSFET gen 1 and gen 2 .XT should be the maximum operation junction temperature $T_{VJ,OP,MAX}$

PC lifetime and maximum operation junction temperature $T_{VJ,OP,MAX}$ of for gen 1 SiC MOSFET FF33MR12W1M1H_B11 versus percentage of $I_{D,10yrCC}$, in pulse charging mode and CC mode are calculated and plotted in Fig.19 for comparison.

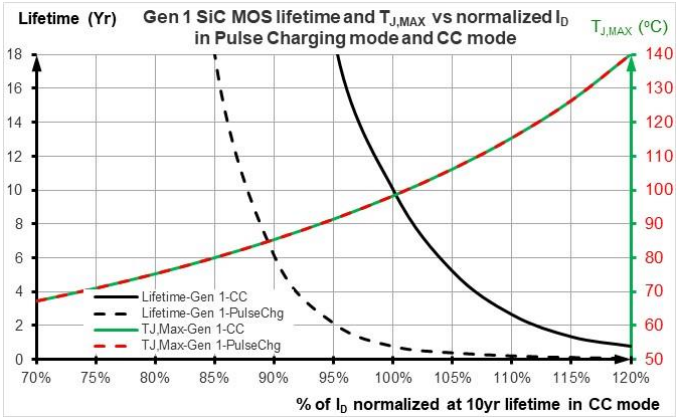

Fig. 19 Gen 1 SiC MOSFET PC lifetime and maximum operation junction temperature $T_{VJ,OP,MAX}$ versus current amplitude, in pulse charging mode and CC mode for comparison. Current amplitude is express as % of I_D normalized to 100% at 10-year lifetime in CC mode.

The PC lifetime in pulse charging mode using Gen 2 .XT SiC MOSFET is compared with CC mode and shown in Fig. 20. Note that with much higher PC lifetime of .XT SiC MOSFET, the operation limit is shifting back from PC lifetime to $T_{VJ,MAX}$, as indicate by SiC MOSFET T_{VJ} already reached the limit of 175ºC when charging current exceeds 102% of $I_{D,10yrCC}$.

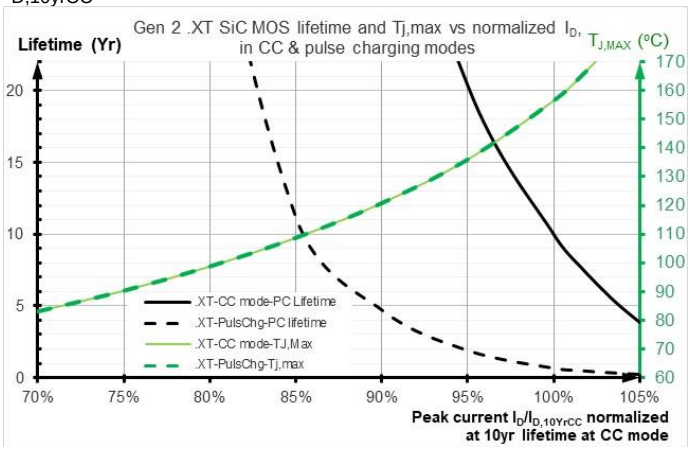

Fig. 20 Gen 2 .XT SiC MOSFET PC lifetime and maximum operation junction temperature $T_{VJ,OP,MAX}$ versus pulse current start from zero, with amplitude as % of $I_{D,10YrCC}$ which give 10-year lifetime at CC mode.

The relationship of $T_{VJ,OP,MAX}$ with current amplitude I_D between pulse charging and CC modes are the same, for both Gen 1 and Gen 2 .XT SiC MOSFET. PC lifetime in pulse charging mode is only 8% and 6.8% of that in CC mode at $I_{D,10yrCC}$, for Gen 1 and Gen 2 .XT SiC MOSFET respectively, due to much higher number of ΔT_J in the pulse charging mode. To achieve 10 years of PC lifetime in pulse charging mode, $T_{VJ,OP,MAX}$ and pulse current pulse amplitude has to be further derated as follow

SiC MOSFET	$T_{VJ,OP,MAX}$	$I_{D,10yrCC}$
Gen 1	83 ºC	88%
Gen 2 .XT	110 ºC	86%

PC lifetime versus max operation junction temperature $T_{VJ,OP,MAX}$ in CC and pulse charging modes, using Gen 1 and Gen 2 .XT SiC MOSFET, are compared in Fig.21. At the same lifetime of 10 years, $T_{VJ,OP,MAX}$ for Gen 2 .XT are 58 ºC and 27ºC higher than Gen 1 in CC mode and pulse charging mode respectively.

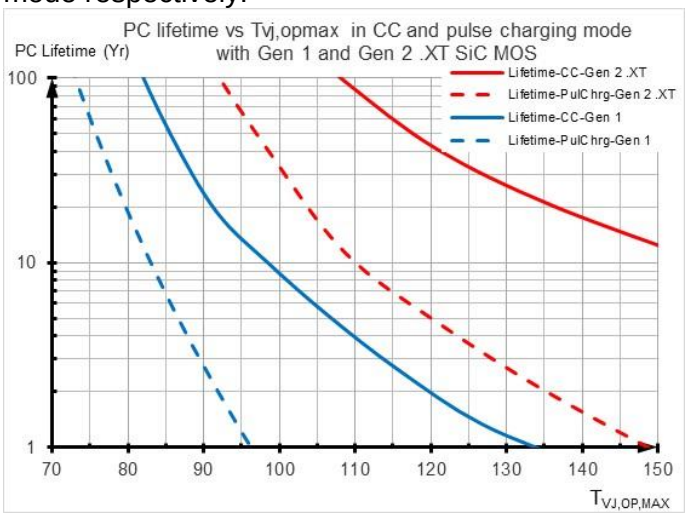

Fig.21 Comparison of PC lifetime versus max operation junction temperature $T_{VJ,OP,MAX}$ in CC and pulse charging modes for Gen 1 and Gen 2 .XT SiC MOSFET

The max operation junction temperature $T_{VJ,OP,MAX}$ of Gen1 and Gen 2 .XT SiC MOSFET in CC, pulse charging and CC-pulse charging modes are summarized in the table below.

		SiC MOSFET	
Lifetime = 10 yr		Gen 1	Gen 2 .XT
Mode	Cooling	$T_{VJ,OP,MAX}$	$T_{VJ,OP,MAX}$
CC	All	98.5	156.5
Pulse charging	All	83.0	110.3
CC-Pulse charging-50%	Air	89.9	122.9
	Liquid	85.5	108.6

8. Temperature control to compensate ΔT_H

As shown in Fig. (5)-(7), the heatsink temperature T_H has larger than 20°C change during a charging cycle, which add to the overall ΔT_J and thus consume PC lifetime of SiC MOSFET. Automatic temperature control (ATC) [26-27] techniques can be used to maintain heatsink temperature constant, e.g. in forced-air cooled system, additional heater on heatsink can be installed to minimize ΔT_H during charging cycle interval, and thus and minimize ΔT_J. The heater should dissipate the same power losses as SiC MOSFET, be turned off when charging start and turned on when charging stop, and thus maintain the heatsink power dissipation constant. To reduce the heater power required, cooling fan may also be started and stopped together with charging operation.

Conclusion

Due to its rapid load cycling operation nature, DC EV fast charger is a demanding application to SiC MOSFET on PC lifetime. Very substantial derating on SiC MOSFET junction temperature $T_{VJ,OP}$ is required to achieve a 10 years lifetime under typical operation profile using common CC charging strategy.

Meanwhile, advanced charging strategies had been developed to improve battery lifetime, charging

time and coulombic efficiency, e.g. MSCC and pulse charging. However, all these charging strategies will further increase the number or magnitude of SiC MOSFET ΔT_J, and further shorten PC lifetime compared to CC mode, resulting in unrealistic short PC lifetime time or junction temperature derating down to 83°C. New technology to increase SiC MOSFET PC lifetime is thus required to meet application requirement.

Use of copper top-side metallization and bond wire, together with diffusion soldering for die attach, collectively known as .XT technology, can increase SiC MOSFET PC lifetime by 22 times. SiC MOSFET with .XT technology can be used in DC EV fast charger with all charging modes, and satisfy the lifetime requirement with much less junction temperature derating.

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