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POWER STORY:

Gate-Driver IC Progress Pushes SMPS to New Levels of Power Density

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PARTNER CONTENT

Gate-Driver IC Progress Pushes SMPS to New Levels of Power Density

By Hubert Baierl, Marketing Director, Infineon Technologies

Long-term durable galvanic isolation technology and multiple innovations in gate-driver IC output stages and packages

Progress is a constant in many electronics areas. Nowadays, in 3.3-kW switched-mode power supplies (SMPS) with 98% efficiency and 1U form factor, power densities of 100 W/in.^{3} can be attained. This is made possible by a smart choice of superjunction power MOSFETs (e.g., CoolMOS™) and silicon carbide MOSFETs (e.g., CoolSiC™) in the totem-pole PFC stage and using gallium nitride power switches (e.g., CoolGaN™) to operate the high-voltage LLC stage. Digital control of the PFC and the LLC is indispensable, just as the use of planar magnetics and advanced gate-driver ICs (e.g., EiceDRIVER™) play an important role in making this possible.

KEY MARKET TRENDS

Robust galvanic isolation

Galvanic isolation is used where a ground-loop separation between two (or more) parts of a system is a must. The main reasons for galvanic isolation include:

- Avoiding ground shifts (resulting from the normal operation of power switches) that affect the system's proper functioning
- Preventing surges or pulses that will compromise system integrity
- Protecting people from harmful electric shock

Today, the "gold standard" in terms of component level norms for galvanic isolated gate-driver ICs is the German VDE norm, DIN VDE V 0884-11:2017-01 (VDE 0884-11).

The VDE 0884-11 is the first industry norm for any galvanic isolated semiconductor products (i.e., regardless of whether optically or magnetically or capacitively isolated) that considers the isolation barrier properties at zero hours, i.e., when the manufacturer tests the products. The VDE 0884-11 takes a 20-year operational lifetime perspective. To cover this, gate-driver ICs are subjected to a time-dependent dielectric-breakdown life-test time to breakdown, which is geared toward a 37.5-year limit (see **Table 1**).

Well-known component-level isolation norms like UL 1577, IEC 60747-5-5, or the since-expired VDE 0884-10 do not include this operational lifetime consideration.

Because VDE 0884-11 is a German norm, it has been migrated into the largely comparable international IEC 60747-17 norm, which was published on Sept. 20, 2020.

The VDE 0884-11 contains a very important statement that should not be overlooked:

"Safe electrical isolation is guaranteed only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits."

This sentence is particularly important when people need to be protected against electric shock.

Imagine the following worst-case example in a half-bridge: The high-side MOSFET has a gate-drain short while the low-side MOSFET

Component standard for		Optical Isolator		Magnetic & Capacitive Isolator	
Input-to-Output Isolation Test		UL 1577	IEC 60747-5-5	VDE 0884-10 (expired)	VDE 0884-11 IEC 60747-17
Type	V_{ISO}; V_{IOTM} HV-50 Hz AC Test	Yes; V_{ISO}	Yes; V_{IOTM}	Yes; V_{IOTM}	Yes; V_{IOTM}
	Isolation Partial Discharge Test	N/A	Yes	Yes	Yes
	V_{IOSM} = 10 kV Surge Pulse Test	N/A	Yes	Yes	Yes
	TDDB Life-Test t_{BD}	N/A	N/A	N/A	**Yes** 37.5-year TDDB limit for 20-year application lifetime
Safety Factors defining Test voltages		N/A	N/A	Yes	Voltage safety factor: 1.2 Lifetime safety factor: 1.875 for reinforced / 1.3 for basic
Describes both Sample Testing (60 s) and Production Test Methods / Levels (1 s)		Yes	Yes	Yes	Yes
Mandatory quarterly monitoring		N/A	Yes	Yes	Yes

Table 1: *Component-level isolation norm overview*

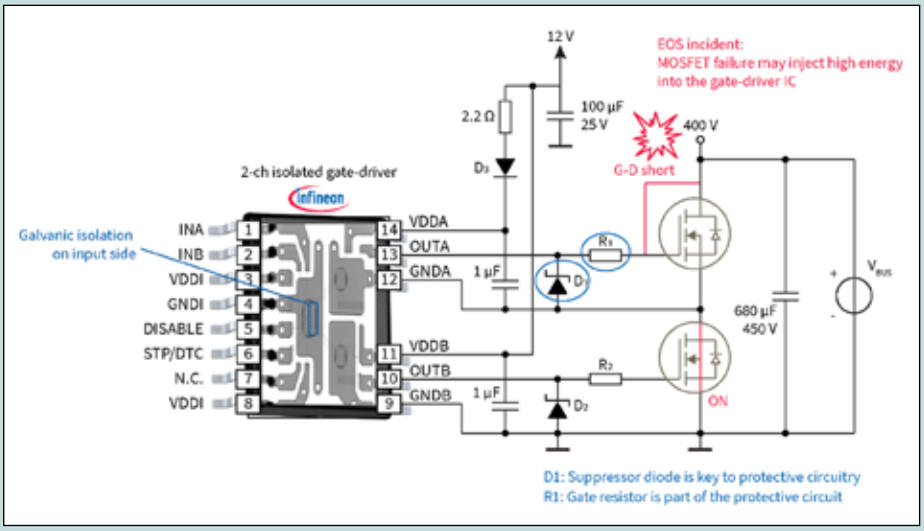

Figure 1: *EOS test setup*

is on. In such an electrical overstress (EOS) situation, currents of more than 600 A can be observed to flow toward the gate-driver IC output. To protect the gate-driver IC output, the gate-resistor (R1) is complemented by the suppressor diode (D1) (see **Figure 1**). The suppressor diode bypasses the gate-driver output and directs the current flow to the half-bridge midpoint. Consequently, the gate-driver IC's isolation function from the output to its input side remains intact, provided a proper application design is chosen.

In addition to preserving this isolation function, no bare metal, normally covered by mold compound material, must become visible; i.e., the package integrity must be maintained.

EOS experiments have shown that gate driver ICs with the isolation barrier embedded on the input side of the IC, such as the EiceDRIVER™ 2EDR family from Infineon Technologies, meet both of these requirements, even without the suppressor diode (D1) being in place.

Multiple areas of progress

Short UVLO output-stage startup time

Bootstrap supply of high-side gate-driver ICs is common because it is a very cost-effective solution. For this reason, half- and full-bridges in high-voltage LLCs (typ. 400-V DC-bus voltage) or hard-switching full-bridges on the primary side of low-voltage DC/DC converters (e.g., 48 V to 12 V) typically have bootstrap circuitries.

Bootstrapped designs benefit from short gate-driver IC UVLO startup time in multiple ways:

- Fast normal system startup
- Short LLC startup time after a brown-out longer than, for example, 200 ms, which typically equates to 10 mains cycles
- Short LLC startup time when the restart release is given after the activation of system-level protection
- No mains-power-transformer saturation due to asymmetric high-side versus low-side PWM operation during the ramp-up of the bootstrap supply

When using dual-channel galvanic isolated gate-driver ICs with 2-µs typical UVLO startup time in a bootstrapped high-side, only four high-side pulses are skipped until the half-bridge can start operating (provided the V_{DD} increase of the high-side is what is deemed to be typical). A similar gate-driver IC with a UVLO startup time of 10 µs or more easily can lead to skipping of 10 or more high-side pulses. This significantly delays the start of the half-bridge operation (**Figure 2**).

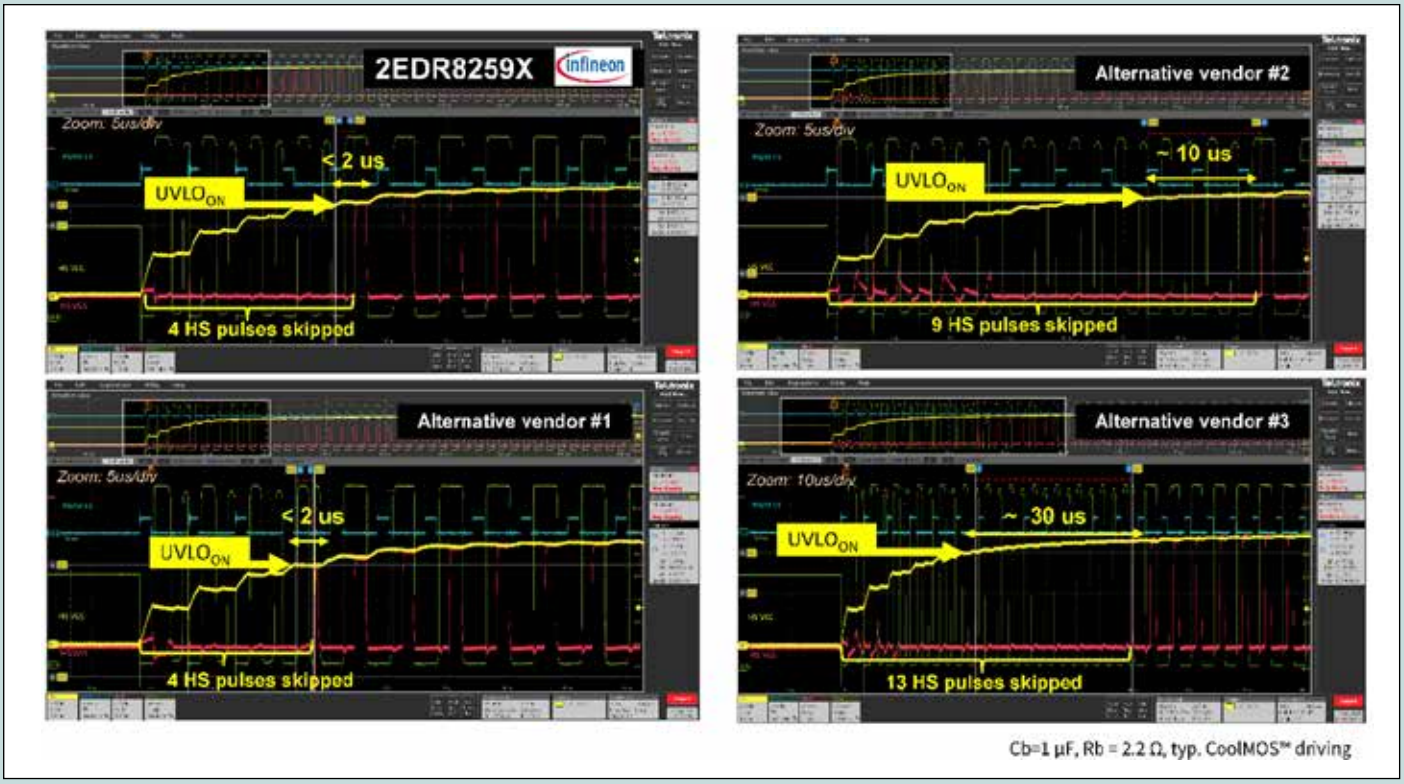

Figure 2: *UVLO startup time comparison of state-of-the-art dual-channel isolated gate-driver ICs*

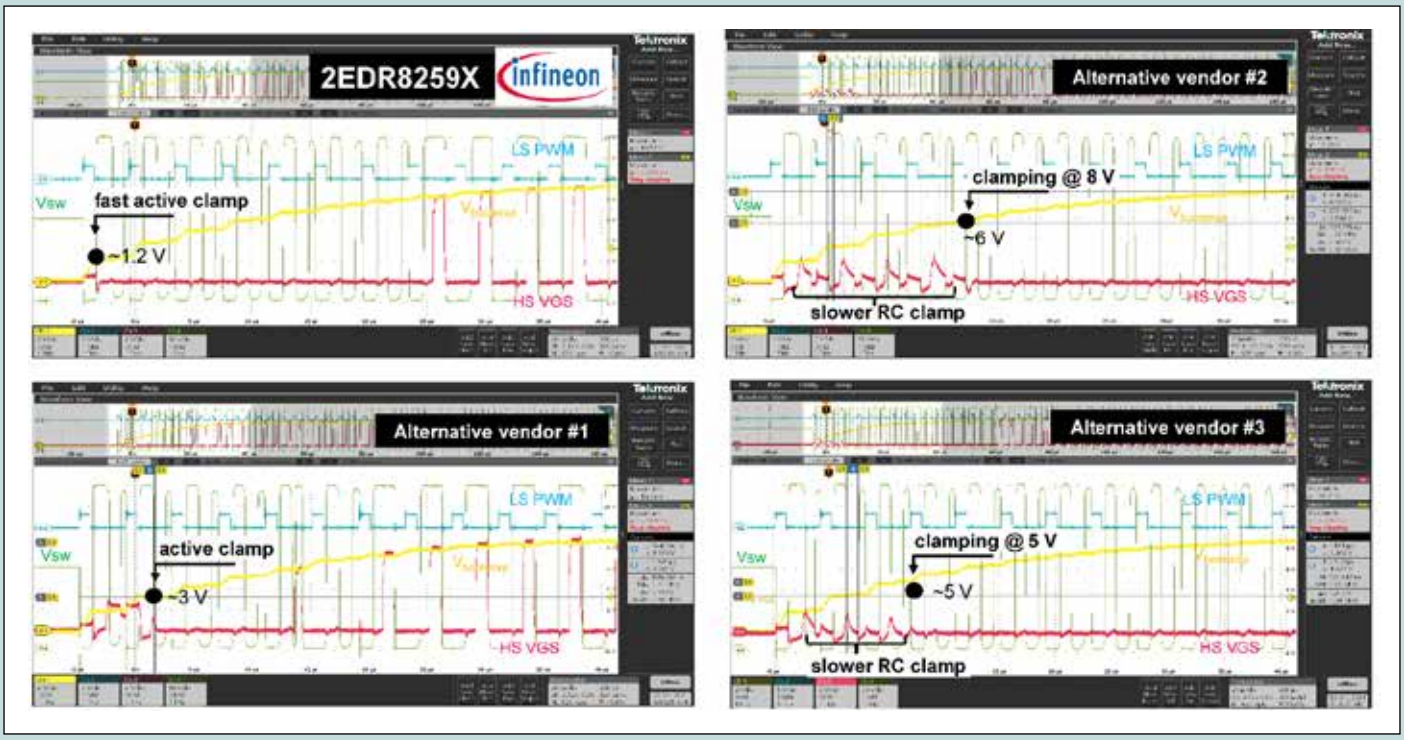

Figure 3: *An active output clamp acts faster than an output stage with an internal RC clamp.*

Right UVLO shutdown time

When it gets to UVLO-triggered output-stage shutdown, the primary objective is to be fast enough to protect the switching device from thermal overload.

Concurrently, if only an intermittent drop below the $UVLO_{off}$ threshold happens, the switching stage should not be turned off.

Practical experience shows that a shutdown delay of 500 ns is a good choice to avoid that noise or ringing on V_{DD}, which, for example, can be caused by a load jump and initiates an undesired output-stage shutdown.

Active output clamping

The purpose of output clamping is to ensure that the output stage is safely off while the gate-driver supply is still below the $UVLO_{on}$ threshold. This reduces the risk of shoot-through during bootstrapped startup of half-bridges.

When the supply is above the $UVLO_{on}$ threshold, the gate-driver IC is expected to propagate the control input to the output stage; i.e., the output is no longer clamped but following the input signal.

In a bootstrapped half-bridge stage, when the low-side is switching to charge the boost capacitor, the capacitive voltage divider consisting of C_{GD} and C_{GS} of the high-side switch causes an increase of V_{GS} over its on-threshold. Gate-driver IC output clamping has the purpose to avoid V_{GS} exceeding this on-threshold — effectively, it short-circuits the on-threshold. If output clamping does not happen, the high-side switch turns on simultaneously with the low-side, creating a half-bridge shoot-through.

Advanced gate-driver ICs have an output-clamping circuit that becomes active at V_{DD} levels as low as 1.2 V. This is perfect for a "schoolbook-like" startup of the high-side switch (see **Figure 3**).

In contrast, if a gate-driver IC has a slow internal RC clamping circuit, a certain level of shoot-through occurs during the startup of the half-bridge until V_{DD} is eventually high enough to activate an output-clamping circuitry. This is undesirable because it leads to EOS for the switching devices.

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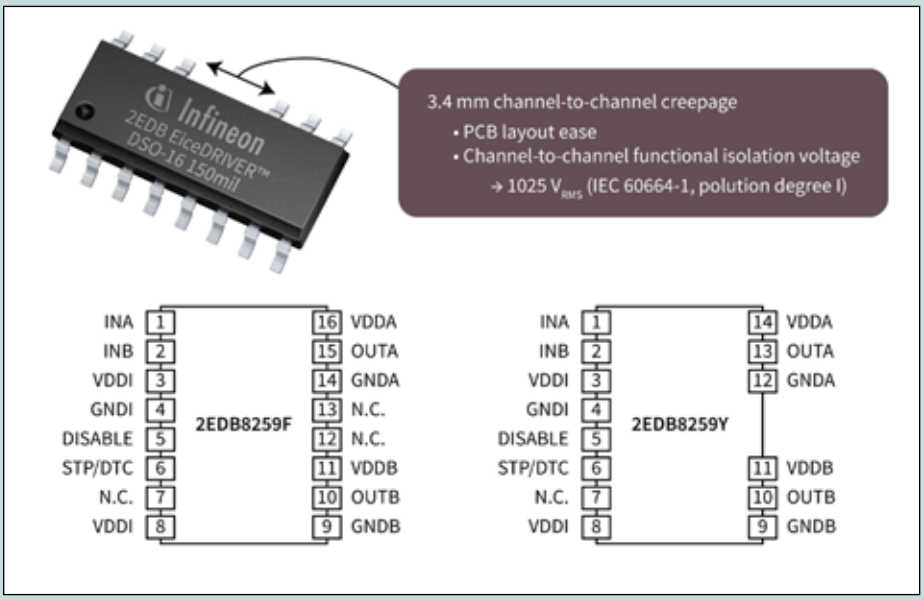

Figure 4: *14-pin versus 16-pin DSO package comparison*

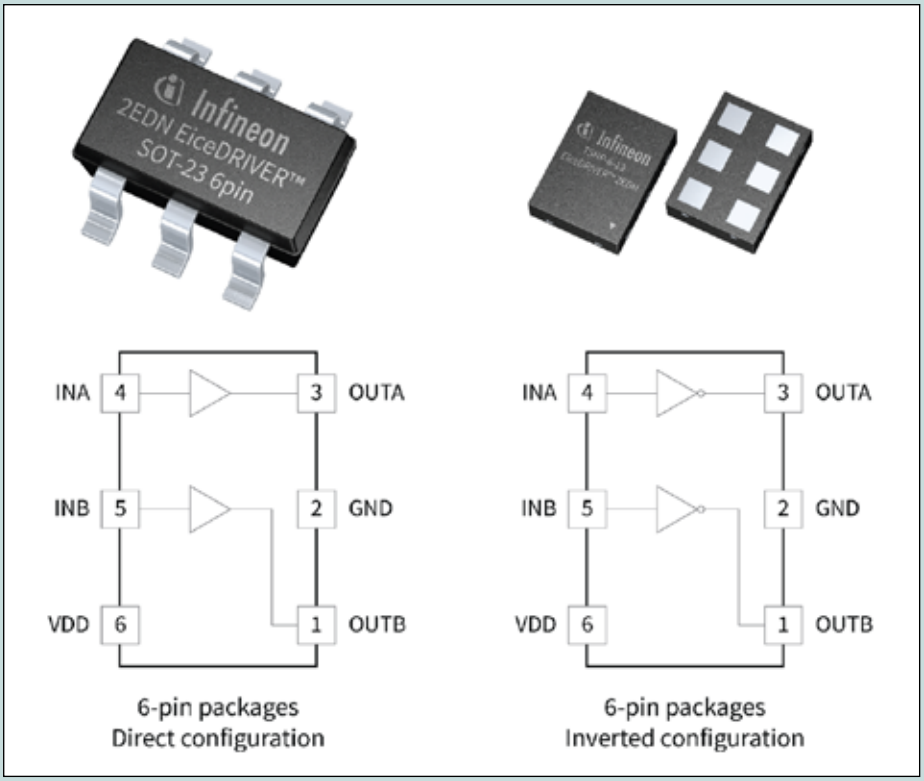

Figure 5: *Examples of dual-channel low-side gate-driver ICs in small-form–factor packages*

Shoot-through protection with configurable deadtime

Introducing deadtime in half-bridges enables the switch's tail current to decay, after the switch has been turned off and prior to the other side of the half-bridge being turned on. Otherwise, shoot-through would likely occur. For superjunction power MOSFETs, e.g., CoolMOS™ from Infineon Technologies, typical decay times are in the range of 300 ns.

In a properly working system, the software running in the controller IC caters to this deadtime. This way, the controller IC manages the effective duty cycle of that switching stage. When determining the software-controlled deadtime, the real-time performance of the controller IC hardware, the operating system, and the application software all come into play. Consequently, effective software-based deadtimes are typically not shorter than 300 ns. In most cases, they are significantly longer.

To hedge against cases of malfunction in the software-based deadtime control, the shoot-through and deadtime control built into the gate-driver IC serves as a second-level safety mechanism to prevent shoot-through.

Modern-day dual-channel isolated gate-driver ICs offer a configurable deadtime setting through an external resistor. The selectable deadtimes range from as short as 10 ns to as long as 1,000 ns. This renders such gate-driver ICs very versatile for a range of power-switch technologies, including GaN power switches. The accuracy of this deadtime can be as good as ±15%. As a matter of fact, this is frequently substantially more precise than the actual control IC-based deadtime control.

Package innovations

Dual-channel galvanic isolated gate-driver ICs in 150- and 300-mm DSO packages are frequently offered in a 14-pin configuration. At the gate-driver IC level, the difference between the traditional 16-pin and the increasingly more popular 14-pin configuration is that formerly "no connect" pins on the output side are physically no longer present (**Figure 4**).

This opens up additional PCB top-level routing options. Alternatively, because the resultant channel-to-channel creepage distance is increased to 3.4 mm, referring to IEC 60664-1, Pollution Class I, this can permit a channel-to-channel functional isolation voltage of up to 1,025 V_{RMS}.

Where the package size of galvanic isolated gate-driver ICs is of great importance, designers can now use leadless 4 × 4-mm² package options. The PCB area savings from a 4 × 4-mm² gate-driver IC, relative to the default 5 × 5-mm² form factor, is 36%. The input-to-output isolation rating corresponds to V_{ISO} = 2,250 V_{RMS} (UL 1577).

While most modern dual-channel low-side gate-driver ICs feature two enable inputs, these inputs are frequently tied to a fixed potential, which means they are effectively not used. Therefore, what is the reason for having such inputs, especially when high power density is desired?

Dual-channel low-side gate-driver ICs with six-pin packages, such as leaded SOT-23 or even leadless ultra-tiny 1.1 × 1.5-mm² six-pin packages like TSNP, can be a very pragmatic and cost-effective approach (**Figure 5**). This way, all the benefits that a gate-driver IC brings — such as digital on/off behavior, defined UVLO, 5-A strong output stages, and single-digit nanosecond propagation delay accuracy — are there. Concurrently, PCB area consumption is minimized and PCB layout flexibility is improved.

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CONCLUSION

Galvanic isolation integrated into gate-driver ICs has evolved from a product feature with certification only valid at the zero-hour status to a product property that is specified for an operational lifetime of 20 years. With proper application design in place, the isolation function and package integrity can remain uncompromised even in severe cases of EOS.

Shortening UVLO startup time expedites system startup and avoids mains-power-transformer saturation. Right-dimensioned UVLO shutdown times hedge against thermal overstress of switching devices and help maintain operational robustness in case of V_{DD} noise or ringing.

While the gate-driver supply is still below the $UVLO_{on}$ threshold, active output clamping provides a low-impedance path of the gate-driver ICs output to the ground. This is the most versatile approach to avoid shoot-through of half-bridge stages during bootstrapped startup.

Configurable shoot-through protection and deadtime control built into the gate-driver IC hardware are important second-level safety mechanisms. Package innovation includes the removal of unused pins, formerly declared to be "no connects," and gets us to ever-smaller dimensions. ■

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REFERENCES

[1]Baierl, H. (2018). "EiceDRIVERTM Solve Ground Shift Issues in Power Supplies." Elektronicnet.com.
[2]Baierl, H. (May 2018). "No more ground-shift challenges to your SMPS design." Power Electronics News.
[3]Baierl, H. (May 2013). "Intelligent diagnostics optimize factory-floor up-times." EE Times Europe.
[4]Baierl, H. (May 2011). "Providing Intelligent Protection." Bodo Power Systems.

Hubert Baierl *has product marketing responsibility for EiceDRIVER™ gate-driver ICs and ISOFACE™ products at Infineon Technologies. The gate-driver ICs he supports are mainly used in CoolMOS™ superjunction MOSFETs, CoolSiC™ SiC MOSFETs, CoolGaN™ GaN HEMTs, and low- and medium-voltage OptiMOS™ switching applications. Baierl holds a master's degree in electrical engineering from Louisiana State University, U.S., as well as an MBA from Universität Augsburg, Germany.*

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