

Conducted EMI Reduction Techniques for Wireless Power Systems

The article presents the wireless power transfer (WPT) systems operation and challenges in meeting EMI, especially the conducted emission requirements. A solution and its operation is described using a system model, considering key parasitics elements of the system.

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Introduction

Over the past decade, inductive wireless power transfer (WPT) has seen widespread adoption across various industries. Major industry standards such as Qi managed by Wireless Power Consortium (WPC) are advancing newer standards such as Magnetic Power Profile (MPP) with Qi2 for better user experience and efficiency.

The convenient and fast charging experience makes inductive WPT an ideal solution for automotive, industrial, and smartphone charging applications. Moreover, market trends are now shifting towards battery-powered products that require even higher power charging

EMI in WPT systems

EMI management is a crucial aspect of WPT design due to the presence of electromagnetic fields in the large air gap between the PTx and PRx coils. Thus, it is imperative to understand all potential sources of EMI for mitigation during design.

EMI is typically in two categories: conducted emissions (CE) and radiated emissions (RE). Both can interfere with electronics; therefore, regulations limit allowable emissions so that all devices can operate normally and simultaneously. This article describes possible sources of CE EMI and presents some mitigation techniques.

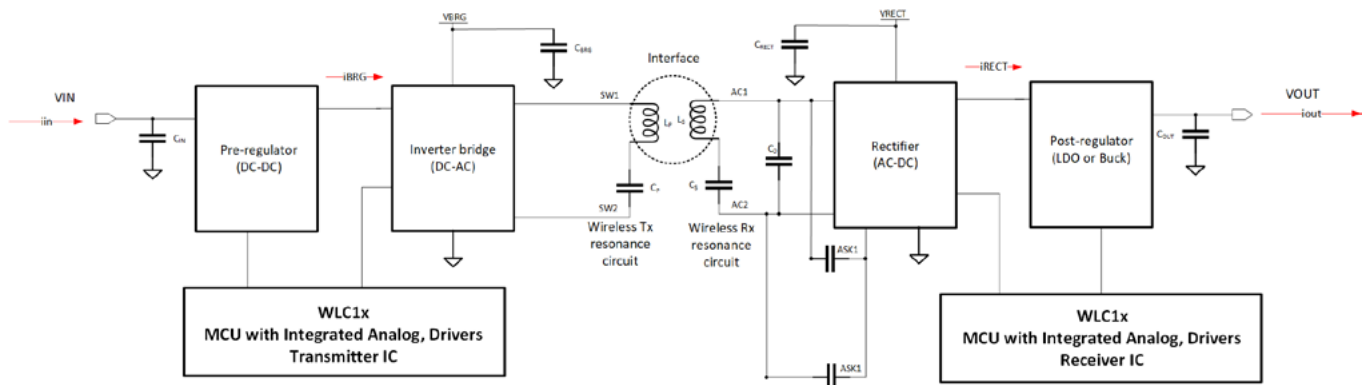


Figure 1: Typical wireless charging system

capabilities such as home robots, light electric vehicles (e-bikes), portable speakers, and consumer healthcare devices. However, with greater power comes the system challenges of electromagnetic compatibility (EMC), safety, and efficiency over and above standardization.

This article describes key design aspects of WPT systems with special focus on conducted electromagnetic interference (EMI). Throughout this article, the block system diagram in Figure 1 is considered to describe the functional blocks of the system and impacts on EMI.

WPT system overview

The WPT system consists of a power transmitter (PTx) and a power receiver (PRx). Power flow is from the PTx (source) to PRx (load). The transmitter coil inductively couples to a receiver coil to transmit power to PRx, which is regulated using an in-band feedback loop. The typical WPT system comprises multiple power conversion switching stages starting from VIN: pre-regulator (DC-DC), full-bridge inverter (DC-AC), and rectifier (AC-DC). All these switching stages are potential sources that generate EMI.

To effortlessly manage all the stages, Infineon offers a wide range of highly integrated wireless charging controllers and power MOSFETs for automotive and consumer applications and provides reference solutions with configuration options that help meet stringent regulatory and compliance requirements. Visit our dedicated [Wireless Charging website](#) to find more information on WLC1x controllers and OptiMOS™ FETs.

Common-mode (CM) current and its impact on conducted emission (CE)

Common-mode (CM) currents are one of the main sources for CE EMI. The CM current is the difference between the positive and negative rail currents; it is created by pulsing nonsymmetric nodes (such as SW1 and SW2) and parasitic capacitances.

To explain the potential CM current paths, a circuit of a WPT system along with a line impedance stabilization network (LISN) is shown in Figure 2a, which is based on [1]. The LISN and Earth GND are parts of the standard CE EMI measurement test setup. Figure 2a represents potential parasitic capacitances of the system including those from switching nodes of the inverter (C_{gs}) and PCB GND to the reference plane/Earth (C_{gg}). The CM current contributes to a significant amount of energy in CE.

CM current sources and paths

In Figure 2a, the switching nodes of the inverters SW1 and SW2 (Q2 and Q4 drains) are sources of CM voltages because ensuring symmetric switching is difficult owing to cost and production variations caused by imperfect drivers, clocks, and parasitic MOSFET capacitances. Subtle asymmetries between SW1 and SW2 result in CM voltage differences, which induce a CM voltage (see V_{cm1} and V_{cm2}).

In a typical power converter, V_{cm1} and V_{cm2} result in a CM current through parasitic capacitances C_{gs} and C_{gg} . In case of WPT, two additional parasitic capacitances from the coils to the reference GND plane are also present (C_{gc}) [1]. C_{gc} is formed by the transmitter coil as it is a fairly large piece of copper, which appears as one plate

of a capacitor when the previously introduced CM voltages (V_{cm1} and V_{cm2}) exist across its windings caused by SW1 and SW2. These voltages result in the CM current via C_{gc} that conducts back to the LISN through the Earth GND. These CM currents contribute to CE when they return to the main power line through the LISN and Earth GND connection instead of the PCB GND connection.

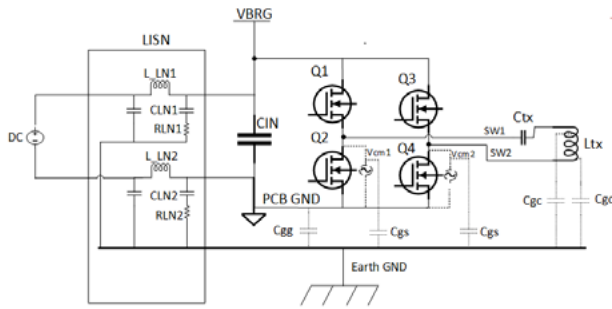


Figure 2a: Circuit diagram of the test equipment and inverter with parasitic capacitances shown

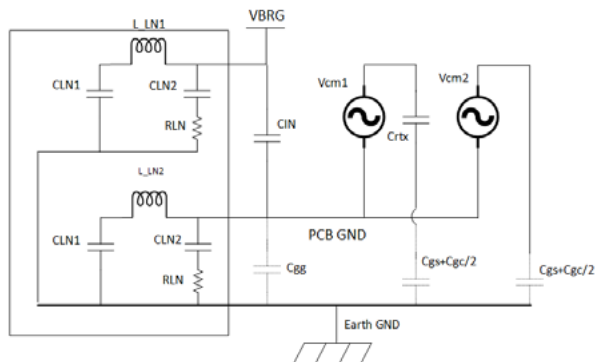


Figure 2b: Equivalent circuit with parasitic capacitances

Figure 2: Circuit diagrams showing test equipment and inverter (2a), and the modified equivalent circuit with parasitic capacitances (2b)

A further simplified equivalent circuit is shown in Figure 2b. For understanding the CM current paths through C_{gc} , a linear variation of the electric field and capacitance is assumed across the coil; thus, the total lumped capacitances are shown as two equal capacitances from each end of the transmitter coil ($C_{gs} + C_{gc}/2$).

Considering the CE test frequency (150 kHz–30 MHz) as the frequency of interest, C_{IN} and C_{tx} can be considered as shorted, which results in the modified equivalent circuit shown in Figure 3a, which also shows the CM current paths. It is clear that in addition to C_{gg} and C_{gs} , additional parasitic capacitances (C_{gc}) also result in CM currents [1]. This additional CM current due to the C_{gc} capacitance deteriorates the CE performance.

Proposed solution for CM current mitigation

To overcome the impact of the CM current due to C_{gc} , a PCB shielding filter is proposed. The PCB shield is connected to the PCB GND; it reduces or eliminates the effect of the C_{gc} capacitance by introducing a new capacitance, C_{shield} (Figure 3b), which becomes the dominant capacitance.

C_{shield} redirects the current that was flowing through the Earth GND to PCB GND, equalizing the absolute value of the current in the positive and negative power supply conductors powering the device. This reduces the CM current flowing to the Earth GND and via the LISN. The effect of the shield PCB is shown in the equivalent circuit (Figure 3b). The shield PCB design should ensure a capacitance (C_{shield}) of a much higher value than C_{gc} . This dominant capacitance can be created without impacting the magnetic field by creating traces and GND connection with a single PCB. Note that the traces must be equally spaced across the PCB and each trace width and air gap must be thin (~5 mil).

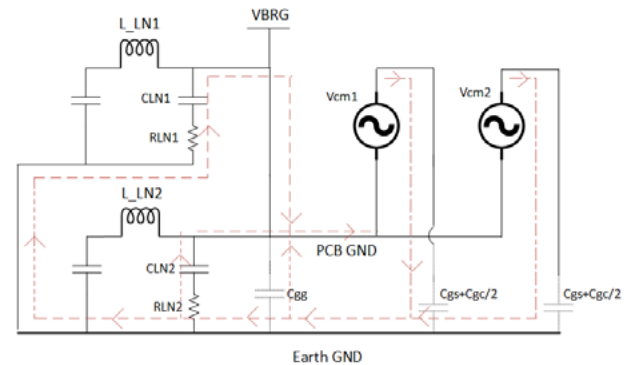


Figure 3a: Modified equivalent circuit and CM currents

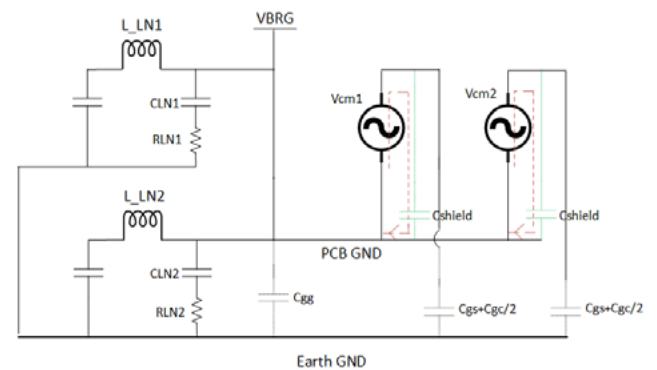


Figure 3b: Equivalent circuit and CM currents with shield PCB

Figure 3: Modified equivalent circuit with CM currents, (3a) equivalent circuit and CM currents with shield PCB (3b)

A similar analysis holds good for PRx: a shield PCB improves the CE performance for PRx. The parasitic capacitance between the PTx and PRx coils when they are mated comes in play for the PRx CM current.

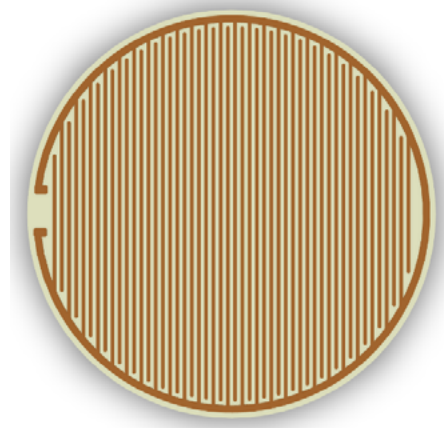


Figure 4: PCB shield for CE

Other design considerations for optimum CE performance

Note that CM currents result from CM voltages that are directly related to the speed of the switching node (slew rate). Therefore, increasing the drain-to-source capacitance of the inverter FETs (Q2 and Q4) or the external capacitance on these nodes also helps minimize the negative impact of the CM current on CE.

The external capacitance on the switching node also affects the zero voltage switching (ZVS) performance. A higher switching node capacitance improves the CE performance; however, it might over-damp the switching node response and negatively impact the efficiency. Thus, it is important to tune the switching node capacitances for ZVS and optimum CE performance. Refer [2] for details.

Experimental results for CE

The following test results represent a common CE test result per CISPR 32 from a WPT system. It is common for the fundamental inverter frequency to appear in the EMI spectrum during testing if proper tuning and shielding are not in place. Figure 5 shows the difference in the EMI performance before and after the implementation of the proposed solution. After applying shielding and tuning the inverter ZVS, the previous EMI result is improved.

Conclusion

The article explained the WPT ecosystem and mode of operation in brief and presented a basic overview of EMI types and potential sources. Using the circuit model of a WPT system, the related parasitic capacitances were presented and explained. Reference [1] is used to arrive at the equivalent circuit with parasitic capacitances.

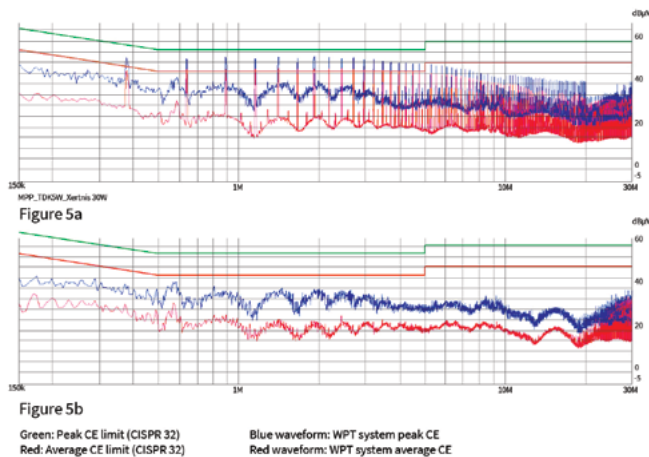


Figure 5: CE result with proper tuning and good layout practices

A shield PCB approach is presented and its positive impact on CE performance is analyzed with the help of an equivalent circuit and experimental results. Other design aspects of WPT systems which would affect CE performance are also detailed.

For more information about Infineon's Wireless Charging solutions – click [here](#).

References

- [1] Chunyu Wu, Hongseok Kim, Srinath Penugonda, and Jun Fan: "Analysis and Modeling of the Common-Mode Conducted EMI From a Wireless Power Transfer System for Mobile Applications", IEEE Transactions on Electromagnetic Compatibility, Vol. 63, No. 6, December 2021; <https://ieeexplore.ieee.org/document/9468413>
- [2] Infineon Technologies AG: "Hardware design guidelines for WLC transmitter (WLC1115), AN234666", Infineon website, 2022

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Milind Dighrasker is Director Applications at Infineon and has 20+ years of experience. He holds a Master's degree in Power Electronics and has 11 patents in the areas of his interest: bi-directional DC/DC converters, wireless power transfer, PFC circuits, and battery charging.

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