Designing a 30 kW 3-phase Interleaved T-Type Vienna PFC for AI Server Power Supply

How topology, device strategy, and real-time control shape the next generation of AI power supplies

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As AI server rack power continues to rise, substantial changes in server rack architectures evolve as shown in Figure 1. Current generation racks (Gen 1) contain both power delivery components as well as backup power and IT payload, leveraging single-phase PSUs of increasing wattages. As rack power levels go beyond 250 kW the next generation (Gen2) architecture is shifting towards dedicated sidecar racks for power delivery and backup power, with PSUs shifting toward three-phase AC input, HVDC distribution and power levels up to 30 kW (Figure 1, [1]).

The scope of this article is to demonstrate the 3-phase PFC evaluation board design and exceptional efficiency and power density to enable next generation PSUs.

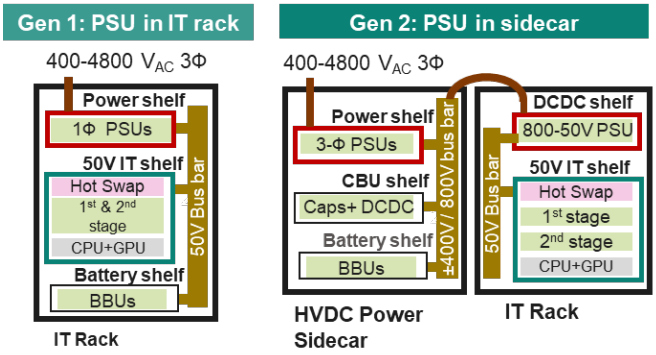


Figure 1: Power evolution for AI server rack architecture and PSUs

Board specifications

The newly developed EVAL_30KW_TTYPE_PFC (Figure 2) demonstrates a 30 kW, three-phase interleaved T-Type Vienna PFC front end for AI server power supplies in 1U form factor. The platform combines 650 V CoolGaN™ Bidirectional Switch (BDS) in the back-to-back path of the T-type Vienna, 1200 V CoolSiC™ MOSFETs in the high-voltage rectifier path, and PSOC™ Control C3 Performance Line for full digital control.

Design specifications	
Input voltage range	360 V_{AC} ~ 528 V_{AC} line to line voltage (3 phase)
Output voltage	890 V_{DC} nominal
Output current	33.33 A
Output power max	30 kW
Efficiency	> 99%
Power factor (load > 10%)	PF > 0.98, 20% ➞ 80% load iTHD < 10%, 20% ➞ 80% load
Temperature ambient	-5°C to 45°C (OCP)
Size	133 x 342 x 40 mm

This evaluation board is designed to naturally fit into the complete PSU, where it can feed a downstream DC-DC stage, which is an arrangement that becomes relevant once the architecture moves toward next generation PSUs with three-phase input and HVDC output ([1]).

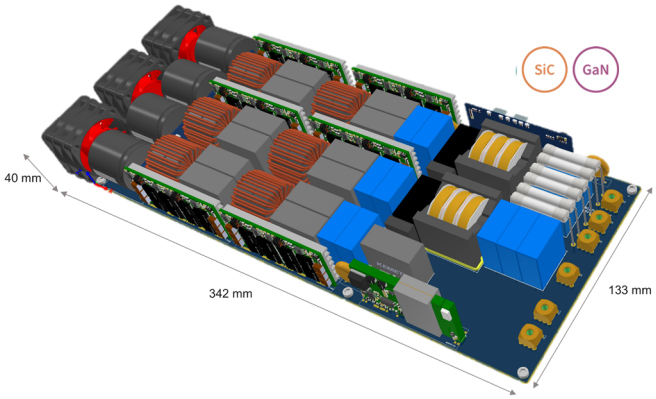


Figure 2: Board and component overview

Interleaved 30 kW T-Type Vienna front end

At 30 kW, the PFC stage is crucial to reach the required efficiency, power density and thermal behavior, of an AI server PSU. The design is no longer only about scaling up the power; it is about choosing a topology that can handle three-phase input, establish a high-voltage DC bus efficiently, and fit in the specified server PSU form factor.

The board presented is valuable because it makes practical design trade-offs visible. At this power level, conduction loss, choke design and current ripple, gate-drive quality, control design, and the use of wide-bandgap devices all have a direct influence on the electrical and thermal behavior of the platform.

The interleaved architecture of this board was chosen because it addresses several board-level requirements at once:

- **Low height fitting in 1U server power shelves form factor.** In the interleaved implementation, the current in each inductor choke is equal to half the phase current, resulting in smaller inductor size.
- **Manageable input filtering effort.** The presented design implements two CH270060GT cores with 28 turns for each of the interleaved stages. The switching frequency associated with each choke current is 72 kHz, while the effective ripple frequency per phase is 144 kHz. Figure 3 illustrates the effect of ripple cancellation at the phase current side. Leading to EMI filter reduction.
- **Better thermal management.** Interleaving also helps by distributing power losses of switches and magnetics across different areas of the board, which leads to more flexible and relaxed ther-

mal solutions and heat sinks design, and avoids concentrating the full thermal burden in one local region of the layout.

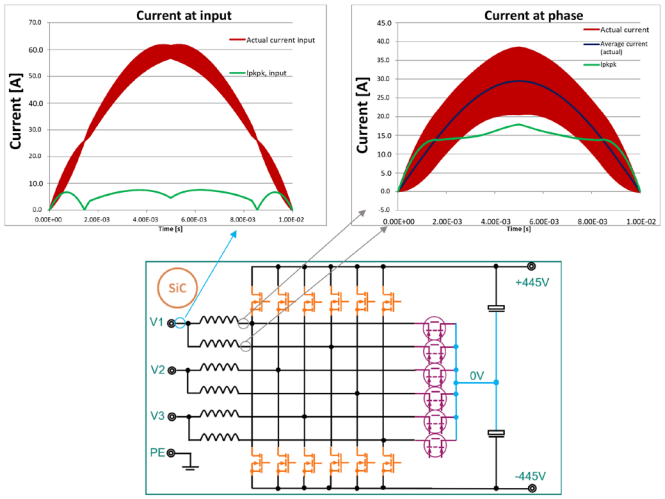


Figure 3: Interleaving rationale: phase current vs. input current, ripple reduction, and EMI implication

PSOC™, SiC, and GaN BDS on the board

As mentioned earlier, the board architecture (Figure 4) is built around three elements:

- 650 V CoolGaN™ BDS in the bidirectional switching path
- 1200 V CoolSiC™ MOSFETs in the higher-voltage rectification path
- PSOC™ Control C3 Performance Line for digital control

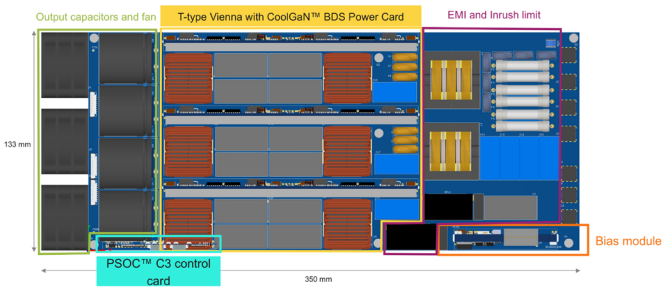


Figure 4: Board distribution of EVAL_30KW_TTYPE_PFC

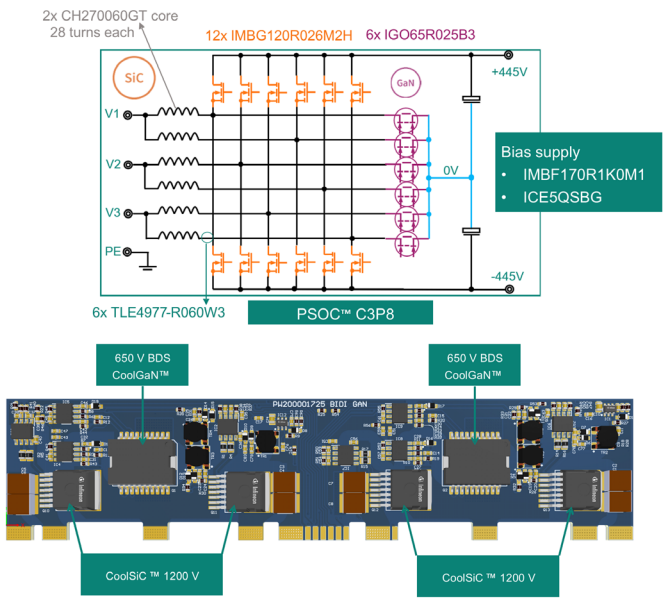


Figure 5: Power card with the power semiconductors to implement an interleaved T-type Vienna rectifier

Together, these elements define how the platform reaches its efficiency, controllability, and density targets at 30 kW. The GaN BDS path is fundamental to the T-type Vienna implementation, as it realizes the bidirectional switching function in a compact and efficient way. Each phase implements a power card with the interleaved stages as shown in Figure 5. The back side of the power card is empty of components and a heatsink is mounted to cool down the power semiconductors in bottom side cooled SMD packages.

The power stage includes IMBG120R026M2H and IGO65R025B3, with 1EDB9275F and 1EDB7275F gate drivers, TLE4977 R060W3 current sensors, and a dedicated bias implementation based on IMBF170R1K0M1 and ICE5QSBG.

The PSOC™ Control Performance Line implementation is one of the strongest differentiators of the board. The control architecture uses a three-CPU system (PSC3P8), which enables clustering the different functions needed to implement the power conversion in interleaved T-type Vienna rectifier. The main CPU subsystem is not used in the present implementation and it could be conveniently used for housekeeping and communications functions as well as telemetry and black box functions in the final application. The real-time power-conversion tasks are implemented in the Programmable Power Control Accelerator (PPCA). In the current partitioning, CPU0 handles PFC1 current-loop control, modulation, and PLL, while CPU1 handles PFC2 current-loop control, modulation, and the voltage loop (Figure 6). This gives each interleaved channel a clear control role and makes the implementation more scalable and easier to optimize.

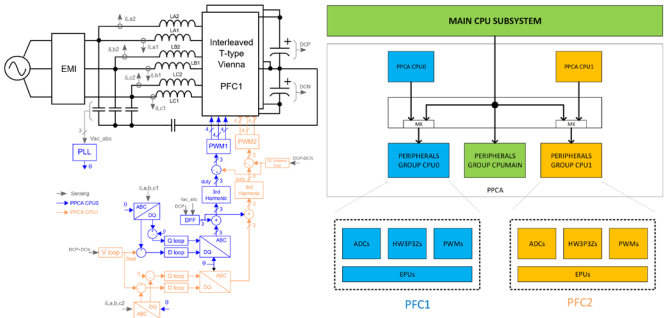


Figure 6: Digital control block diagram

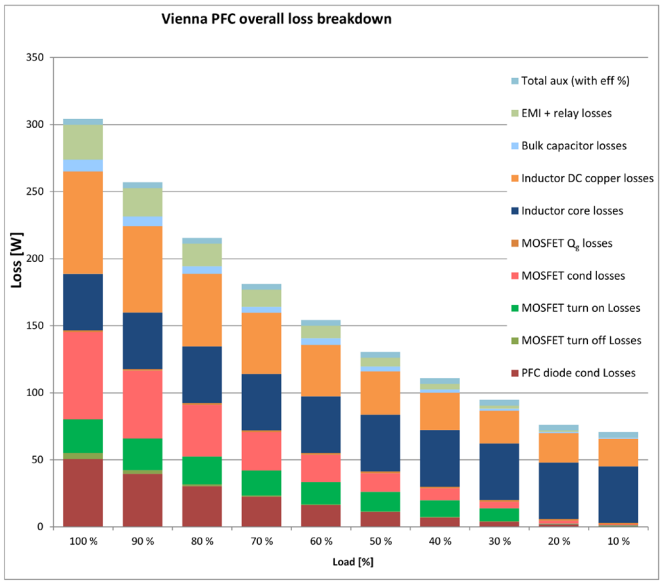


Figure 7: Breakdown of power losses at different load conditions

Power loss distribution

At 30 kW, the power stage cannot be judged by efficiency alone. We also must understand where the losses sit, how they shift with load, and what that means for magnetics, thermal spreading, and the next round of optimization. In our nominal operating view at 415 V_{AC} line-to-line and 890 V_{DC}, the dominant full-load contributions come from conduction losses in the CoolGaN™ BDS path and from core and conduction losses in the inductor. At lighter load, the inductor core losses become predominant. Figure 7 shows a breakdown of all power losses at different load conditions.

Measured results

The measured results show that the board operates as intended. Testing on the EVAL_30kW_TTYPE_PFC platform with 650 V CoolGaN™ BDS was carried out at 400 Vrms line-to-line voltage and 50 Hz, excluding fan power. Under those conditions, efficiency rises from roughly 92% at low load to a peak of about 99% near 60% load, and remains at 98.84% at full load. Full-load power loss is approximately 352 W, Figure 8.

Input-current quality is equally outstanding across the operating range, PF is well above 0.99 at 20% load and above, with a THD well under 6% from the same load point, Figure 9.

Figure 10 shows stable output DC voltage, defined grid-to-virtual-neutral behavior, and the expected choke-current behavior in one interleaved stage, alongside clean input AC waveforms.

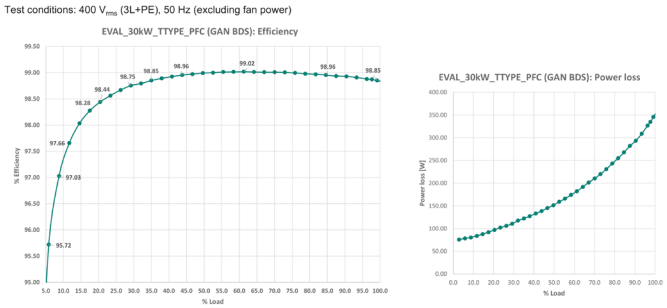


Figure 8: Measured efficiency and power loss

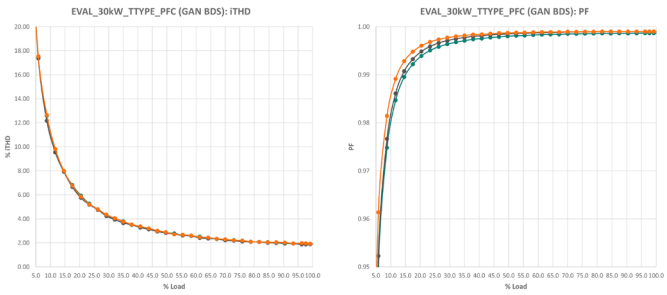
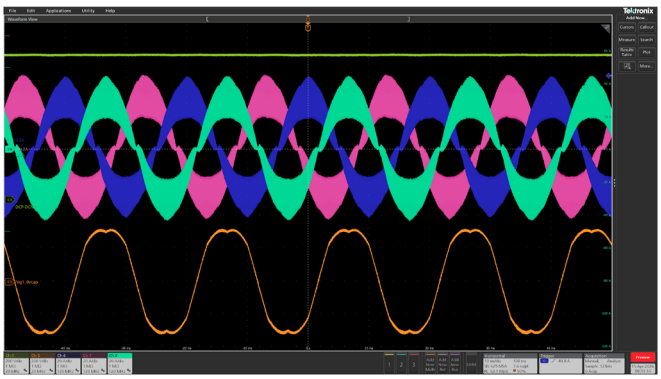


Figure 9: Measured iTHD and power factor



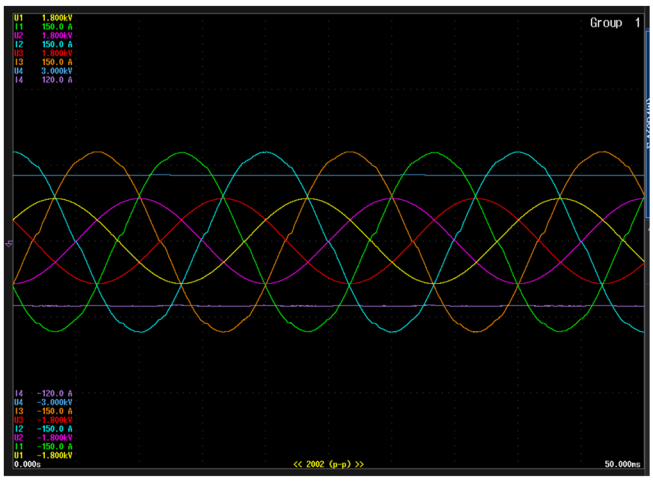


Figure 10: PFC stage waveforms (top to bottom): Output DC voltage (dark green)–, PFC choke currents in one of the interleaved stages (green, pink, blue), grid to AC virtual neutral (Orange), zoomed in PFC choke currents (orange, green, blue), and input AC waveforms (yellow, purple, red).

Summary

The 30 kW 3-phase PFC evaluation board from Infineon demonstrates the next evolutionary step in AI power. High-efficiency and power density are achieved by adopting wide-bandgap devices. The PSOC™ digital controller offers the capability and resources needed for an interleaved T-Type PFC converter. To learn more about how Infineon is powering AI from the grid to the core, visit https://infineon.com/aipsu

References

Infineon Technologies AG: Evolving power supplies and rack architectures to meet AI server demand; whitepaper; October 2025; (https://www.infineon.com/gated/infineon-evolving-power-supplies-and-rack-architectures-to-meet-ai-server_8ae9cd21-516d-4a3a-a681-84449d100fee)

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