XDP™ XDP711-001 hot-swap controller errata

Wide input voltage range (7 V to 80 V) system monitoring and protection IC

About this document

Scope and purpose

This document lists the errata of the XDP™ XDP711-001 system monitoring and protection IC. It is recommended that the device behavior and proposed workarounds are considered for the application.

Intended audience

This document is intended for XDP711-001 users.

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1 Errata

1.1 VIN_UV_HYST not working after POR when UV/EN pin is connected to VDD_VIN through a voltage divider

If, after power-on reset (POR) (first start-up), the EN_DG timer expires before VIN_UV_FAULT_LIMIT is crossed, the FET correctly turns on when the input voltage at the VDD_VIN pin crosses VIN_UV_FAULT_LIMIT + VIN_UV_HYST level. Otherwise, the FET turns on when the EN_DG timer expires.

Workaround

- Use the ON bit in the OPERATION command to keep the FET off until desired
- When a UV/EN pin has a voltage divider from VDD_VIN, the farther away the UV analog limit is from the digital, the more time (depending on Vin slew rate) it takes for the voltage to reach the digital limit after the UV/EN threshold has been crossed, giving more time for EN_DG to expire
- Make the EN_DG timer as fast as possible so that it expires before VIN_UV_FAULT_LIMIT is crossed

References

[1] Infineon Technologies: *XDP™ XDP711-001 hot-swap controller datasheet;* Available online

[2] Infineon Technologies: *XDP™ XDP711 hot-swap controller PMBus® commands;* Available online

Revision history

Document revision	Date	Description of changes
1.0	2025-07-03	Initial release

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