Appendix

HybridPACK™ HD – Power Module Compact Model

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restricted

AGREEMENT ON THE USE OF HybridPACK™ HD COMPACT MODELS

- The information given in this presentation is given as a hint for the implementation of the Infineon Technologies components only and shall not be regarded as any description of warranty of a certain functionality, conditions or quality of the Infineon Technologies components. The statements contained in this communication, including any recommendation or suggestion or methodology, are to be verified by the user before implementation, as operating conditions and environmental factors may differ. The recipient of this presentation must verify any function described herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this presentation.

- Infineon offers design support tools and simulation models for Infineon Technologies AG HybridPACK™ HD power modules: PLECS, LTSpice*, and SIMetrix*. These models provide basic and qualitative results, for example, on the influence of the parasitic inductance of the connected DC link. This provides additional support in the (pre-) development phase of power semiconductor systems using Infineon products. *Exclusively available for Infineon HybridPACK™ HD – A2.1 modules.

- The intended audiences for product information and simulation models are qualified technical personnel, as design engineers, technicians and developers of electronic systems.

- Infineon takes no warranty that the models provided by Infineon Technologies fully reflect all specifications and operating characteristics of the respective semiconductor product.

- The model describes the characteristics of a device according to the stated maturity level. The current datasheet information for HybridPACK™ HD power modules always represents the design guideline and the only actual performance specification.

- The compact models are validated using electrical characterization measurements of the respective power module type (hardware). Based on the validated simulation results, the simulation show sufficient agreement across a wide range of electrical characterization measurements. However, deviations between the simulation results and the hardware measurements are to be expected.

- Although these compact models can be a useful tool for evaluating HybridPACK™ HD performance, they cannot predict performance under all conditions and are not intended as a substitute for hardware verification testing. The model is subject to change without notice. Infineon assumes no responsibility for errors or simulation issues.

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Module Compatibility:

F01MR14A60MA2XT_ENG

F01M2R14A60MA2XT_ENG

F01M5R14A60MA2XT_ENG

- Power Module ENG maturity level **A2.1**

Good to know:

Power Module Compact Model Version: **A2.1**

- updated versions can be identified by version numbering
  - -vx.y = consecutive number, 1 … x, describing majority level of the Compact Model Version
  - -vx.y = consecutive number, 1 … y, describing minor changes of previous Compact Model Version
- changes without prior notice

Module Compact Models available on request for:

- **SIMetrix**
- **LTspice**

Good to know:

- **SIMetrix:** no remark
- **Ltspice:** LTspice lacks the rigorous pre-simulation checks and ends up flagging this as an error. Based on this wrong error message the simulation may complete with an error message.
  - Option1: Use the results, no incorrect simulation results due to this wrong error message could be identified.
  - Option2: Using the SIMetrix simulator with the SIMetrix model

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HybridPACK™ HD – Power Module Compact Model Appendix LTSpice

Pin assignment of the compact model according to the module datasheet circuit

P1 = 1
N1 = 2
AC1 = 3
SYS01_G = 5
SYS01_S = 6
SYS01_D = 4
SYS02_G = 8
SYS02_S = 9
SYS02_D = 7
Tcase = chip temperature

Available files:
*.lib = Module LTspice model
*_L1_.asy = Symbol w/Tcase
*_L0_.asy = Symbol w/o Tcase

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Header in encrypted LTspice models

Recommended header:
(The „* Begin:* - Line is not necessary)

Lines from LTspice encryption process **(Required)**

Infineon disclaimer

```
1  * LTspice Encrypted File
2  *
3  * This encrypted file has been supplied by a 3rd
4  * party vendor that does not wish to publicize
5  * the technology used to implement this library.
6  *
7  * Permission is granted to use this file for
8  * simulations but not to reverse engineer its
9  * contents.
10 *
11 * DISCLAIMER
12 *
13 * INFINEON'S MODEL TERMS OF USE
14 *
15 * BY DOWNLOADING AND/OR USING ...
16 *
17  9A 38 10 40 A3 54 49 7E AB F2 33 2C 69 8E AC 41
18  7B FE 20 0E 76 AC F1 30 A3 0E 78 84 15 C4 22 19
```


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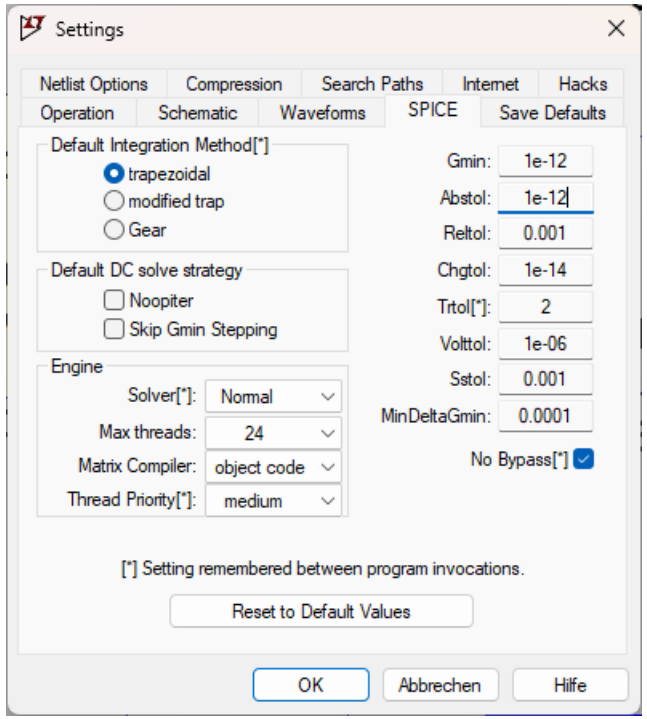
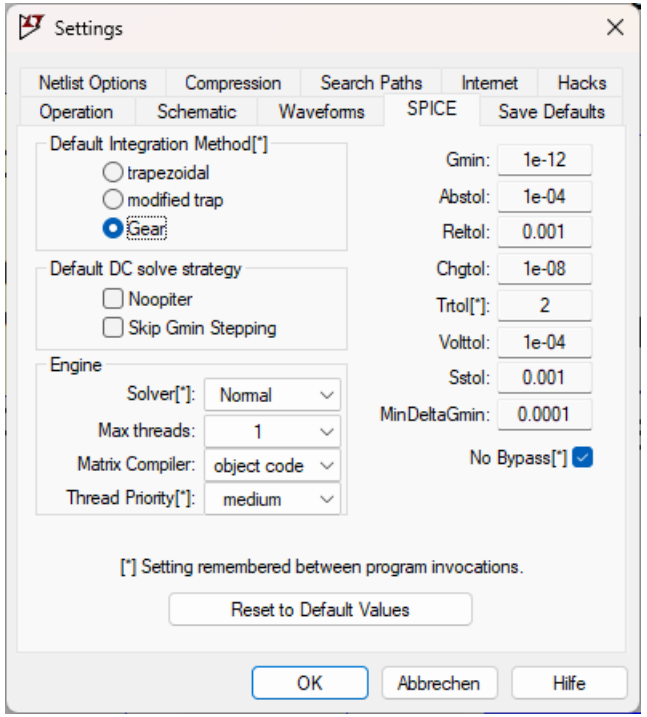
General Hint LTSpice

The default settings in LTspice are these:



It is better to **start with relaxed settings**. The setting can be toughened on demand.

Relaxed settings:



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