Comparison of CTM to DTM of IR3897

This comparison serves as both of CTM verification and its error estimate reference.

3-die CTM Compared to **DTM** on the evaluation board
Q1 is top-side FET, Q2 is bottom-side FET, IC is control IC

DTM -- Detailed Thermal Model
CTM -- Compact Thermal Model

Normal condition comparison

T_ambient = 25 deg C, 1 phases, two Fets power loss ratio= Q1/Q2, Pd_Q1+Q2= 3W, Pd_IC = 0.085W;

case #	Q1/Q2	Pd_pak	airflow	heatsink	T_Q1		T_Q1 rise diff.	T_Q2		T_Q2 rise diff.	T_IC		T_IC rise diff.
					DTM	CTM		DTM	CTM		DTM	CTM	
		(W)	(LFM)	H=15mm	(deg C)	(deg C)	%	(deg C)	(deg C)	%	(deg C)	(deg C)	%
1	0.5	3.085	200	yes	72.8	73.7	1.8	92.5	91.6	-1.4	49.3	49.2	-0.6
2	1	3.085	200	yes	82.5	82.6	0.1	82.7	82.7	-0.1	48.9	48.9	-0.1
3	2	3.085	200	yes	92.2	91.5	-1.1	72.9	73.8	1.8	48.5	48.6	0.2
4	0.5	3.085	200	no	84.0	84.4	0.6	107.0	106.2	-0.9	61.1	61.0	-0.3
5	1	3.085	200	no	93.7	93.8	0.1	96.1	96.1	0.1	60.4	60.4	0.2
6	2	3.085	200	no	103.9	103.2	-0.9	85.2	86.0	1.4	59.7	59.8	0.4

Note: For these normal cases, the junction temperature rise difference is within 1.4%. (red number is junction temperature)

Extreme condition comparison

Q1/Q2 = 1 for the following cases

case #	voided	Pd_pak	airflow	heatsink	T_Q1		T_Q1 rise diff.	T_Q2		T_Q2 rise diff.	T_IC		T_IC rise diff.
					DTM	CTM		DTM	CTM		DTM	CTM	
		(W)	(LFM)	H=15mm	(deg C)	(deg C)	%	(deg C)	(deg C)	%	(deg C)	(deg C)	%
7	VIN pad	3.085	200	yes	89.77	89.5	-0.5	83.5	83.6	0.2	49.2	49.3	0.2
8	SW pad	3.085	200	yes	83.3	83.5	0.4	90.5	90.3	-0.4	49.6	49.5	-0.3
9	VIN pad	3.085	200	no	103.2	103.0	-0.3	97.6	97.8	0.3	61.0	61.2	0.5
10	SW pad	3.085	200	no	95.5	95.9	0.5	107.1	107.6	0.6	61.9	61.9	0.1

Note: For these extreme cases, the junction temperature rise difference is within 0.6%. (red number is junction temperature)
VIN pad voided --- the under-package solder pad below top-side Fet is voided.
SW pad voided --- the under-package solder pad below bottom-side Fet is voided.