International
IOR Rectifier

Data Sheet No. PD60198 revF

IR2166(S)&(PbF)

PFC & BALLAST CONTROL IC

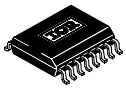
Features

- PFC, Ballast control and half-bridge driver in one IC
- Critical conduction mode boost type PFC
- No PFC current sense resistor required
- Programmable preheat frequency
- Programmable preheat time
- Programmable run frequency
- Programmable over-current protection
- Programmable end-of-life protection
- Programmable dead time
- Internal ignition ramp
- Internal fault counter
- DC bus under-voltage reset
- Shutdown pin with hysteresis
- Internal 15.6V zener clamp diode on Vcc
- Micropower startup (150μA)
- Latch immunity and ESD protection
- Parts also available LEAD-FREE

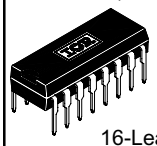
Description

The IR2166 is a fully integrated, fully protected 600V ballast control IC designed to drive all types of fluorescent lamps. PFC circuitry operates in critical conduction mode and provides for high PF, low THD and DC Bus regulation. The IR2166 features include programmable preheat and run frequencies, programmable preheat time, programmable dead-time, programmable over-current protection, and programmable end-of-life protection. Comprehensive protection features such as protection from failure of a lamp to strike, filament failures, end-of-life protection, DC bus undervoltage reset as well as an automatic restart function, have been included in the design. The IR2166 is available in both 16-lead PDIP and 16-lead (narrow body) SOIC packages.

Packages

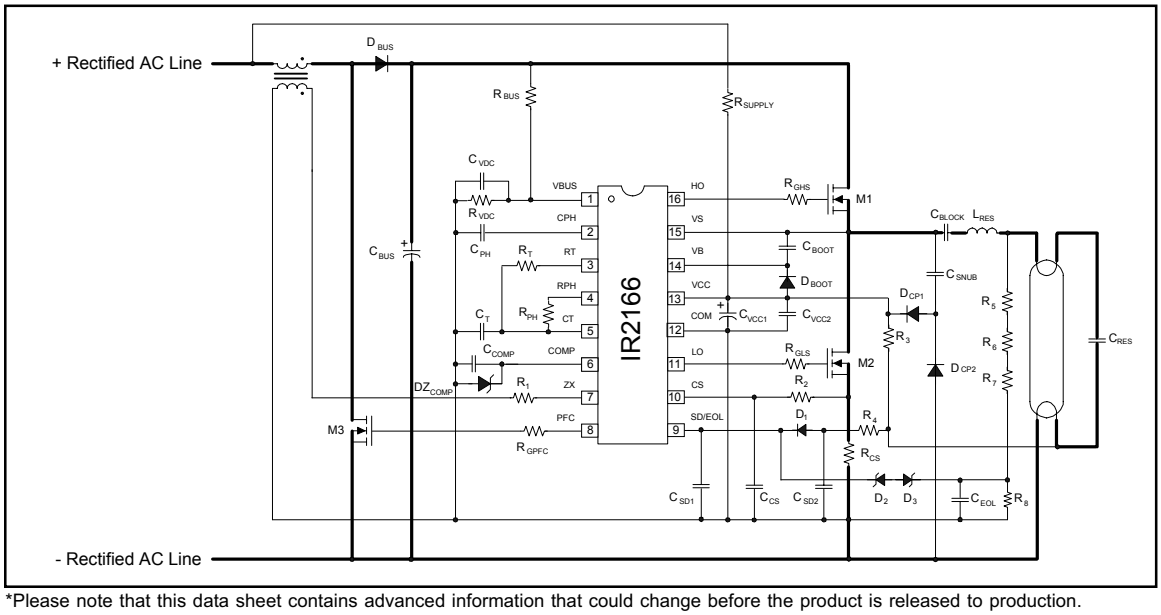


16-Lead SOIC
(narrow body)



16-Lead PDIP

IR2166 Application Diagram



*Please note that this data sheet contains advanced information that could change before the product is released to production.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{PFC}	PFC gate driver output voltage		-0.3	V_{CC} + 0.3	
I_{OMAX}	Maximum allowable output current (HO, LO, PFC) due to external power transistor miller effect		-500	500	mA
V_{BUS}	V_{BUS} pin voltage		-0.3	V_{CC} + 0.3	V
V_{CT}	CT pin voltage		-0.3	V_{CC} + 0.3	
I_{CPH}	CPH pin current		-5	5	mA
I_{RPH}	RPH pin current		-5	5	
V_{RPH}	RPH pin voltage		-0.3	V_{CC} + 0.3	V
I_{RT}	RT pin current		-5	5	mA
V_{RT}	RT pin voltage		-0.3	V_{CC} + 0.3	V
V_{CS}	Current sense pin voltage		-0.3	5.5	
I_{CS}	Current sense pin current		-5	5	mA
$I_{SD/EOL}$	Shutdown pin current		-5	5	
I_{CC}	Supply current (Note 1)		-20	20	
I_{ZX}	PFC inductor current, zero crossing detection input current		-5	5	
I_{COMP}	PFC error compensation current		-5	5	
dV/dt	Allowable offset voltage slew rate		-50	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(16-Pin PDIP)	—	1.80	W
	$P_D = (T_{JMAX}-T_A)/Rth_{JA}$	(16-Pin SOIC)	—	1.40	
Rth_{JA}	Thermal resistance, junction to ambient	(16-Pin PDIP)	—	70	°C/W
		(16-Pin SOIC)	—	86	
T_J	Junction temperature		-55	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: This IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_{BS}	High side floating supply voltage	V_{CC} - 0.7	V_{CLAMP}	V
V_S	Steady state high side floating supply offset voltage	-1	600	
V_{CC}	Supply voltage	V_{CCUV+}	V_{CLAMP}	
I_{CC}	Supply current	Note 2	10	mA
C_T	CT lead capacitance	220	—	pF
$I_{SD/EOL}$	End-of-life lead current	-1	1	mA
I_{CS}	Current sense lead current	-1	1	
I_{ZX}	Zero crossing detection pin current	-1	1	
T_J	Junction temperature	-25	125	°C

Note 2: Enough current should be supplied into the V_{CC} lead to keep the internal 15.6V zener clamp diode on this lead regulating its voltage, V_{CLAMP}.

Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, V_{BUS} = Open, R_T = 39.0kΩ, R_{PH} = 100kΩ, C_T = 470 pF, V_{CPH} = 0.0V, V_{SD} = 0.0V, V_{COMP} = 0.0V, V_{CS} = 0.0V, C_{LO} = C_{HO} = 1000pF, T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Supply Characteristics						
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	10.0	11.5	12.5	V	V_{CC} rising from 0V
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	8.5	9.5	10.7		V_{CC} falling from 14V
V_{UVHYS}	V_{CC} supply undervoltage lockout hysteresis	1.5	2.0	3.0		
I_{QCCUV}	UVLO mode quiescent current	145	170	290	µA	V_{CC} = 8V
I_{QCC}	Quiescent V_{CC} supply current	—	2.3	4.0	mA	CT connected toCOM VCC =14V
V_{CLAMP}	V_{CC} zener clamp voltage	14.3	15.6	17	V	I_{CC} = 10mA
Floating Supply Characteristics						
I_{QBS0}	Quiescent V_{BS} supply current	-1	0	5	µA	V_{HO} = V_S (C_T = 0V)
I_{QBS1}	Quiescent V_{BS} supply current	5	30	70		V_{HO} = V_B (C_T = 14V)
V_{BSMIN}	Minimum required V_{BS} voltage for proper HO functionality	—	2.5	—	V	
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V

Electrical Characteristics cont.

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, V_{BUS} = Open, R_T = 39.0kΩ, R_{PH} = 100kΩ, C_T = 470 pF, V_{CPH} = 0.0V, V_{SD} = 0.0V, V_{COMP} = 0.0V, V_{CS} = 0.0V, C_{LO} = C_{HO} = 1000pF, T_A = 25°C unless otherwise specified.

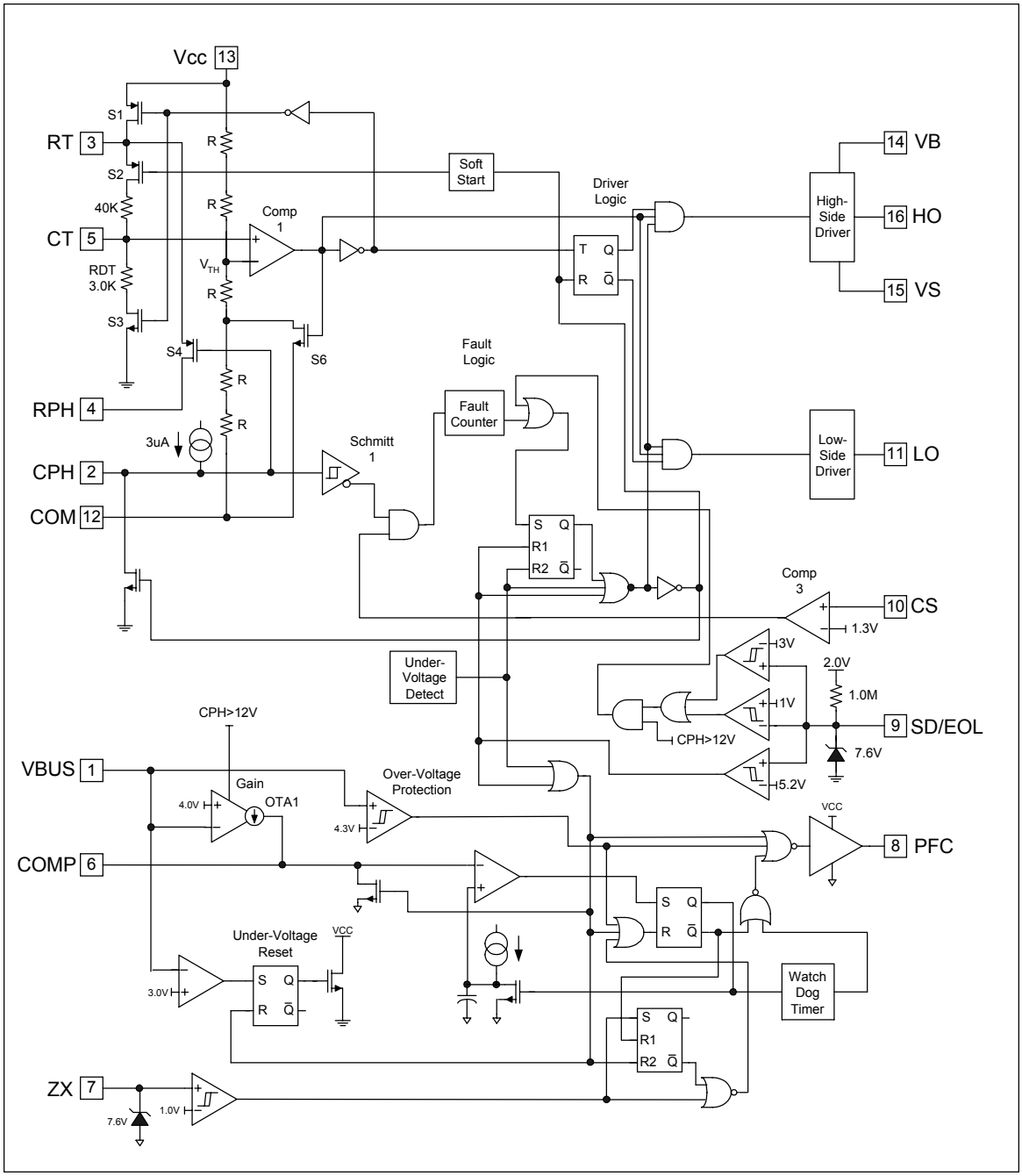
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
PFC Error Amplifier Characteristics						
$I_{COMP\ SOURCE}$	Error amplifier output current sourcing	5	35	55	µA	V_{CPH} = 14V V_{BUS} = 3.5V
$I_{COMP\ SINK}$	Error amplifier output current sinking	-62	-30	-12	µA	V_{CPH} = 14V V_{BUS} = 4.5V
V_{COMPOH}	Error amplifier output voltage swing (high state)	10.5	13.5	14.5	V	V_{BUS} = 3.0V
V_{COMPOL}	Error amplifier output voltage swing (low state)	—	0.25	4	V	V_{BUS} = 5.0V
PFC DC Bus Regulation						
V_{BUSOV}	Overvoltage comparator threshold	3.8	4.3	4.7	V	V_{COMP} = 4.0V
$V_{BUSOV\ HYS}$	Overvoltage comparator hysterisis	150	300	400	mV	V_{COMP} = 4V
$V_{VBUS\ REG}$	VBUS internal reference voltage	3.7	4.0	4.2	V	V_{COMP} = 4V
PFC Zero Current Detector						
V_{ZX}	ZX pin comparator threshold voltage	1.1	1.65	2	V	V_{COMP} = 4V
V_{ZXhys}	ZX pin comparator hysterisis	75	300	800	mV	V_{COMP} = 4V
$V_{ZXclamp}$	ZX pin clamp voltage (high state)	6.3	7.5	9.1	V	I_{ZX} = 5mA
PFC Watch-dog						
t_{WD}	Watch-dog pulse interval	90	400	824	µS	ZX = 0V, $V_{COMP>}$ =2V
Ballast Control Oscillator Characteristics						
fosc	Oscillator frequency	39	42	50	kHz	Run mode
		73	78	84		Preheat mode
d	Oscillator duty cycle	—	50	—	%	
V_{CT+}	Upper C_T ramp voltage threshold	6.8	8.4	10.7	V	V_{CC} = 14V
V_{CT-}	Lower C_T ramp voltage threshold	1.8	4.6	5.6	V	V_{CC} = 14V
V_{CTFLT}	Fault-mode C_T lead voltage	—	0	—	V	SD > 5.0V or CS >1.3V
t_{DLO}	LO output deadtime	0.7	1.0	1.5	usec	CT = 470pF
t_{DHO}	HO output deadtime	0.7	1.0	1.5	usec	CT = 470pF
Ballast Control Preheat Characteristics						
I_{CPH}	CPH pin charging current	2.6	3.2	4.6	µA	V_{CPH}=5V,CT=0V, V_{BUS}=0V
V_{CPHFLT}	Fault-mode CPH pin voltage	—	0	—	mV	SD > 5.0V or CS >1.3V
RPH Characteristics						
I_{RPHLK}	Open circuit RPH pin leakage current	—	0.1	—	µA	
V_{RPHFLT}	Fault-mode RPH pin voltage	—	0	—	mV	SD > 5.0V or CS >1.3V

Electrical Characteristics cont.

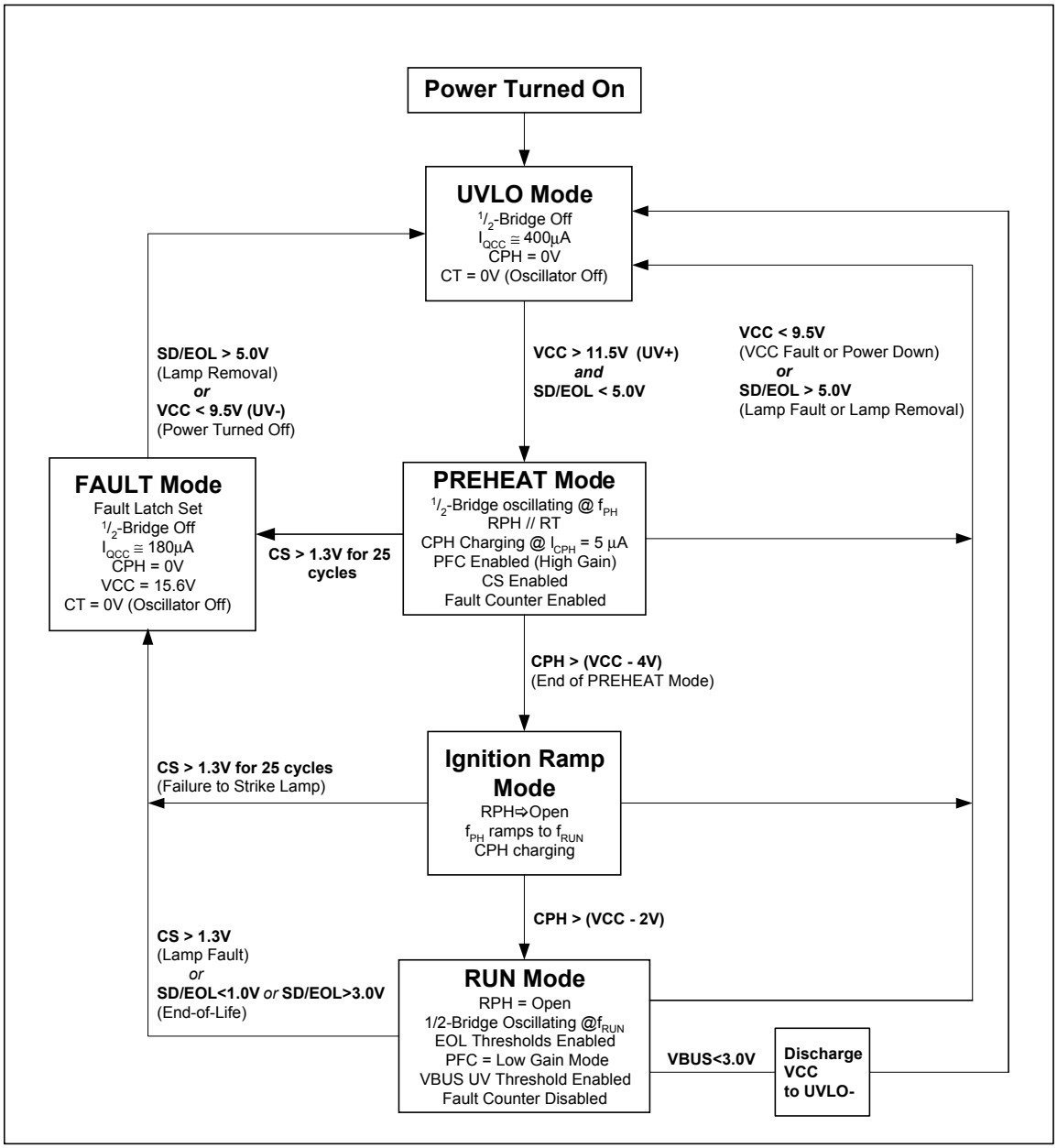
V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, V_{BUS} = Open, R_T = 39.0kΩ, R_{PH} = 100kΩ, C_T = 470 pF, V_{CPH} = 0.0V, V_{SD} = 0.0V, V_{COMP} = 0.0V V_{CS} = 0.0V, C_{LO} = C_{HO} = 1000pF, T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
RT Characteristics						
I_{RTLK}	Open circuit RT pin leakage current	—	0.1	—	µA	CT = 10V
V_{RTFLT}	Fault-mode RT pin voltage	—	0	—	mV	SD > 5.0V or CS >1.3V
Protection Circuitry Characteristics						
V_{SDTH+}	Rising shutdown pin reset threshold voltage	4.5	5.2	5.6	V	
V_{SDHYS}	Shutdown pin 5.0V threshold hysteresis	100	150	350	mV	
V_{SDEOL+}	Rising shutdown pin end-of-life threshold volt.	2.4	3.0	3.6	V	V_{CPH}>12V
V_{SDEOL-}	Falling shutdown pin end-of-life threshold volt.	0.7	1.0	1.6		
V_{CSTH+}	Over-current sense threshold voltage	0.91	1.2	1.3		V_{CPH}>7.5V
#FAULT-	Number of sequential over-current fault cycles before IC shuts down	25	75	90	Cycles	V_{CPH}>7.5V, CYCLES CS > 1.3V
V_{BUSUV-}	The VBUS threshold below which the IC shuts down	2.6	3.0	3.3	V	
V_{CPH}	CPH pin end-of-life enable threshold	10.3	12	13.2		
Gate Driver Output Characteristics (HO, LO and PFC pins)						
VOL	Low-level output voltage	—	0	100	mV	Io = 0
VOH	High-level output voltage	—	0	100		V_{BIAS} - Vo, Io = 0
tr	Turn-on rise time	—	110	210	nsec	C_{HO} = C_{LO} = C_{PFC} = 1nF
tf	Turn-off fall time	—	55	160		
I0+	HO, LO, PFC source current	—	300	—	mA	
I0-	HO, LO, PFC sink current	—	400	—		

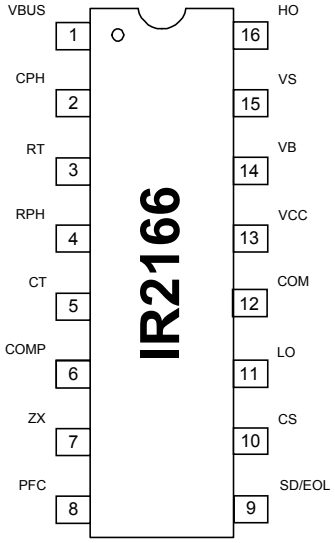
Block Diagram



State Diagram

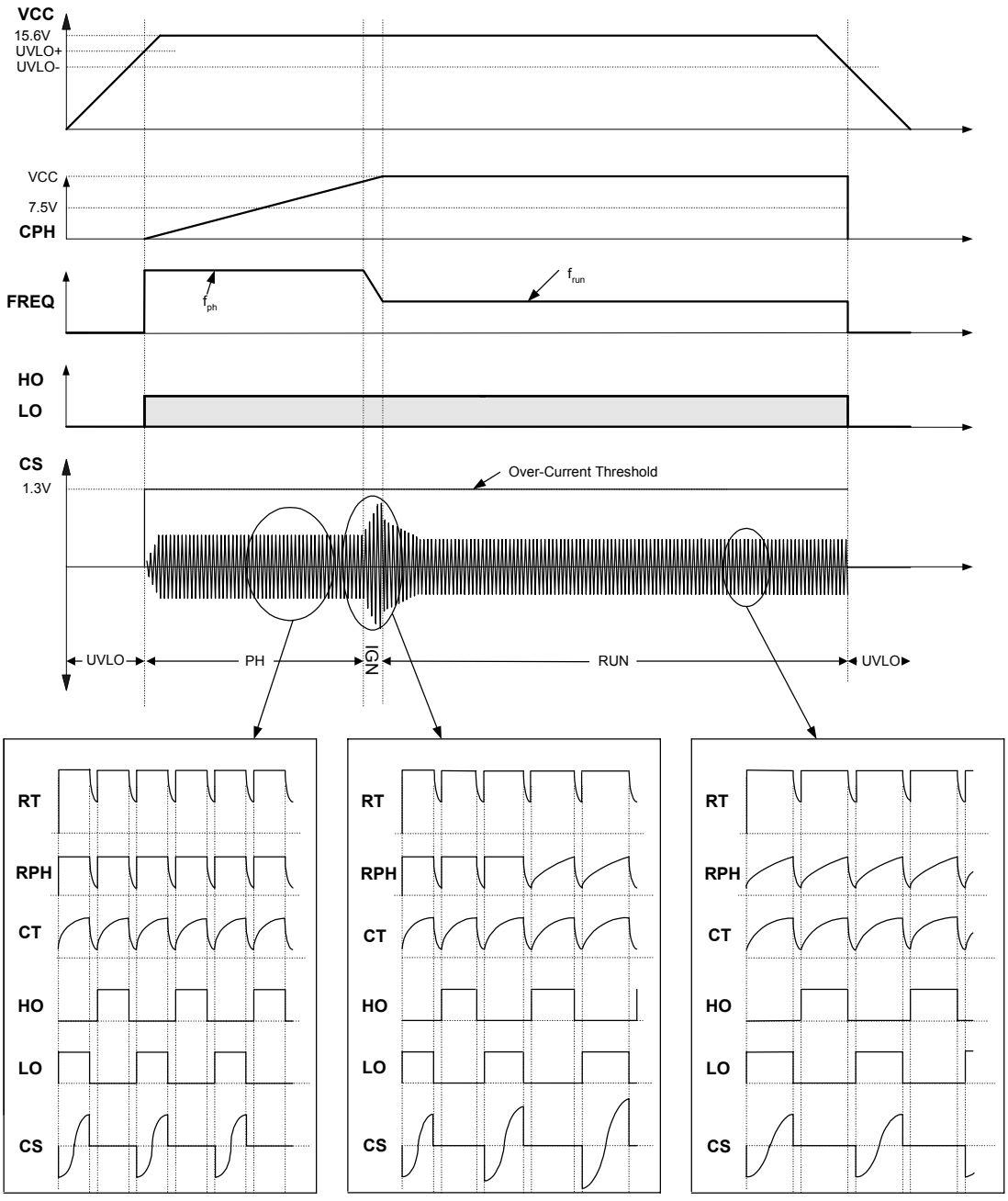


Lead Assignments & Definitions



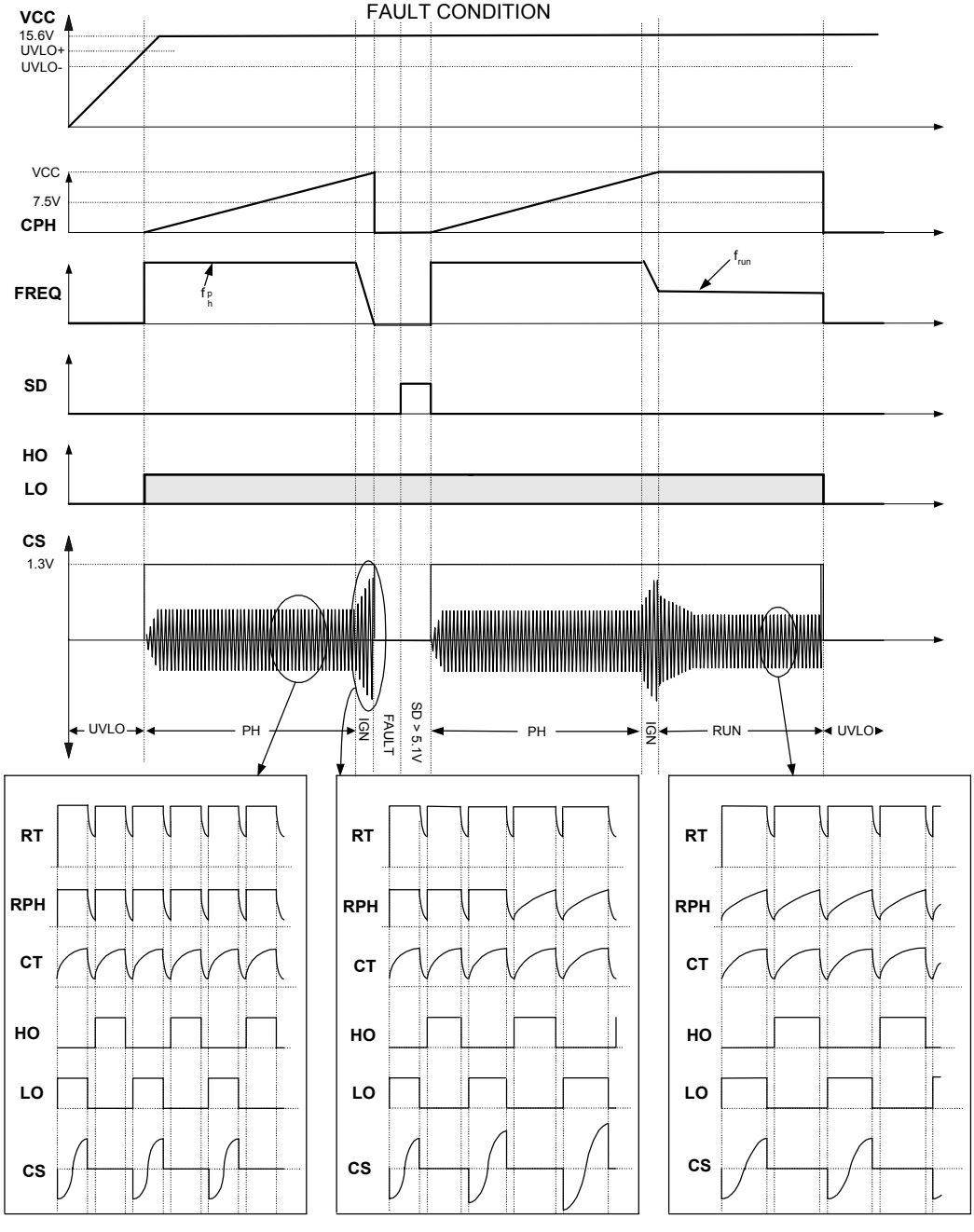
Pin #	Symbol	Description
1	VBUS	DC Bus Sensing Input
2	CPH	Preheat Timing Capacitor
3	RT	Minimum Frequency Timing Resistor
4	RPH	Preheat Frequency Timing Resistor
5	CT	Oscillator Timing Capacitor
6	COMP	PFC Error Amplifier Compensation
7	ZX	PFC Zero-Crossing Detection
8	PFC	PFC Gate Driver Output
9	SD/EOL	Shut-Down/End of Life Sensing Circuit
10	CS	Current Sensing Input
11	LO	Low-Side Gate Driver Output
12	COM	IC Power & Signal Ground
13	VCC	Logic & Low-Side Gate Driver Supply
14	VB	High-Side Gate Driver Floating Supply
15	VS	High Voltage Floating Return
16	HO	High-Side Gate Driver Output

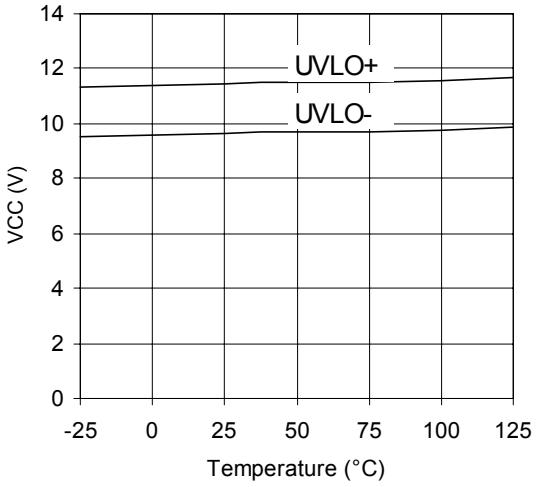
BALLAST TIMING DIAGRAMS
NORMAL OPERATION



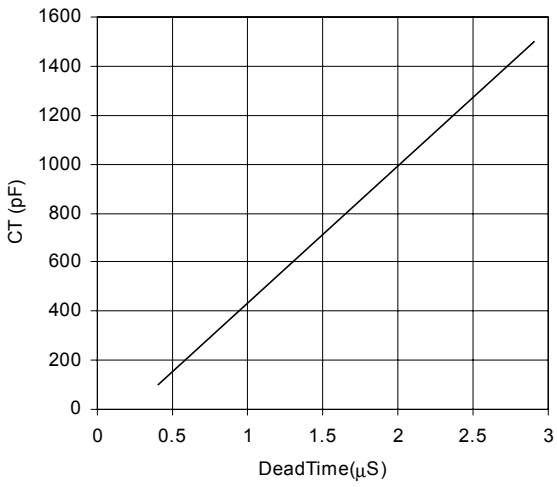
BALLAST TIMING
DIAGRAMS

FAULT CONDITION

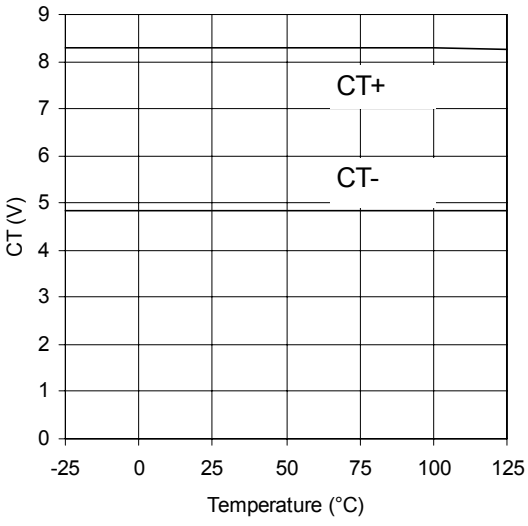




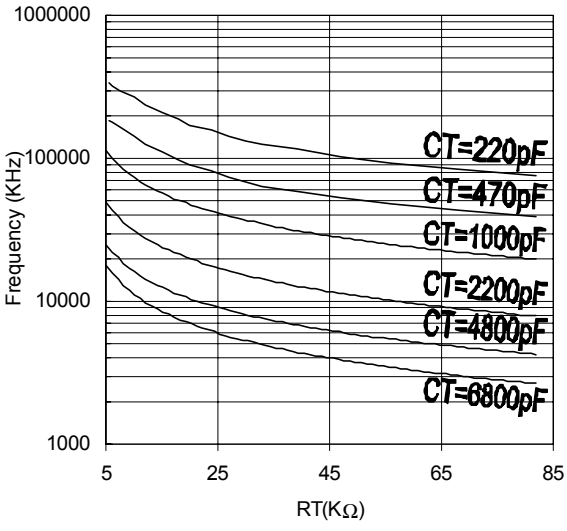
Graph 1. VCCUV+, VCCUV- vs TEMP



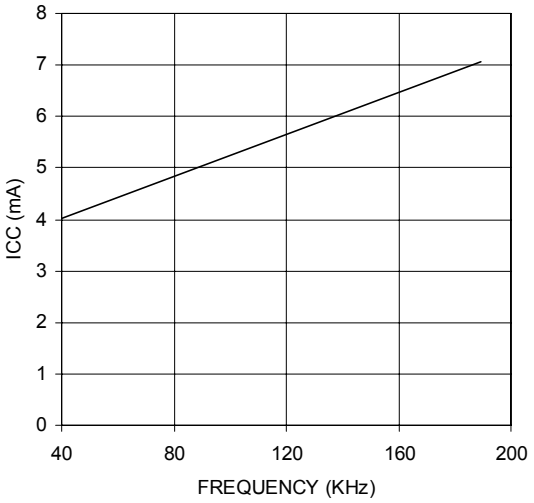
Graph 2. CT vs Dead Time



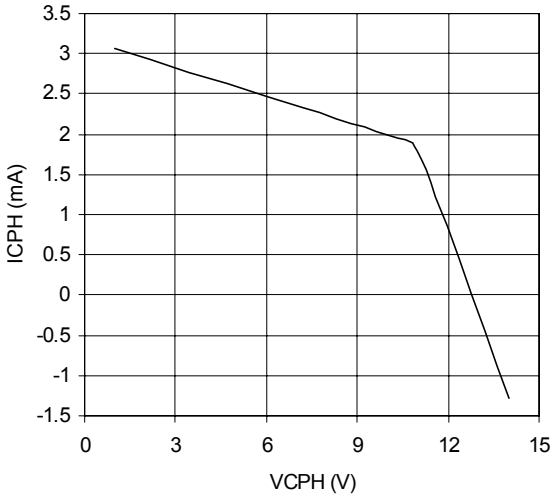
Graph 3: CT+, CT- vs TEMP



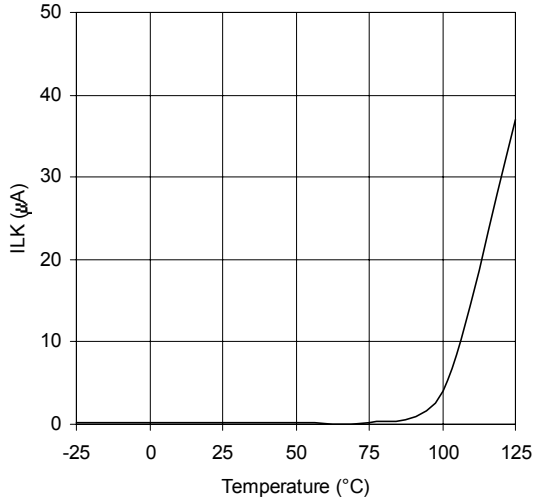
Graph 4: Frequency vs RT



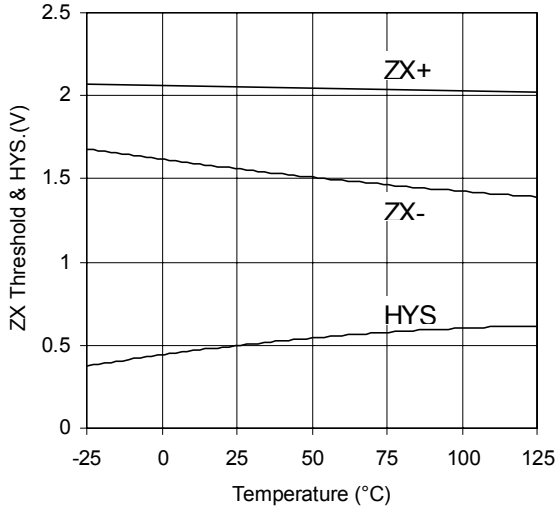
Graph 5: ICC vs Frequency



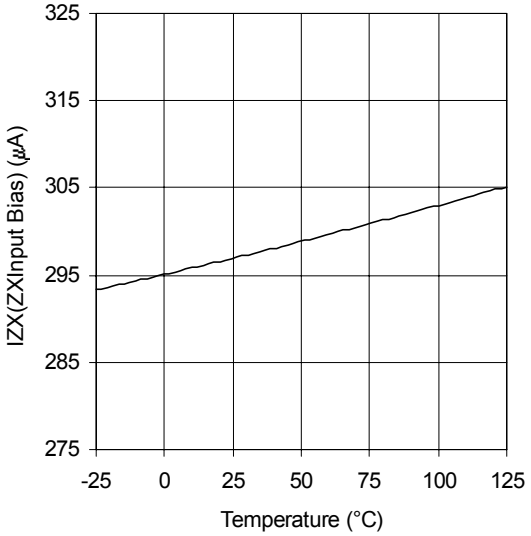
Graph 6: ICPH vs VCPH



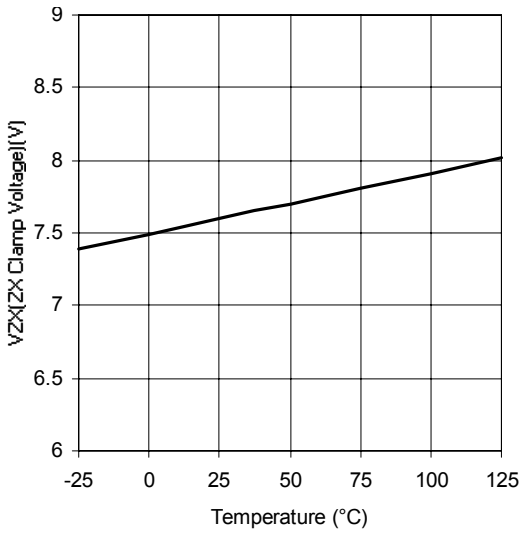
Graph 7. ILK vs TEMP



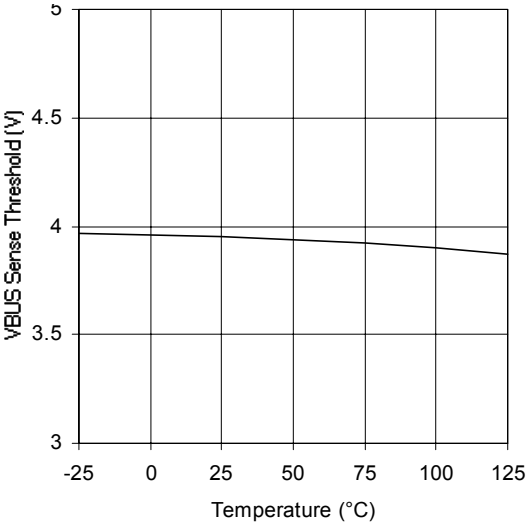
Graph 8: ZX+, ZX- vs TEMP



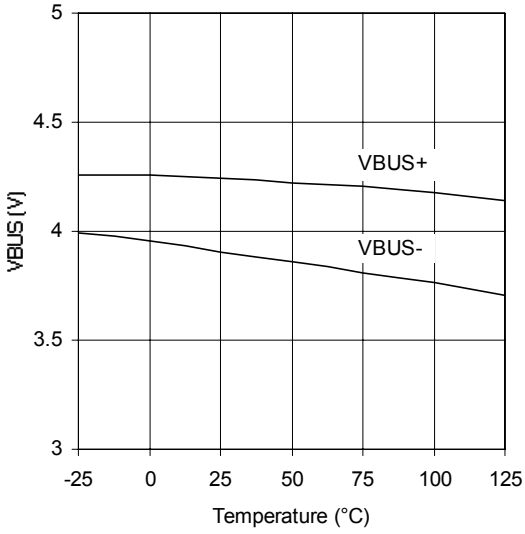
Graph 9: IZX (ZX Input Bias) vs TEMP



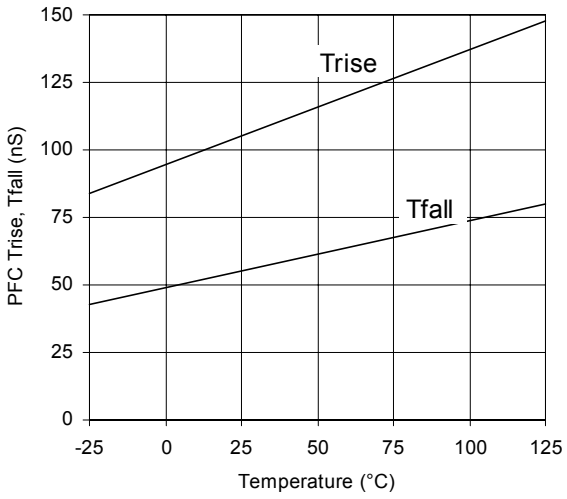
Graph 10: VZX (ZX Clamp Voltage) vs TEMP



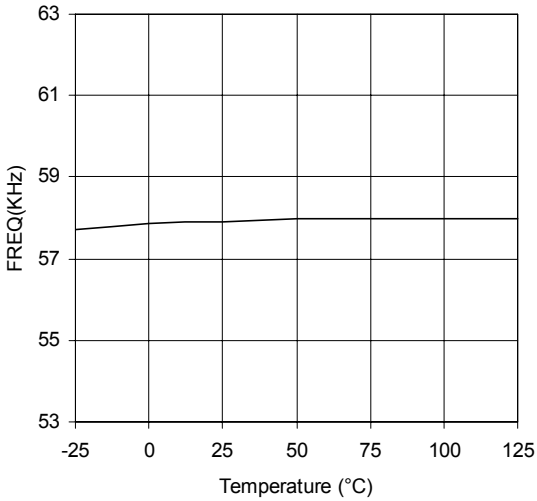
Graph 11: VBUS Sense Thresh vs TEMP



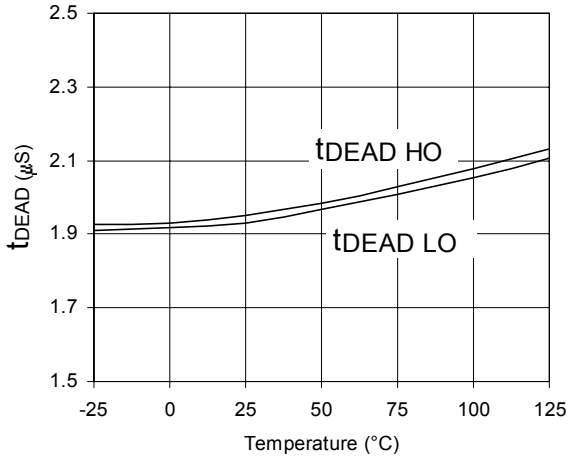
Graph 12: VBUS+, VBUS- vs TEMP



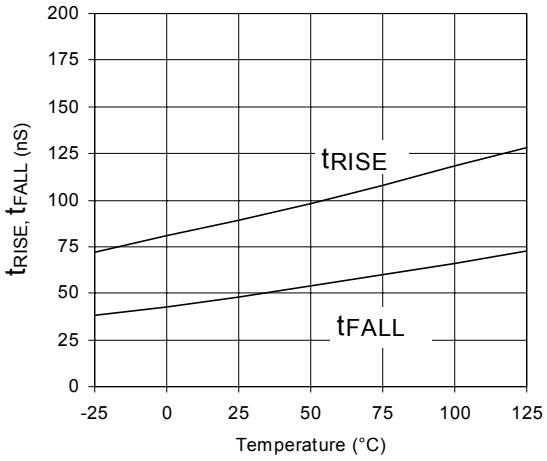
Graph 13: PFC Trise, Tfall vs TEMP



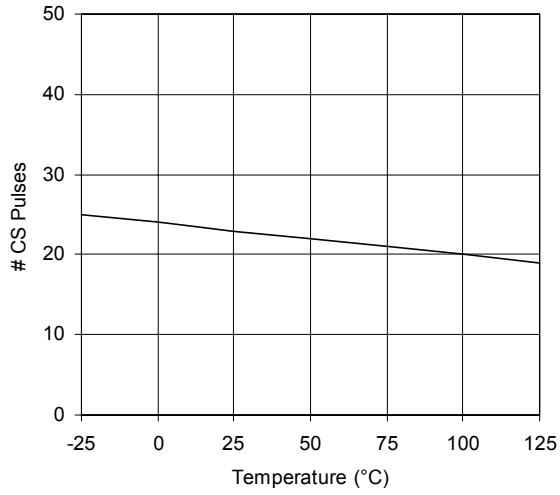
Graph 14: Frequency vs TEMP



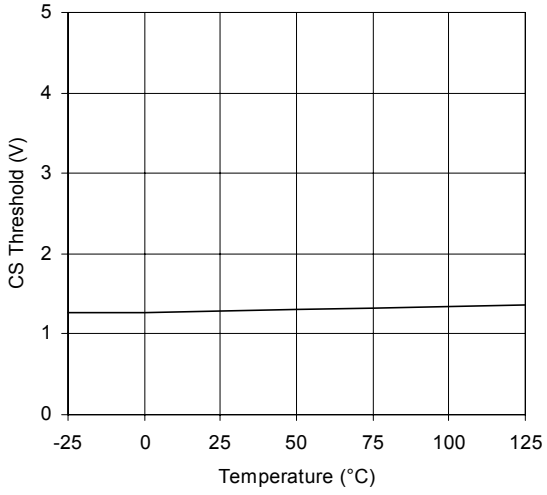
Graph 15: $t_{DEAD\ HO}$, $t_{DEAD\ LO}$ vs TEMP



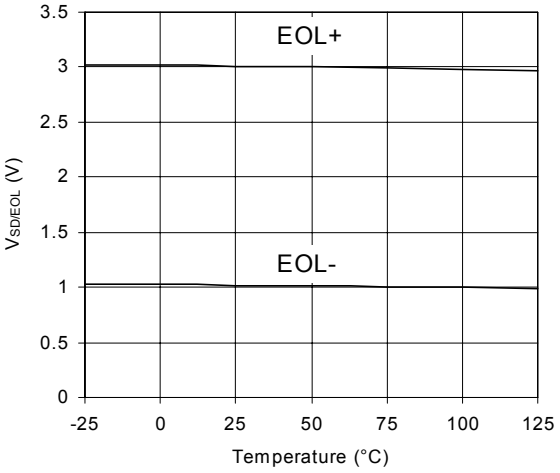
Graph 16: t_{RISE}, t_{FALL} vs TEMP



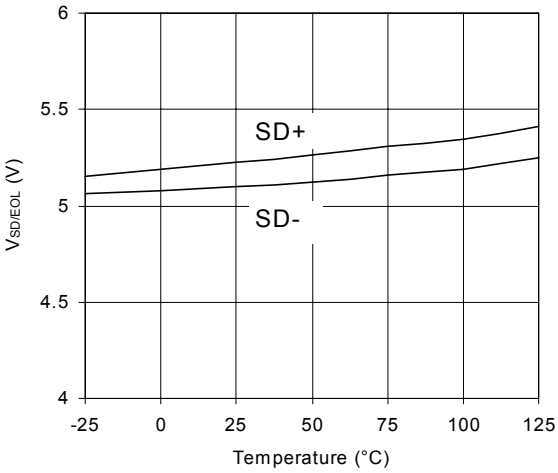
Graph 17: CS Pulses vs TEMP



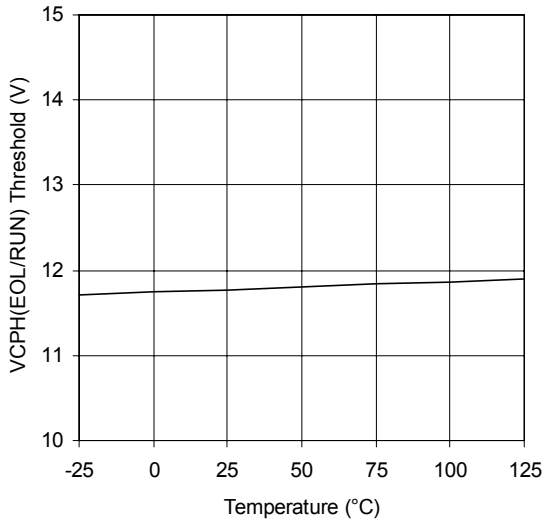
Graph 18: CS Threshold vs TEMP



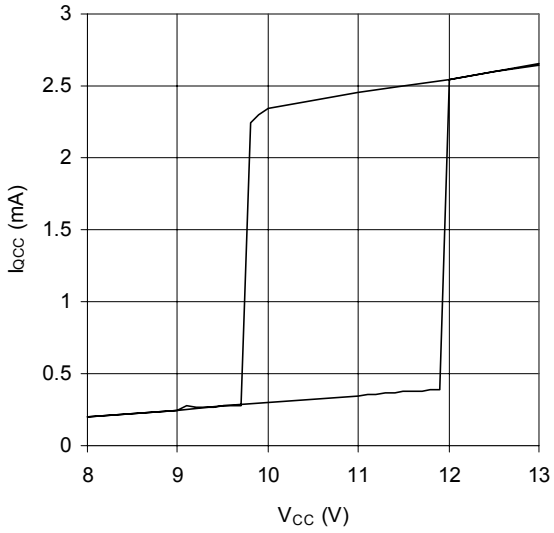
Graph 19: EOL+,EOL- vs TEMP



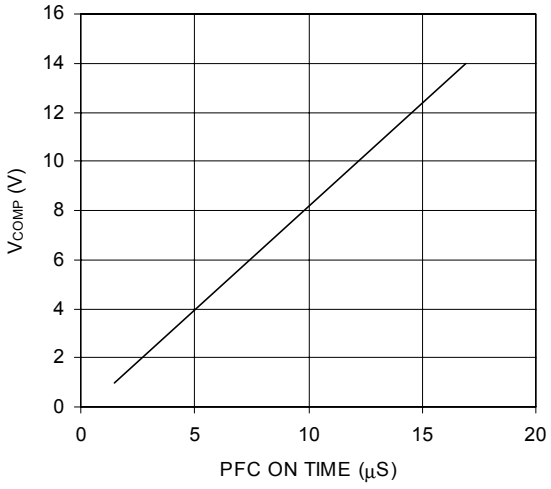
Graph 20: SD+, SD- vs TEMP



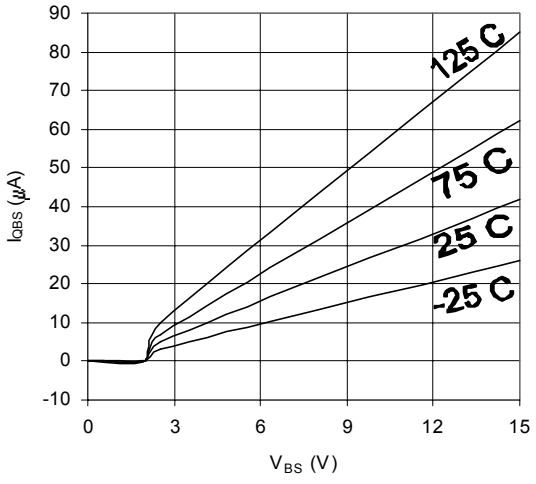
Graph 21: VCPH (EOL/RUN) Threshold vs TEMP



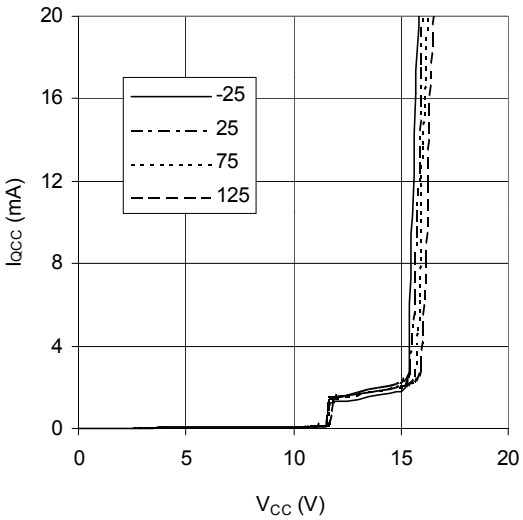
Graph 22: I_{QCC} vs V_{CC} UVLO Hysteresis



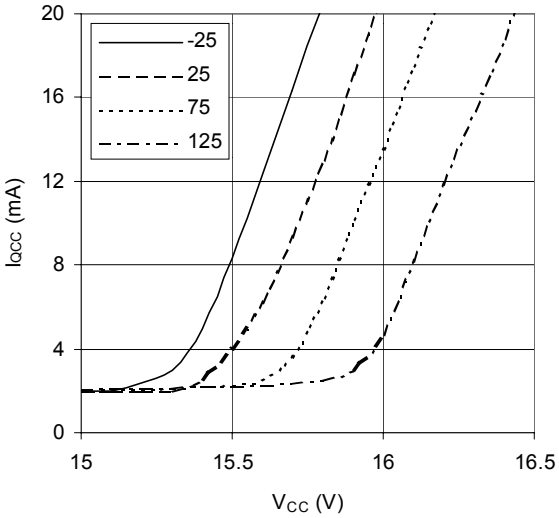
Graph 23: VCOMP vs PFC ON TIME



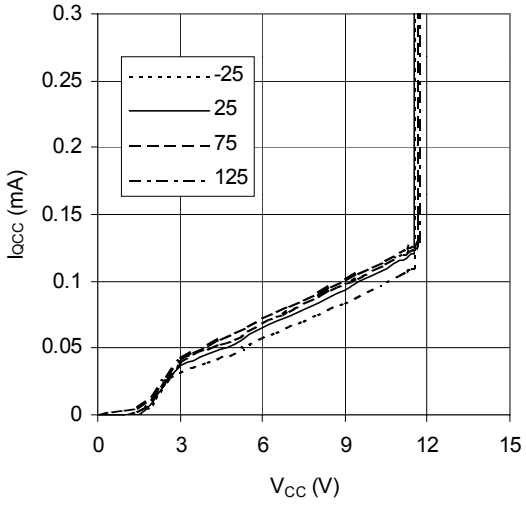
Graph 24: $I_{QBS}(1)$ vs V_{CC} vs Temp



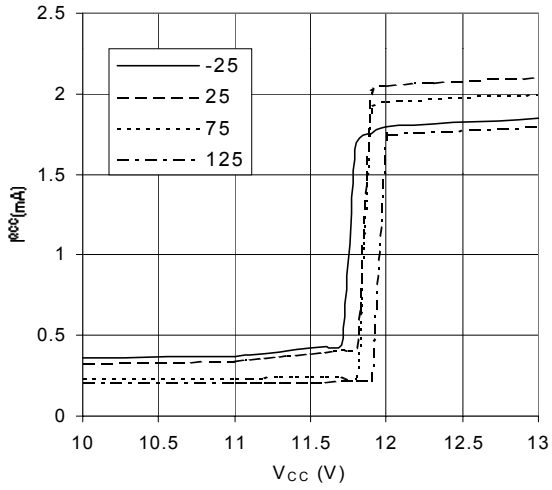
Graph 25. I_{QCC} vs V_{CC} vs Temp



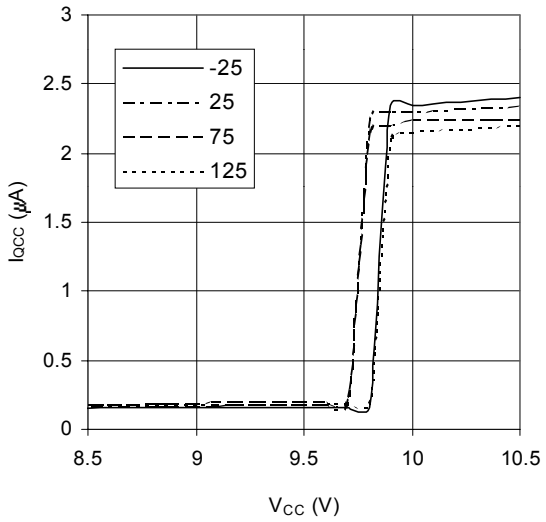
Graph 26. I_{QCC} vs V_{CC} vs Temp
Internal Zener Diode Curve



Graph 27. I_{QCC} vs V_{CC} vs Temp
Micropower Startup Mode



Graph 28: I_{QCC} vs V_{CC} vs Temp V_{CCUV+}



Graph 29: I_{QCC} vs V_{CC} vs Temp V_{CCUV-}

I. Ballast Section
Functional Description

Under-voltage Lock-Out Mode (UVLO)

The under-voltage lock-out mode (UVLO) is defined as the state the IC is in when VCC is below the turn-on threshold of the IC. To identify the different modes of the IC, refer to the State Diagram shown on page 7 of this document. The IR2166 undervoltage lock-out is designed to maintain an ultra low supply current of less than 400uA, and to guarantee the IC is fully functional before the high and low side output drivers are activated. Figure 1 shows an efficient supply voltage using the start-up current of the IR2166 together with a charge pump from the ballast output stage (R_{SUPPLY}, C_{VCC}, D_{CP1} and D_{CP2}).

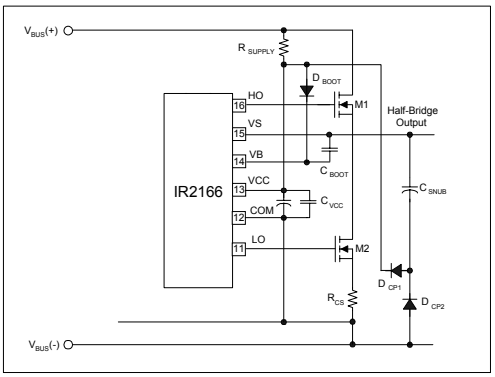


Figure 1, Start-up and supply circuitry.

The start-up capacitor (CVCC) is charged by current through supply resistor (RSUPPLY) minus the start-up current drawn by the IC. This resistor is chosen to set the line input voltage turn-on threshold for the ballast . Once the capacitor voltage on VCC reaches the start-up threshold, and the SD pin is below 5.0 volts, the IC turns on and HO and LO begin to oscillate. The capacitor begins to discharge due to the increase in IC operating current (Figure 2).

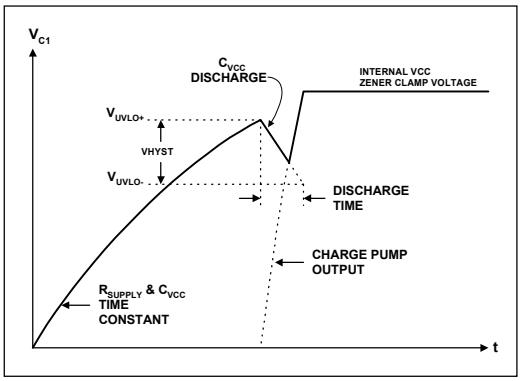


Figure 2, Supply capacitor (C_{VCC}) voltage.

During the discharge cycle, the rectified current from the charge pump charges the capacitor above the IC turnoff threshold. The charge pump and the internal 15.6V zener clamp of the IC take over as the supply voltage. The start-up capacitor and snubber capacitor must be selected such that enough supply current is available over all ballast operating conditions. A bootstrap diode (DBOOT) and supply capacitor (CBOOT) comprise the supply voltage for the high side driver circuitry. To guarantee that the high-side supply is charged up before the first pulse on pin HO, the first pulse from the output drivers comes from the LO pin. During under-voltage lockout mode, the high- and low-side driver outputs HO and LO are both low, pin CT is connected internally to COM to disable the oscillator, and pin CPH is connected internally to COM for resetting the preheat time.

Preheat Mode (PH)

The preheat mode is defined as the state the IC is in when the lamp filaments are being heated to their correct emission temperature. This is necessary for maximizing lamp life and reducing the required ignition voltage. The IR2166 enters preheat mode when VCC exceeds the UVLO positive-going threshold. HO and LO begin to

oscillate at the preheat frequency with 50% duty cycle and with a dead-time which is set by the value of the external timing capacitor, CT, and internal deadtime resistor, RDT. Pin CPH is disconnected from COM and an internal 3μA current source (Figure 3)

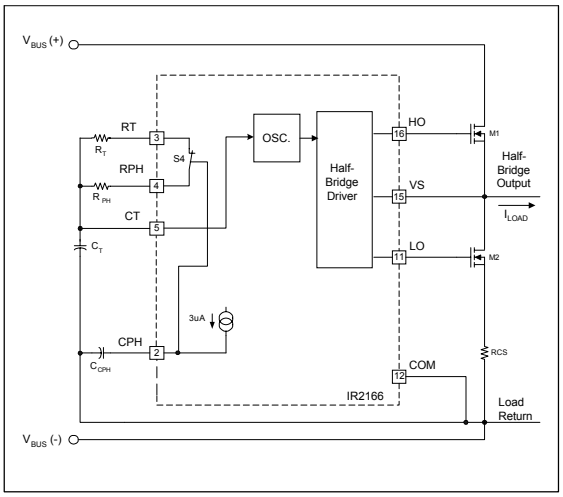


Figure 3, Preheat circuitry.

charges the external preheat timing capacitor on CPH linearly. The over-current protection on pin CS is disabled during preheat. The preheat frequency is determined by the parallel combination of resistors RT and RPH, together with timing capacitor CT. CT charges and discharges between 1/3 and 3/5 of VCC (see Timing Diagram, page 9). CT is charged exponentially through the parallel combination of RT and RPH connected internally to VCC through MOSFET S1. The charge time of CT from 1/3 to 3/5 VCC is the on-time of the respective output gate driver, HO or LO. Once CT exceeds 3/5 VCC, MOSFET S1 is turned off, disconnecting RT and RPH from VCC. CT is then discharged exponentially through an internal resistor, RDT, through MOSFET S3 to COM. The discharge time of CT from 3/5 to 1/3 VCC is the dead-time (both off) of the output gate drivers, HO and LO. The selected value of CT together with RDT therefore program the desired dead-time (see Design Equations, page 26, Equations 1 and 2). Once CT discharges below 1/3 VCC, MOSFET S3 is turned off, disconnecting RDT from COM, and MOSFET S1 is turned on, connecting RT and RPH again to VCC. The frequency remains at the preheat frequency until the voltage on pin CPH exceeds 10V and the IC enters Ignition Mode. During the preheat mode, the over-current protection together with the fault counter are enabled. The peak ignition current must not exceed the maximum allowable current ratings of the output stage MOSFETs. Should this voltage exceed the internal threshold of 1.3V, the internal FAULT Counter begins counting the sequential over-current faults (See Timing Diagram). If the number of over-current faults exceed 25, the IC will enter FAULT mode and gate driver outputs HO, LO and PFC will be latched low.

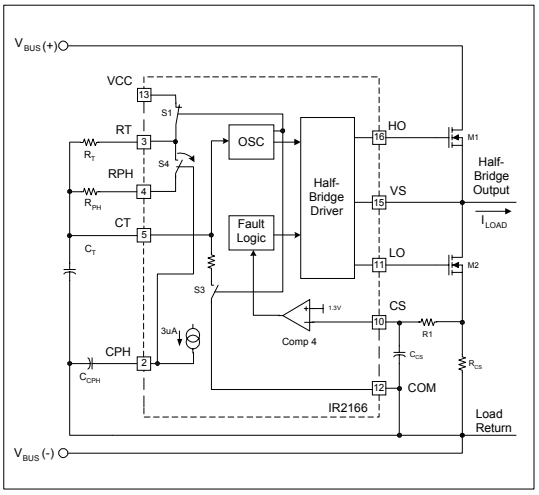


Figure 4, Ignition circuitry.

Ignition Mode (IGN)

The ignition mode is defined as the state the IC is in when a high voltage is being established across the lamp necessary for igniting the lamp. The IR2166 enters ignition mode when the voltage on pin CPH exceeds 10V.

Pin CPH is connected internally to the gate of a P-channel MOSFET (S4) (see Figure 4) that connects pin RPH with pin RT. As pin CPH exceeds 10V, the gate-to-source voltage of MOSFET S4 begins to fall below the turn-on threshold of S4. As pin CPH continues to ramp towards VCC, switch S4 turns off slowly. This results in resistor RPH being disconnected smoothly from resistor RT, which causes the operating frequency to ramp smoothly from the preheat frequency, through the ignition frequency, to the final run frequency. The over-current threshold on pin CS will protect the ballast against a non-strike or open-filament lamp fault condition. The voltage on pin CS is defined by the lower half-bridge MOSFET current flowing through the external current sensing resistor RCS. The resistor RCS therefore programs the maximum allowable peak ignition current (and therefore peak ignition voltage) of the ballast output stage. If the number of over current pulses exceed 25, the IC will enter fault mode and gate driver outputs HO, LO and PFC will be latched low.

Run Mode (RUN)

Once the lamp has successfully ignited, the ballast enters run mode. The run mode is defined as the state the IC is in when the lamp arc is established and the lamp is being driven to a given power level. The run mode oscillating frequency is determined by the timing resistor RT and timing capacitor CT (see Design Equations, page 26, Equations 3 and 4). Should hard-switching occur at the half-bridge at any time due to an open-filament or lamp removal, the voltage across the current sensing resistor, RCS, will exceed the internal threshold of 1.3 volts and the IC will enter FAULT mode and gate driver outputs HO, LO and PFC will be latched low.

DC Bus Under-voltage Reset

Should the DC bus decrease too low during a brownout line condition or overload condition, the resonant output stage to the lamp can shift near or below resonance. This can produce hard-switching at the half-bridge which can damage the half-bridge switches or, the DC bus can decrease too far and the lamp can extinguish. To protect against this, the VBUS pin includes a 3.0V under-voltage threshold. Should the voltage at the VBUS pin decrease below 3.0V, VCC will be discharged to the UVLO- threshold and all gate driver outputs will be latched low.

For proper ballast design, the designer should design the PFC section such that the DC bus does not drop until the AC line input voltage falls below the rated input voltage of the ballast (See PFC section). When correctly designed, the voltage measured at the VBUS pin will decrease below the internal 3.0V threshold and the ballast will turn off cleanly. The pull-up resistor to VCC (R_{SUPPLY}) will then turn the ballast on again with the AC input line voltage increasing to the minimum specified value causing VCC to exceed UVLO+.

R_{SUPPLY} should be set to turn the ballast on at the minimum specified ballast input voltage. The PFC should then be designed such that the DC bus decreases at an input line voltage that is

lower than the minimum specified ballast input voltage. This hysteresis will result in clean turn-on and turnoff of the ballast.

CS and EOL Fault Mode (FAULT)

Should the voltage at the SD/EOL pin exceed 3V or decrease below 1V during RUN mode, the IC enters fault mode and all gate driver outputs, HO, LO and PFC, are latched off in the 'low' state. CPH is discharged to COM for resetting the preheat time, and CT is discharged to COM for disabling the oscillator. To exit fault mode, VCC must be recycled back below the UVLO negative-going turn-off threshold, or, the shutdown pin, SD, must be pulled above 5.2 volts. Either of these will force the IC to enter UVLO mode (see State Diagram, page 7). Once VCC is above the turn-on threshold and SD is below 5.0 volts, the IC will begin oscillating again in the preheat mode. The current sense function will force the IC to enter FAULT mode only after the voltage at the current sense pin has been pulsed about 25 times with a voltage greater than 1.3 volts during preheat and ignition modes only. These over-currents must occur during the on-time of LO. During run mode, a single pulse on the CS pin above 1.3V will force the IC to enter FAULT mode.

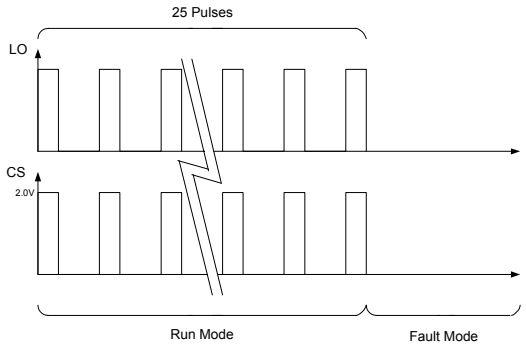


Figure 5: FAULT counter during preheat and ignition

II. PFC Section Functional Description

In most electronic ballasts it is necessary to have the circuit act as a pure resistive load to the AC input line voltage. The degree to which the circuit matches a pure resistor is measured by the phase shift between the input voltage and input current and how well the shape of the input current waveform matches the shape of the sinusoidal input voltage. The cosine of the phase angle between the input voltage and input current is defined as the power factor (PF), and how well the shape of the input current waveform matches the shape of the input voltage is determined by the total harmonic distortion (THD). A power factor of 1.0 (maximum) corresponds to zero phase shift and a THD of 0% represents a pure sinewave (no distortion). For this reason it is desirable to have a high PF and a low THD. To achieve this, the IR2166 includes an active power factor correction (PFC) circuit which, for an AC line input voltage, produces an AC line input current. The control method implemented in the IR2166 is for a boost-type converter (Figure 6) running in critical-conduction mode (CCM). This means that during each switching cycle of the PFC MOSFET, the circuit waits until the inductor current discharges to zero before turning the PFC MOSFET on again. The PFC MOSFET is turned on and off at a much higher frequency (>10KHz) than the line input frequency (50 to 60Hz).

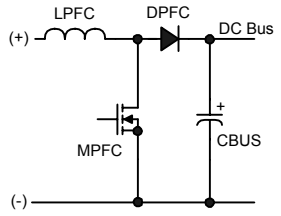


Figure 6: Boost-type PFC circuit

When the switch MPFC is turned on, the inductor LPFC is connected between the rectified line input (+) and (-) causing the current in LPFC to charge up linearly. When MPFC is turned off, LPFC is connected between the rectified line input (+) and the DC bus capacitor CBUS (through diode DPFC) and the stored current in LPFC flows into CBUS. As MPFC is turned on and off at a high-frequency, the voltage on CBUS charges up to a specified voltage. The feedback loop of the IR2166 regulates this voltage to a fixed value by continuously monitoring the DC voltage and adjusting the on-time of MPFC accordingly. For an increasing DC bus the on-time is decreased, and for a decreasing DC bus the on-time is increased. This negative feedback control is performed with a slow loop speed and a low loop gain such that the average inductor current smoothly follows the low-frequency line input voltage for high power factor and low THD. The on-time of MPFC therefore appears to be fixed (with an additional modulation to be discussed later) over several cycles of the line voltage. With a fixed on-time, and an off-time determined by the inductor current discharging to zero, the result is a system where the switching frequency is free-running and constantly changing from a high frequency near the zero crossing of the AC input line voltage, to a lower frequency at the peaks (Figure 7).

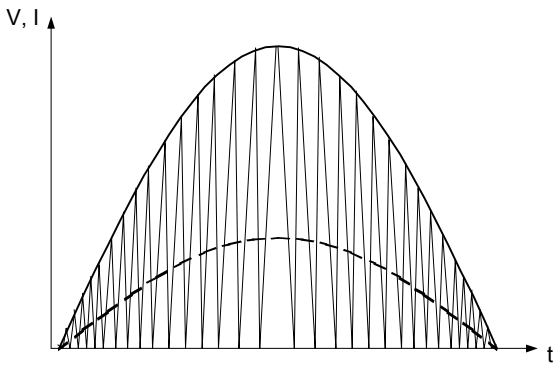


Figure 7: Sinusoidal line input voltage (solid line), triangular PFC Inductor current and smoothed sinusoidal line input current (dashed line) over one half-cycle of the line input voltage.

When the line input voltage is low (near the zero crossing), the inductor current will charge up to a small amount and the discharge time will be fast resulting in a high switching frequency. When the input line voltage is high (near the peak), the inductor current will charge up to a higher amount and the discharge time will be longer giving a lower switching frequency. The triangular PFC inductor current is then smoothed by the EMI filter to produce a sinusoidal line input current.

The PFC control circuit of the IR2166 (Figure 8) only requires four control pins: VBUS, COMP, ZX and PFC. The VBUS pin is for sensing the DC bus voltage (via an external resistor voltage divider), the COMP pin programs the on-time of MPFC and the speed of the feedback loop, the ZX pin detects when the inductor current discharges to zero (via a secondary winding from the PFC inductor), and the PFC pin is the low-side gate driver output for MPFC.

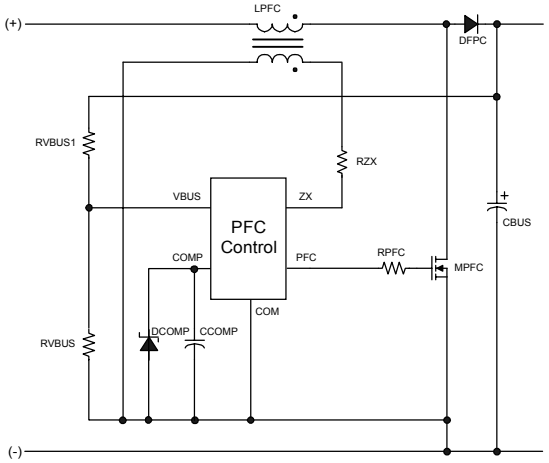


Figure 8:IR2166 simplified PFC control circuit

The VBUS pin is regulated against a fixed internal 4V reference voltage for regulating the DC bus voltage (Figure 9). The feedback loop is performed by an operational transconductance amplifier (OTA) that sinks or sources a current to the external capacitor at the COMP pin. The resulting voltage on the COMP pin sets the threshold for the charging of the internal timing capacitor (C1) and therefore programs the on-time of MPFC. During preheat and ignition modes of the ballast section, the gain of the OTA is set to a high level to raise the DC bus level quickly. When the voltage on the VBUS pin exceeds 3V, the gain is set to a low level to reduce overshoot. When the voltage on the VBUS pin exceeds 4V, the gain is set to a high level again to minimize the transient on the DC bus which can occur during ignition. During run mode, the gain is then decreased to a lower level necessary for achieving high power factor and low THD.

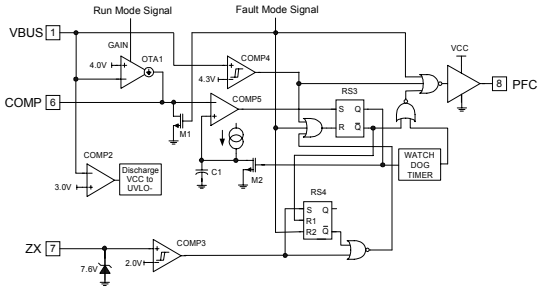


Figure 9: IR2166 detailed PFC control circuit

The off-time of MPFC is determined by the time it takes the LPFC current to discharge to zero. This zero current level is detected by a secondary winding on LPFC which is connected to the ZX pin. A positive-going edge exceeding the internal 2V threshold signals the beginning of the off-time. A negative-going edge on the ZX pin falling below 1.7V will occur when the LPFC current discharges to zero which signals the end of the off-time and MPFC is turned on again (Figure 10). The cycle repeats itself indefinitely until the PFC section is disabled due to a fault detected by the ballast section (Fault Mode), an over-voltage or under-voltage condition on the DC bus, or, the negative transition of ZX pin voltage does not occur. Should the negative edge on the ZX pin not occur, MPFC will remain off until the watch-dog timer forces a turn-on of MPFC for an on-time duration programmed by the voltage on the COMP pin. The watch-dog pulses occur every 400µs indefinitely until a correct positive- and negative-going signal is detected on the ZX pin and normal PFC operation is resumed.

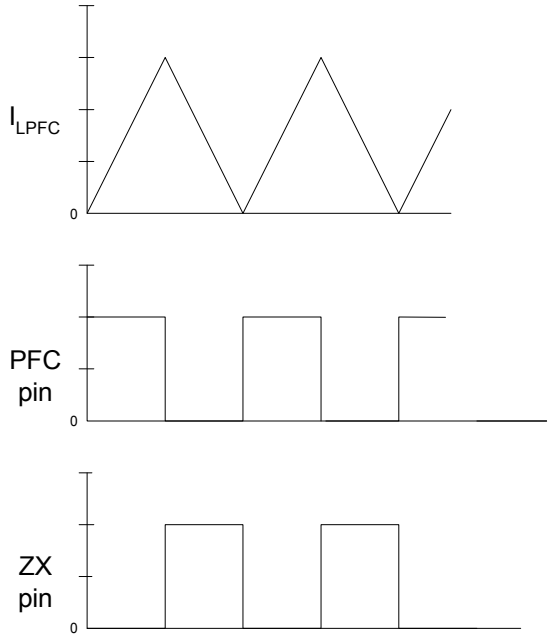


Figure 10: LPFC current, PFC pin and ZX pin timing diagram.

modulation circuit has been added to the PFC control. This circuit dynamically increases the on-time of MPFC as the line input voltage nears the zero-crossings (Figure 11). This causes the peak LPFC current, and therefore the smoothed line input current, to increase slightly higher near the zero-crossings of the line input voltage. This reduces the amount of cross-over distortion in the line input current which reduces the THD and higher harmonics to low levels.

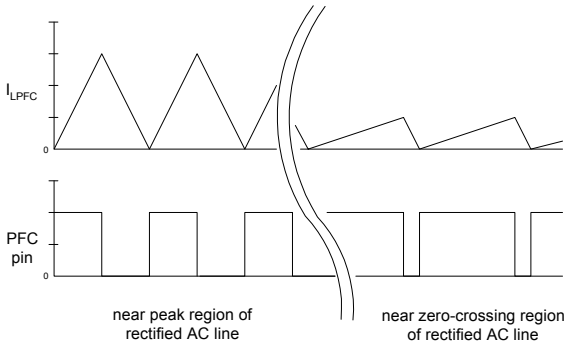


Figure 11: On-time modulation near the zero-crossings.

On-time Modulation

A fixed on-time of MPFC over an entire cycle of the line input voltage produces a peak inductor current which naturally follows the sinusoidal shape of the line input voltage. The smoothed averaged line input current is in phase with the line input voltage for high power factor but the total harmonic distortion (THD), as well as the individual higher harmonics, of the current can still be too high. This is mostly due to cross-over distortion of the line current near the zero-crossings of the line input voltage. To achieve low harmonics which are acceptable to international standard organizations and general market requirements, an additional on-time

Over-voltage Protection (OVP)

Should over-voltage occur on the DC bus causing the VBUS pin to exceed the internal 4.3V threshold, the PFC output is disabled (set to a logic 'low'). When the DC bus decreases again causing the VBUS pin to decrease below the internal 4V threshold, a watch-dog pulse is forced on the PFC pin and normal PFC operation is resumed.

Under-voltage Reset (UVR)

When the line input voltage is decreased, interrupted or a brown-out condition occurs, the PFC feedback loop causes the on-time of MPFC

to increase in order to keep the DC bus constant. Should the on-time increase too far, the resulting peak currents in LPFC can exceed the saturation current limit of LPFC. LPFC will then saturate and very high peak currents and di/dt levels will occur. To prevent this, the maximum on-time is limited by limiting the maximum voltage on the COMP pin with an external zener diode DCOMP (Figure 8). As the line input voltage decreases, the COMP pin voltage and therefore the on-time will eventually limit. The PFC can no longer supply enough current to keep the DC bus fixed for the given load power and the DC bus will begin to drop. Decreasing the line input voltage further will cause the VBUS pin to eventually decrease below the internal 3V threshold (Figure 9). When this occurs, VCC is discharged internally to UVLO-, the IR2166 enters UVLO mode and both the PFC and ballast sections are disabled (see State Diagram). The start-up supply resistor to VCC, together with the micro-power start-up current of the IR2166, determine the line input turn-on voltage. This should be set such that the ballast turns on at a line voltage level above the under-voltage turn-off level. It is the correct selection of the value of the supply resistor to VCC and the zener diode on the COMP pin that correctly program the on and off line input voltage thresholds for the ballast. With these thresholds correctly set, the ballast will turn off due to the 3V under-voltage threshold on the VBUS pin, and on again at a higher line input voltage (hysterisis) due to the supply resistor to VCC. This hysterisis will result in a proper reset of the ballast without flickering of the lamp, bouncing of the DC bus or re-ignition of the lamp when the DC bus is too low.

PFC Over-Current Protection (optional)

In case of fast on/off interruptions of the mains input voltage or during normal lamp ignition, the DC bus voltage level can decrease below the instantaneous rectified line voltage. Should this occur, the PFC inductor current and PFC MOSFET current can increase to high levels causing the PFC inductor to saturate and/or the PFC MOSFET to become damaged. During fast on/off interruptions of the input mains voltage, the DC bus can drop during the time when the mains voltage is interrupted (off). Since VCC is still above UVLO-, the IC will continue to operate and will increase the COMP pin voltage to increase the PFC MOSFET on-time due to the dropping of the DC bus. When the mains voltage returns again quickly, (before VCC reaches UVLO-), the on-time of the PFC MOSFET is too long for the given mains voltage level resulting in high PFC inductor and MOSFET currents that can saturate the inductor and/or damage the PFC MOSFET (Figure 12).

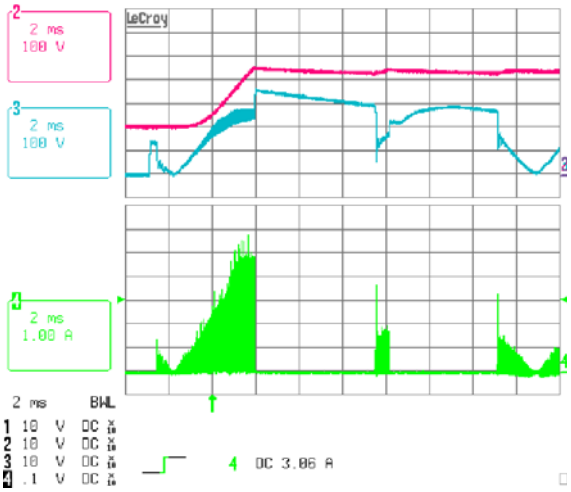
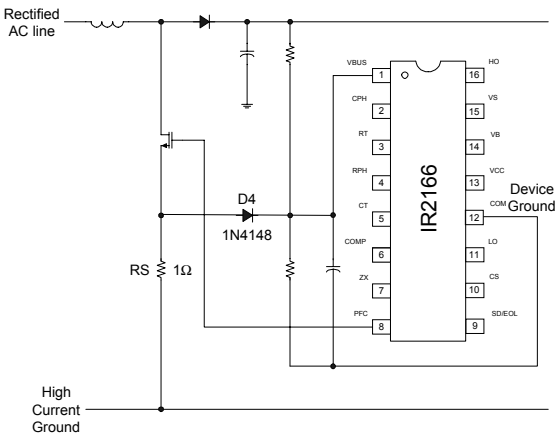


Figure 12, High PFC inductor current during fast mains on/off (upper trace: DC Bus, 100V/div; middle trace: AC line input voltage, 100V/div; lower trace: PFC inductor current 1A/div).

During lamp ignition, the DC bus can drop below the rectified AC line voltage causing current to conduct directly from the output of the rectifier, through the PFC inductor and diode, to the DC bus capacitor. This results in a low-frequency offset of current in the PFC inductor. Since the zero-crossing detection circuit only detects the high-frequency zero-crossing of the inductor current, the PFC MOSFET will turn on again each cycle before the inductor current has reached zero. This causes the PFC to work in a continuous conduction mode and the sum of the low-frequency and high-frequency components of current can saturate the PFC inductor and/or damage the PFC MOSFET.

To protect against these conditions, a current sense resistor (RS) can be inserted between the source on the PFC MOSFET and ground, and a diode (D4) connected from the top of this current-sensing resistor to the VBUS pin (Figure 13).



13, External over-current protection circuit

Should high currents occur, the voltage across the current-sensing resistor (RS) will exceed the 4.3V over-voltage protection threshold at the VBUS pin and the PFC MOSFET will turn off safely limiting the current. The watch-dog timer will then restart the PFC as normal (Figure 14). The current sensing resistor value should be selected such that the over-current protection does not false trip during normal operation over the entire line voltage range and load range. A current-sensing resistor value, for example, of 1.0 W will set the over-current protection threshold to about 5 A peak.

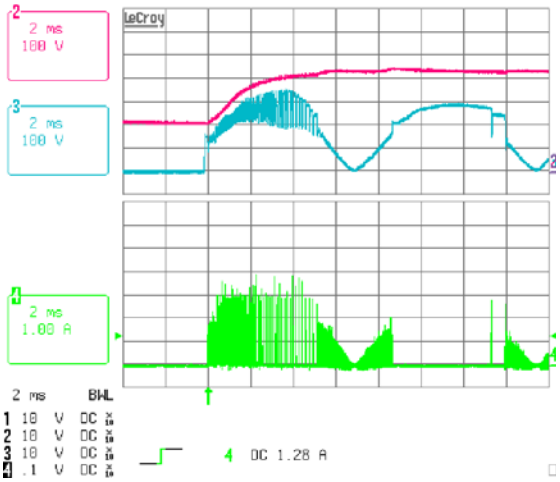


Figure 14, PFC inductor current limited using over-current protection circuit (upper trace: DC Bus, 100V/div; middle trace: AC line input voltage, 100V/div; lower trace: PFC inductor current 1A/div).

The effect that these line and load conditions have on the performance of the ballast depends on the saturation level of the PFC inductor, the selection of the PFC MOSFET, the DC bus capacitor value, the maximum on-time limit set by DZCOMP, and, how fast VCC decreases below UVLO- when the DC bus drops during ignition (the 3V reset on the VBUS pin does not become active until RUN mode). For these reasons, the ballast designer should perform these mains interrupt and ignition tests carefully to determine the robustness of their final design and to decide if this additional over-current protection circuit is necessary.

Ballast Design Equations

Note: The results from the following design equations can differ slightly from experimental measurements due to IC tolerances, component tolerances, and oscillator over- and undershoot due to internal comparator response time.

Step 1: Program Dead-time

The dead-time between the gate driver outputs HO and LO is programmed with timing capacitor CT and an internal dead-time resistor RDT. The dead-time is the discharge time of capacitor CT from 3/5VCC to 1/3VCC and is given as:

$$t_{DT} = C_T \cdot 1475 \quad \text{[Seconds]} \qquad (1)$$

or

$$C_T = \frac{t_{DT}}{1475} \qquad \text{[Farads]} \qquad (2)$$

Step 2: Program Run Frequency

The final run frequency is programmed with timing resistor RT and timing capacitor CT. The charge time of capacitor CT from 1/3VCC to 3/5VCC determines the on-time of HO and LO gate driver outputs. The run frequency is therefore given as:

$$f_{RUN} = \frac{1}{2 \cdot C_T (0.51 \cdot R_T + 1475)} \quad \text{[Hertz]} \ (3)$$

or

$$R_T = \frac{1}{1.02 \cdot C_T \cdot f_{RUN}} - 2892 \quad \text{[Ohms]} \ (4)$$

Step 3: Program Preheat Frequency

The preheat frequency is programmed with timing resistors RT and RPH, and timing capacitor CT. The timing resistors are connected in parallel internally for the duration of the preheat time. The preheat frequency is therefore given as:

$$f_{PH} = \frac{1}{2 \cdot C_T \cdot \left(\frac{0.51 \cdot R_T \cdot R_{PH}}{R_T + R_{PH}} + 1475 \right)} \ \text{[Hertz]} \ (5)$$

or

$$R_{PH} = \frac{\left(\frac{1}{1.02 \cdot C_T \cdot f_{PH}} - 2892 \right) \cdot R_T}{R_T - \left(\frac{1}{1.02 \cdot C_T \cdot f_{PH}} - 2892 \right)} \quad \text{[Ohms]} \ (6)$$

Step 4: Program Preheat Time

The preheat time is defined by the time it takes for the capacitor on pin CPH to charge up to 10 volts. An internal current source of 3uA flows out of pin CPH. The preheat time is therefore given as:

$$t_{PH} = C_{PH} \cdot 3.33e6 \qquad \text{[Seconds]} \ (7)$$

or

$$C_{PH} = t_{PH} \cdot 0.3e-6 \qquad \text{[Farads]} \ (8)$$

Step 5: Program Maximum Ignition Current

The maximum ignition current is programmed with the external resistor RCS and an internal threshold of 1.3 volts. This threshold determines the over-current limit of the ballast, which can be exceeded when the frequency ramps down towards resonance during ignition and the lamp does not ignite. The maximum ignition current is given as:

$$I_{IGN} = \frac{1.3}{R_{CS}} \qquad \text{[Amps Peak] (9)}$$

or

$$R_{CS} = \frac{1.3}{I_{IGN}} \qquad \text{[Ohms] (10)}$$

PFC Design Equations

Step1: Calculate PFC inductor value:

$$L_{PFC} = \frac{(VBUS - \sqrt{2} \cdot VAC_{MIN}) \cdot VAC_{MIN}^{2} \cdot \eta}{2 \cdot f_{MIN} \cdot P_{OUT} \cdot VBUS} \quad \text{[Henries]} \quad (1)$$

where,

$VBUS$ = DC bus voltage
VAC_{MIN} = Minimum rms AC input voltage
η = PFC efficiency (typically 0.95)
f_{MIN} = Minimum PFC switching frequency at minimum AC input voltage
P_{OUT} = Ballast output power

Step 2: Calculate peak PFC inductor current:

$$i_{PK} = \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{VAC_{MIN} \cdot \eta} \quad \text{[Amps Peak]} \quad (2)$$

Note: The PFC inductor must not saturate at i_{PK} over the specified ballast operating temperature range. Proper core sizing and air-gapping should be considered in the inductor design.

Step 3: Calculate maximum on-time:

$$t_{ON\ MAX} = \frac{2 \cdot P_{OUT} \cdot L_{PFC}}{VAC_{MIN}^{2} \cdot \eta} \quad \text{[Seconds]} \quad (3)$$

Step 4: Calculate maximum COMP voltage:

$$V_{COMP\ MAX} = \frac{t_{ON\ MAX}}{0.9E-6} \quad \text{[Volts]} \quad (4)$$

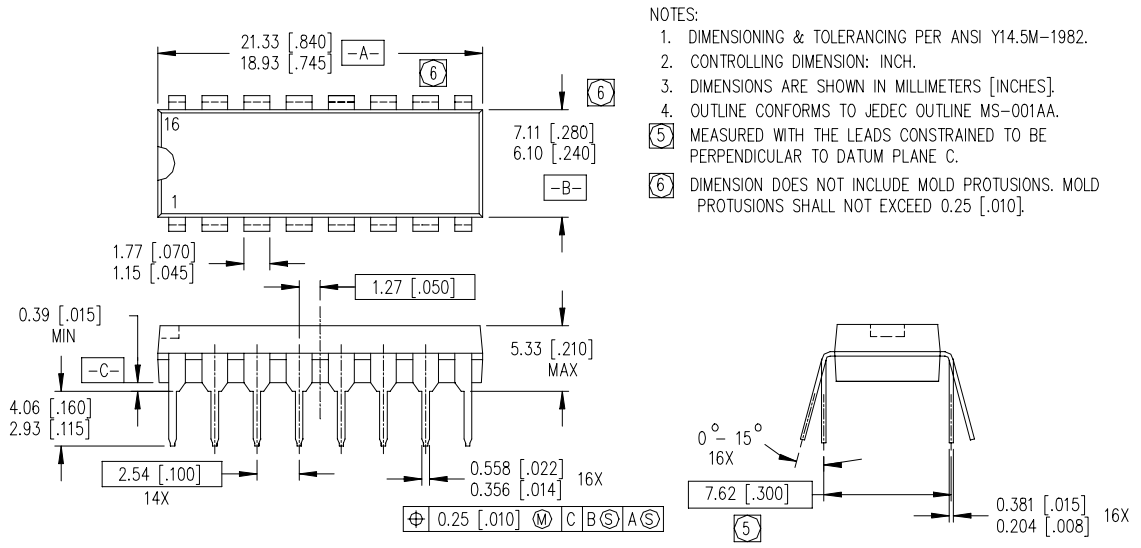
Step 5: Select zener diode DCOMP value:

$$D_{COMP} \text{ zener voltage} \approx V_{COMP\ MAX} \quad \text{[Volts]} \quad (5)$$

Step 6: Calculate resistor RSUPPLY value:

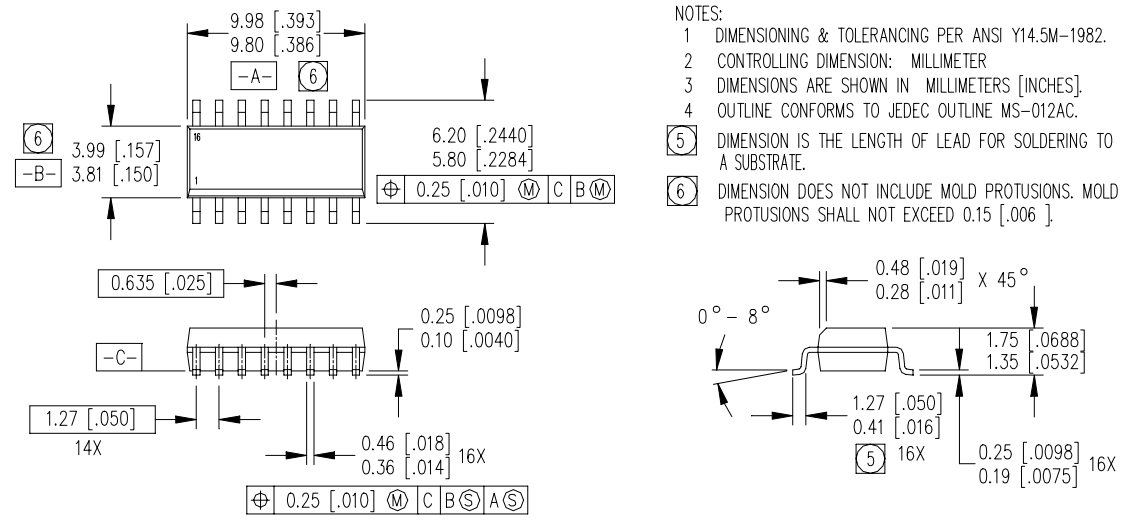
$$R_{SUPPLY} = \frac{VAC_{MIN_{PK}} + 10}{IQCCUV} \quad \text{[Ohms]} \quad (6)$$

Case outline



16 Lead PDIP

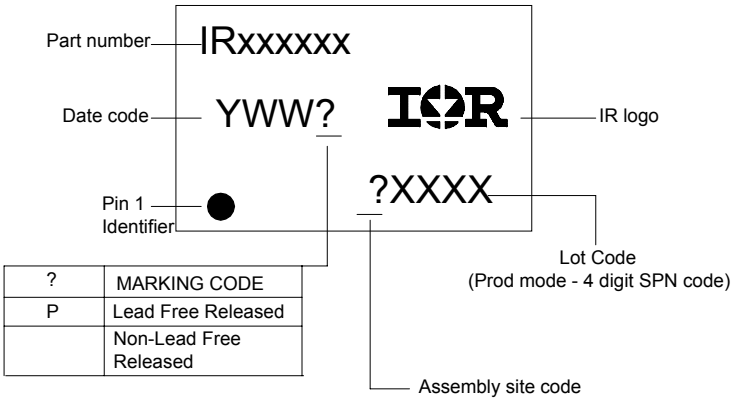
01-6015
01-3065 00 (MS-001A)



16 Lead SOIC (narrow body)

01-6018
01-3064 00 (MS-012AC)

LEADFREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

ORDER INFORMATION

Basic Part (Non-Lead Free)
16-Lead PDIP IR2166 order IR2166
16-Lead SOIC IR2166S order IR2166S

Leadfree Part
16-Lead PDIP IR2166 order IR2166PbF
16-Lead SOIC IR2166S order IR2166SPbF

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
Data and specifications subject to change without notice. 11/30/2006