8-phase Dual Loop Voltage Regulator

Features

- Digital controller assisted with high performance analog front ends with a fully programmable ARM® Cortex™ –M0 Processor
- Compliant with Intel™ VR13, VR13HC, and VR14 Server VR Vendor PWM Enabling Specification Rev 1.88 (October 2021)
- Compliant with Intel™ VR14.Cloud Rev 1.06 (Jan 2025) Advanced Telemetry Level 2 and Security Level 2
- Compliant with Intel™ IMVP9.1/9.2 VR Vendor PWM Enabling Specification Rev 1.0 (May 2023)
- Compliant with Intel™ SVID Protocol Spec Rev 1.95 (June 2023)
- Compliant with PMBus Rev 1.4 (January 2022) serial interface
  - Query voltage, current, temperature faults
  - Fault Response
  - Maximum supported bus speed 1 MHz
  - Support 1.8/3.3 V operation
  - Support PAGE_PLUS_WRITE/PAGE_PLUS_READ
- Compliant with PMBus Part III - AVSBus Rev 1.4 (January 2022)
- Compliant with PMBus Level 2 Secure Device Specification Rev 2.02 (May 2023)
- Output voltage regulation range
  - 0.25 V to 1.52 V (5 mV/step)
  - 0.5 V to 3.04 V (10 mV/step)
  - 0.05 V to 3.1 V (1 mV/step)
- Digitally controlled phasing for full flexibility in both loop configuration and phase firing order
- Digital current emulation for TLVR inductor support
- Configurable autonomous phase add/drop
- Automatic phase detection at start-up
- Supports start-up into pre-bias voltage
- Integrated power stage current sense
- Differential output voltage sense
- Fast current balancing with current-mode control
- Digitally programmable PID (Proportional, Integral, Differential) loop compensation
- Digitally programmable loadline slope
- Digital temperature compensation
- Direct input (+12 V) voltage and current sense
- Extensive fault detection and protection capability
  - IUVP, OUVP & OOVP (fixed and tracking)
  - OCP instantaneous (total current)
  - Multiple OTP thresholds
  - Peak phase current pulse limiting
  - Negative current limit protection
  - TLVR secondary Open/Short detection
  - Blackbox recording before system shutdown
- Internal non-volatile memory (NVM) to store multiple custom configurations
- RoHS compliant and Halogen free 40-lead QFN plastic package

Potential applications

- Vcore power regulation for Intel™ VR13, VR13HC, VR14 based Microprocessors in server, workstations and high-end desktop applications.
- High Current ASIC, PMBus POLs in AI server and telecom applications

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22/78

Description

This XDPE digital dual loop 8 phase controller provides power for AI server, telecom, Intel™ VR13, VR13HC, VR14 server, workstation, and high-end desktop applications that use AVS bus. Voltage on either the first loop or the second loop is provided by a multi-phase buck converter with up to 8 synchronous-rectified channels. The controller's phase configuration is flexible in how the phases are allocated to the 2 loops. Any phase can be assigned to either loop and the phase firing order is fully programmable to offer the ultimate in phase configuration flexibility. Typically, configurations of 8+0, 7+1… 0+8 phases are supported.

Command and monitoring functions are controlled through the PMBus, AVS and SVID interfaces which supports dynamic voltage identification with 1mV/step in AVS mode or 5 mV/step or 10 mV/step in Intel mode, output range up to 3.1 V, offset and trim resolution of 625 uV and accuracy better than 0.5%.

The controller utilizes digital technology to implement all control functions, providing the ultimate system solution in terms of flexibility and stability. Advanced control loop features, such as current mode control, variable frequency operation, Active Transient Response (ATR/FATR), fast DVID response, automatic phase shedding and Pulse Frequency Modulation (PFM) enable optimal response to a highly dynamic load with fast di/dt load transients across a wide range of load current.

The controller supports multi-vendor pin compatible integrated power stages with trivalent PWM interfaces, fast response, integrated current sense, integrated temperature sense, and advanced fault detection capability, interface and signaling.

In addition to supporting power stage fault protection features, the controller also includes a set of sophisticated over-voltage, under-voltage, over-temperature, over-current, and phase fault protections. These attributes provide a complete and advanced protection feature set for microprocessor and power systems.

Table 1 Part number and package summary

Part Number	Package
XDPE1C284A	40-lead 5 mm x 5 mm QFN PG-VQFN-40

1 Ordering information

Table 2 Ordering information

Base Part Number	Package Type	Form	Quantity	Orderable Part Number	Note
XDPE1C284A	QFN 5 mm x 5 mm	Tape and Reel	4000	XDPE1C284A0000XTMA1	Standard Part Number with default configuration
				XDPE1C284AxyzzXTMA1	Customer Specific Part Number, where x=Firmware ID, and yzz=Customer Config File ID (Codes assigned by Product Marketing)

1.1 Sample programming

The customer can program the parts to their specific system requirements using software/hardware available from Infineon or through other controller programming 3rd Parties (contact Infineon for recommendations). Infineon Field Application Engineers are available to assist with system and configuration file optimization and programming of the controllers. Alternatively, samples can be ordered with a customer specific configuration pre-programmed at the factory, but lead times for these types of samples are significantly longer than for standard default configuration samples. The generic part numbering format is shown below:

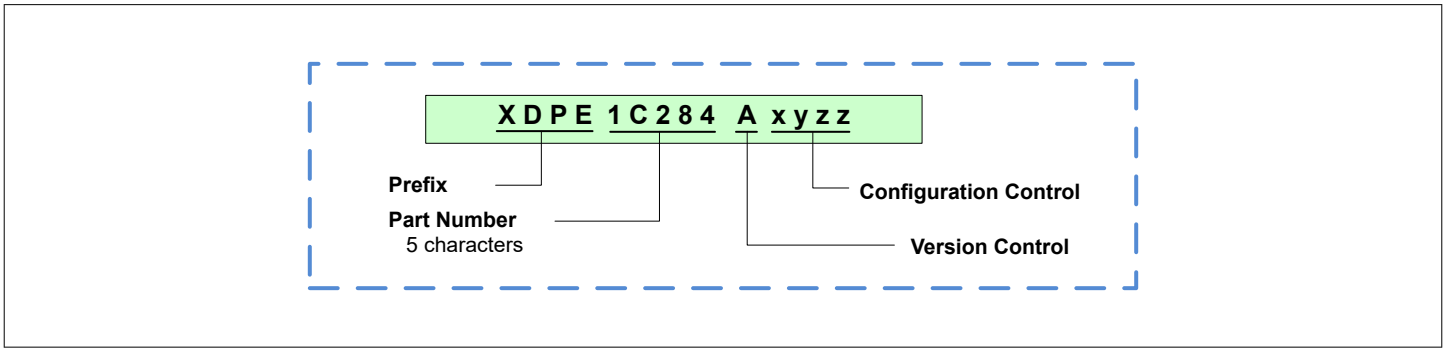

Figure 1 Part number decoding

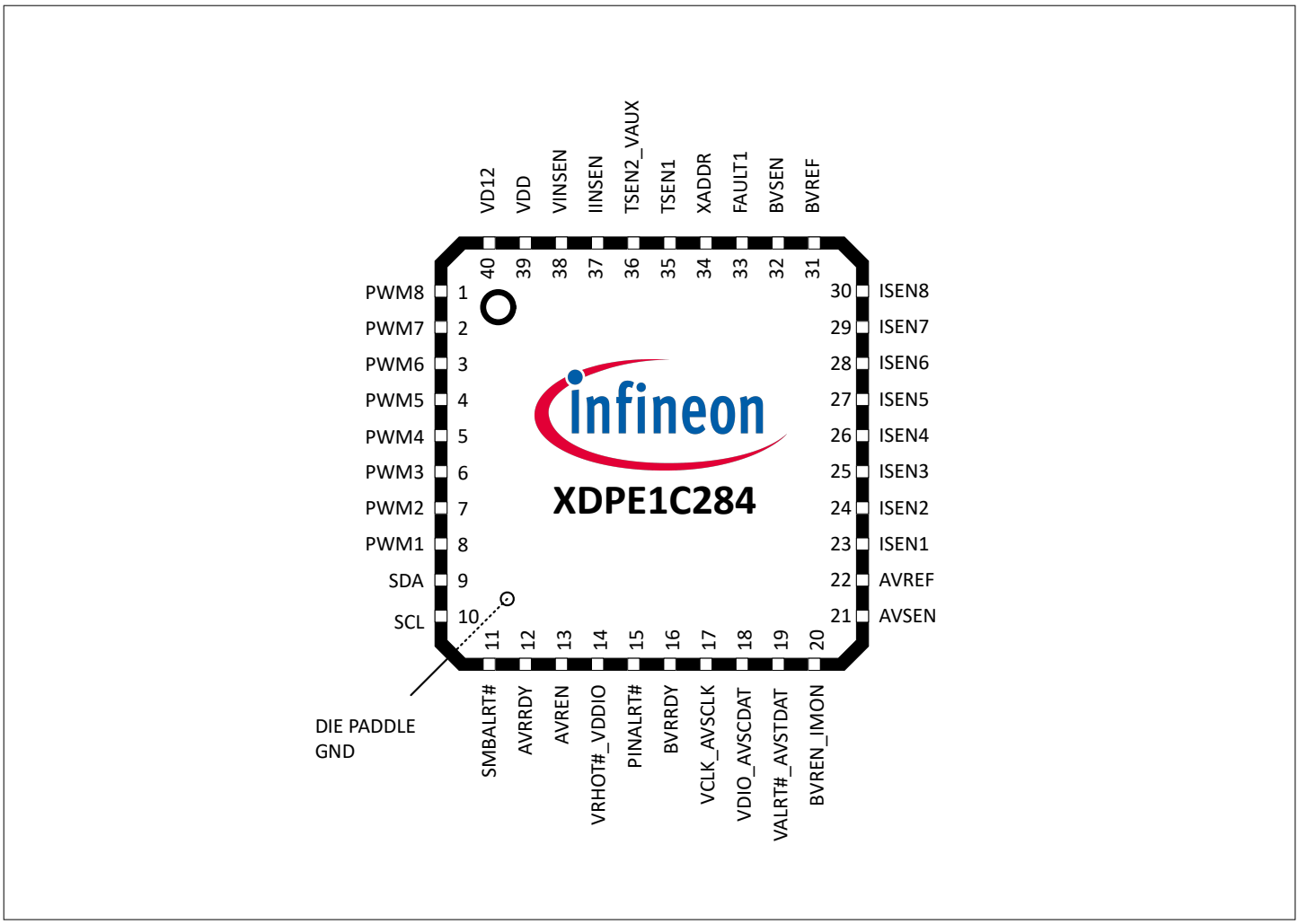

Figure 2 Package top view

2 Package marking

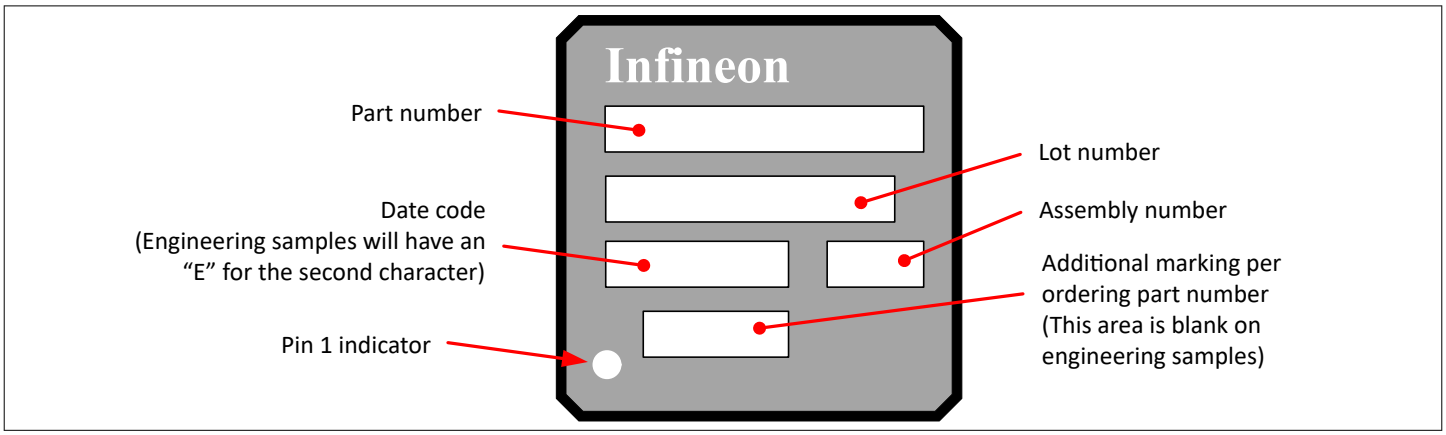

Figure 3 Package marking

3 Environmental qualifications

Table 3 Environmental qualifications

Qualification Level		Industrial	
Moisture Sensitivity		QFN Package	MSL1
ESD	**Human Body Model**	JS-001 Class 2	
	Charged Device Model	JS-002, Class C3	
RoHS Compliant		Yes	

Revision history

XDPE1C284A Short

Revision 2026-08-04, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-08-04	Release of final version

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