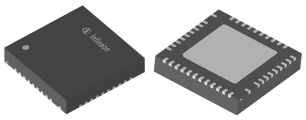
Features



- Wide input voltage range: 7 V to 80 V with surge immunity
- Integrated 100 V, ~1.5 mΩ OptiMOS™ FET with current sensor
- Digital controller and built-in GATE driver
- Maximum continuous Current: up to 30 A
- Inrush current protection using digital SOA control with active FET SOA protection
- Parallel operation for higher current applications with active current sharing at start-up
- "Primary/standalone" or "secondary" device operation mode for stacking multiple eFuses
- Integrated die temperature sensor
- Analog current (IMON) reporting and monitoring with up to ± 1% accuracy
- Dedicated current and voltage ADCs: 12-bit resolution
- Accurate telemetry: V ≤ ±0.5%, I ≤ ± 1%, P ≤ ± 2%, E ≤ ± 3%
- Telemetry averaging (V, I, P) with "peaks and valleys"
- Fast, programmable short circuit protection
- Programmable fault response: auto-retry and latch-off
- Programmable fault protections: input undervoltage, input overvoltage, output undervoltage, overcurrent, severe overcurrent, turn-on time, pre-charged output voltage (VDS), FET health, thermal shutdown, etc.
- PMBus™ v1.3 interface with up to 1 MHz speed
- Permanent WRITE protection
- One-time programmable non-volatile memory
- At least seven unique programmable device addresses
- Sequential turn-on capability
- IPC2221B and IPC9592B high-voltage compliant
- PG-LIQFN-42 lead, 7 mm x 7 mm package
- - 40°C to + 125°C operating junction temperature

Potential applications

- Servers and datacenters
- 24 V 48 V industrial systems
- Power distribution systems
- Network routers and switches
- Power supplies
- Test equipment

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

XDP730 is a 30 A smart eFuse with integrated ~1.5 mΩ $R_{DS(on)}$ OptiMOS™ FET, current sensor, digital controller and a built-in GATE driver. It is an IPC2221B and IPC9592B HV standard compliant device that ensures reliable inrush current control and continuous system health monitoring. The digital SOA control with active SOA protection ensures that the integrated MOSFET always operates under safe conditions. When multiple XDP730 ICs are connected in parallel, the active current sharing during start-up maintains safety conditions in high-power systems. A simplified schematic is shown below for reference.

XDP730 provides accurate system telemetry (V, I, P, T, E) and reports analog current at the IMON pin for post-processing. It incorporates various system protections and generates appropriate protection responses depending on the incident's severity. Auto-retry and latch-off are the allowed response types. The XDP730 has a one-time programmable non-volatile memory and a high-speed PMBus™ interface for communication.

The device is available in a 7 mm x 7 mm 42–pin PG-LIQFN package and is specified over a - 40°C to + 125°C junction temperature range.

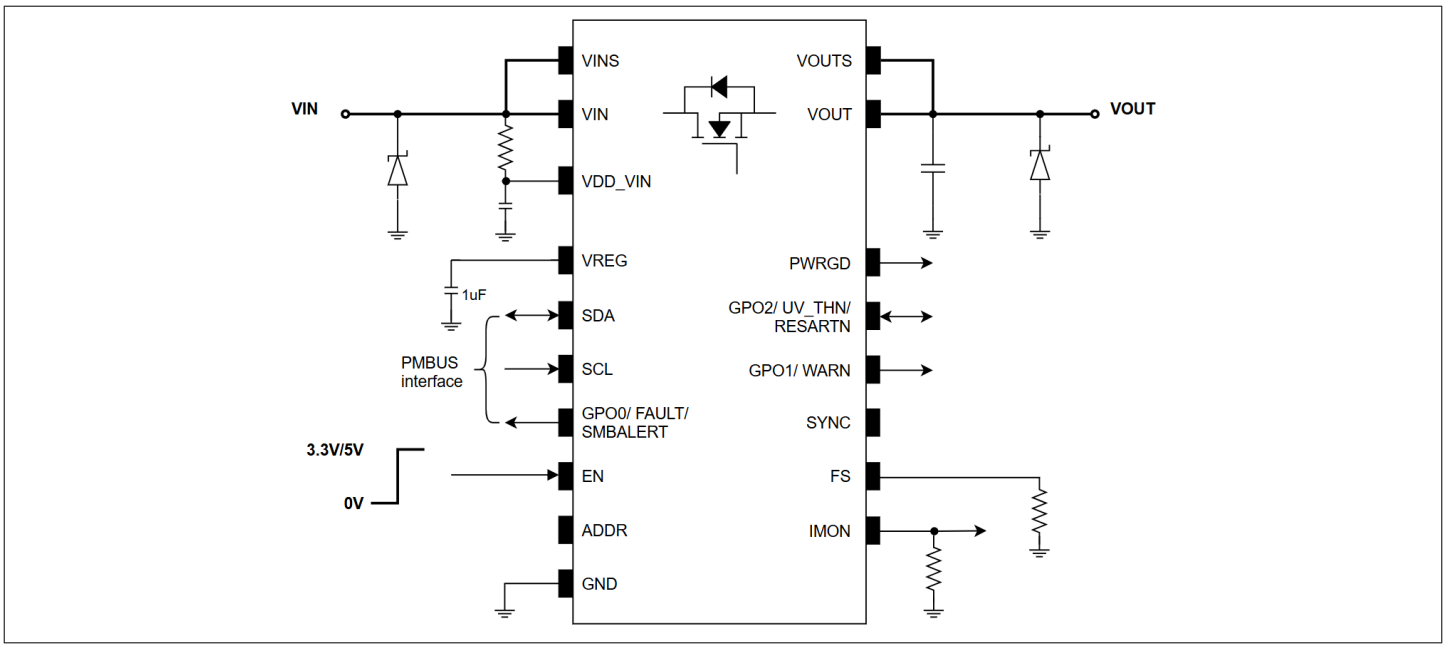

VIN
VINS
VIN
VDD_VIN
VREG
1uF
SDA
PMBUS
interface
SCL
GPO0/ FAULT/
SMBALERT
3.3V/5V
0V
EN
ADDR
GND
VOUTS
VOUT
VOUT
PWRGD
GPO2/ UV_THN/
RESARTN
GPO1/ WARN
SYNC
FS
IMON

Table of contents

1 Pin configuration

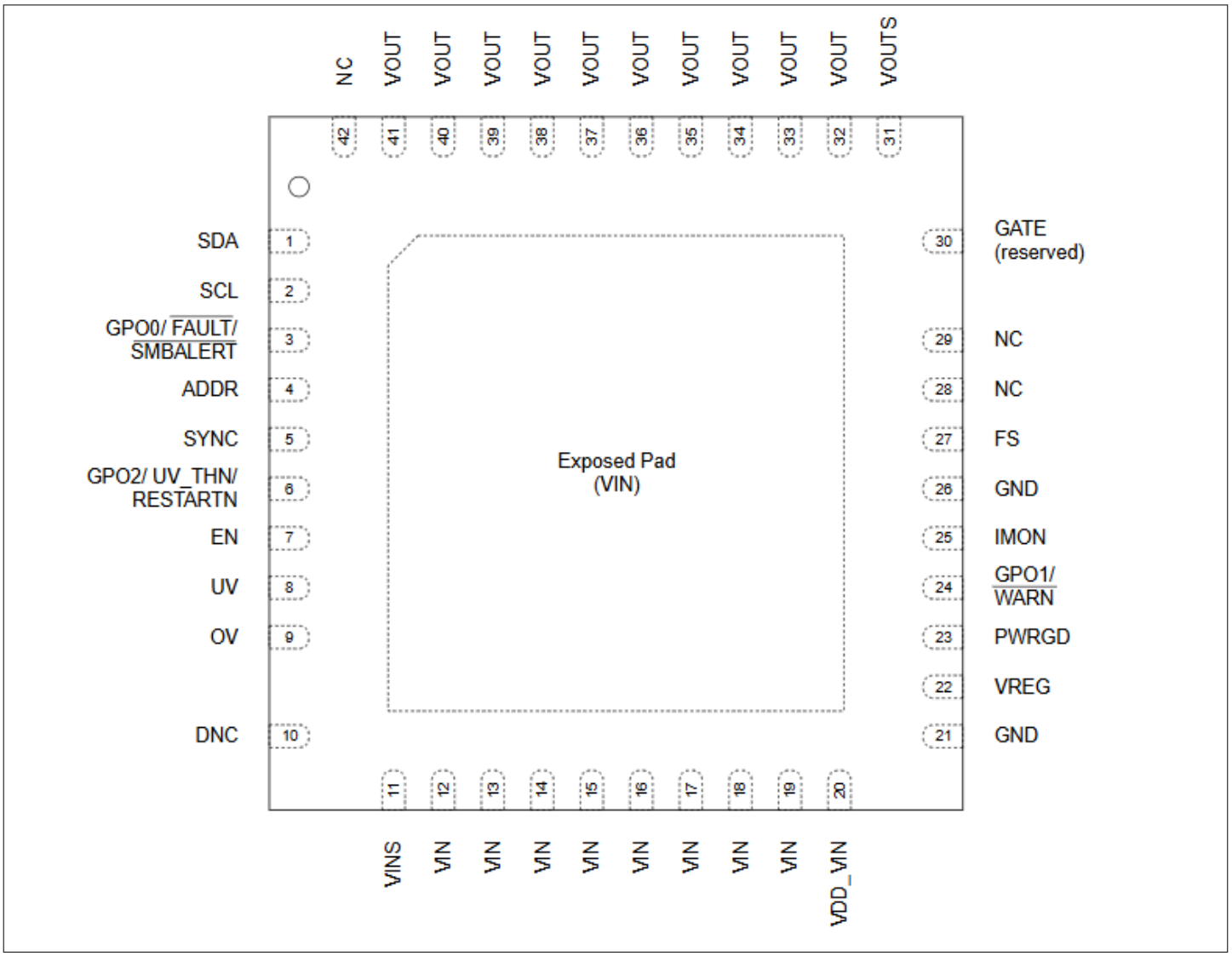


Figure 1 XDP730 device pinout (top view)

Table 1 XDP730 pinout

Pin #	Name	Type	Description	if unused, connect to
1	SDA	IO	PMBus™ data open drain pin.	Pull-up to VREG or external source
2	SCL	I	PMBus™ clock input pin. The interface is rated to 1 MHz.	Pull-up to VREG or external source

(table continues...)

Table 1 (continued) XDP730 pinout

Pin #	Name	Type	Description	if unused, connect to
3	GPO0/ FAULT/ SMBALERT	O	General-purpose digital output 0. Pin configuration is programmable. FAULT open drain output. This pin asserts low when a fault has occurred. The faults that can trigger this pin are configurable. SMBALERT open drain output. It can be selected to report (active low) faults and/or warnings. Default Configuration: FAULT	Open
4	ADDR	I	Device address configuration input pin. It can be left open or tied to GND through a resistor for a total of seven unique PMBus™ device addresses. This pin is also used to configure the device mode. If this pin is directly tied to GND then the device operates as "SECONDARY" device, otherwise it operates as "PRIMARY/standalone" device.	Open
5	SYNC	IO	SYNC open drain pin with internal pull-up. This pin is used to synchronize multiple XDP730 devices connected in parallel. It is similar to the FAULT pin with one exception, see details.	Open
6	GPO2/ UV_THN/ RESTARTN	IO	General-purpose digital output 2. Pin configuration is programmable. UV throttle open drain output. This pin asserts low during input undervoltage throttling. RESTARTN input. Falling edge triggered automatic restart input (with internal pull-up resistor of 100 kΩ). The MOSFET remains off for a configured time and then turns back on. Default configuration: RESTARTN	Open
7	EN	I	Enable input pin. The MOSFET is turned on when $V_{EN} \geq V_{EN\_UTH}$.	Pull-up to VREG
8	UV	I	Input undervoltage pin. The UV fault is triggered if $V_{UV} < V_{UV\_LTH}$.	-
9	OV	I	Input overvoltage pin. The OV fault is triggered if $V_{OV} > V_{OV\_UTH}$.	-
10	DNC		Do not connect pin.	Open
11	VINS	I	Input voltage sense pin.	VIN
12 - 19	VIN	I	Input voltage terminal.	VIN

(table continues...)

Table 1 (continued) XDP730 pinout

Pin #	Name	Type	Description	if unused, connect to
20	VDD_VIN	I	Power supply pin. A 100 Ω – 100 nF RC filter is recommended at this pin.	VIN
21	GND	-	Ground reference terminal (to be connected to system ground).	GND
22	VREG	O	VREG (internal 5 V regulator) output pin. A 1 µF capacitor from this pin to GND is mandatory.	Connect a 1 µF capacitor from this pin to GND
23	PWRGD	O	Power good open drain output pin. It is asserted high when VOUT has reached its final level i.e. steady state, the MOSFET is fully enhanced and no faults are detected.	Open
24	GPO1/ WARN	O	General-purpose digital output 1. Pin configuration is programmable. Warning open drain output. This pin is asserted low when a warning is triggered. The warnings that can trigger this pin are configurable. Default configuration: WARN.	Open
25	IMON	IO	Analog current monitor pin. This pin reports/sources a current proportional to the monitored MOSFET current (IMON) level. This pin is also monitored for current protection levels and telemetry. A resistor is recommended from this pin to GND.	Open
26	GND	-	Ground reference terminal (to be connected to system ground).	GND
27	FS	I	Fail-Safe pin for turn-on fail safety. A resistor greater than 8.9 kΩ is recommended from this pin to GND.	Open
28, 29	NC	-	Not connected pin.	-
30	GATE (reserved)	O	Gate pin of internal MOSFET referenced to VOUT. This pin must be left floating.	Open
31	VOUTS	I	Output voltage sense pin.	VOUT
32 - 41	VOUT	O	Output voltage terminal.	VOUT
42	NC	-	Not connected pin.	-
EP	VIN	I	Input voltage terminal.	VIN

2 Functional description

The XDP730 is a 30 A smart eFuse with integrated low $R_{DS(on)}$ OPTIMOS™ FET, current sensor, die temperature sensors, digital controller and a built-in GATE driver. It is PMBus™ v1.3 compliant, which allows the system microcontroller to control, configure and debug the device as well as monitor its telemetry data.

The device becomes fully operational when the voltage on the VDD_VIN pin crosses 9 V. If there are no faults and the EN pin is pulled HIGH, then the enable deglitch timer is initiated which allows the input supply on VIN pins to stabilize. The device waits until this timer has expired and then starts the MOSFET turn-on procedure. Its proprietary digital SOA control ensures that the inrush current never exceeds the safe operating limits of the MOSFET. The device establishes stable output voltage at VOUT pins after the MOSFET is successfully turned on. The PWRGD pin is used to signal the load/microcontroller that VOUT is ready.

The input voltage, current, output voltage, internal MOSFET temperature and internal controller temperature are constantly monitored by the device for proper telemetry and protection. It also reports a current proportional to the current flowing through the device on the IMON pin. There are many protections incorporated in this device to protect itself and the system load. These include input undervoltage, input overvoltage, overcurrent, severe overcurrent, overtemperature, thermal shutdown and MOSFET health checks to name a few. All these protection-related settings are configured using PMBus™ commands. Also, it can intelligently protect the system load against input surge events. Depending on the retry settings, the device will either auto-retry or latch-off when a fault event has occurred. A dedicated user-triggerable RESTARTN pin/command is also available which will turn-off the MOSFET and then turns it back on after the RESTART timer has expired. This device has the ability to quickly discharge its output voltage based on the configuration. The One-time programmable (OTP) section of the memory allows the user to permanently store the device configuration. To enhance security, this device also comes with a “permanent WRITE protection” feature which makes it immune to all the future PMBus™ WRITE operations.

This device is designed to address the ever-increasing power demands of the market. Multiple XDP730 devices can be connected in parallel to increase the system power. The SYNC pin and FS pin always ensure that all the devices in the chain are synchronized, and the main/PRIMARY device is alive in the system. A fault in any device will cause all the devices to turn off their MOSFETs, thus disconnecting the system load from the input supply. The PRIMARY device will then react according to its fault response settings whereas the SECONDARY devices will simply follow the PRIMARY device.

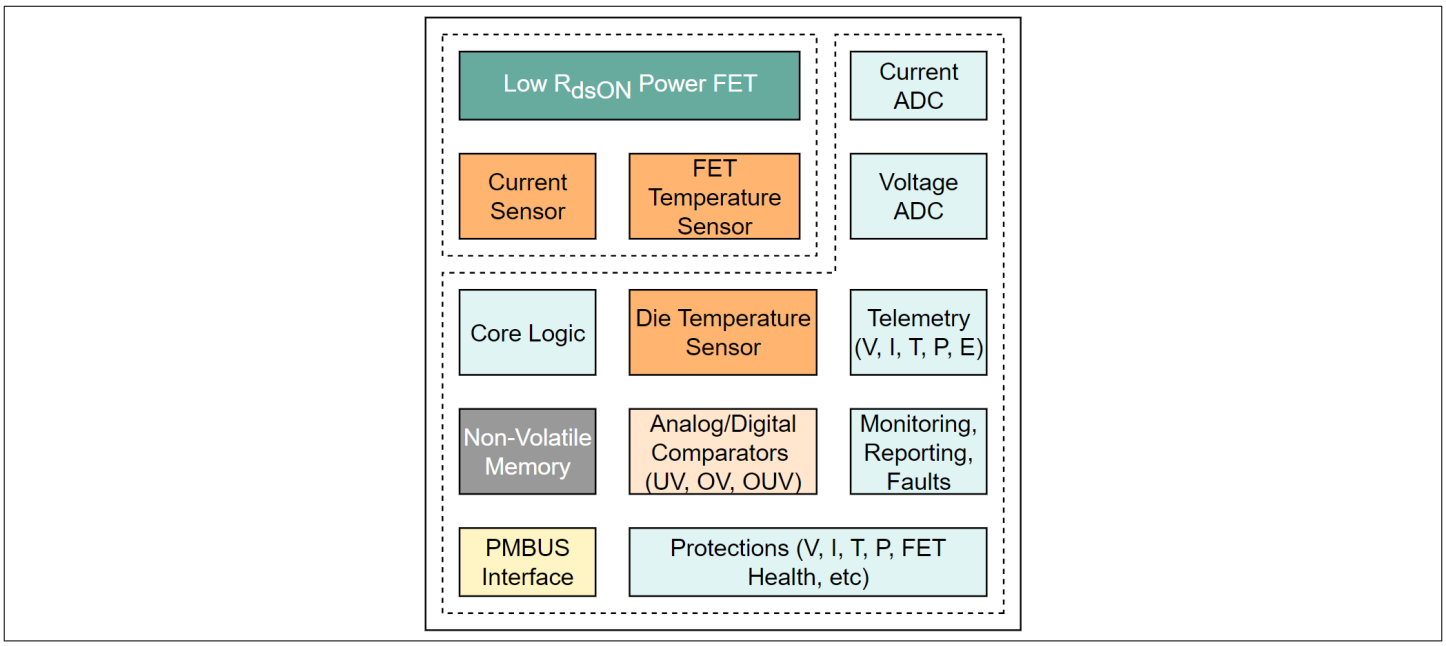


Figure 2 Simplified block diagram

2.1 Operational states

A simplified device state machine is shown in Figure 3. It shows all the important state transitions to understand the device operation.

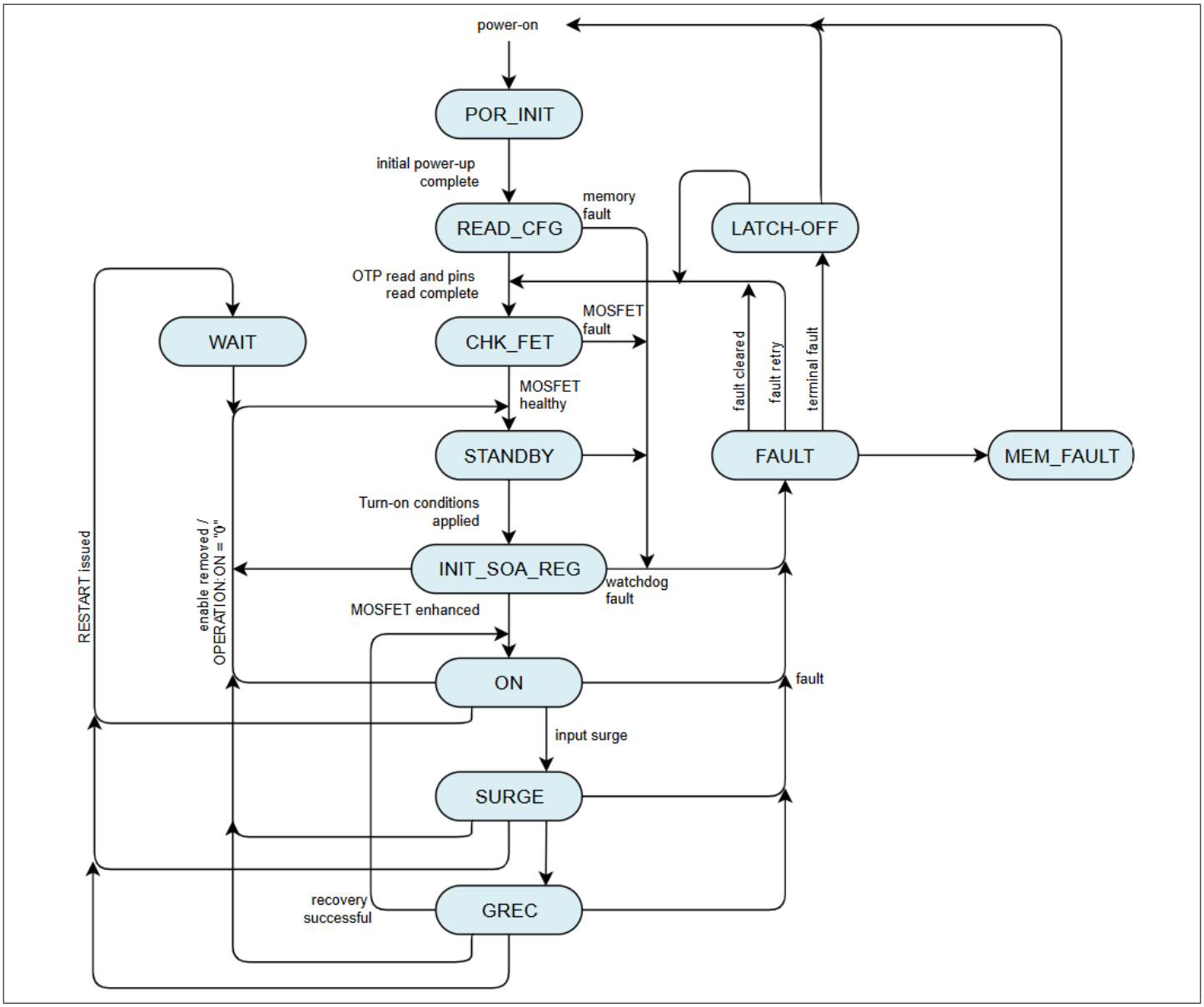


Figure 3 Simplified state machine

Table 2 Operational states description

	State	Name	Description	Next state (no fault)	Next state (fault)
Initialization	0	POR_INIT	Internal circuitry is initialized as soon as VDD_VIN > 7 V.	READ_CFG	NA
	1	READ_CFG	POR and initialization complete. OTP memory and external pins are read at this point.	CHK_FET	FAULT
Power-up procedure	2	CHK_FET	MOSFET is checked for gate to source or gate to drain shorts.	STANDBY	FAULT

(table continues...)

Table 2 (continued) Operational states description

	State	Name	Description	Next state (no fault)	Next state (fault)
	3	STANDBY	• VIN is within a valid range (within UV and OV limits), device temperature is in appropriate range and EN signal is deasserted or OPERATION:ON bit is cleared. • Device transitions to next state when MOSFET turn-on conditions are applied and the EN_DG timer has expired.	INIT_SOA_REG	FAULT
	4	INIT_SOA_REG	MOSFET turn-on watchdog timer starts running. SOA regulation phase: • Device regulates the current according to the programmed SOA, depending on VDS value (see details) in order to charge the output capacitor. • INIT_SOA_REG phase stops when MOSFET V_{DS} < 1.0 V, V_{GS} > 7.8 V and no faults are detected during this procedure. • Due to the current regulation, the time spent in this state depends on the output capacitance value. Device transitions to STANDBY state if EN is deasserted or OPERATION:ON bit is cleared.	ON or STANDBY	FAULT
Normal operation i.e. steady state	5	ON	Steady state is reached i.e. MOSFET is fully enhanced. • Turn-on watchdog timer is reset at this point. • IMON pin starts reporting the proportional current. Device transitions to STANDBY state (if EN is deasserted or OPERATION:ON bit is cleared) or SURGE state (if input surge is detected) or WAIT state (if RESTART is issued).	ON or STANDBY or SURGE or WAIT	FAULT

(table continues...)

Table 2 (continued) Operational states description

	State	Name	Description	Next state (no fault)	Next state (fault)
Idle	7	FAULT	Fault has occurred. Device will stay idle in FAULT state until: • Fault conditions are cleared in the case of non-retry dependent faults. • Cool down timer expires in the case of retry dependent faults. If retry counter has expired or latch-off fault has occurred, then the device will go to LATCH_OFF state directly after FAULT. In case of memory fault, the device transitions into MEM_FAULT.	CHK_FET or LATCH_OFF	NA
	8	LATCH_OFF	If the maximum number of retries has been reached, the device will latch off until faults are cleared and latch-off is released.	POR_INIT or CHK_FET	NA
	9	MEM_FAULT	If an OTP read or write error is detected, the device will go to FAULT and consecutively MEM_FAULT state, which initiates the controller's latch-off. A power cycle is required to go out of MEM_FAULT.	POR_INIT (power cycling)	NA
	10	WAIT	A RESTART command has been issued by the user. • Device turns off its MOSFET and stays in this state until restart timer expires. • After this time, the device goes to STANDBY and, if the necessary conditions are met, MOSFET is automatically turned back on, going to ON state.	STANDBY	NA

(table continues...)

Table 2 (continued) Operational states description

	State	Name	Description	Next state (no fault)	Next state (fault)
	11	SURGE	Input surge (high dv/dt) suppression state. Device transitions to GREC state to attempt recovery or to STANDBY state (if EN is deasserted or OPERATION:ON bit is cleared) or WAIT state (if RESTART is issued).	GREC or STANDBY or WAIT	FAULT
	12	GREC	Recovery is attempted by pulling the V_{GS} to the MOSFET's threshold voltage level. Device transitions to ON state if recovery is successful or to STANDBY state (if EN is deasserted or OPERATION:ON bit is cleared) or WAIT state (if RESTART is issued).	ON or STANDBY or WAIT	FAULT

2.2 Configuration modes

In XDP730, the ADDR pin is used to configure two important parameters namely the device mode of operation and the PMBus device address. This pin is sensed in the READ_CFG state during the device start-up sequence. As shown in Table 3 below, the device mode can only be set by using an appropriate resistor value from this pin to ground (GND). However, the PMBus device address can be either programmed through the PMBUS_CFG command when ADDR pin is open or GND, or as a byproduct of the ADDR pin resistor setting.

Table 3 Configuration of ADDR pin

ADDR pin voltage (V)	ADDR pin resistance (kΩ)	Device mode	Base address field [6:4]	Device address field [3:0]
V_{ADDR} > 2.8 (Open)	Open	PRIMARY	set via PMBUS_CFG command Default = 001	set via PMBUS_CFG command (default = 0000)
2.2 < V_{ADDR} ≤ 2.8	24.9			0001
1.7 < V_{ADDR} ≤ 2.2	19.6			0010
1.3 < V_{ADDR} ≤ 1.7	15			0011
0.9 < V_{ADDR} ≤ 1.3	11			0100
0.6 < V_{ADDR} ≤ 0.9	7.5			0101
0.3 < V_{ADDR} ≤ 0.6	4.53			0110
V_{ADDR} ≤ 0.3 (GND)	GND	SECONDARY		set via PMBUS_CFG command (default = 0000)

Connecting this pin directly to GND configures the device as a SECONDARY device, otherwise it is configured as a PRIMARY device. This is extremely useful in parallelizing multiple XDP730 devices for high power designs. In order to turn-on its MOSFET, the SECONDARY device relies on the I_{FS} current from the PRIMARY device for failsafe check using

the FS pin. The SECONDARY device does not have an independent retry capability as it simply follows the PRIMARY device in the system. Refer Chapter 4 section for high power design.

Similar to the device mode configuration, the comparators used for the input undervoltage (UV) and overvoltage (OV) protections can also be configured. By default, UV and OV faults are triggered by sensing the voltage at the VINS pin using internal digital comparators. If the user desires a faster response, then the analog comparators at UV and OV pins can be used by configuring the MODE (MODE:MODE_P and MODE:MODE_S) command.

2.3 Power-up sequence

When using XDP730 in an application, the main input power supply bus is connected to the VIN pins whereas the VDD_VIN pin is connected to the VIN through an RC filter. This RC filter helps to get a stabilized VDD_VIN level, which is the input supply to the device's controller section. When the VDD_VIN level rises above 7 V, the internal regulator VREG output is set to ~5 V level and all the analog/digital pins are released after a successful check. It is mandatory to connect a 1 uF capacitor from the VREG pin to GND. Figure 4 shows a simplified XDP730 power-up sequence.

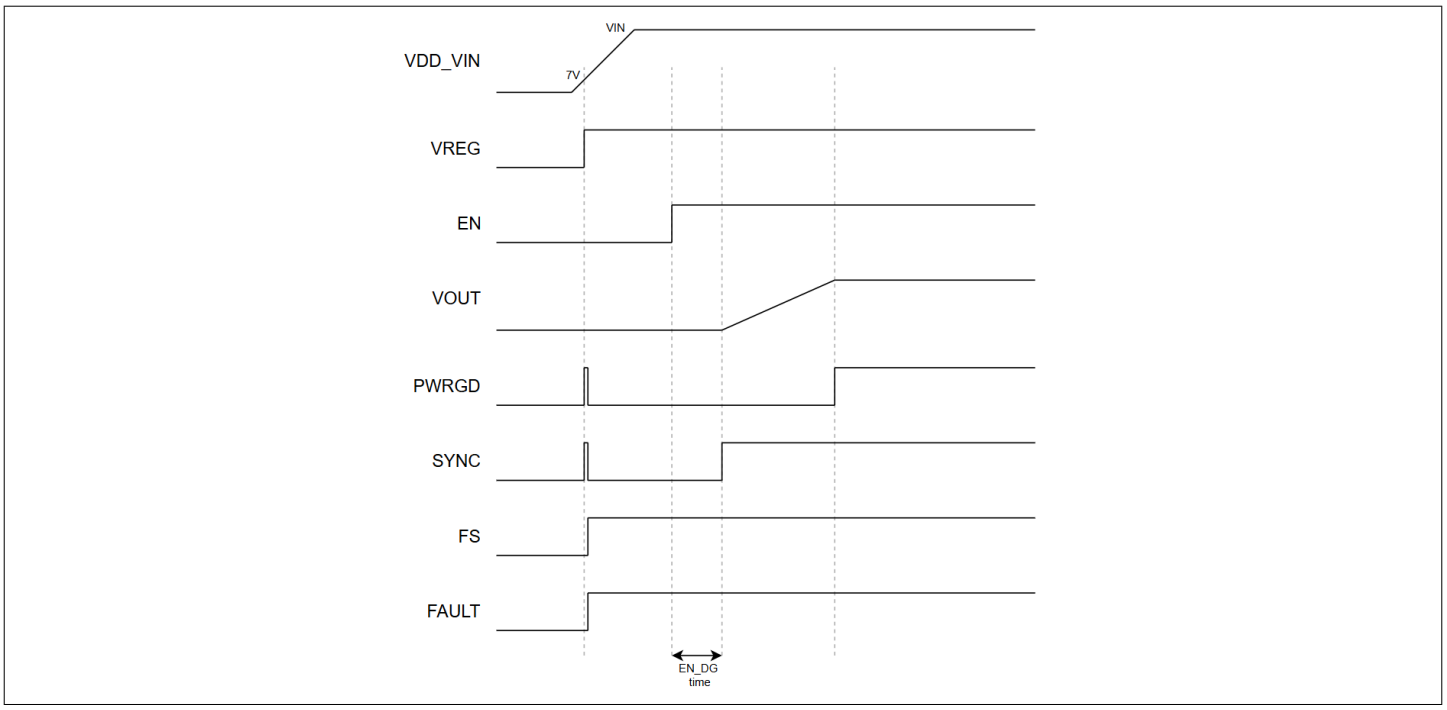


Figure 4 XDP730 power-up sequence (PWRGD and FAULT tied to VREG)

2.3.1 FailSafe

The device has a turn-on fail safety mechanism to ensure that the SECONDARY devices in the system will not turn-on their MOSFETs if the PRIMARY device is damaged. After a successful device power-up, the PRIMARY configured device will source I_{FS} current on the FS pin. A resistor from this pin to GND aids every device in the system to constantly sense its FS pin voltage i.e. V_{FS}. Each device will only allow its MOSFET to turn-on if the V_{FS} >= V_{FS_TH}, otherwise it triggers a SYNC fault.

***Note**: The device will enter LATCH-OFF state when a SYNC fault is triggered due to FS. It can only be released reliably, by performing a device power cycle.*

2.3.2 SYNC procedure

When multiple XDP730 devices are connected in parallel to increase system power, it becomes extremely crucial to properly synchronize them. This is achieved by connecting all the SYNC pins together. Every device has a SYNC pin with internal control and sense lines. At device power-up, the SYNC pin is internally held low by the device until all checks are successful. It is only released and pulled high once the enable deglitch timer has expired without any fault conditions. This way all the devices will turn-on their MOSFETs at the same time when SYNC goes HIGH, provided all

other turn-on conditions are present. When a fault is triggered, the device will pull its SYNC pin low based on the type of fault. This is seen by the other devices almost immediately which forces them to turn-off their MOSFETs to protect the system. The SECONDARY configured device also performs a SYNC handshaking protocol to ensure that the PRIMARY device in the system is properly taking control over the SECONDARYs. If, for some reason, the PRIMARY device fails to respond within t_{SYNC_HSK} then the SECONDARY device will treat it as an unsuccessful SYNC handshaking and gets latched off.

Attention**: **SYNC pin is functionally similar to the FAULT pin.

***Note**:*
- *At power-up, the device starts to actively pull its SYNC pin LOW at the end of the READ_CFG state.*
- *Disabling the SYNC fault and its reporting on the FAULT pin using ENABLE_FAULTS and MASK_FAULTS commands respectively, must be avoided.*

2.3.3 Enable and disable

A dedicated EN pin is introduced in XDP730 to enable or disable the device output by controlling the MOSFET. There is an analog comparator at the EN pin which senses its voltage. As shown in the table, the MOSFET is allowed to turn-on if the voltage on the EN pin is higher than the threshold level i.e. V_{EN_UTH}, along with the mentioned conditions.

Table 4 MOSFET turn-on conditions

FS	SYNC	OPERATION:ON bit	EN	State of the MOSFET
V_{FS} >= V_{FS_TH}	H	"1"	H	Active (can be ON; or OFF due to fault)
V_{FS} < V_{FS_TH}	x	x	x	OFF
x	L	x	x	OFF
x	x	"0"	x	OFF
x	x	x	L	OFF

An enable deglitch timer (EN_DG) is started when the EN pin is pulled high. This timer protects the device from contact bouncing during hotswap events and is fully programmable via PMBus™. It is recommended that a non-zero enable deglitch timer is always used. By default, the device has 8 ms enable deglitch timer value.

In addition to enabling/disabling the device, the EN pin can also be used to clear any faults using its HIGH-to-LOW transition as described in Chapter 2.12.2.2. Only the OTP memory (MEM) fault is not affected by this EN transition.

Attention**: **At power-up, the MOSFET can only be turned on when VINS is above the input undervoltage fault level plus hysteresis (or the UV pin voltage is above the V_{UV_UTH}) and VINS is below the input overvoltage fault level minus hysteresis (or the OV pin voltage is below the V_{OV_LTH}).

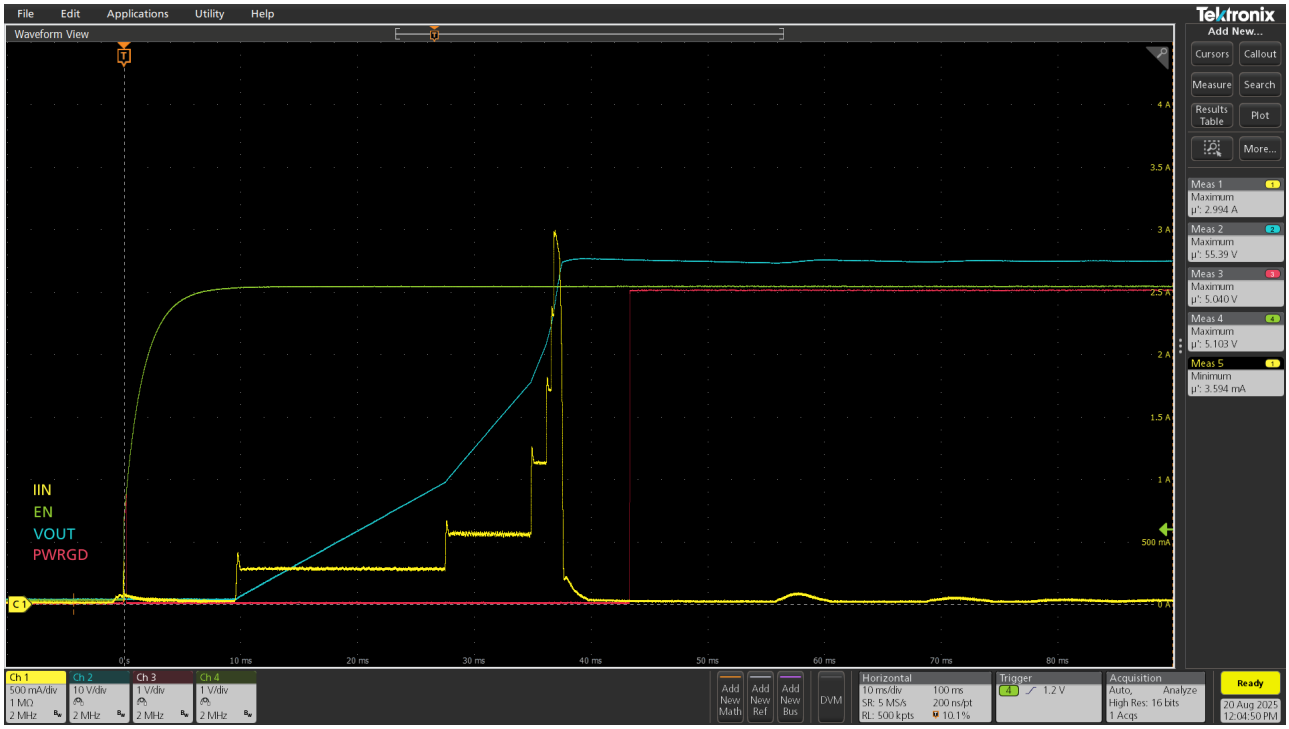


Figure 5 Default turn-on; C_{OUT} = 270 µF

2.3.3.1 Undervoltage function

Generally, every system that uses an eFuse is designed for a specific operating voltage range. The XDP730 has two undervoltage protections for monitoring the minimum input and output voltages. By default, the input undervoltage is configured to sense the voltage at the VINS pin using a digital comparator. When the VINS voltage falls to/below the digitally programmed limit, the input undervoltage protection (UV) is triggered. If needed, the device can be configured to use an analog comparator at the UV pin for faster response. When the UV pin voltage falls to/below V_{UV_LTH}, the input undervoltage protection (UV) is triggered. The equation below can be used to calculate the values of the resistor divider network at the UV pin as shown in Figure 6. At a given time, the input undervoltage can be configured to use either the digital comparator or the analog comparator. The output undervoltage protection is only achieved using the digital comparator at the VOUTS pin. Depending on the device configuration, the MODE command is used to select the appropriate comparator modes for UV and OV detections.

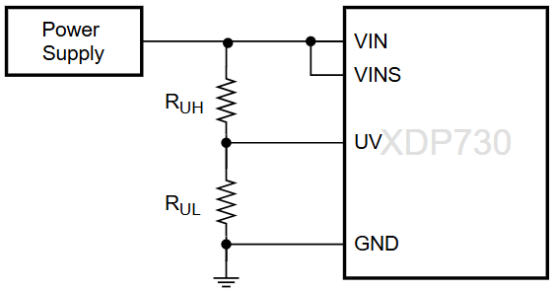


Figure 6 Input undervoltage protection

$$UV(V) = V_{UV\_LTH}(V) \times \frac{R_{UH}(k\Omega) + R_{UL}(k\Omega)}{R_{UL}(k\Omega)} \quad (1)$$

where V_{UV_LTH} is the input undervoltage threshold in Volt and UV is the desired undervoltage limit in Volt.

***Note**: Changing the UV comparator mode on the fly i.e. when the MOSFET is ON, must be avoided.*

2.3.3.2 Overvoltage function

Similar to input undervoltage, the XDP730 has input overvoltage protection for monitoring the maximum input voltage. By default, the input overvoltage is configured to sense the voltage at the VINS pin using a digital comparator. When the VINS voltage rises to/above the digitally programmed limit, the input overvoltage protection (OV) is triggered. If needed, the device can be configured to use an analog comparator at the OV pin for faster response. When the OV pin voltage rises to/above V_{OV_UTH}, the input overvoltage protection is triggered. The equation below can be used to calculate the values of the resistor divider network at the OV pin as shown in Figure 7. At a given time, the input overvoltage can be configured to use either the digital comparator or the analog comparator.

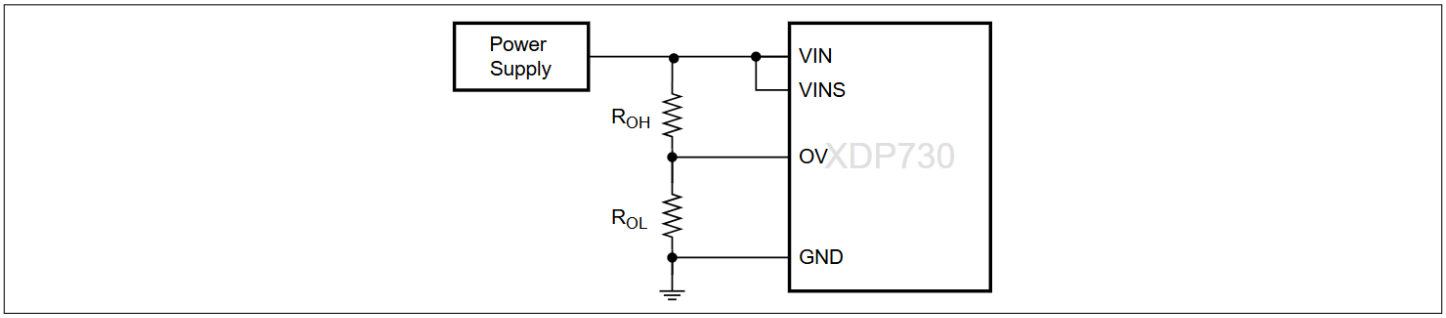


Figure 7 Input overvoltage protection

$$OV(V) = V_{OV\_UTH}(V) \times \frac{R_{OH}(k\Omega) + R_{OL}(k\Omega)}{R_{OL}(k\Omega)} \quad (2)$$

where V_{OV_UTH} is the input overvoltage threshold in Volt and OV is the desired overvoltage limit in Volt.

***Note**: Changing the OV comparator mode on the fly i.e. when the MOSFET is ON, must be avoided.*

In a PRIMARY configured device, there is an additional "backup" on-chip overvoltage (OVIN) limit to protect the device against bad design or OV configuration. It can be programmed to 70 V, 75 V, 80 V or 85 V using the V_SNS_CFG command. By default, the device is configured to have 80 V as the OVIN protection level.

2.4 Inrush current control

The main purpose of an eFuse is to minimize the inrush current during hotswap events, especially in high-availability systems such as servers, data centers, etc. Most eFuses in the market use soft-start, i.e. dvdt method of inrush current control. Although this approach is relatively simple to implement in eFuse, it is not completely safe for the MOSFET. During MOSFET turn-ON, the current can easily go beyond the safe operating area (SOA) limits due to the linear dvdt start-up method, which can damage the MOSFET. Therefore, we at Infineon use our proprietary “Digital SOA control” approach for the inrush current control as shown in Figure 8. This approach keeps the MOSFET in the SOA during the turn-ON procedure and is simple to configure from the user's perspective.

The SOA control loop consists of a closed loop system that senses the input voltage, output voltage and the current flowing through the MOSFET internally. The device calculates the MOSFET’s V_{DS} by subtracting VOUT from VIN i.e. V_{DS} = VIN - VOUT, and regulates the MOSFET’s current according to the SOA/control loop limits. This regulation is achieved by adjusting the MOSFET’s V_{GS}.

For legacy compatibility, there are a few pre-programmed constant SOA data lines (0.25 A, 0.5 A, 1 A, 1.5 A, 2 A) that can be selected using PMBus™ to mimic soft-start/dvdt method for inrush control.

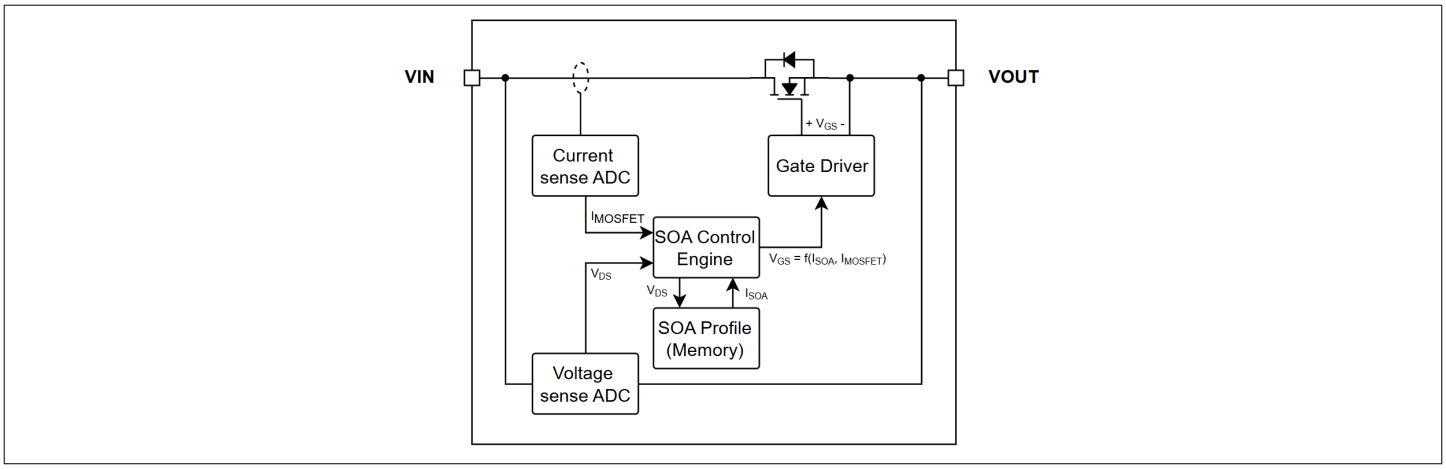


Figure 8 Digital SOA based inrush current control

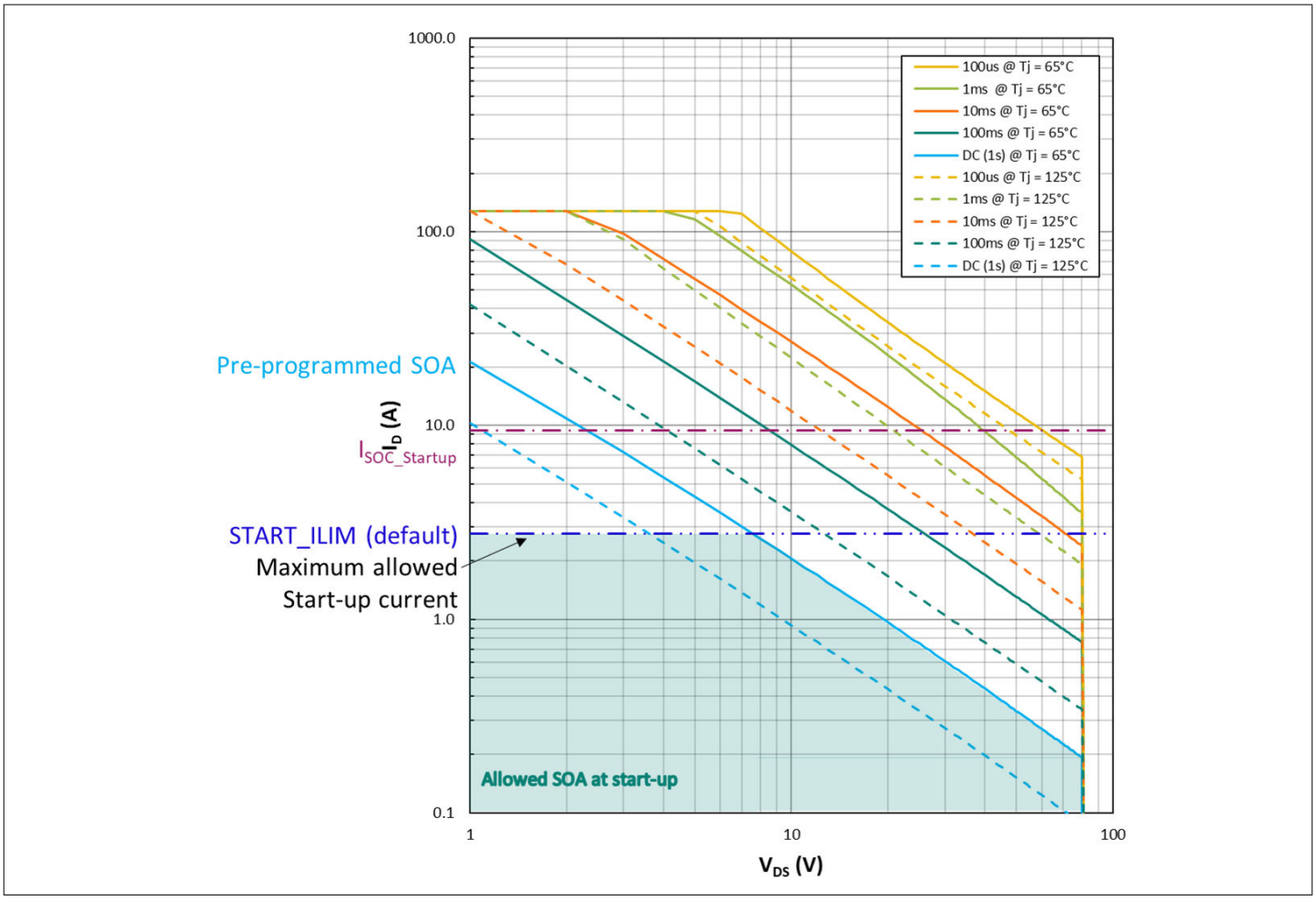


Figure 9 MOSFET's SOA chart

The control loop limits of a device are configured according to three different limits as shown in Figure 9.

- **Programmed MOSFET SOA limit**: The MOSFET's SOA data is pre-programmed into the device. This SOA is normalized to 65°C and 125°C junction temperature to account for systems that is working at higher ambient temperatures. Depending on the MOSFET temperature, the appropriate SOA line is used for inrush control. If the MOSFET temperature is below 105°C then 65°C SOA line is considered else 125°C SOA line is used.

- **Severe overcurrent (SOC) limit**: The severe overcurrent limit ($I_{SOC\_STARTUP}$) also known as short circuit current limit provides a fast response in case the inrush current reaches a critical level.
- **Start-up current (START_ILIM) limit**: The maximum start-up current limit ($I_{START\_ILIM(MAX)}$) is fixed in every eFuse. Using PMBus™ command, the user can adjust this limit as a percentage of the $I_{START\_ILIM(MAX)}$. This configurability allows the user to increase or decrease the MOSFET's turn-on time. The start-up current limit is only considered during inrush control i.e. MOSFET turn-on. It is disregarded as soon as steady state i.e. ON state is reached.

During MOSFET turn-on, the device provides a bias current to turn on the MOSFET in a controlled manner avoiding any SOA violations while ensuring that the system is turned on without any inrush event. The intersection of the previously mentioned three control loop limits define the maximum allowed start-up current.

The Figure 9 shows the MOSFET's SOA with the default control loop limits.

- Blue (solid and dash) lines indicate the pre-programmed SOA limits of the MOSFET.
- Magenta (long dash dot) line indicates the fixed SOC limit during start-up.
- Dark blue (long dash dot dot) line indicates the programmed default start-up current limit i.e. START_ILIM.
- Highlighted area indicates the intersection of all the control loop limits i.e. allowed SOA at start-up.

The SOA is digitally stored as a look-up table with 80 values, corresponding to V_{DS} = 1 V to 80 V. Each entry represents the MOSFET's current allowed for that V_{DS} level and has a resolution of 0.5 A. The following example demonstrates the inrush current control in a typical 54 V input application.

- Before the MOSFET is turned on, there is 54 V at the input and 0 V at the output with respect to ground. As the output capacitor is discharged at the start-up, V_{DS} = 54 V.
- The device starts charging the output capacitor by regulating the MOSFET. As shown in Figure 9, the control loop allows an I_{SOA} = 0.25 A at 54 V.
- As the capacitor charges, the V_{DS} of the MOSFET starts to reduce which allows more current to flow through the MOSFET as per the control loop limits. For example, when V_{DS} reaches 35 V, the allowed MOSFET current is increased to 0.5 A.
- Similarly, when V_{DS} reaches 10 V the allowed MOSFET current will be increased to 2 A.
- Thus, the current increases until the capacitor is charged to the VIN level and the MOSFET is fully enhanced.

This current limitation delays the charging of the output capacitor, significantly reducing the inrush current at start-up while keeping the MOSFET within its SOA limits.

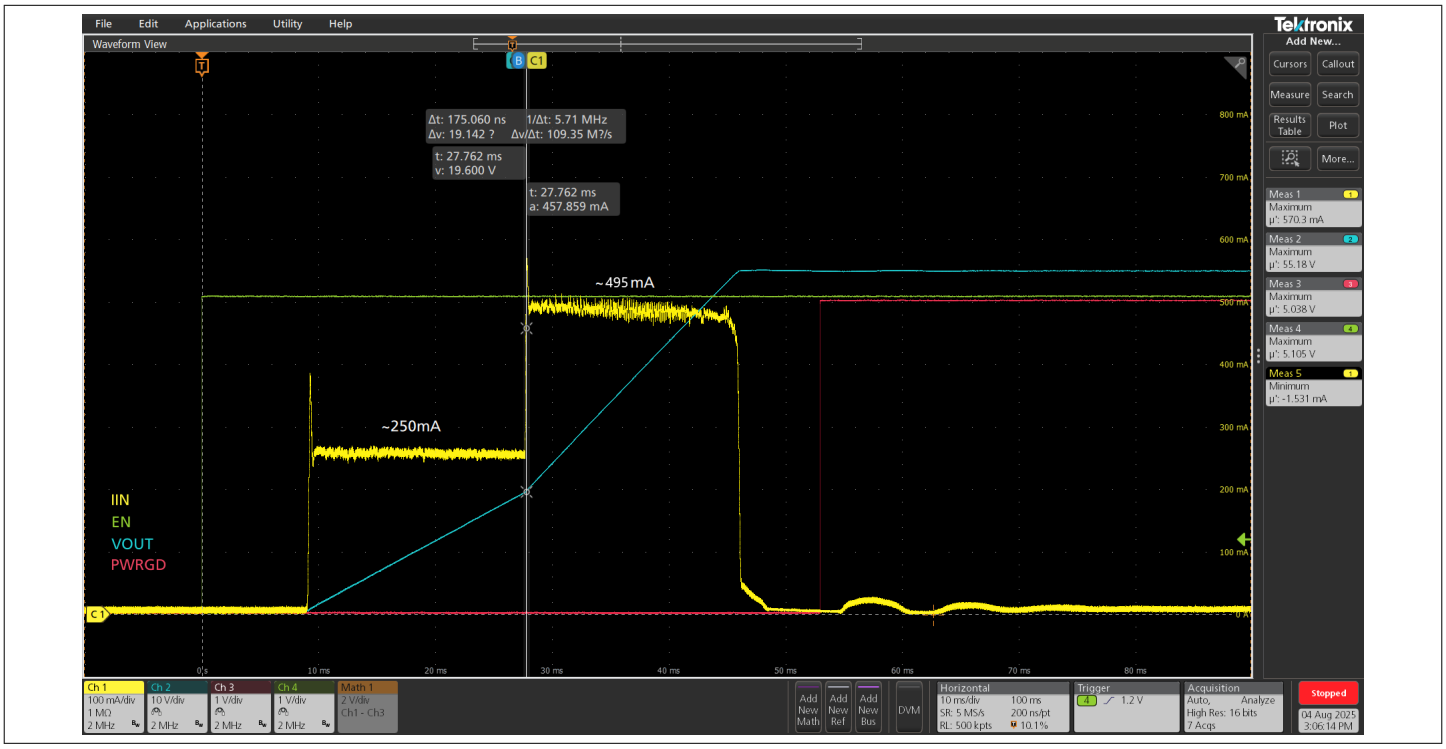


Figure 10 Inrush control with START_ILIM set to 9% of $I_{START\_ILIM(MAX)}$ i.e. ~495 mA; C_{OUT} = 270 µF

2.5 Current limit settings

The XDP730 has multiple current protection levels for maximum flexibility/configurability. This includes a start-up current limit (START_ILIM), two overcurrent limits (SYS_OC_LIMIT and LOCAL_OC_LIMIT) and a severe overcurrent limit (SOC_LIMIT_x).

2.5.1 Start-up current setting

In this device, the start-up current limit is set using dedicated START_ILIM bits in the I_SNS_CFG2 command. This level is active only during MOSFET turn-on i.e. INIT_SOA_REG state. By default, the start-up current limit is configured to be 50% of $I_{START\_ILIM(MAX)}$. The Table 5 below shows the allowed START_ILIM settings.

Table 5 Start-up current limit settings

START_ILIM [2:0]	Description
000	100% of $I_{START\_ILIM(MAX)}$
001	75% of $I_{START\_ILIM(MAX)}$
010	50% of $I_{START\_ILIM(MAX)}$ (default)
011	25% of $I_{START\_ILIM(MAX)}$
100	15% of $I_{START\_ILIM(MAX)}$
101	12.5% of $I_{START\_ILIM(MAX)}$
110	9% of $I_{START\_ILIM(MAX)}$
111	5% of $I_{START\_ILIM(MAX)}$

2.5.2 Overcurrent setting

After a successful start-up, the device enters the ON state and activates the overcurrent (OC) protection along with the continuous current reporting on its IMON pin. The IMON current gain is set digitally using the TELEMETRY_AVG command. By default, the IMON gain is set to 20 µA/A of the current flowing through the MOSFET. There are two overcurrent levels (i.e. system overcurrent and local overcurrent) that can trigger the overcurrent protection in the device.

2.5.2.1 System overcurrent setting

Only in a PRIMARY configured device, the system overcurrent protection is triggered if the IMON pin voltage (V_{IMON}) reaches the reference threshold (V_{SYS_OC}) level set using I_SNS_CFG1:SYS_OC_LIMIT bits. The equation (3) is used to set this limit between 0 V to 1.35 V with ~6.5098 mV resolution step. By default, the SYS_OC_LIMIT = 154dec (i.e. V_{SYS_OC} = 1.0025 V) is programmed in the device.

$$SYS\_OC\_LIMIT(in \quad decimal) = V_{SYS\_OC}(V) \times 153.61445 \tag{3}$$

The IMON resistor required to generate the system overcurrent protection can be calculated using the following equation (4).

$$R_{IMON}(\Omega) = \frac{V_{SYS\_OC}(V)}{G_{IMON}(\mu A/A) \times 10^{-6} \times I_{SYS\_OC}(A)} \tag{4}$$

It is possible to add some deglitch/delay time to the system overcurrent detection. The SOA_TMR:SOAD_TMR command is used to configure the system overcurrent deglitch time between 0 ms and 2000 ms. The device comes pre-programmed with a 2 ms default system overcurrent deglitch time.

***Note**: It is recommended to program the SYS_OC_LIMIT between 40dec (0x28) and 207dec (0xCF) for reliable OC detection.*

2.5.2.2 Local/backup overcurrent setting

There is a local/backup overcurrent limit to protect the device if the system overcurrent protection is not set properly. This local overcurrent limit is configurable from 0 A to 63.5 A with 0.5 A resolution step using I_SNS_CFG1:LOCAL_OC_LIMIT bits. There is a programmable fast deglitch timer to delay the local overcurrent protection from 50 µs to 1 ms. Using the SOA_TMR:LOCAL_OC_TMR bit, it can be selected between the fast deglitch timer (OCD_TMR) or a slow deglitch timer (SOAD_TMR) for the local overcurrent protection. By default, the device is configured to have 200 µs fast deglitch time for a local overcurrent limit of 40 A.

2.5.3 Severe overcurrent setting

During short circuit (i.e. surge or high di/dt current) events, the current flowing through the MOSFET may reach a dangerous level which can critically damage the system load. The device has a fast comparator to protect against such severe overcurrent (SOC) incidents. It can quickly respond by turning off the MOSFET with a strong pull-down current. The complete SOC response time from the moment it is detected till the MOSFET is turned off is t_{SOC_DG}. The SOC protection level is digitally programmable using I_SNS_CFG2:SOC_LIMIT_x bits, from 0 A to 126 A with a 2 A resolution step. It is possible to have different SOC level settings based on the device configuration. There is also an analog deglitch timer that can be configured to delay the SOC detection. This timer is programmed (0 ns, 200 ns, 500 ns, 1000 ns) using SOA_TMR command. By default, the device is pre-programmed to have 80 A (for PRIMARY) / 88 V (for SECONDARY) SOC level and 0 ns deglitch time.

The SOC level during the start-up procedure is fixed to $I_{SOC\_STARTUP}$.

2.6 Power good (PWRGD)

A power good (PWRGD) pin is available in this device which can be used as a flag or to control the system load. It is asserted i.e. pulled high when the device enters the ON state to indicate that the MOSFET is fully enhanced (V_{GS} > 7.8 V and V_{DS} < 1.0 V) and there are no fault conditions. When a fault is triggered or RESTART is issued, the MOSFET is turned off and this pin is de-asserted i.e. pulled low. It will also be de-asserted if the MOSFET turn on conditions, shown in Table 4 are not met. There are two separate digitally programmable deglitch timers associated with this pin. They help to delay the PWRGD pin assertion and de-assertion respectively. Using the PWRGD_DG_TMR command, these timers can be individually programmed from 0 ms to 15 ms. By default, the device is pre-programmed to have a 5 ms deglitch time for PWRGD pin assertion and 0 ms for de-assertion.

***Note**: The PWRGD pin remains asserted when the surge immunity feature is enabled and activated, regardless of the V_{GS} voltage level.*

2.7 Thermal protection

Thermal protection is an important feature in any eFuse as it indicates and protects the device (and system load) against thermal instability. The device has two levels of thermal protection thanks to the dedicated temperature sensors in the MOSFET and controller. In this device, the "TEMPERATURE_1" refers to the internal MOSFET temperature and "TEMPERATURE_2" refers to the on-chip controller temperature. The MOSFET overtemperature protection level is digitally programmable using the OT_FAULT_LIMIT command. Additionally, the ONCHIP_TSD_FAULT_LIMIT command is used for configuring the controller's thermal shutdown protection level.

By default, the device is programmed to ~166.5°C and 145°C for MOSFET overtemperature and controller thermal shutdown level respectively.

2.8 Restart

The user may want to "reset" the device anytime during steady state operation i.e. MOSFET is ON. This can be done by issuing a RESTART PMBus™ command. If this feature is triggered, the MOSFET will turn off, thus removing power from the output. Also, a user-configurable RESTART_TMR is started immediately. The device will transition to the STANDBY

state after RESTART_TMR has expired. If all the necessary conditions shown in Table 4 are met, then the MOSFET automatically turns back on. The RESTART_TMR is configured digitally using the RETRY command.

Depending on the GPO2 pin configuration, the RESTART can also be triggered using the GPO2 i.e. RESTARTN pin (falling edge triggered). By default, the GPO2 pin is configured as RESTARTN pin and the RESTART_TMR is set to 9.28 s.

***Note**: The OTP memory must not be programmed when the RESTART_TMR is running.*

2.9 MOSFET power down

The MOSFET turn-off can be triggered automatically due to a fault or manually by the user (EN or RESTART or OPERATION:ON bit). The MOSFET is generally turned off using I_{GATE_SPD} pull-down current except for OVIN and SOC fault events. Since OVIN and SOC events are critical for the device and the system load, a strong/fast pull-down current I_{GATE_FPD} is used for turning off the MOSFET immediately to avoid V_{DS} overshoots. The I_{GATE_SPD} pull-down current is digitally configurable using the TURN_OFF_CTRL command. By default, the device is configured to turn off the MOSFET with 1250 µA slow pull-down current and 1 A fast pull-down current.

2.10 Quick output discharge

The device has an output discharge feature to quickly discharge the output capacitor (C_{OUT}) at the VOUT pin using an internal current source I_{QOD} to GND. This helps to quickly remove the residual charge left on the C_{OUT}. The QOD feature is enabled/disabled using the MODE command. If enabled, it is activated when the user turns off the MOSFET using the EN, RESTART or OPERATION command. A fixed deglitch timer t_{QOD} is started when the MOSFET is turned off. The current source I_{QOD} is activated only after the deglitch timer has expired. The output discharge is automatically deactivated after $t_{QOD\_Discharge}$ time has elapsed. It can be immediately deactivated if any of the following conditions exist.

- MOSFET is turned ON i.e. the device transitions to INIT_SOA_REG state
- VOUT < 2 V
- Fault condition occurred

This feature can elevate the device temperature due to the increased power dissipation from the internal current source. Therefore, the QOD is disabled if the thermal protections are triggered. By default, the device comes with QOD disabled.

2.11 General purpose pins

This device has three general purpose input/output pins to cover multiple functionalities. These include GPO0, GPO1 and GPO2 pins that can be configured using GPO_CFG command. The different functionalities of these pins are shown in Table 6, Table 7 and Table 8 respectively.

Table 6 GPO0 pin configuration

GPO_CFG:GPO0_CFG	Description
00	Pin is configured as active low FAULT (default)
01	Pin reflects GPO0_ST status
10	RESERVED
11	Pin is configured as active low SMBALERT, reporting depends on the GPO_CFG:SMBALERT setting

Table 7 GPO1 pin configuration

GPO_CFG:GPO1_CFG	Description
00	Pin is configured as active low WARN (default)

(table continues...)

Table 7 (continued) GPO1 pin configuration

GPO_CFG:GPO1_CFG	Description
01	Pin reflects GPO1_ST status
10	RESERVED
11	RESERVED

Table 8 GPO2 pin configuration

GPO_CFG:GPO2_CFG	Description
00	Pin is configured as functional
01	Pin is configured for UV throttle function
10	RESERVED
11	Pin is configured as RESTARTN input with pull-up resistor (default)

Depending on the GPO0 and SMBALERT configuration, the SMBALERT pin can be configured to provide an overview of all the enabled warnings, faults or both. The SMBALERT pin can only be released/unlatched by following the Alert Response Address protocol in Chapter 2.14.2.1.

By default, the device is configured to have FAULT functionality, WARN functionality and RESTARTN functionality on GPO0, GPO1 and GPO2 pins respectively.

2.12 Protections

2.12.1 Faults

This device incorporates many protections that ensure safe operation of the device and system load in different scenarios. Depending on the device configuration shown in Table 3, this device can address up to 15 different faults. Using the ENABLE_FAULTS command, the user can individually enable/disable each fault protection. There is a dedicated MASK_FAULTS command to mask/unmask the reporting of each fault on the FAULT pin. A fault can be enabled with or without reporting on the FAULT pin but the reverse is not possible. The FAULT pin will be pulled low and the MOSFET is turned off when a fault is triggered. The FAULT pin remains low for a minimum of t_{FAULT_MIN} regardless of the duration of the actual fault condition. This ensures that the system microcontroller can properly detect the FAULT pin reporting. The status of the faults being triggered is checked using the STATUS_FAULTS command. Masking a fault will only affect the FAULT pin but not its status bit. Therefore, it is highly recommended to unmask a particular fault at the same time when it is enabled. Depending on the fault type, the FAULT pin is released either after the fault condition is removed or when the fault status bit is cleared. The fault status bits will remain set until they are cleared:

- using CLEAR_FAULTS command
- or, toggling EN pin HIGH-to-LOW
- or, by a power cycle

To service the faults properly, the CLEAR_FAULTS command and EN pin toggling are ignored until fault processing has finished. There are priorities assigned to each fault. If a high-priority fault is triggered while processing a lower-priority fault, then the device will immediately start processing the higher-priority fault. The device will resume the lower-priority fault process only after the high-priority fault serving is finished. If multiple faults with the same priority are triggered at the same time, then the device will act on a first-come-first-serve basis. The GPO0 pin can be configured to operate as an active low SMBALERT pin. Depending on the SMBALERT configuration, the faults can be programmed to latch this pin.

***Note**:*
- *FAULT pin is asserted low until the fault condition is removed. It also depends on the retry settings for retry-based faults.*
- *SMBALERT pin is latched low when a fault and/or warning has occurred. This pin can only be released/ unlatched by following the Alert Response Address protocol (Chapter 2.14.2.1).*

Table 9 provides an overview of when a fault's detection and processing is active.

Table 9 Faults overview table

Fault name and priority*1	State of the device											Fault availability*2
	POR_INIT	READ_CFG	CHK_FET	STAND BY	INIT_SOA_REG	ON	SURGE	GREC	FAULT	WAIT	MEM_FAULT/ LATCH_OFF	
MEM (1)	-	X	X	X	X	X	X	X	X	X	X	P/S
SGD (2)	-	-	X	X	-	-	-	-	X	-	-	P/S
SGS (2)	-	-	-	-	X*3	-	-	-	-	-	-	P/S
UR (2)	-	-	-	-	-	-	-	-	X*4	-	-	P
SOC (3)	-	-	-	-	X	X*5	-	X	X	-	-	P/S
VDS (4)	-	-	-	X*6	-	-	-	-	-	-	-	P
OT (4)	-	-	-	X	X	X	-	X	-	-	-	P/S
TSD (4)	-	-	-	X	X	X	-	X	-	-	-	P/S
OVIN (5)	-	-	-	X	X	X	-	X	X	-	-	P
OV (6)	-	-	-	X	X	X	-	X	X	-	-	P/S
UV (7)	-	-	-	X	X	X	-	X	X	-	-	P/S
OUV (8)	-	-	-	-	-	X	-	X	-	-	-	P
WD (9)	-	-	-	-	X	-	-	X	-	-	-	P/S
OC (9)	-	-	-	-	-	X	-	-	-	-	-	P/S
SYNC (10)	-	-	-	X	X	X	-	X	-	-	-	P/S

Attention**:* ****1): Fault priority level decreases as we go down the table.
****2): Indicates the device configuration, P = PRIMARY and S = SECONDARY.***
****3): Right at the point when the watchdog timer expires.***
****4): It can only occur in the FAULT state when the retry counter expires after any of the retry fault events (SOC, OT, TSD, OUV, WD, OC, SYNC).***
****5): If RETRY:SRG_PROT_EN bit is set to '0' (surge protection is disabled).***
****6): Detection is active after POR or the RESTART event.***

2.12.1.1 Memory fault

OTP Memory (MEM) Fault

During device power-up i.e. in READ_CFG state, if an OTP (i.e. pre-configuration) read or write error is detected then a MEM fault is triggered in the device. As a result, the device turns off its MOSFET and gets latched off by entering the MEM_FAULT state: This fault can be cleared only through a device power cycle i.e. the device will restart from the POR_INIT state. This fault is reported only in the STATUS_BYTE and STATUS_WORD commands.

2.12.1.2 Damaged MOSFET faults

This device comes with three internal MOSFET checks to mainly determine if there are any shorted pins. To ensure that the MOSFET is not damaged, it is recommended to have the shorted MOSFET pin faults enabled and unmasked.

Shorted MOSFET Gate-Drain (SGD) fault

This fault checks if the Gate and Drain pins of the MOSFET are shorted. It is triggered if:

- In the CHK_FET state after $t_{SGD\_FLT\_DG}$ expires, the MOSFET's V_{GS} goes above 1 V.
- Or, after the device enters the FAULT or STANDBY state and activates any gate pull-down, the MOSFET's V_{GS} does not go below 1 V within $t_{FLT\_PD\_GATE}$.

When this fault is triggered, the device will turn off its MOSFET and get latched off. The fault is released only through the latch-off release procedure.

Shorted MOSFET Gate-Source (SGS) fault

If for some reason, the MOSFET is not able to turn on within the programmed watchdog time and its V_{GS} is below 1 V then the SGS fault will be issued. When this fault is triggered, the device will turn off its MOSFET and get latched off. The fault is released only through the latch-off release procedure.

***Note**: The watchdog timer setting from the WATCHDOG_TMR command is used for this fault even if the WD fault is disabled. If a specific timer value is desired to delay the SGS detection then the watchdog timer must be configured accordingly.*

Pre-charged output voltage (VDS) fault

This fault can be enabled only in a PRIMARY configured device as shown in Table 9. It is detected during the device power-up after the enable deglitch timer (EN_DG) has expired for the first time. The V_{DS} level of the MOSFET is measured digitally using the VINS and VOUTS pins i.e. V_{DS} = VIN - VOUT. Using the V_SNS_CFG command, the VDS fault level can be programmed. This fault is released if the V_{DS} voltage of the MOSFET exceeds the programmed fault level or the output voltage is lower than 2 V.

If this fault is enabled, it is recommended that the EN_DG timer is set to a non-zero value so that the supply voltage is stable when VDS fault is checked.

2.12.1.3 Voltage faults

System input undervoltage (UV) fault

As mentioned in Chapter 2.3, the input voltage sensing can be configured to use digital or analog comparators. If the digital comparator is selected then the UV fault is triggered when the VINS pin voltage drops to/below the programmed fault level i.e. VIN_UV_FAULT_LIMIT or VIN_UV_FAULT_LIMIT_S. Alternatively, if the analog comparator is selected then the fault is triggered when the UV pin voltage drops to/below V_{UV_LTH}. In both cases, the UV fault detection can be delayed by programming the appropriate UV_TMR value using the V_TMR command.

This fault is released when the sensed voltage rises to/above the fault level plus UV hysteresis or V_{UV_UTH} level for digital and analog comparators respectively. Based on device configuration, the V_SNS_CFG or VIN_UV_FAULT_LIMIT_S command is used to set the UV hysteresis level.

To avoid any false triggering of the UV fault during device power-up, the UV detection starts only after the fault level (analog or digital) is crossed and the EN_DG timer has expired for the first time.

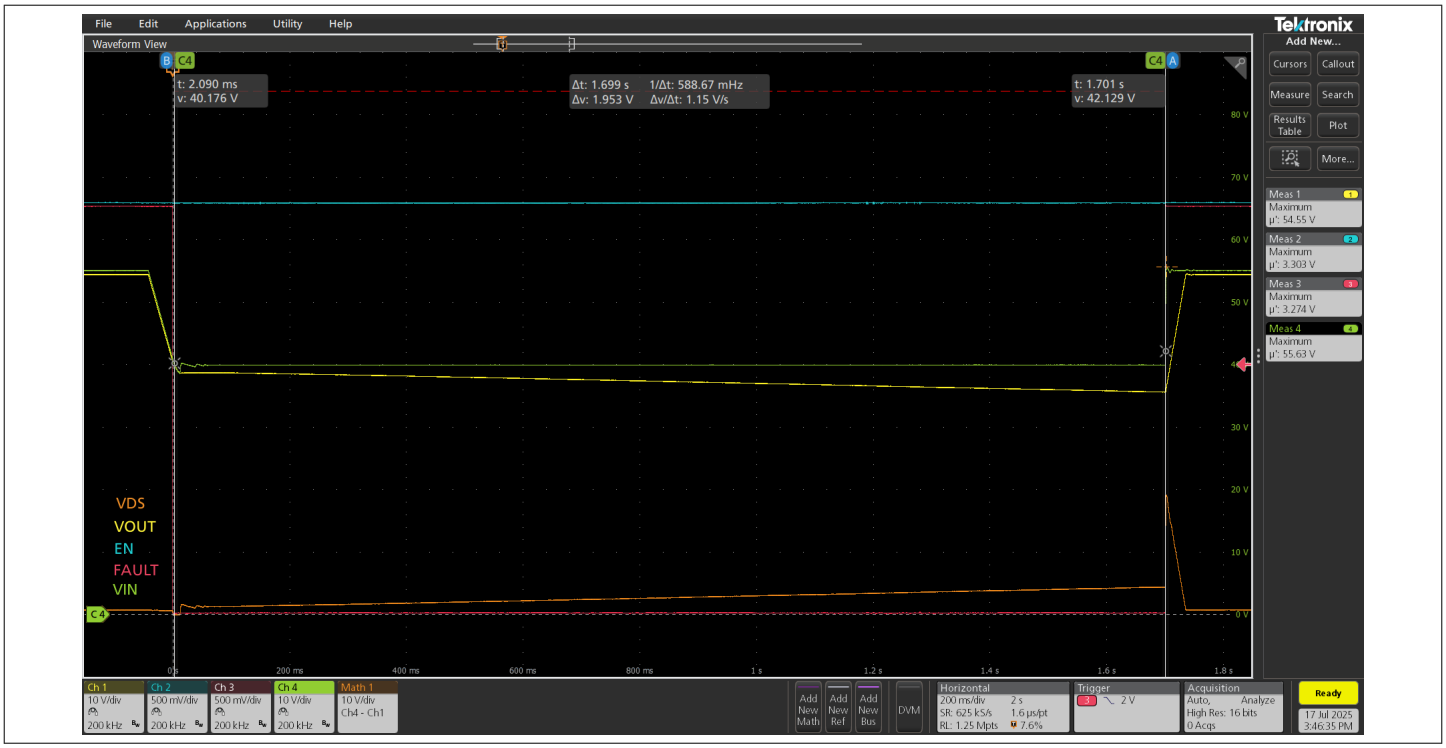


Figure 11 Input UV fault (VIN_UV_FAULT_LIMIT = 40 V) being triggered followed by a successful fault release

System input overvoltage (OV) fault

If the digital comparator is selected, then the OV fault is triggered when the VINS pin voltage rises to/above the programmed fault level i.e. VIN_OV_FAULT_LIMIT or VIN_OV_FAULT_LIMIT_S. Alternatively, if the analog comparator is selected then the OV fault is triggered when the OV pin voltage raises to/above V_{OV_UTH}. In both cases, the OV fault detection can be delayed by programming the appropriate OV_TMR value using the V_TMR command.

This fault is released when the sensed voltage drops to/below the fault level minus OV hysteresis or V_{OV_LTH} level for digital and analog comparators respectively. Based on the device configuration, the V_SNS_CFG or VIN_OV_FAULT_LIMIT_S command is used to set the OV hysteresis level.

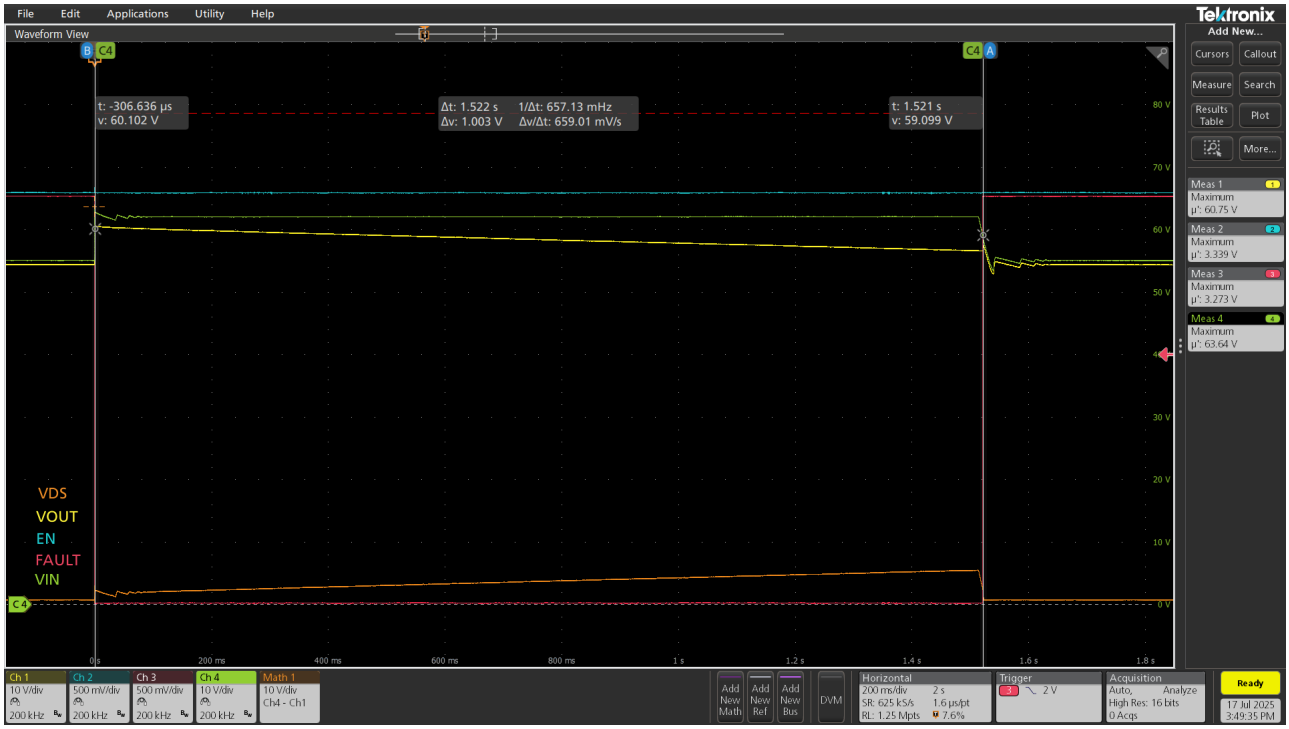


Figure 12 Input OV fault (VIN_OV_FAULT_LIMIT = 60 V) being triggered followed by a successful fault release

On-chip input overvoltage (OVIN) fault

This fault acts as a backup to the OV fault and it can be enabled only in a PRIMARY configured device as shown in Table 9. If the VINS pin voltage rises to/above the OVIN_FAULT_LIMIT set using the V_SNS_CFG command, the OVIN_TMR is initiated which is configured using the V_TMR command. When it expires, the OVIN fault is triggered and the MOSFET is immediately turned off with a strong/fast pull-down current. This fault is released when the input voltage drops to/below the OVIN_FAULT_LIMIT minus V_{OVIN_HYS}.

Output undervoltage (OUV) fault

This fault can be enabled only in a PRIMARY configured device as shown in Table 9. If the output voltage sensed at the VOUTS pin drops to/below the OUV fault level set using the VOUT_UV_FAULT_LIMIT command, the OUV_TMR timer set using the V_TMR command is initiated. If the output voltage raises to/above the fault level plus 2.06 V fixed hysteresis before this timer expires then the system continues normal operation otherwise the OUV fault is triggered and the MOSFET is turned off with a regular pull-down. The device will follow the retry settings.

It is recommended to set the OUV fault level below the UV fault limit as it can send the device into the LATCH_OFF state based on the retry settings. If both of them are set to the same level or if the OUV is set to a level above UV, the device will be sent to the LATCH_OFF state, instead of FAULT due to UV. Thus, requiring the latch-off release process to free the device.

2.12.1.4 Current faults

Overcurrent (OC) fault

As mentioned in Chapter 2.5, the OC condition can be detected in two ways through system OC and local OC.

In a PRIMARY configured device, when the IMON pin voltage reaches the programmed fault reference threshold level set using the I_SNS_CFG1 command, the SOAD_TMR deglitch timer programmed using the SOA_TMR command is initiated. If the V_{IMON} drops below the fault level minute hysteresis (10% of fault level) before this timer expires, then the device continues normal operation otherwise the OC fault is triggered.

Alternatively, when the current through the MOSFET rises to/above the programmed current level set using the I_SNS_CFG1 command, the deglitch timer (SOAD_TMR or OCD_TMR) configured using the SOA_TMR command is initiated. If the current through the MOSFET drops below the fault level before this timer expires, the device continues normal operation otherwise the OC fault is triggered.

When the OC fault is triggered, the MOSFET is turned off with a regular pull-down and the device will follow the retry settings.

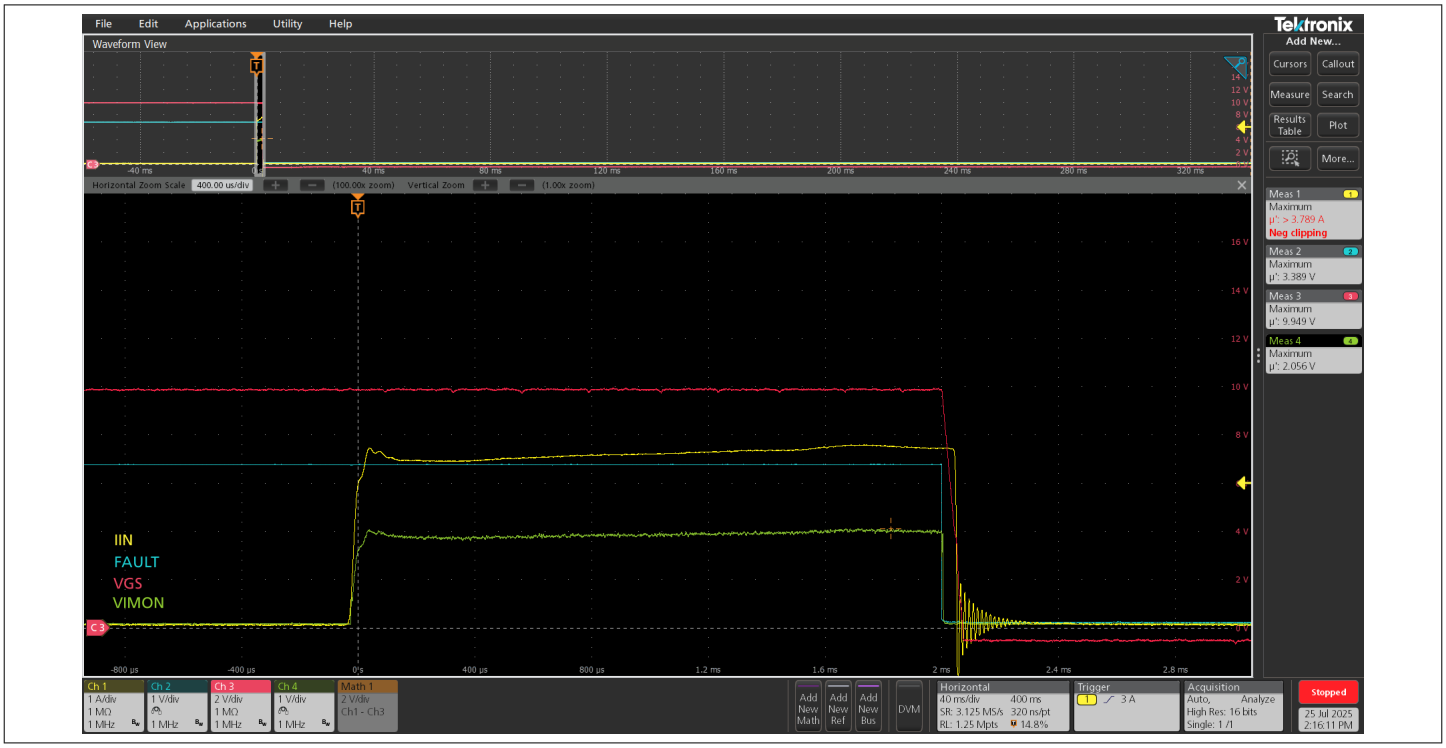


Figure 13 Overcurrent fault (V_{IMON} > 1.0025 V) being triggered after 2 ms deglitch time; R_{IMON} = 27.5 kΩ

Severe overcurrent (SOC) fault

When the current flowing through the MOSFET rises to/above the programmed SOC level set using the I_SNS_CFG2 command, the SOC_DG_TMR deglitch timer configured using the SOA_TMR command is initiated. If the current through the MOSFET drops below the fault level before this timer expires, the device continues normal operation otherwise the SOC fault is triggered.

Since it is a critical fault, the MOSFET is turned off immediately with a strong/fast pull-down when the SOC fault is triggered and the device will follow the retry settings.

***Note**: During MOSFET turn-on i.e. in INIT_SOA_REG state, the SOC level is fixed to $I_{SOC\_STARTUP}$*

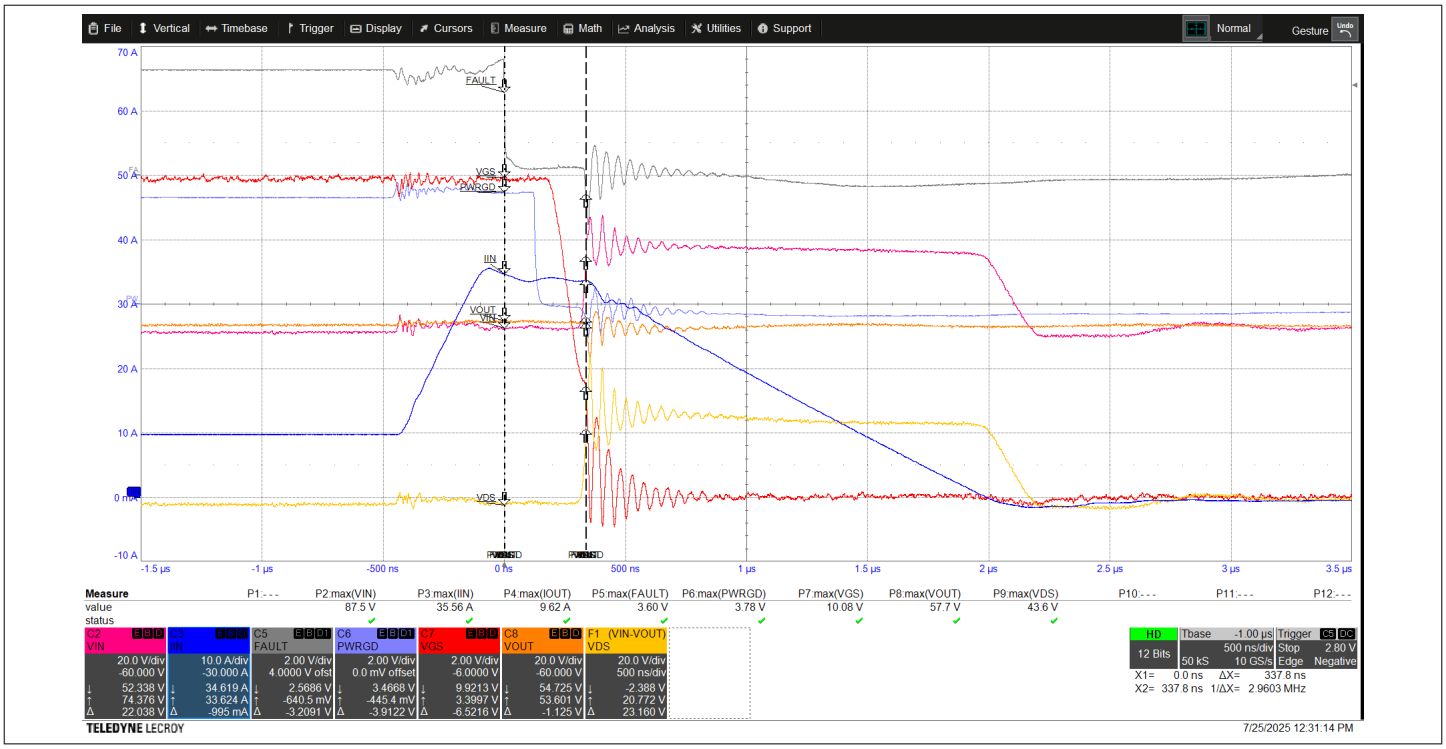


Figure 14 **Severe overcurrent fault (SOC_LIMIT_P = ~30 A) being triggered followed by a fast MOSFET turn-off within ~400 ns**

2.12.1.5 Thermal faults

MOSFET overtemperature (OT) fault

This fault depends on the temperature sensed inside the MOSFET. If the MOSFET's temperature rises to/above the fault level programmed using the OT_FAULT_LIMIT command, the OT fault is triggered. As a result, the MOSFET is turned off with a regular pull-down current. The device waits until the MOSFET is completely turned off and its temperature drops below the programmed fault level minus hysteresis (T_{OT_HYS}). After this waiting period, the device will follow the retry settings.

Controller thermal shutdown (TSD) fault

The TSD fault relies on the temperature sensed inside the controller. If the controller's temperature rises to/above the fault level programmed using the ONCHIP_TSD_FAULT_LIMIT command, the TSD fault is triggered. As a result, the MOSFET is turned off with a regular pull-down current. The device waits until the MOSFET is completely turned off and the controller's temperature drops below the programmed fault level minus hysteresis (T_{TSD_HYS}). After this waiting period, the device will follow the retry settings.

2.12.1.6 Power-up faults

Unsuccessful MOSFET start-up, i.e. watchdog (WD) fault

The timer required for triggering the WD fault is programmed using the WATCHDOG_TMR command. As soon as the MOSFET turn-on procedure is initiated i.e. in the INIT_SOA_REG state, this timer is started. If the MOSFET is not fully enhanced (i.e. V_{DS} < 1 V and V_{GS} > 7.8 V) before the timer expires, the WD fault is triggered. The device will follow the retry settings after the MOSFET is turned off with a regular/slow pull-down current.

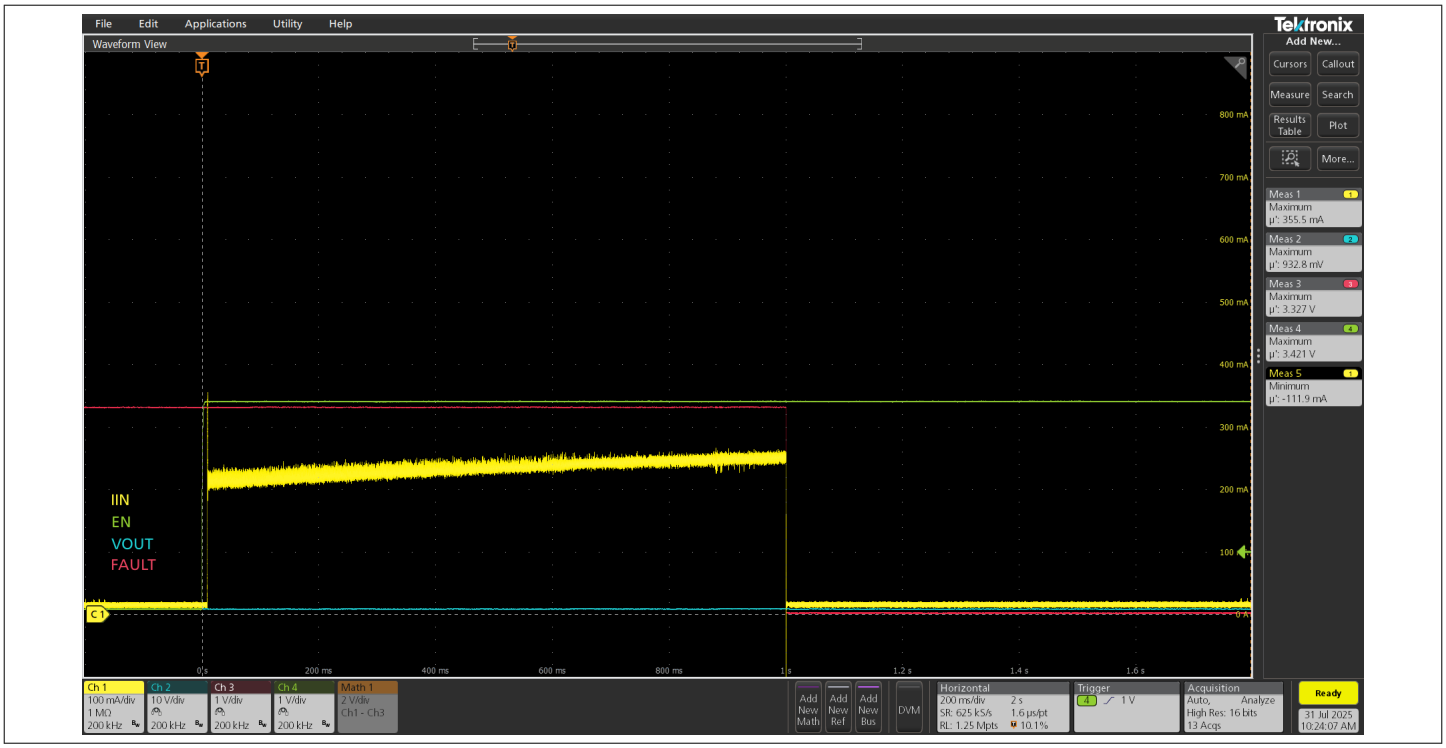


Figure 15 Start-up into short protection triggers watchdog (WD) fault after 1 s

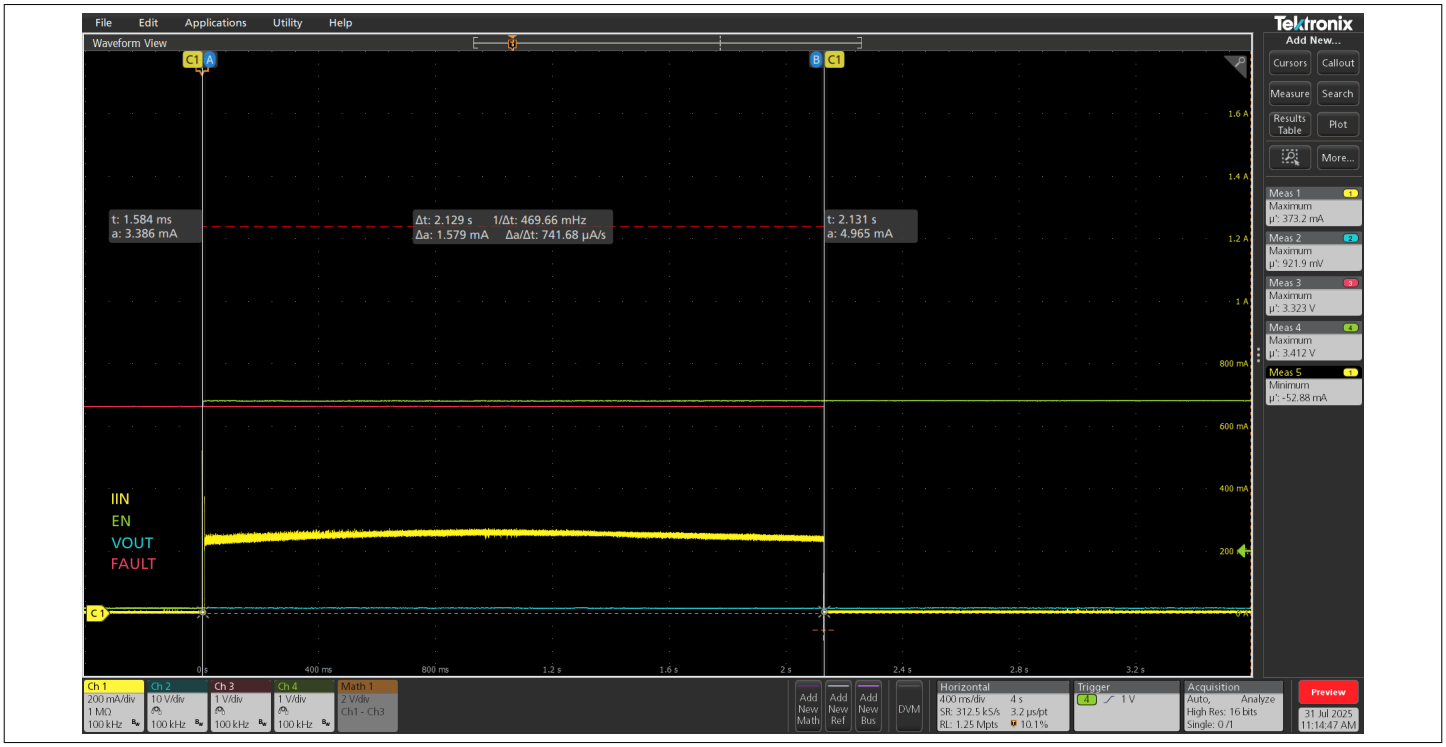


Figure 16 Start-up into short protection triggers thermal shutdown fault (TSD) after ~2.12 s; WD fault is either disabled or programmed to a higher value i.e. > 2 s

Unsuccessful retry (UR) fault

This fault can be enabled only in a PRIMARY configured device as shown in Table 9. The retry counter is programmed using the RETRY command. It decrements on each retry attempt after one of the retry faults is triggered (SOC, OT, TSD, OUV, WD, OC, SYNC). The UR fault is detected when the programmed retry counter expires i.e. maximum number

of programmed retries has been reached. As a result, the device keeps its MOSFET turned off and enters the LATCH-OFF state.

2.12.1.7 Internal protection fault

SYNC Fault

This fault is used to synchronize all the devices in a high-power system. The SYNC fault is triggered in the device if:

- Failsafe check is unsuccessful i.e. $V_{FS} < V_{FS\_TH}$
- Or, the SYNC pin is externally pulled LOW

The device will turn off its MOSFET with a regular pull-down and follow the retry settings. It is highly recommended to keep this fault always enabled and unmasked.

***Note**: Disabling this fault in the PRIMARY device is deemed as a bad design practice that will result in a system-level latch-off due to the SECONDARY device's unsuccessful SYNC handshaking.*

VREG fault

If, at any point in time, the VREG pin voltage goes below 4.1 V then the device will trigger an automatic power-on reset which resets the volatile memory. This fault is not reported to the user.

2.12.2 Fault response

This device has a configurable fault response for SOC, OT, TSD, OUV, WD, OC and SYNC faults. Using the RETRY command, the device can be programmed to attempt an auto-retry or directly latch off when any of these faults are triggered. The fault response for the remaining faults is already mentioned in Chapter 2.12.1. It must be noted that the auto-retry function is only possible in a PRIMARY configured device. The SECONDARY device will simply follow the PRIMARY device with the help of its SYNC pin connection.

2.12.2.1 Auto-retry

There are three main parameters in the RETRY command i.e. retry counter, retry OK deglitch timer, and cool-down timer. If the retry counter is set to a non-zero value, the device will attempt auto-retry to turn-on the MOSFET, if the other conditions are met. The number of retries can be programmed from 1 to 32 using RETRY:RETRY_COUNTER bits. If the retry counter is set to "0" then the device latches off without any retry. The retry counter can also be disabled, which means the device will keep retrying an infinite number of times until it is turned off or reset. Before every retry attempt, the device will wait for a cool-down period configured using RETRY:COOLD_TMR bits. During this period, the device remains in the FAULT state by ignoring the fault release prompts such as the CLEAR_FAULTS command and EN pin toggling. After the cool-down has expired, the device will attempt to turn-on the MOSFET if all the other turn-on conditions shown in Table 4 are met and no fault conditions exist.

If a successful MOSFET turn-on is achieved during a retry attempt, the retry OK deglitch timer programmed using the RETRY:RETD_TMR bits will be initiated when the ON state is reached. The retry counter will be set to its initial state if no fault has occurred during this time. If the maximum number of retries is reached without success then the UR fault is issued.

***Note**: Setting RETD_TMR = 0 disables the reset of the retry counter.*

2.12.2.2 Latch-off

Depending on the type of latch-off fault, the device will eventually enter the LATCH_OFF or MEM_FAULT states. In these states, the device will continue to:

- keep its MOSFET turned off
- latch the state of all the status commands (except for the STATUS_CML command to support COMM warning reporting in these states)
- latch the state of status pins (i.e. PWRGD, FAULT/SMBALERT, WARN)
- keep service blocks (including VREG), telemetry, communication PMBus interface and necessary digital core running to support data communication

The following faults immediately trigger device latch-off:

- OTP memory (MEM) fault
- Shorted MOSFET gate-drain (SGD) fault
- Shorted MOSFET gate-source (SGS) fault

The following faults will immediately trigger the device latch-off if the retry counter is set to "0":

- Severe overcurrent (SOC) fault
- MOSFET overtemperature (OT) fault
- Controller thermal shutdown (TSD) fault
- Output undervoltage (OUV) fault
- Watchdog (WD) fault
- Overcurrent (OC) fault
- SYNC fault

The UR fault results in device latch-off when the number of retries expires.

2.12.2.2.1 Latch-off release

The device will come out of the LATCH_OFF or MEM_FAULT states if a power cycle is issued which starts the device operation from the POR_INIT state.

Alternatively, the device can come out of the LATCH_OFF (not applicable to MEM_FAULT) state using:

- CLEAR_FAULTS command
- Or, EN pin toggling (HIGH-to-LOW transition)
- Or, power cycling

If either of these methods is used, the device will:

- de-assert/release the status pins (i.e. PWRGD, FAULT/SMBALERT, WARN)
- clear the FAULT and WARNING status commands
- continue operation from the CHK_FET state

2.12.3 Input surge immunity

The surge immunity feature protects the system load against short surge pulses. The device will turn off its MOSFET when a surge event is detected and then turn it back on if the surge is gone. This feature reuses the severe overcurrent (SOC) fault comparator with its deglitch timer to detect the current glitches induced by input voltage surges. When this feature is enabled using the RETRY command, the device follows the surge immunity protection procedure by going into the SURGE state followed by GREC state. The PWRGD, SYNC and FAULT pins remain unchanged along with the STATUS_FAULTS command.

SURGE state: The MOSFET is turned off with a strong pull-down (I_{GATE_FPD}) and then the device waits for a certain time before it goes into the GREC state.

GREC state: The device activates the gate pull-up of the MOSFET to bring it above the V_{GS} threshold level. The output capacitor continues to be charged until the MOSFET gets fully enhanced. If SOC conditions are still present in this state, SOC fault is triggered. The device stays in the GREC state for a minimum of 500 ns to safeguard the transition between different SOC threshold levels, avoiding false SOC fault triggers.

For MOSFET protection during recovery, the recovery watchdog timer can be configured from 1 ms to 100 ms or the same as the general watchdog timer using the WATCHDOG_TMR command. This timer starts running at the beginning of the GREC state i.e., recovery phase. If the recovery is not successful before the timer expires, the device issues a watchdog (WD) fault. The device will exit the surge immunity procedure if the turn-on conditions shown in Table 4 are removed, RESTART is issued or a fault is detected in GREC state.

Both the SOC fault and the surge protection feature has to be enabled for the device to follow the surge protection procedure. If surge protection is disabled and the SOC fault is enabled then the SOC fault procedure is followed normally.

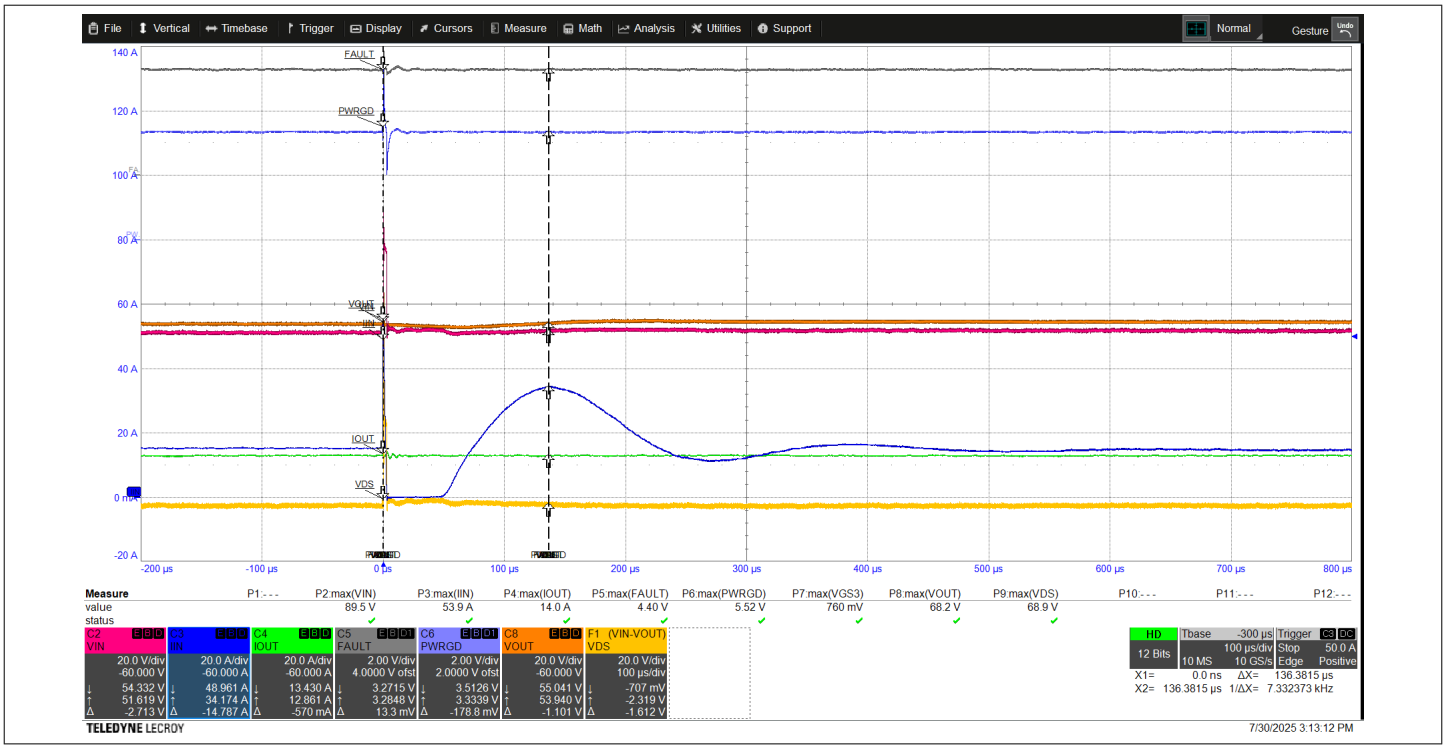


Figure 17 Input surge immunity protection triggers a fast MOSFET turn-off (SOC_LIMIT_P = 50 A) followed by a successful recovery; C_{OUT} = 1 mF

2.12.4 Warnings

Warnings are defined as simple alerts that do not control the MOSFET but can be used by the system microcontroller to decide if any action is needed. Using the ENABLE_WARNS command, the user can individually enable/disable 11 different warnings. There is a dedicated MASK_WARNS command to mask/unmask the reporting of each warning on the WARN pin. Similar to faults, each warning can be enabled with or without reporting on the WARN pin but the reverse is not possible. The WARN pin will be pulled low when a warning level is triggered without affecting any other pins. The status of the warnings being triggered is checked using the STATUS_WARNS command. Masking a warning will only affect the WARN pin but not its status bit. The WARN pin is released either after the warning condition is removed or when the warning status bit is cleared. The warning status bits will remain set until they are cleared:

- using CLEAR_FAULTS command
- or, toggling EN pin HIGH-to-LOW
- or, by a power cycle

***Note**: Due to the nature of the COMM warning, there are some exceptions to the way it is reported on the WARN pin and cleared. Refer Chapter 2.12.4.6 for more details.*

Table 10 provides an overview of when a warning's detection and processing is active.

Table 10 Warnings overview table

Warning name	State of the device										
	POR _INIT	READ _CFG	CHK _FET	STAND BY	INIT _SOA _REG	ON	SURGE	GREC	FAULT	WAIT	MEM_ FAULT/ LATCH _OFF
VGSL	-	-	-	-	-	X	-	-	-	-	-

(table continues...)

Table 10 (continued) Warnings overview table

Warning name	State of the device										
	POR_INIT	READ_CFG	CHK_FET	STAND BY	INIT_SOA_REG	ON	SURGE	GREC	FAULT	WAIT	MEM_FAULT/ LATCH_OFF
OT	-	-	-	X	X	X	X	X	X	-	-
TSD	-	-	-	X	X	X	X	X	X	-	-
UV	-	-	-	X	X	X	X	X	X	-	-
OV	-	-	-	X	X	X	X	X	X	-	-
OUV	-	-	-	-	-	X	X	X	-	-	-
OOV	-	-	-	X	X	X	X	X	X	-	-
OUC	-	-	-	-	-	X	-	-	-	-	-
OOC	-	-	-	X	X	X	X	X	-	-	-
OP	-	-	-	X	X	X	X	X	-	-	-
COMM	-	-	X	X	X	X	X	X	X	X	X

2.12.4.1 Damaged MOSFET warning

Gate-Source low voltage (VGSL) warning

If the V_{GS} of the MOSFET goes below 7.8 V, the VGSL warning is triggered indicating that there might be gate-source or gate-drain issues over the lifetime. This warning is cleared as soon as the MOSFET's V_{GS} voltage rises above the same warning level.

2.12.4.2 Voltage warnings

Input undervoltage (UV) warning

If the input voltage sensed at the VINS pin drops to/below the warning level programmed using the VIN_UV_WARN_LIMIT command, the UV warning is triggered. This warning is cleared when the input voltage rises above this level plus 2.06 V fixed hysteresis.

***Note**: UV warning can be mapped on the GPO2 pin by configuring it as UV_THN, refer* Chapter 2.12.5.

Input overvoltage (OV) warning

If the input voltage sensed at the VINS pin rises to/above the warning level programmed using the VIN_OV_WARN_LIMIT command, the OV warning is triggered. This warning is cleared when the input voltage drops below this level minus 2.06 V fixed hysteresis.

Output undervoltage (OUV) warning

If the output voltage sensed at the VOUTS pin drops to/below the warning level programmed using the VOUT_UV_WARN_LIMIT command, the OUV warning is triggered. This warning is cleared when the output voltage rises above this level plus 2.06 V fixed hysteresis.

Output overvoltage (OOV) warning

If the output voltage sensed at the VOUTS pin rises to/above the warning level programmed using the VOUT_OV_WARN_LIMIT command, the OOV warning is triggered. This warning is cleared when the output voltage drops below this level minus 2.06 V fixed hysteresis.

2.12.4.3 Current warnings

Output undercurrent (OUC) warning

If the IMON pin voltage drops to/below the warning level programmed using the IOUT_UC_WARN_LIMIT command, the OUC warning is triggered. This warning is cleared when the V_{IMON} rises above this level plus a fixed digital hysteresis of 128 LSBs. Refer Chapter 4.4 for V_{IMON} (V) to IOUT (A) conversion.

To avoid false triggering of the OUC warning due to low current levels during INIT_REG_SOA or at the beginning of the ON states, the OUC detection will start only after the current goes above the programmed OUC level for the first time in the ON state.

Output overcurrent (OOC) warning

If the IMON pin voltage rises to/above the warning level programmed using the IOUT_OC_WARN_LIMIT command, the OOC warning is triggered. This warning is cleared when the V_{IMON} drops below this level minus a fixed digital hysteresis of 128 LSBs. Refer Chapter 4.4 for V_{IMON} (V) to IOUT (A) conversion.

2.12.4.4 Power warning

Output overpower (OP) warning

If the input power (VIN * IOUT) rises to/above the warning level programmed using the PIN_OP_WARN_LIMIT command, the OP warning is triggered. This warning is cleared when the power drops below this level minus a fixed digital hysteresis of 256 LSBs.

***Note**: IOUT refers to the current telemetry based on the IMON pin.*

2.12.4.5 Thermal warnings

MOSFET overtemperature (OT) warning

If the MOSFET temperature rises to/above the warning level programmed using the OT_WARN_LIMIT command, the OT warning is triggered. This warning is cleared when the MOSFET temperature drops below this level minus T_{OT_HYS} fixed hysteresis.

Controller thermal shutdown (TSD) warning

If the controller's temperature rises to/above the fixed warning level $TSDW_{UTH}$, the TSD warning is triggered. This warning is cleared when the temperature drops below $TSDW_{LTH}$ level.

2.12.4.6 Communication warning

PMBus interface communication (COMM) warning

This warning is triggered if the PMBus communication (read or write) detects any failures. COMM is the only warning that is enabled during the LATCH_OFF state. Since the WARN pin status is latched during this state, the warning is not reported through this pin. The only way to detect this warning during LATCH_OFF is to read the STATUS_CML command.

***Note**: WARN pin is not cleared by clearing the STATUS_CML command after a COMM warning. WARN pin is a reflection of the COMM bit in the STATUS_WARNS command, so this bit has to be cleared to release the WARN pin.*

2.12.5 UV throttle

As mentioned in Chapter 2.11, the GPO2 pin can be configured as the UV_THN i.e. UV throttle pin. The UV_THN pin is used to inform the microcontroller that the input undervoltage condition is limited and input supply throttling should be considered. It is an extended form of the UV warning with dedicated deglitch/recovery timers and programmable hysteresis. These timers and hysteresis are programmed using the UV_TH_TMR and V_SNS_CFG commands respectively.

When the voltage at the VINS pin drops below the threshold i.e. VIN_UV_WARN_LIMIT level, the deglitch timer is started. If the voltage remains below the threshold plus the digital hysteresis when the deglitch timer expires, then

the UV_THN pin is pulled low. Similarly, when the VINS pin voltage rises above the threshold plus digital hysteresis, the recovery timer is started. If the voltage remains above the threshold plus the digital hysteresis when the recovery timer expires, then the UV_THN pin is pulled HIGH.

Figure 18 illuistrates the UV throttle function.

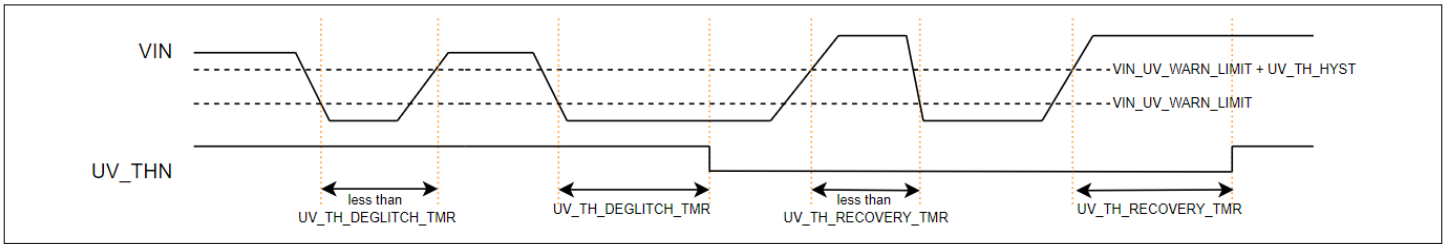


Figure 18 UV throttle function

2.13 Telemetry

The device provides real-time accurate measurement and calculation data for:

- Input voltage
- Output voltage
- Load/MOSFET current (by means V_{IMON})
- Input power
- Energy
- Internal MOSFET temperature
- On-chip controller temperature

All information is provided through the PMBus interface by issuing the corresponding commands. The figure below shows the detailed telemetry flow of the device.

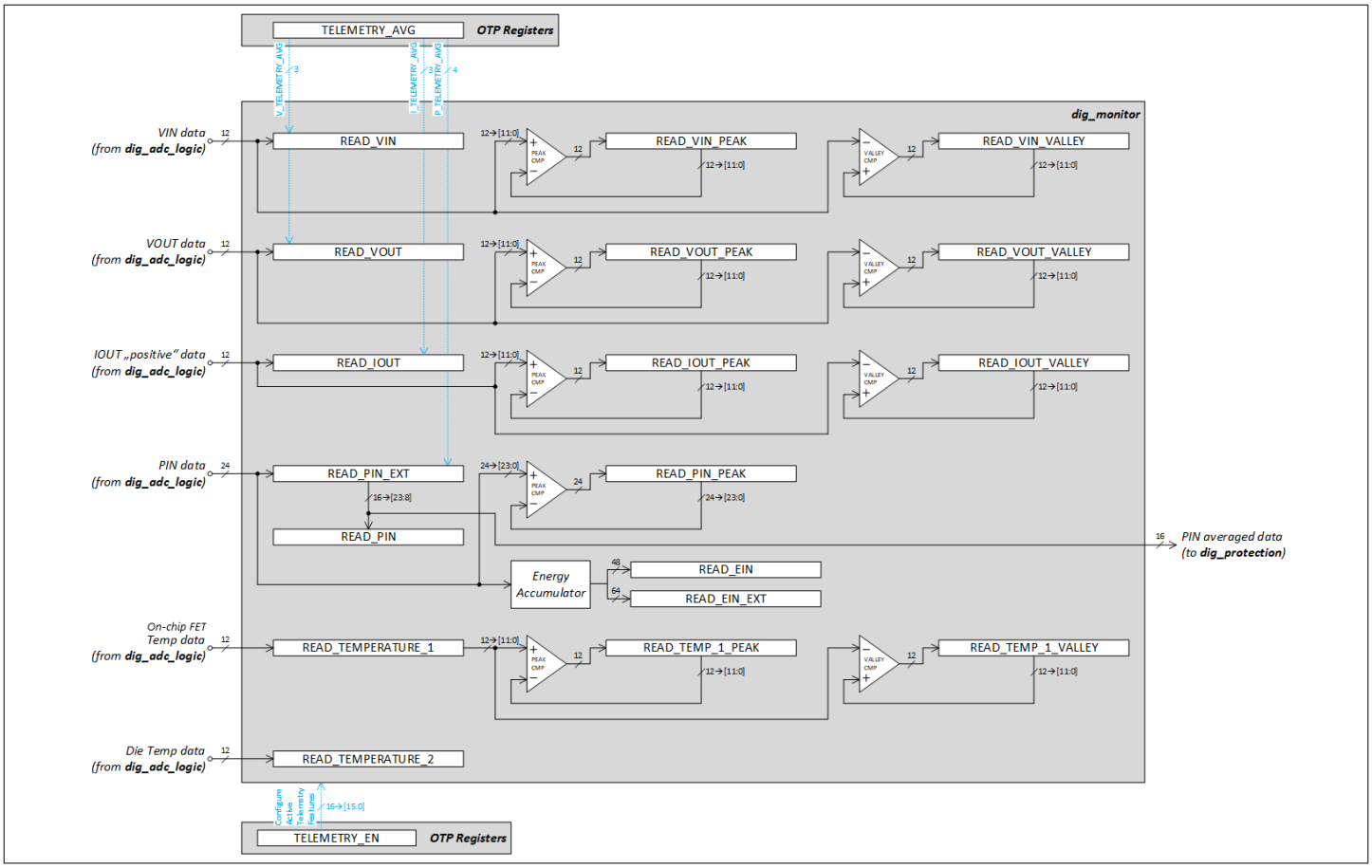


Figure 19 Telemetry flow

The following table shows the sensing points of the different telemetry features and their associated PMBus™ commands.

Table 11 Telemetry summary

Parameter	Sensing	Averaging configuration	Telemetry data		
			Instantaneous/ averaged	Peak	Valley
Input voltage	VINS pin	V_TELEMETRY_AVG	READ_VIN	READ_VIN_PEAK	READ_VIN_VALLEY
Load/MOSFET current	IMON pin	I_TELEMETRY_AVG	READ_IOUT	READ_IOUT_PEAK	READ_IOUT_VALLEY
Output voltage	VOUTS pin	V_TELEMETRY_AVG	READ_VOUT	READ_VOUT_PEAK	READ_VOUT_VALLEY
Input power (16 bits)	Input voltage x Load/MOSFET current	P_TELEMETRY_AVG	READ_PIN	-	-
Input power (24 bits)			READ_PIN_EXT	READ_PIN_PEAK	-
Energy (48 bits)	Input power accumulated over time	-	READ_EIN	-	-

(table continues...)

Table 11 (continued) Telemetry summary

Parameter	Sensing	Averaging configuration	Telemetry data		
			Instantaneous/ averaged	Peak	Valley
Energy extended (64 bits)		-	READ_EIN_EXT	-	-
Internal MOSFET temperature	Internal MOSFET temperature sensor	-	READ_TEMPERATURE_1	READ_TEMP_1_PEAK	READ_TEMP_1_VALLEY
On-Chip controller temperature	On-chip controller temperature sensor	-	READ_TEMPERATURE_2	-	-

2.13.1 Averaged and instantaneous telemetry

Averaged telemetry data

The TELEMETRY_AVG command is used to configure the averaging settings for the input voltage, output voltage, load/ MOSFET current and input power telemetry data. The voltages and current can be averaged up to 128 samples while the power can be averaged up to 32768 samples.

Table 12 Voltage and current telemetry averaging

I_TELEMETRY_AVG and/or V_TELEMETRY_AVG bits	Averaged amount of samples
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

Table 13 Power telemetry averaging

P_TELEMETRY_AVG bits	Averaged amount of samples
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64

(table continues...)

Table 13 (continued) Power telemetry averaging

P_TELEMETRY_AVG bits	Averaged amount of samples
0111	128
1000	256
1001	512
1010	1024
1011	2048
1100	4096
1101	8192
1110	16384
1111	32768

Instantaneous telemetry data

Instantaneous measurements are obtained by setting the corresponding TELEMETRY_AVG:x_TELEMETRY_AVG bits to "0", so that only one sample is taken.

2.13.2 Peaks and valleys

x_PEAK and x_VALLEY commands are used to report the maximum and minimum values respectively, measured since the last time the command was cleared.

Peaks information is available for the following parameters:

- Input voltage
- Output voltage
- Load/MOSFET current
- Input power
- Internal MOSFET temperature

Valleys information is available for the following parameters:

- Input voltage
- Output voltage
- Load/MOSFET current
- Internal MOSFET temperature

The x_PEAK and x_VALLEY commands are cleared after reading their contents or through a device power cycle. After reset, the first value read is compared to the previous peak (0x000) or valley (0xFFF) and it becomes the new peak or valley respectively. This process continues until the user reads this data. As shown in Figure 19, peaks and valleys are calculated from instantaneous data before it is averaged regardless of the averaging setting.

2.13.3 Telemetry via PMBus

The following formula converts the PMBus direct format data into "real world" values.

$$X = \frac{1}{m} \times \left(Y \times 10^{-R} - b \right) \tag{5}$$

where:

X = Calculated "real world" value in the appropriate units (A, V, °C, etc.)

m = Slope coefficient, is a two-byte, two’s complement integer

Y = Two byte two's complement integer received from the PMBus device
b = Offset, is a two-byte, two's complement integer
R = Exponent, is a one-byte, two's complement integer

To convert from "real world" values to PMBus direct format, use the following formula:

$$Y = \left(mX + b\right) \times 10^{R} \tag{6}$$

where:
Y = two byte two's complement integer to be sent to the unit
m = Slope coefficient, is the two-byte, two's complement integer
X = "real world" value, in units such as Amperes or Volts, to be converted for transmission
b = Offset, is the two-byte, two's complement integer
R = Exponent, is the decimal value equivalent to the one byte, two's complement integer.

The coefficients for these formulas are specified in the following table:

Table 14 PMBus coefficients

Parameter	Command	m	b	R
Voltage	VOUT_OV_WARN_LIMIT, VOUT_UV_FAULT_LIMIT, VOUT_UV_WARN_LIMIT, VIN_OV_FAULT_LIMIT, VIN_OV_WARN_LIMIT, VIN_UV_FAULT_LIMIT, VIN_UV_WARN_LIMIT, READ_VIN, READ_VIN_PEAK, READ_VIN_VALLEY, READ_VOUT, READ_VOUT_PEAK, READ_VOUT_VALLEY	4653	0	-2
Current	IOUT_OC_WARN_LIMIT, IOUT_UC_WARN_LIMIT, READ_IOUT, READ_IOUT_PEAK, READ_IOUT_VALLEY	24668	0	-4
Power and Energy	READ_PIN_EXT, READ_PIN_PEAK	11484	0	1
	PIN_OP_WARN_LIMIT, READ_PIN, READ_EIN, READ_EIN_EXT	4486	0	-1

(table continues...)

Table 14 (continued) PMBus coefficients

Parameter	Command	m	b	R
MOSFET temperature	OT_FAULT_LIMIT, OT_WARN_LIMIT, READ_TEMPERATURE_1, READ_TEMP_1_PEAK, READ_TEMP_1_VALLEY	54	22521	-1
Controller temperature	READ_TEMPERATURE_2	23	6225	-1

***Note**: Refer Chapter 4.4 for examples.*

2.13.4 Input power calculation

The input power is calculated as a product of the input voltage and the load/MOSFET current values. The power calculation is performed each time a current measurement is taken, by multiplying the recent values of load/MOSFET current and the input voltage before their corresponding averaging. Input power can be reported in a 16-bit format (READ_PIN) and/or an extended 24-bit format (READ_PIN_EXT).

2.13.5 Energy calculation

Energy is the input power accumulated over time. The calculated input power value is added to a power accumulator that may increment a rollover counter if the value exceeds the maximum accumulator value. The power accumulator also increments a power sample counter. The power accumulator and power sample counter are read using the same READ_EIN command to ensure that the accumulated value and sample count are from the same point in time.

The system microcontroller reading the data assigns a time stamp when the data is read. By calculating the time difference between consecutive READ_EIN values and determining the delta in power consumed, the microcontroller can determine the total energy consumed over that period.

***Note**: READ_EIN_EXT command has 16 extra ROLLOVER_COUNT bits for an extended energy reading.*

2.14 Communication interface (PMBus)

The Power Management Bus (PMBus™) is an open-standard digital power management protocol: simple, standard, flexible, extensible, and easy to program. The PMBus command language enables communication between components of a power system: CPUs, power supplies, power converters, and more.

The supported features and commands in this device are based on the PMBus™ specification Rev 1.3.1 parts I, II and III.

Communication via PMBus™ is possible right after the internal circuitry initialization, which takes around 2 ms after the VDD_VIN is applied.

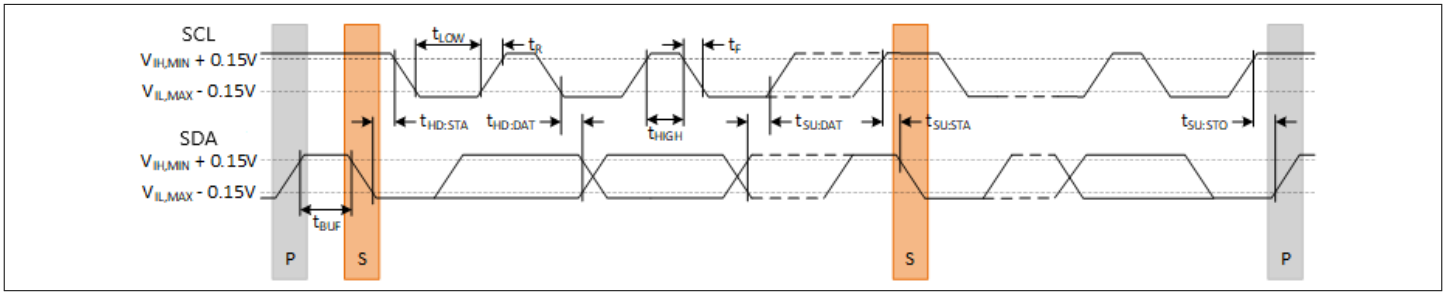


Figure 20 PMBus™ timing diagram

2.14.1 Supported functions

The PMBus™ is specified to cover a lot of different applications in the realm of power management. For a hot-swap/ eFuse application, only a subset of commands is used.

2.14.1.1 Addressing

The device has a slave address controlled by PMBUS_CFG command or by address pins. There are seven different addresses available for external resistor setting. See Table 3.

2.14.1.2 Protocol violations

XDP730 supports the following protocol violations:

- Command not valid
- Command too short
- Data not valid
- Error at repeated start
- Extra Byte in command
- Page not valid
- Read bit set in address
- Read too few bits
- Read too few bytes
- Read too many bytes
- Send too few bits
- Send too many bytes

2.14.1.3 Timeout

If a device is holding onto the bus then the bus may freeze. If the microcontroller sees such an issue it may stop the clock for $t_{TIMEOUT}$. This may also happen if another slave holds the bus incorrectly. This causes all slaves to reset their PMBus™ interfaces and be ready for a new start command.

2.14.2 Protocol

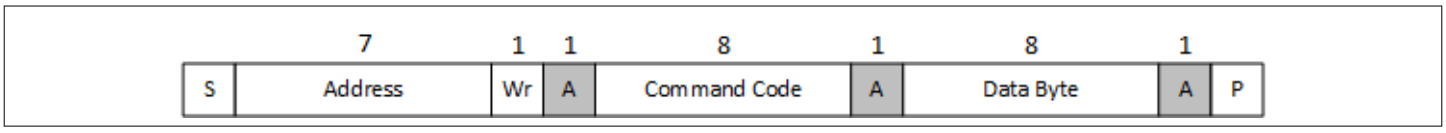


Figure 21 Write byte protocol

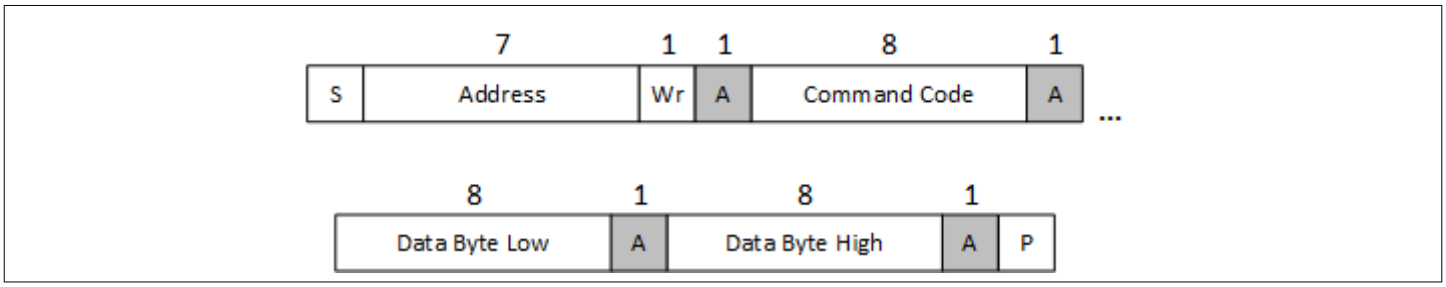


Figure 22 Write word protocol

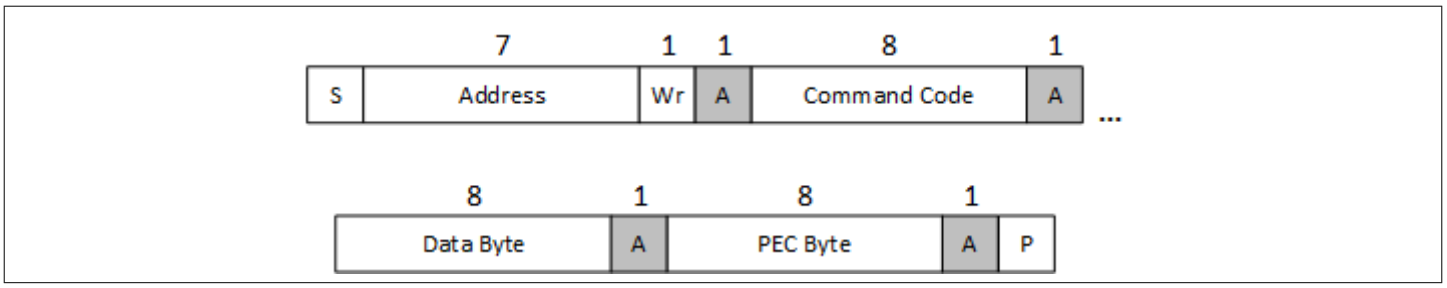


Figure 23 Write byte protocol with PEC

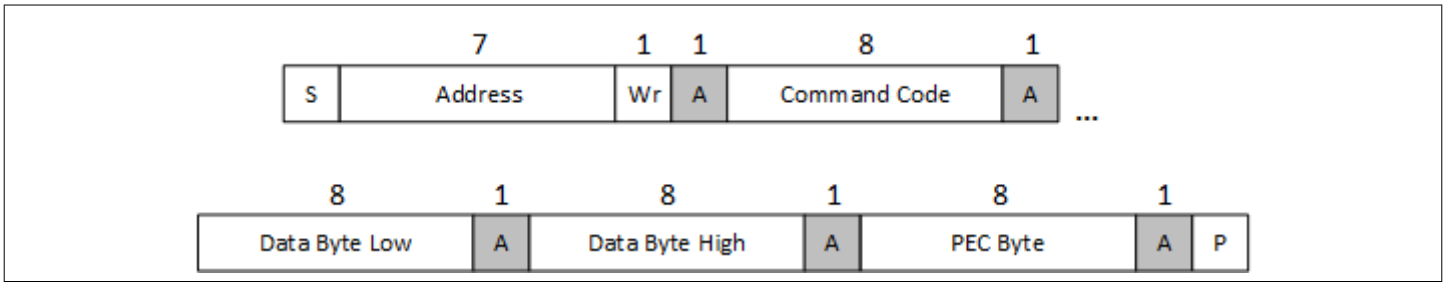


Figure 24 Write word protocol with PEC

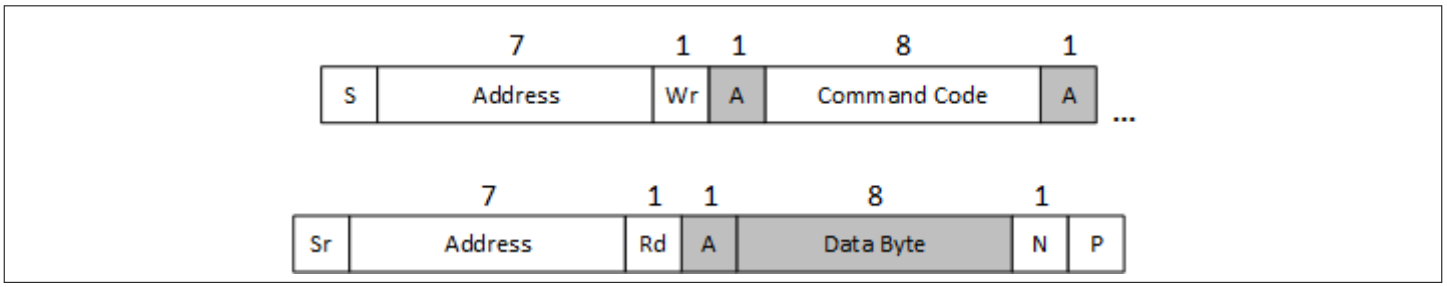


Figure 25 Read byte protocol

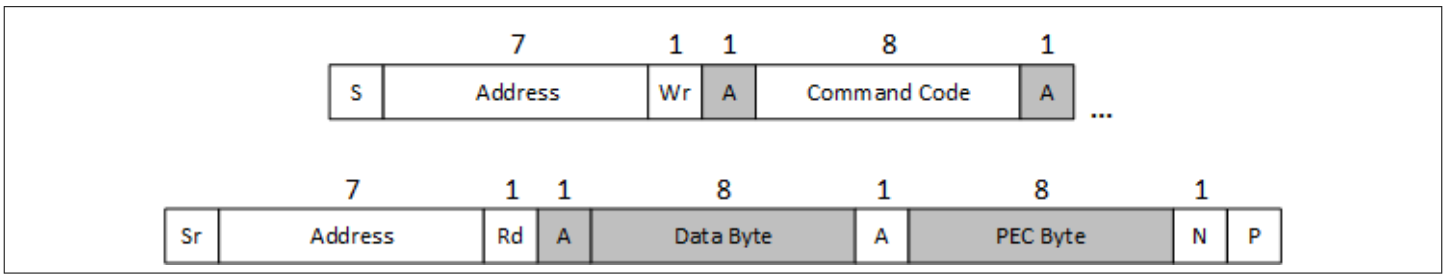


Figure 26 Read byte protocol with PEC

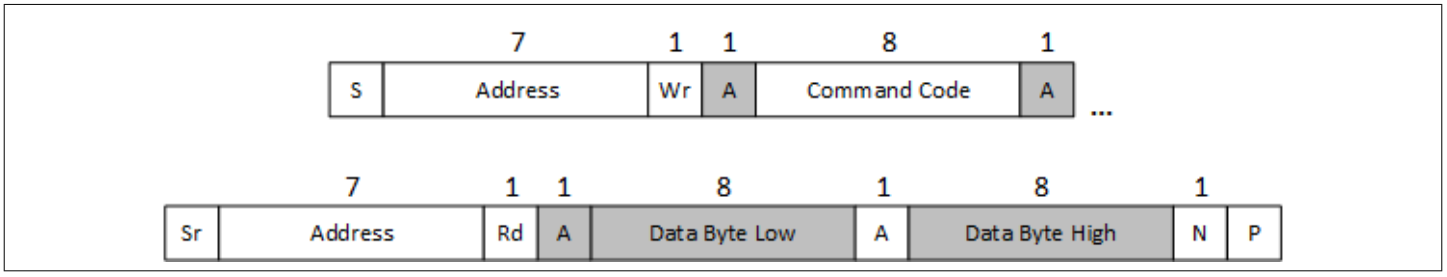


Figure 27 Read word protocol

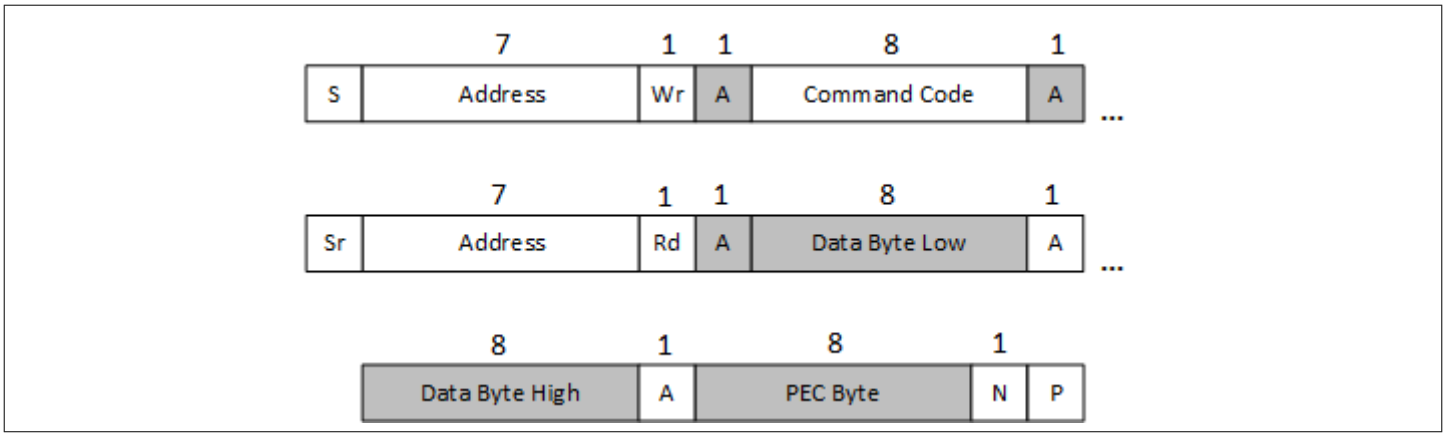


Figure 28 Read word protocol with PEC

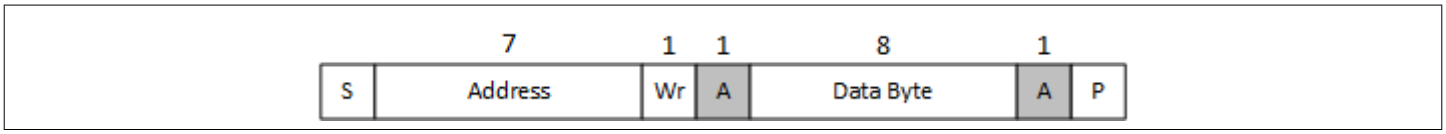


Figure 29 Send byte protocol

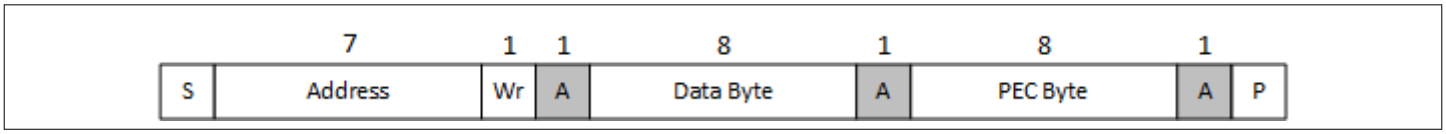


Figure 30 Send byte protocol with PEC

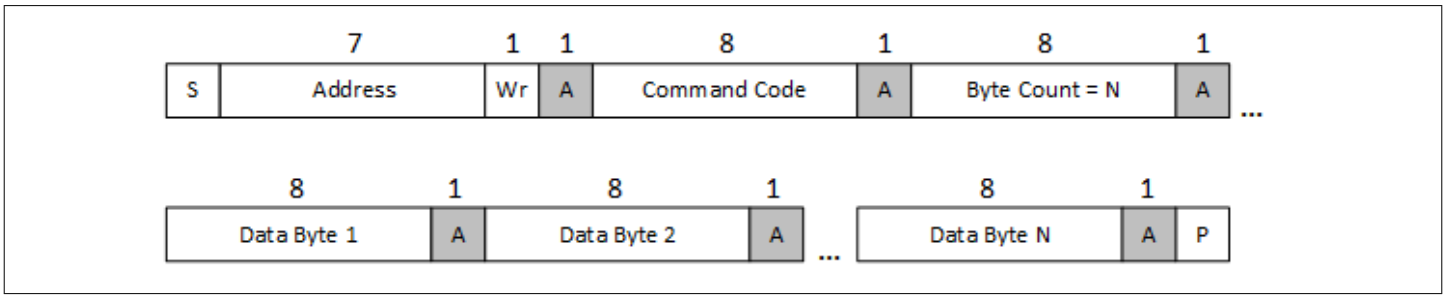


Figure 31 Block write

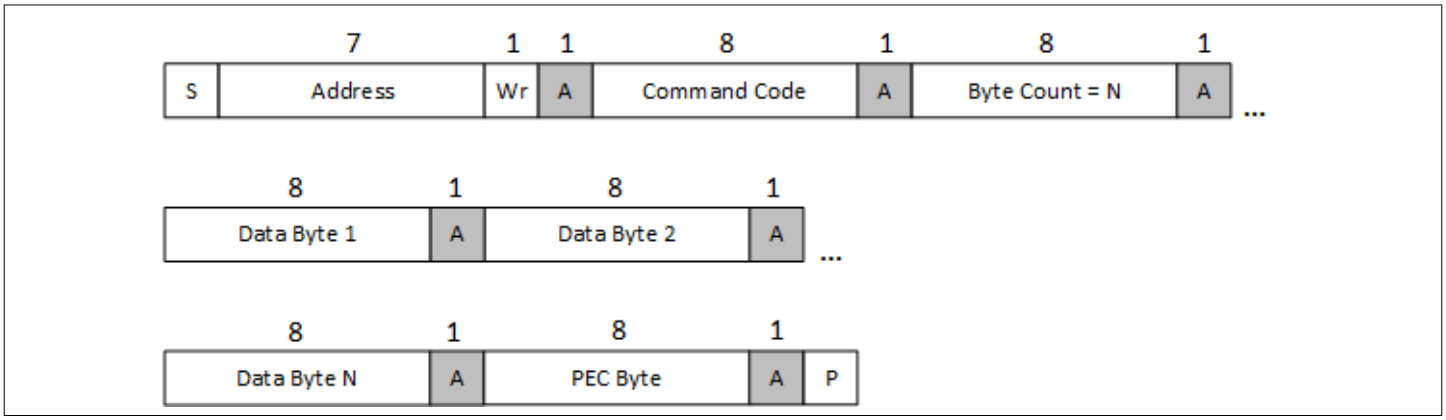


Figure 32 Block write with PEC

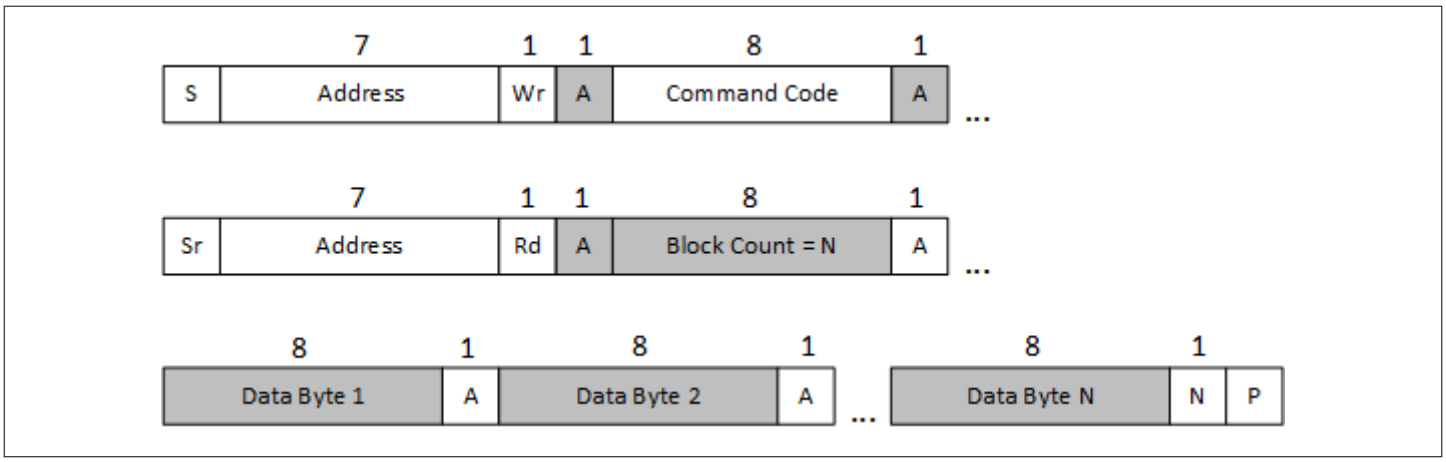


Figure 33 Block read

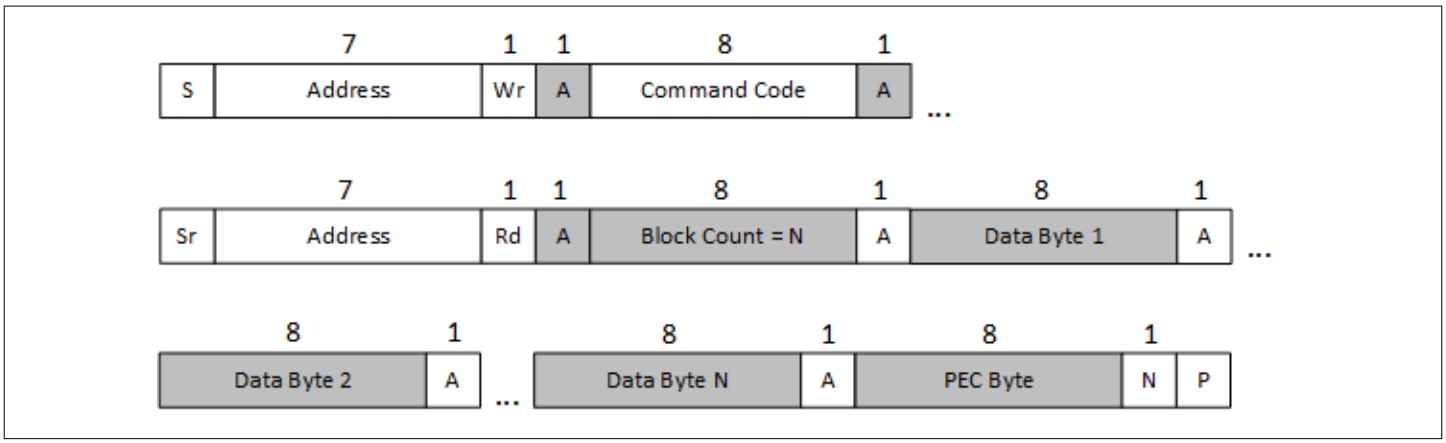


Figure 34 Block read with PEC

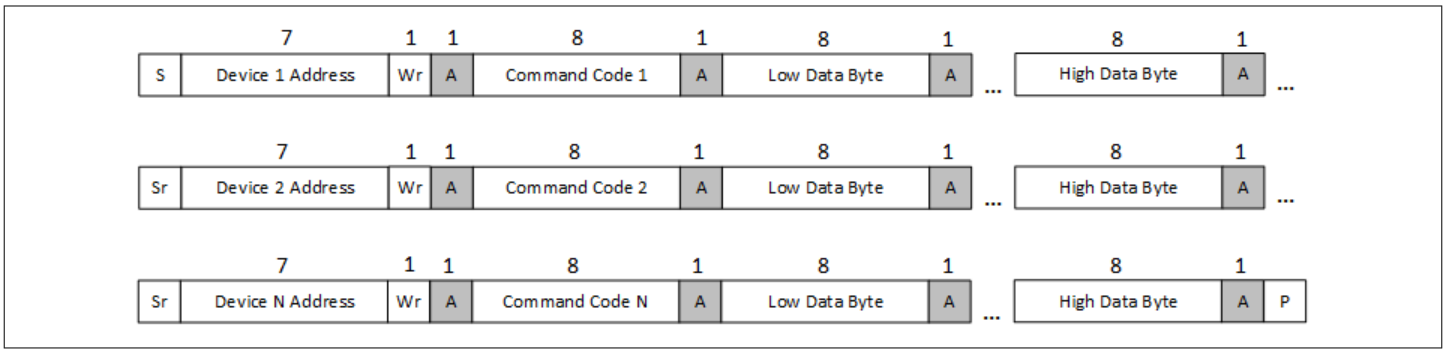


Figure 35 Group command protocol

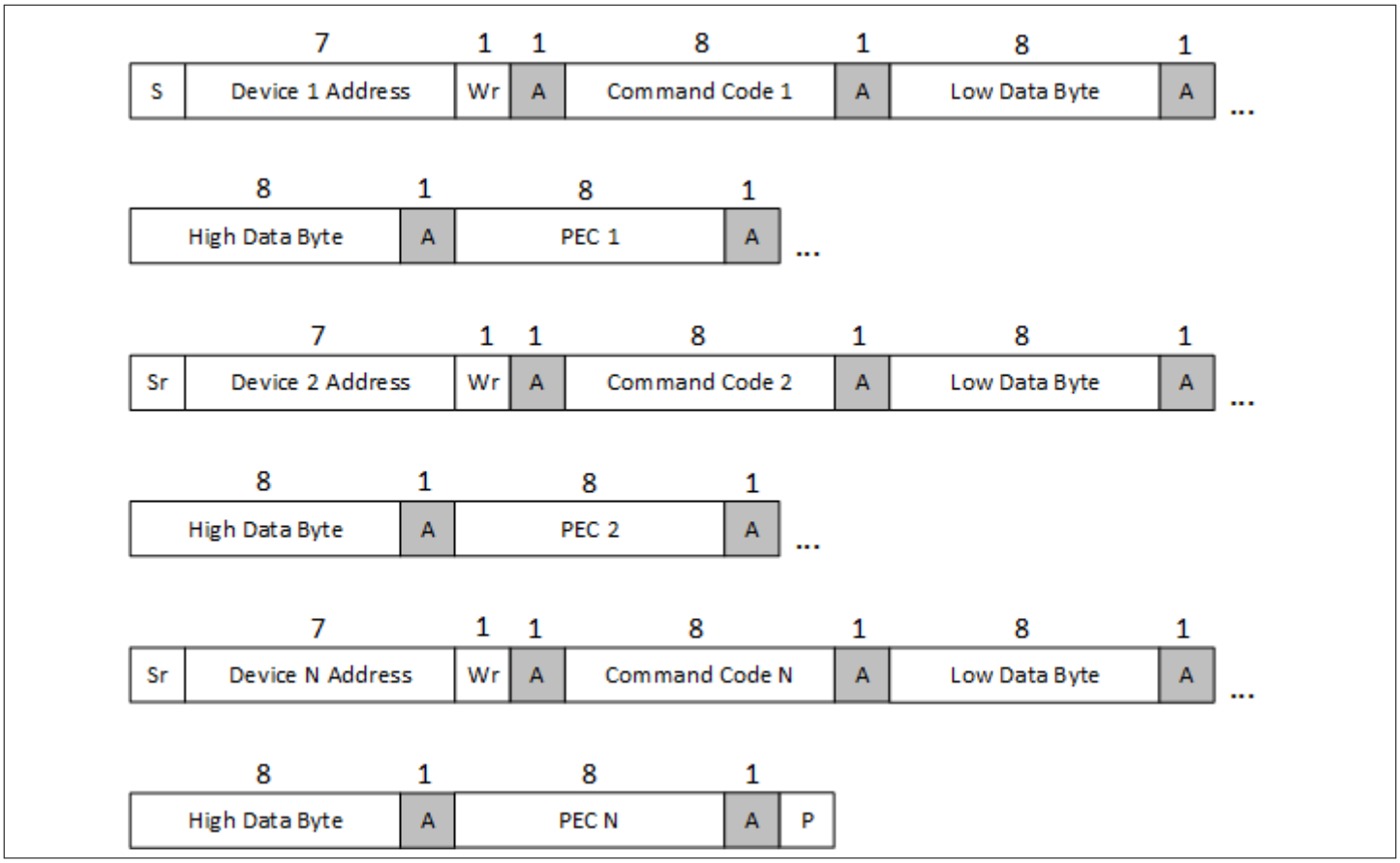


Figure 36 Group command protocol with PEC

2.14.2.1 Alert response address (ARA) protocol

XDP730 supports SMBus alert response address. This is a method to allow the microcontroller to locate the device that has issued an alert i.e. SMBALERT, if there are multiple devices connected to the same bus.

1. Device issues an SMBALERT on GPO0 (depending on GPO_CFG command configuration). This is just a normal fault/warning being signaled.
2. Microcontroller sends a special address 0x0C with READ bit "1" (i.e. 0x19).
3. Device responds with its own address:
   - If more than one device responds, the lowest address wins and disables its alert.
4. The microcontroller continues to process all alerts by the same process until there are no alerts signaled.

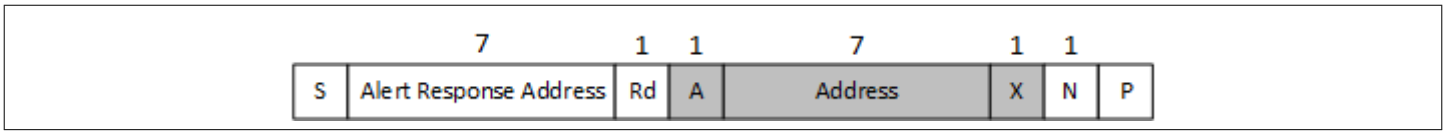


Figure 37 A 7-bit-addressable device responds to an ARA

Figure 38 A 7-bit-addressable device responds to an ARA with PEC

Figure 39 shows an example of the ARA protocol. In this case, the PMBus device address was set to 0x10, and the device releases its SMBALERT pin after responding to the ARA protocol request.

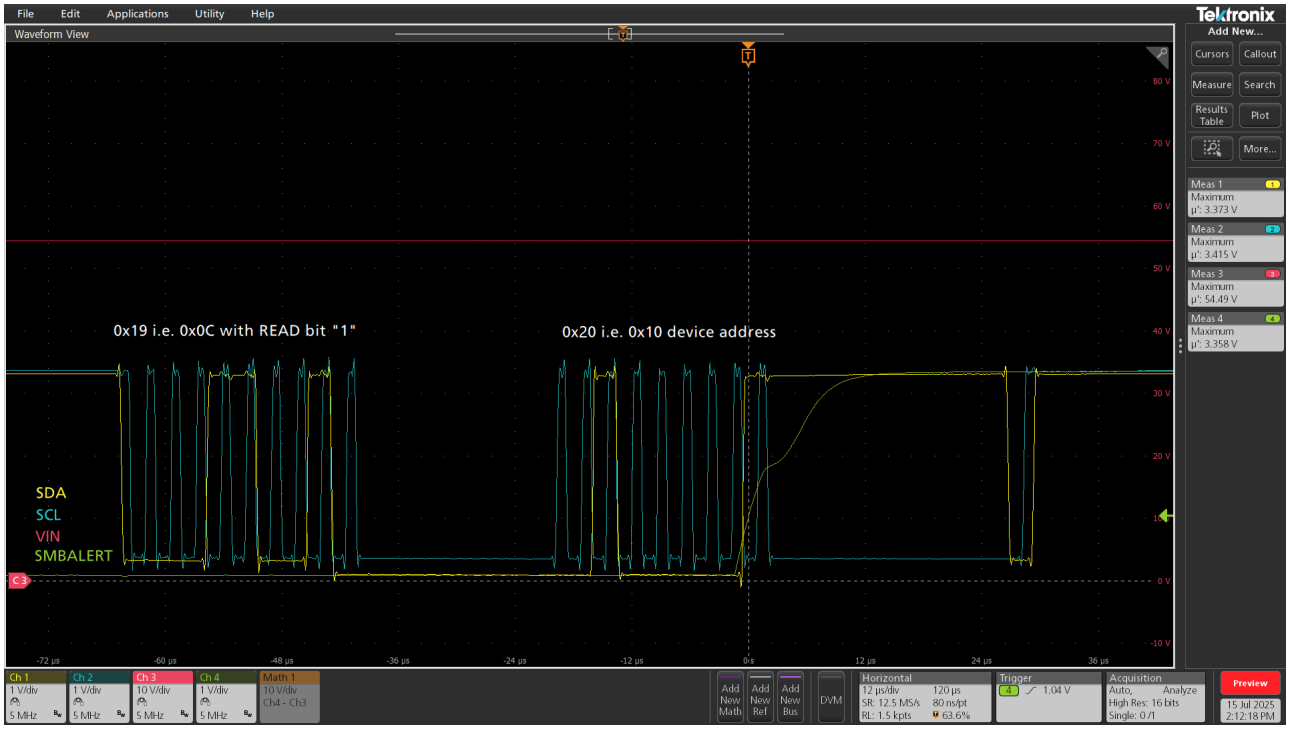


Figure 39 SMBALERT pin being released after a successful ARA protocol

2.14.3 PMBus commands

Table 15 List of PMBus™ commands

Command name	Command code	Included in OTP	Description	Default value
OPERATION	0x01	Yes	Used to turn the eFuse on/off in conjunction with the input from the EN pin.	0x80
CLEAR_FAULTS	0x03	No	Used to clear any fault/warning bits that have been set.	0x0000
CAPABILITY	0x19	No	Supported PMBus features.	0xD0
VOUT_OV_WARN_LIMIT	0x42	Yes	Sets the output overvoltage warning limit.	0x0FFF
VOUT_UV_WARN_LIMIT	0x43	Yes	Sets the output undervoltage warning limit.	0x0000
VOUT_UV_FAULT_LIMIT	0x44	Yes	Sets the output undervoltage fault limit (Primary).	0x05D1
IOUT_OC_WARN_LIMIT	0x4A	Yes	Sets the output overcurrent warning limit.	0x0FFF
OT_FAULT_LIMIT	0x4F	Yes	Sets the internal MOSFET's overtemperature fault limit.	0x0C4F
OT_WARN_LIMIT	0x51	Yes	Sets the internal MOSFET's overtemperature warning limit.	0x0FFF
VIN_OV_FAULT_LIMIT	0x55	Yes	Sets the input overvoltage fault limit (Primary).	0x0B45
VIN_OV_WARN_LIMIT	0x57	Yes	Sets the input overvoltage warning limit.	0x0FFF

(table continues...)

Table 15 (continued) List of PMBus™ commands

Command name	Command code	Included in OTP	Description	Default value
VIN_UV_WARN_LIMIT	0x58	Yes	Sets the input undervoltage warning limit.	0x0000
VIN_UV_FAULT_LIMIT	0x59	Yes	Sets the input undervoltage fault limit (Primary).	0x06D1
PIN_OP_WARN_LIMIT	0x6B	Yes	Sets the input overpower warning limit.	0xFFFF
STATUS_BYTE	0x78	No	Returns a summary of the most critical faults.	0x40
STATUS_WORD	0x79	No	Returns a summary of the most critical faults. The STATUS_BYTE occupies low byte in this command.	0x0840
STATUS_VOUT	0x7A	No	Returns a summary of the output voltage fault/warnings.	0x00
STATUS_IOUT	0x7B	No	Returns a summary of the current fault/ warning.	0x00
STATUS_INPUT	0x7C	No	Returns a summary of the input faults/ warnings.	0x00
STATUS_TEMPERATURE	0x7D	No	Returns a summary of the internal MOSFET's temperature fault/warning.	0x00
STATUS_CML	0x7E	No	Returns a summary of the communication interface and memory fault/warning.	0x00
STATUS_OTHER	0x7F	No	Returns the status of SMBALERT.	0x00
STATUS_MFR_SPECIFIC	0x80	No	Returns a summary of the general device status.	0x00
READ_EIN	0x86	No	Returns the instantaneous input energy reading.	0x000000000000
READ_VIN	0x88	No	Returns the instantaneous input voltage reading.	0x0000
READ_VOUT	0x8B	No	Returns the instantaneous output voltage reading.	0x0000
READ_IOUT	0x8C	No	Returns the instantaneous current (digitized IMON) reading.	0x0000
READ_TEMPERATURE_1	0x8D	No	Returns the instantaneous internal MOSFET's temperature reading.	0x0000
READ_TEMPERATURE_2	0x8E	No	Returns the instantaneous on-chip controller's temperature reading.	0x0000
READ_PIN	0x97	No	Returns the instantaneous input power reading.	0x0000
PMBUS_REVISION	0x98	No	Returns the PMBus revision to which the device is compliant.	0x33
MFR_ID	0x99	No	Returns manufacturer ID name.	0x004649

(table continues...)

Table 15 (continued) List of PMBus™ commands

Command name	Command code	Included in OTP	Description	Default value
MFR_MODEL	0x9A	No	Returns manufacturer device model name.	*
MFR_REVISION	0x9B	No	Returns manufacturer device silicon revision.	0x0001
VIN_OV_FAULT_LIMIT_S	0xCD	Yes	Sets the input overvoltage fault limit and its hysteresis (Secondary).	0x3BA2
VIN_UV_FAULT_LIMIT_S	0xCE	Yes	Sets the input undervoltage fault limit and its hysteresis (Secondary).	0x2674
PMBUS_CFG	0xD0	Yes	Used to configure the PMBus device address and speed selection.	0x10
MODE	0xD1	Yes	Used to configure QOD, comparators mode and MOSFET SOA.	0x0183
V_SNS_CFG	0xD4	Yes	Used to configure voltage sense and protections.	0x0428
I_SNS_CFG_1	0xD5	Yes	Used to configure overcurrent fault limits.	0x4D50
I_SNS_CFG_2	0xD6	Yes	Used to configure start-up current and the severe overcurrent limits.	0x5942
UV_TH_TMR	0xD7	Yes	Used to configure UV throttle timers.	0x2828
WATCHDOG_TMR	0xD8	Yes	Used to configure EN deglitch and maximum allowed MOSFET turn-on timers.	0x0329
V_TMR	0xD9	Yes	Used to configure voltage protection timers.	0x0000
GPO_CFG	0xDB	Yes	Used to configure the GPO pins.	0x0300
IOUT_UC_WARN_LIMIT	0xDC	Yes	Sets the output undercurrent warning limit.	0x0000
ONCHIP_TSD_FAULT_LIMIT	0xDD	Yes	Sets the on-chip controller's thermal shutdown fault limit.	0x02
ENABLE_FAULTS	0xDE	Yes	Used to enable/disable all the faults.	0xFFDB
MASK_FAULTS	0xDF	Yes	Used to mask/unmask the faults on the FAULT pin.	0xFFDB
STATUS_FAULTS	0xE0	No	Returns the status of all the faults.	0x0000
ENABLE_WARNS	0xE1	Yes	Used to enable/disable all the warnings.	0x0000
MASK_WARNS	0xE2	Yes	Used to mask/unmask the warnings on the WARN pin.	0x0000
STATUS_WARNS	0xE3	No	Returns the status of all the warnings.	0x0000
PWRGD_DG_TMR	0xE4	Yes	Used to configure the PWRGD degltich timers.	0x50
SOA_TMR	0xE5	Yes	Used to configure current protection timers.	0x0143
TURN_OFF_CTRL	0xE6	Yes	Used to configure MOSFET's turn-off/pull-down strength.	0x0006

(table continues...)

Table 15 (continued) List of PMBus™ commands

Command name	Command code	Included in OTP	Description	Default value
RETRY	0xE7	Yes	Used to configure the RESTART timer, input surge immunity and fault response i.e. Retry settings.	0x080F
TELEMETRY_EN	0xE8	Yes	Used to enable/disable different telemetry.	0x7FFF
TELEMETRY_AVG	0xE9	Yes	Used to configure the V/I/T telemetry averaging and IMON gain selection.	0x0400
WRITE_OTP	0xEA	Yes	Used to configure PMBus WRITE protection and OTP programming.	0x00
STATUS_MEM	0xEB	No	Returns the status of OTP programming.	0x00
RESTART	0xEC	No	Used to initiate a user-generated RESTART event.	0x0000
READ_PIN_EXT	0xEE	No	Returns the instantaneous input power reading (extended).	0x000000
READ_VIN_PEAK	0xEF	No	Returns the most recent maximum VIN value. It is automatically cleared when the data is read.	0x0000
READ_VOUT_PEAK	0xF0	No	Returns the most recent maximum VOUT value. It is automatically cleared when the data is read.	0x0000
READ_IOUT_PEAK	0xF1	No	Returns the most recent maximum IOUT (digitized IMON) value. It is automatically cleared when the data is read.	0x0000
READ_PIN_PEAK	0xF2	No	Returns the most recent maximum PIN value. It is automatically cleared when the data is read.	0x000000
READ_TEMP_1_PEAK	0xF3	No	Returns the most recent maximum MOSFET's temperature value. It is automatically cleared when the data is read.	0x0000
READ_VIN_VALLEY	0xF4	No	Returns the most recent minimum VIN value. It is automatically cleared when the data is read.	0x0FFF
READ_VOUT_VALLEY	0xF5	No	Returns the most recent minimum VOUT value. It is automatically cleared when the data is read.	0xFFFF
READ_IOUT_VALLEY	0xF6	No	Returns the most recent minimum IOUT (digitized IMON) value. It is automatically cleared when the data is read.	0xFFFF
READ_TEMP_1_VALLEY	0xF7	No	Returns the most recent minimum MOSFET's temperature value. It is automatically cleared when the data is read.	0xFFFF

(table continues...)

Table 15 (continued) List of PMBus™ commands

Command name	Command code	Included in OTP	Description	Default value
STATUS_MODE	0xF9	No	Returns a summary of the GATE pin status, PWRGD signal status and the selected PMBus device address.	0x0000
CONFIG_ID	0xFA	Yes	Used to configure a user-based device identification code.	0x00
READ_EIN_EXT	0xFB	No	Returns the instantaneous input energy reading (extended).	0x00000000

Attention**: * In this device, MFR_MODEL = 0x0000303337504458

2.14.4 Permanent write protection

This device provides a PMBus™ "permanent write protection" feature to block all the write requests as part of the WRITE_OTP command. If the WRITE_OTP:WR_PROTECT bit is set to "1" without burning the OTP then all the future PMBus™ write requests are blocked by the device until the device is power cycled. If WR_PROTECT and WRITE_OTP bits are set together, then the device will permanently block all future PMBus™ write requests. Therefore, it is highly recommended to burn the OTP memory only when the device configuration is finalized. This feature is helpful if the user wants to permanently lock the device/configuration, blocking the attacker from manipulating the configuration.

***Note**: When this feature is activated, the device will ignore all the future PMBus WRITE requests without any COMM warning.*

2.15 Memory

The XDP730 has two types of memory for programmability:

- Volatile memory
- One-time programmable (OTP) memory

The OTP memory can be used to save specific command settings. At device power-up i.e. in the READ_CFG state, all the settings saved in the OTP memory are copied into volatile memory.

To program the desired settings in the internal commands or OTP memory at power-up, the following steps must be followed:

- Apply a voltage at the VDD_VIN pin:
  - ≥ 7 V to program internal commands
  - ≥ 20 V to program OTP memory
- Keep the VINS pin connected to the input voltage source that supplies the VIN pins. This pin senses the input voltage to ensure the level is appropriate for OTP programming.
- Keep the EN pin at chip GND potential.
- Communication via PMBus™ is possible as soon as the STANDBY state is entered. At this point, commands and/or OTP memory can be programmed.
- For successful programming, the on-chip controller temperature of the device must stay below 125°C at all times.

To program OTP:

1. Ensure the STATUS_MEM:OTP_USER bit is set to "0". If it is "1" then it means that the device is already OTP programmed.
2. Program the commands in volatile memory as desired.
3. Set the WRITE_OTP bit.
4. The command configuration is automatically copied to the OTP section.

The PROG_BLOCK and OTP_FAIL bits in the STATUS_MEM command indicate the status of the OTP memory programming according to the following table:

Table 16 OTP programming status

PROG_BLOCK	OTP_FAIL	Meaning
0	0	OTP programming has succeeded if STATUS_MEM:OTP_USER bit is set. Otherwise, programming has not started.
0	1	OTP programming started but failed during programming because of the OTP issue. **Part must be discarded.**
1	0	OTP programming must not be started since temperature or input supply voltage are out of range.
1	1	OTP programming started but failed during programming because of temperature or input supply voltage going out of range during programming. **Part must be discarded.**

Before programming, PROG_BLOCK must be checked in order to determine if temperature and VIN are in range and programming is allowed. PROG_BLOCK indicates the temperature and voltage status in real time. If, after checking PROG_BLOCK, but before programming starts, any of these conditions goes out of range, programming will be blocked, PROG_BLOCK will be set and OTP_FAIL will remain 0. It is possible that, after a blocked attempt of programming, temperature and voltage go back in range, so PROG_BLOCK will read 0 again. Due to this, it is important to understand that, as long as OTP_USER and OTP_FAIL are 0, it is still possible to program the OTP.

If temperature and voltage conditions go out of range during programming, OTP_FAIL will indicate an unsuccessful programming after the operation. If temperature and voltage go back in range, PROG_BLOCK will read 0 again and it is only OTP_FAIL that indicates the programming failed.

3 General product characteristics

3.1 Absolute maximum ratings

Table 17 Absolute maximum ratings

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to GND unless otherwise specified, positive currents are flowing into the pin, T_A = 25°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltage at VDD_VIN, VIN, VINS, VOUT and VOUTS pins	$V_{VDD\_VIN\_DC}$, V_{VIN_DC}, V_{VINS}, V_{VOUT_DC}, V_{VOUTS}	-0.3	-	80	V	-
Voltage transients at VDD_VIN, VIN, VINS, VOUT and VOUTS pins	$V_{VDD\_VIN\_AC}$, V_{VIN_AC}, V_{VINS_AC}, V_{VOUT_AC}, V_{VOUTS_AC}	-0.3	-	100	V	For 500 ms maximum
Voltage slew rate at VDD_VIN, VIN, VINS, VOUT and VOUTS pins	SR_{VDD_VIN}, SR_{VIN}, SR_{VINS}, SR_{VOUT}, SR_{VOUTS}	-	-	80	V/µs	The RC filter (100 Ω/100 nF or etc.) on the VDD_VIN pin is recommended, especially for high voltage applications. An output cap (10 µF min) limits a slew rate on the VOUT pin.
Output voltage at VREG pin	V_{VREG}	-0.3	-	6	V	-
Digital pins output voltage (SDA, GPO0, SYNC, GPO2, GPO1, PWRGD)	V_{SDA}, V_{GPO0}, V_{SYNC}, V_{GPO2}, V_{GPO1}, V_{PWRGD}	-0.3	-	6	V	-
Digital pins input voltage (SCL, SDA, SYNC, GPO2, EN)	V_{SCL}, V_{SDA}, V_{SYNC}, V_{GPO2}, V_{EN}	-0.3	-	6	V	-
Analog pins input voltage (ADDR, UV, OV, FS)	V_{ADDR}, V_{UV}, V_{OV}, V_{FS}	-0.3	-	6	V	-
IMON pin voltage	V_{IMON}	-0.3	-	6	V	-
Junction Temperature range	T_J	-40	-	150	°C	-
Storage Temperature range	T_S	-55	-	150	°C	-

3.2 Functional range

Table 18 Functional and performance ranges description

Absolute voltage range at VDD_VIN (V)	Communication interface	FET Gate	VREG
0 ≤ VDD_VIN < 7	Off	Off (passive pull-down)	Off

(table continues...)

Table 18 (continued) Functional and performance ranges description

Absolute voltage range at VDD_VIN (V)	Communication interface	FET Gate	VREG
7 ≤ VDD_VIN < 9	On	Limited operation: - Off (active pull-down); - limited SOA regulation depending on gate driver supply; - On/enhancement is not guaranteed (but ≥ 4.5 V)	5.0 V (typ.)
9 ≤ VDD_VIN ≤ 80		Full operation: - Off (active pull-down); - full SOA regulation; - On/enhancement (typ. 10.5 V)	

Table 19 Recommended operating range

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to GND unless otherwise specified, positive currents are flowing into the pin, T_A = 25°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage at VDD_VIN pin	V_{VDD_VIN}	7	-	80	V	-
Supply voltage at VDD_VIN pin to enable all features	$V_{VDD\_VIN\_EN}$	9	-	80	V	Refer Chapter 3.2.
Supply voltage filter resistor	R_{VDD_VIN}	100	-	-	Ω	This is needed to support input surge immunity.
Supply voltage at VIN pin	V_{VIN}	7	-	80	V	-
Voltage at VINS, VOUTS and VOUT pins	V_{VINS}, V_{VOUTS}, V_{VOUT}	0	-	80	V	-
Maximum output current	I_{OUT_MAX}	-	30	-	A	-
Digital pins output voltage (SDA, GPO0, SYNC, GPO2, GPO1, PWRGD)	V_{SDA}, V_{GPO0}, V_{SYNC}, V_{GPO2}, V_{GPO1}, V_{PWRGD}	0	-	5.5	V	-
Digital pins input voltage (SCL, SDA, SYNC, GPO2, EN)	V_{SCL}, V_{SDA}, V_{SYNC}, V_{GPO2}, V_{EN}	0	-	5.5	V	-
IMON pin voltage	V_{IMON}	0	-	1.35	V	-
Analog pins input voltage (ADDR, UV, OV, FS)	V_{ADDR}, V_{UV}, V_{OV}, V_{FS}	0	-	5.5	V	-
Junction temperature range	T_J	-40	-	125	°C	-

3.3 Thermal characteristics

Table 20 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance junction-to-case (bottom)	$R_{\Theta JC\_Bot}$	-	5.1	-	K/W	PCB simulation setup as described in Table 21.
Thermal resistance junction-to-case (top)	$R_{\Theta JC\_Top}$	-	18	-	K/W	PCB simulation setup as described in Table 21.
Thermal resistance junction-to-ambient	$R_{\Theta JA}$	-	20.4	-	K/W	PCB simulation setup as described in Table 21.

Table 21 PCB characteristics for thermal simulation

		λ_{therm} [W/m-K]
Metalization	JEDEC 2s2p (JESD 51-7, JESD 51-5)	388
Cooling Area [mm^2]	none	388

***Note**:*
- *Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.*
- *This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org*

3.4 ESD robustness

Table 22 ESD robustness

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ESD robustness HBM	V_{ESD_HBM}	-2000	-	+2000	V	Human Body Model sensitivity as per ANSI/ESDA/JEDEC JS-001
ESD robustness CDM	V_{ESD_CDM}	-500	-	+500	V	Charge device model sensitivity as per ANSI/ESDA/JEDEC JS-002

3.5 Electrical characteristics

Table 23 Electrical characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, typical programmable values are the default configuration of the device, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDD_VIN and VIN						
Supply voltage at VDD_VIN and VIN pins	V_{VDD_VIN}, V_{VIN}	7	54	80	V	-
Current consumption	I_{VDD}	-	7.4	TBD	mA	VDD_VIN supply current; MOSFET is fully ON (IOUT = 0 A); Telemetry is ON
VINS and VOUTS						
VINS pin input current	I_{VINS}	-	34	-	µA	At VINS = 54 V
VOUTS pin input current	I_{VOUTS}	-	34	-	µA	At VOUTS = 54 V
Enable (EN)						
EN pin upper threshold	V_{EN_UTH}	1.14	1.2	1.26	V	-
EN pin lower threshold	V_{EN_LTH}	0.76	0.8	0.84	V	-
Input Undervoltage (UV) protection						
UV pin upper threshold	V_{UV_UTH}	0.95	1	1.05	V	-
UV pin lower threshold	V_{UV_LTH}	0.79	0.83	0.87	V	-
Programmable UV fault limit (Primary)	V_{UV_P}	- - ... - ... -	- 0 ... 37.5 (default) ... 88	- - ... - ... -	V	Set via PMBus™; VIN_UV_FAULT_LIMIT = 0x000 ... VIN_UV_FAULT_LIMIT = 0x6D1 ... VIN_UV_FAULT_LIMIT = 0xFFF
Programmable UV fault limit (Secondary)	V_{UV_S}	- - ... - ... -	- 0 ... 35.5 (default) ... 88	- - ... - ... -	V	Set via PMBus™; VIN_UV_FAULT_LIMIT_S = 0x000 ... VIN_UV_FAULT_LIMIT_S = 0x674 ... VIN_UV_FAULT_LIMIT_S = 0xFFF

(table continues...)

Table 23 (continued) Electrical characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, typical programmable values are the default configuration of the device, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Programmable UV fault hysteresis (Primary)	$V_{UV\_HYS\_P}$	- - ... -	- 2 (default) ... 13	- - ... -	V	Set via PMBus™; V_SNS_CFG:VIN_UV_HYST = 0x0 ... V_SNS_CFG:VIN_UV_HYST = 0xF
Programmable UV fault hysteresis (Secondary)	$V_{UV\_HYS\_S}$	- - - - ... -	- 2 3 4 (default) ... 13	- - - - ... -	V	Set via PMBus™; VIN_UV_FAULT_LIMIT_S:VIN_UV_HYST_S = 0x0 VIN_UV_FAULT_LIMIT_S:VIN_UV_HYST_S = 0x1 VIN_UV_FAULT_LIMIT_S:VIN_UV_HYST_S = 0x2 ... VIN_UV_FAULT_LIMIT_S:VIN_UV_HYST_S = 0xF
Input overvoltage (OV) protection						
OV pin upper threshold	V_{OV_UTH}	0.97	1	1.03	V	-
OV pin lower threshold	V_{OV_LTH}	0.92	0.95	0.98	V	-
Programmable OV fault limit (Primary)	V_{OV_P}	- - ... - ... -	- 0 ... 62 (default) ... 88	- - ... - ... -	V	Set via PMBus™; VIN_OV_FAULT_LIMIT = 0x000 ... VIN_OV_FAULT_LIMIT = 0xB45 ... VIN_OV_FAULT_LIMIT = 0xFFF
Programmable OV fault limit (Secondary)	V_{OV_S}	- - ... - ... -	- 0 ... 64 (default) ... 88	- - ... - ... -	V	Set via PMBus™; VIN_OV_FAULT_LIMIT_S = 0x000 ... VIN_OV_FAULT_LIMIT_S = 0xBA2 ... VIN_OV_FAULT_LIMIT_S = 0xFFF

(table continues...)

Table 23 (continued) Electrical characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, typical programmable values are the default configuration of the device, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Programmable OV fault hysteresis (Primary)	$V_{OV\_HYS\_P}$	- - - ... -	- 1 2 (default) ... 8	- - - ... -	V	Set via PMBus™; V_SNS_CFG:VIN_OV_HYST = 0b000 V_SNS_CFG:VIN_OV_HYST = 0b001 ... V_SNS_CFG:VIN_OV_HYST = 0b111
Programmable OV fault hysteresis (Secondary)	$V_{OV\_HYS\_S}$	- - ... - ... -	- 1 ... 4 (default) ... 8	- - ... - ... -	V	Set via PMBus™; VIN_OV_FAULT_LIMIT_S:VIN_OV_HYST_S = 0b000 ... VIN_OV_FAULT_LIMIT_S:VIN_OV_HYST_S = 0b011 ... VIN_OV_FAULT_LIMIT_S:VIN_OV_HYST_S = 0b111
On-chip input overvoltage (OVIN) protection						
Programmable OVIN fault limit	V_{OVIN}	- - - - -	- 70 75 80 (default) 85	- - - - -	V	Set via by PMBus™; V_SNS_CFG:OVIN_FAULT_LIMIT = 0b00 V_SNS_CFG:OVIN_FAULT_LIMIT = 0b01 V_SNS_CFG:OVIN_FAULT_LIMIT = 0b10 V_SNS_CFG:OVIN_FAULT_LIMIT = 0b11
Fixed OVIN fault hysteresis	V_{OVIN_HYS}	-	5	-	V	-

(table continues...)

Table 23 (continued) Electrical characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, typical programmable values are the default configuration of the device, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output Undervoltage (OUV) protection						
Programmable OUV fault limit	V_{OUV}	- - ... - ... -	- 0 ... 32 (default) ... 88	- - ... - ... -	V	Set via PMBus™; VOUT_UV_FAULT_LIMIT = 0x000 ... VOUT_UV_FAULT_LIMIT = 0x5D1 ... VOUT_UV_FAULT_LIMIT = 0xFFF
Fixed OUV fault hysteresis	V_{OUV_HYS}	-	2.06	-	V	-
VREG						
Output voltage	V_{REG}	4.7	5.0	5.3	V	7 V ≤ VDD_VIN < 80 V
VREG bypass capacitor	C_{VREG}	-	1	-	µF	For V_{REG} = 5 V
Current capability	I_{REG}	-	-	1	mA	To supply external load
Power MOSFET						
On resistance	R_{DS_ON}	-	1.5	1.9	mΩ	For V_{GS} = 10 V
Fast pull-down current	I_{GATE_FPD}	-	1	-	A	-
Programmable slow pull-down current	I_{GATE_SPD}	- - - - -	- 250 500 750 1250 (default)	- - - - -	µA	Set via PMBus™; TURN_OFF_CTRL:GATE_SLOW_PD = 0b00 TURN_OFF_CTRL:GATE_SLOW_PD = 0b01 TURN_OFF_CTRL:GATE_SLOW_PD = 0b10 TURN_OFF_CTRL:GATE_SLOW_PD = 0b11
Start-up current						
Maximum start-up current	$I_{START\_ILIM(max)}$	-	5.5	-	A	-

(table continues...)

Table 23 (continued) Electrical characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, typical programmable values are the default configuration of the device, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Programmable start-up current	START_ILIM	- - - - .. -	- 100 75 50 (default) .. 5	- - - - ... -	%	Set via PMBus™ (as a percentage of $I_{START\_ILIM(max)}$); I_SNS_CFG2:START_ILIM = 0b000 I_SNS_CFG2:START_ILIM = 0b001 I_SNS_CFG2:START_ILIM = 0b010 ... I_SNS_CFG2:START_ILIM = 0b111
Overcurrent protection						
Programmable local OC fault limit	I_{OC}	- - ... - ... -	- 0 ... 40 (default) ... 63.5	- - ... - ... -	A	Set via PMBus™; I_SNS_CFG1:LOCAL_OC_LIMIT = 0x00 ... I_SNS_CFG1:LOCAL_OC_LIMIT = 0x50 ... I_SNS_CFG1:LOCAL_OC_LIMIT = 0x7F
Programmable system OC reference voltage limit	V_{OC}	- - ... - ... -	- 0 ... 1.0025 (default) ... 1.35	- - ... - ... -	V	Set via PMBus™; I_SNS_CFG1:SYS_OC_LIMIT = 0x00 ... I_SNS_CFG1:SYS_OC_LIMIT = 0x9A ... I_SNS_CFG1:SYS_OC_LIMIT = 0xCF

(table continues...)

Table 23 (continued) Electrical characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, typical programmable values are the default configuration of the device, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Short circuit protection						
Programmable SOC fault limit (Primary)	I_{SOC_P}	- - ... - ... -	- 0 ... 80 (default) ... 126	- - ... - ... -	A	Set via PMBus™; I_SNS_CFG2:SOC_LIMIT_P = 0x00 ... I_SNS_CFG2:SOC_LIMIT_P = 0x28 ... I_SNS_CFG2:SOC_LIMIT_P = 0x3F
Programmable SOC fault limit (Secondary)	I_{SOC_S}	- - ... - ... -	- 0 ... 88 (default) ... 126	- - ... - ... -	A	Set via PMBus™; I_SNS_CFG2:SOC_LIMIT_S = 0x00 ... I_SNS_CFG2:SOC_LIMIT_S = 0x2C ... I_SNS_CFG2:SOC_LIMIT_S = 0x3F
Fixed start-up SOC fault limit	$I_{SOC\_STARTUP}$	-	9.375	-	A	Only during inrush current control i.e. in INIT_SOA_REG state
IMON						
IMON gain	G_{IMON}	- - -	- 10 20 (default)	- - -	µA/A	Set via PMBus™; TELEMETRY_AVG:GIMON_SEL = 0b0 TELEMETRY_AVG:GIMON_SEL = 0b1
IMON signal accuracy	$IMON_{ACC}$	-1 -3 -5	- - -	+1 +3 +5	%	IOUT ≥ 10 A; 5 A ≤ IOUT < 10 A; 2 A ≤ IOUT < 5 A
IMON operating voltage	V_{IMON}	-	-	1.35	V	-
Telemetry						
Current sense ADC resolution	ADC_I	–	12	-	bits	-
Voltage sense ADC resolution	ADC_V	-	12	-	bits	-

(table continues...)

Table 23 (continued) Electrical characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, typical programmable values are the default configuration of the device, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Monitored voltage range (input and output voltages)	V_{TLM_RNG}	-	88	-	V	-
Input voltage measurements accuracy	VIN_{ACC}	-1	0.5	1	%	At VINS vs GND: VINS = 40 V to 80 V
Output voltage measurements accuracy	$VOUT_{ACC}$	-1	0.5	1	%	At VOUTS vs GND: VOUTS = 40 V to 80 V
Current measurement accuracy (IMON voltage)	V_{IMON_ACC}	-1.5 -3	0.7 1.4	1.5 3	%	IOUT >= 10 A; 10 A > IOUT >= 5 A
Calculated input power accuracy	PIN_{ACC}	-2.5 -4	1.2 1.9	2.5 4	%	IOUT >= 10 A; 10 A > IOUT >= 5 A (PIN = VIN x IOUT)
Calculated energy accuracy	EIN_{ACC}	-4.5	2.5	4.5	%	PIN accumulated over time
Controller on-chip temperature measurement accuracy	$TEMP2_{ACC}$	-5	-	5	°C	-
MOSFET on-chip temperature measurement accuracy	$TEMP1_{ACC}$	–10	-	10	°C	-
PWRGD and GPOx						
Output low voltage	V_{OL_PG}	-	-	0.4	V	At 10 mA
Input low voltage	V_{IL_PG}	-	-	0.8	V	-
Input high voltage	V_{IH_PG}	2	-	-	V	-
Leakage current	I_{PG}	-	-	5	µA	At 5.5 V; output is HiZ.
Current sink capability	I_{PG_SINK}	-	-	10	mA	-
SDA and SCL						
Input high voltage	V_{IH}	2	-	-	V	-
Input low voltage	V_{IL}	-	-	0.8	V	-
Output low voltage	V_{OL}	-	-	0.4	V	At 20 mA
Leakage current	I_{SDA}	-	-	5	µA	At 5.5 V
Nominal bus voltage	V_{BUS}	3	3.3 or 5	5.5	V	-
Capacitive load per bus segment	C_{BUS}	-	-	400	pF	-
Pin capacitance	C_{SDA}	-	5	10	pF	-

(table continues...)

Table 23 (continued) Electrical characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, typical programmable values are the default configuration of the device, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ADDR						
Pin sense current at device power-up	I_{ADDR}	-	100	-	µA	-
FS						
FS pin sense current	I_{FS}	37	40	43	µA	-
FS pin threshold voltage	V_{FS_TH}	0.27	0.3	0.33	V	-
Quick output discharge (QOD)						
QOD current source	I_{QOD}	-	20	-	mA	-
MOSFET On-chip overtemperature (OT) protection						
Programmable OT fault limit	T_{OT}	- - ... - ... -	- -40 ... 166.5 (default) ... 175	- - ... - ... -	°C	Set via PMBus™; OT_FAULT_LIMIT = 0x000 ... OT_FAULT_LIMIT = 0xC4F ... OT_FAULT_LIMIT = 0xC7D
Programmable OT warning limit	T_{OT_WARN}	- - ... -	- -40 ... 175	- - ... -	°C	Set via PMBus™; OT_WARN_LIMIT = 0x000 ... OT_WARN_LIMIT = 0xC7D
Fixed OT hysteresis	T_{OT_HYS}	10	15	20	°C	-
Controller On-chip thermal shutdown (TSD) protection						
Programmable TSD fault limit	T_{TSD}	- - - -	- 125 135 145 (default)	- - - -	°C	Set via PMBus™; ONCHIP_TSD_FAULT_LIMIT = 0b00 ONCHIP_TSD_FAULT_LIMIT = 0b01 ONCHIP_TSD_FAULT_LIMIT = 0b10
Fixed TSD fault hysteresis	T_{TSD_HYS}	-	10	-	°C	-
Fixed TSD warning upper limit	$TSDW_{UTH}$	-	125	-	°C	-
Fixed TSD warning lower limit	$TSDW_{LTH}$	-	115	-	°C	-

(table continues...)

Table 23 (continued) Electrical characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, typical programmable values are the default configuration of the device, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Retry						
Programmable retry counter	*RC*	- - .. -	- 0 (default) ... infinite	- - ... -	-	Set via PMBus™; RETRY:RETRY_COUNTER = 0b000 ... RETRY:RETRY_COUNTER = 0b111

3.6 Timing characteristics

Table 24 Timing characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, typical parameter values are the default configuration of the device, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Enable (EN) pin						
Fixed EN pin deglitch time	t_{EN_D}	6.5	10	13.5	µs	Input filter before processing the signal.
Programmable EN deglitch time	t_{EN_DG}	- - - - ... -	- 0 4 8 (default) ... 512	- - - - ... -	ms	Set via PMBus™; WATCHDOG_TMR:EN_DG = 0b0000 WATCHDOG_TMR:EN_DG = 0b0001 WATCHDOG_TMR:EN_DG = 0b0010 ... WATCHDOG_TMR:EN_DG = 0b1010
Input Undervoltage (UV) protection						
Fixed UV pin deglitch time	t_{UV_DG}	6.5	10	13.5	µs	Input filter before processing the signal.
Input overvoltage (OV) protection						
Fixed OV pin fixed deglitch time	t_{OV_DG}	6.5	10	13.5	µs	Input filter before processing the signal.

(table continues...)

Table 24 (continued) Timing characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, typical parameter values are the default configuration of the device, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ADC						
Conversion rate of current, voltage and MOSFET temperature measurements	t_{ADC_IVT}	-	102.4	-	µs	-
Conversion rate of controller on-chip temperature measurements	t_{ADC_T}	-	3.3	-	ms	-
PWRGD						
Power good assertion deglitch time	t_{PG_DGR}	- - ... - ... -	- 0 ... 5 (default) ... 15	- - ... - ... -	ms	Set via PMBus™; PWRGD_DG_TMR:PWRGD_DG_TMR = 0b0000 ... PWRGD_DG_TMR:PWRGD_DG_TMR = 0b0101 ... PWRGD_DG_TMR:PWRGD_DG_TMR = 0b1111
Power good deassertion deglitch time	t_{PG_DGF}	- - ... -	- 0 (default) .. 15	- - ... -	ms	Set via PMBus™; PWRGD_DG_TMR:PWRGDN_DG_TMR = 0b0000 ... PWRGD_DG_TMR:PWRGDN_DG_TMR = 0b1111
Faults, warnings and timers						
Time for any gate discharge in fault state	$t_{FLT\_PD\_GATE}$	9	10	11	ms	-
Fault strong pull down activation time for fast gate discharge	$t_{FLT\_PD\_FAST}$	13.5	15	16.5	µs	-
Fault reaction time	$t_{FLT\_GATE\_OFF}$	-	0.3	1.0	µs	From fault triggered to activation of MOSFET's Gate turn-off.
FAULT pin hold time	t_{FAULT_MIN}	20	-	-	µs	At C_L= 50 pF; External pull-up resistor of 10 kΩ.

(table continues...)

Table 24 (continued) Timing characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, typical parameter values are the default configuration of the device, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Programmable retry cool down period	t_{COOLD}	- - ... -	- 0 ... 64 (default)	- - ... -	s	Set via PMBus™; RETRY:COOLD_TMR = 0b000 ... RETRY:COOLD_TMR = 0b111
Programmable retry OK deglitch timer	t_{RETD}	- - - ... -	- 0 0.5 (default) ... 8	- - - ... -	s	Set via PMBus™; RETRY:RETD_TMR = 0b000 RETRY:RETD_TMR = 0b001 ... RETRY:RETD_TMR = 0b111
Programmable UV timer	t_{UV}	- - ... -	- 0 (default) ... 1000	- - ... -	ms	Set via PMBus™; V_TMR:UV_TMR = 0b000 ... V_TMR:UV_TMR = 0b111
Programmable OV timer	t_{OV}	- - ... -	- 0 (default) ... 1000	1000	ms	Set via PMBus™; V_TMR:OV_TMR = 0b000 ... V_TMR:OV_TMR = 0b111
Fixed OVIN detection time	t_{OVIN_DET}	-	-	2.0	µs	-
Programmable OVIN deglitch timer	t_{OVIN}	- - ... -	- 0 (default) ... 1000	- - ... -	µs	Set via PMBus™; V_TMR:OVIN_TMR = 0b000 ... V_TMR:OVIN_TMR = 0b111
Programmable OUV timer	t_{OUV}	- - ... -	- 0 (default) ... 1000	- - ... -	ms	Set via PMBus™; V_TMR:OUV_TMR = 0b000 ... V_TMR:OUV_TMR = 0b111
Programmable watchdog timer	t_{WD}	- - ... - ... -	- 5 ... 1000 (default) ... 15000	- - ... - ... -	ms	Set via PMBus™; WATCHDOG_TMR:WATCHDOG = 0b0000 ... WATCHDOG_TMR:WATCHDOG = 0b1001 ... WATCHDOG_TMR:WATCHDOG = 0b1111

(table continues...)

Table 24 (continued) Timing characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, typical parameter values are the default configuration of the device, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Programmable OC deglitch timer	t_{SOAD}	- - ... - ... -	- 0 ... 2 (default) ... 2000	- - ... - ... -	ms	Used for LOCAL_OC_LIMIT and/or SYS_OC_LIMIT; Set via PMBus™; SOA_TMR:SOAD_TMR = 0b00000 ... SOA_TMR:SOAD_TMR = 0b00011 ... SOA_TMR:SOAD_TMR = 0b11111
Programmable local OC deglitch timer	t_{OCD}	- - - - ... -	- 50 100 200 (default) ... 1000	- - - - ... -	µs	Used for LOCAL_OC_LIMIT; Set via PMBus™; SOA_TMR:OCD_TMR = 0b000 SOA_TMR:OCD_TMR = 0b001 SOA_TMR:OCD_TMR = 0b010 ... SOA_TMR:OCD_TMR = 0b111
SOC fault response time	t_{SOC_DG}	-	400	-	ns	-
Programmable SOC fault deglitch timer	t_{SOC}	- - - - -	- 0 (default) 200 500 1000	- - - - -	ns	Set via PMBus™; SOA_TMR:SOC_DG_TMR = 0b00 SOA_TMR:SOC_DG_TMR = 0b01 SOA_TMR:SOC_DG_TMR = 0b10 SOA_TMR:SOC_DG_TMR = 0b11
QOD						
Fixed QOD deglitch time	$t_{QOD\_Deglitch}$	-	6	-	ms	It is started when the MOSFET is turned off.
Fixed QOD discharge time	$t_{QOD\_Discharge}$	-	1000	-	ms	It is started when the QOD is activated.
SYNC						
SYNC handshaking timeout	t_{SYNC_HSK}	-	10	-	µs	-

(table continues...)

Table 24 (continued) Timing characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, typical parameter values are the default configuration of the device, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
PMBus						
Clock frequency	f_{SCL}	10	-	1000	KHz	-
Detect clock low timeout	$t_{TIMEOUT}$	25	-	35	ms	-
Bus free time between STOP and START condition	t_{BUF}	0.5	-	-	µs	See PMBus timing diagram
Hold time after (REPEATED) START condition	$t_{HD:STA}$	0.26	-	-	µs	After this period, the first clock is generated; See PMBus timing diagram
REPEATED START condition setup time	$t_{SU:STA}$	0.26	-	-	µs	See PMBus timing diagram
STOP condition setup time	$t_{SU:STO}$	0.26	-	-	µs	See PMBus timing diagram
Data hold time	$t_{HD:DAT}$	0	-	-	ns	See PMBus timing diagram
Data setup time	$t_{SU:DAT}$	50	-	-	ns	See PMBus timing diagram
Clock low period	t_{LOW}	0.5	-	-	µs	See PMBus timing diagram
Clock high period	t_{HIGH}	0.26	-	50	µs	See PMBus timing diagram
Clock/data fall time	t_F	-	-	120	ns	The fall time measurement limits are defined as follows: Fall time limits: ($V_{IH,MIN}$ + 0.15 V) to ($V_{IL,MAX}$ - 0.15 V) See PMBus timing diagram
Clock/data rise time	t_R	-	-	120	ns	The rise time measurement limits are defined as follows: Rise time limits: ($V_{IL,MAX}$ - 0.15 V) to ($V_{IH,MIN}$ + 0.15 V) See PMBus timing diagram
PMBus deglitch time	t_{DGL_PMBUS}	50	-	-	ns	-

4 Application information

4.1 Standalone operation

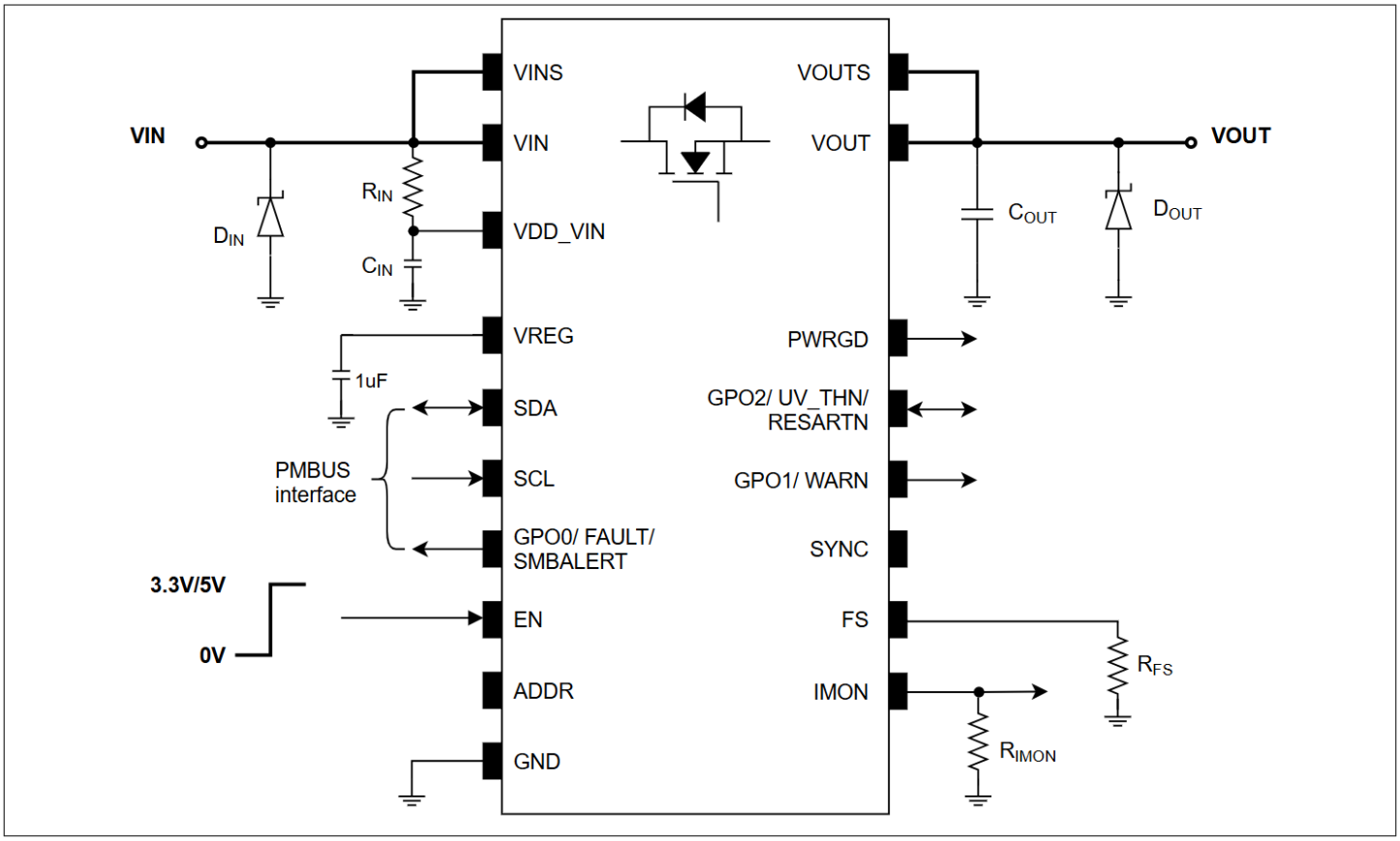


Figure 40 XDP730 typical application schematic (standalone eFuse)

4.2 Parallel operation

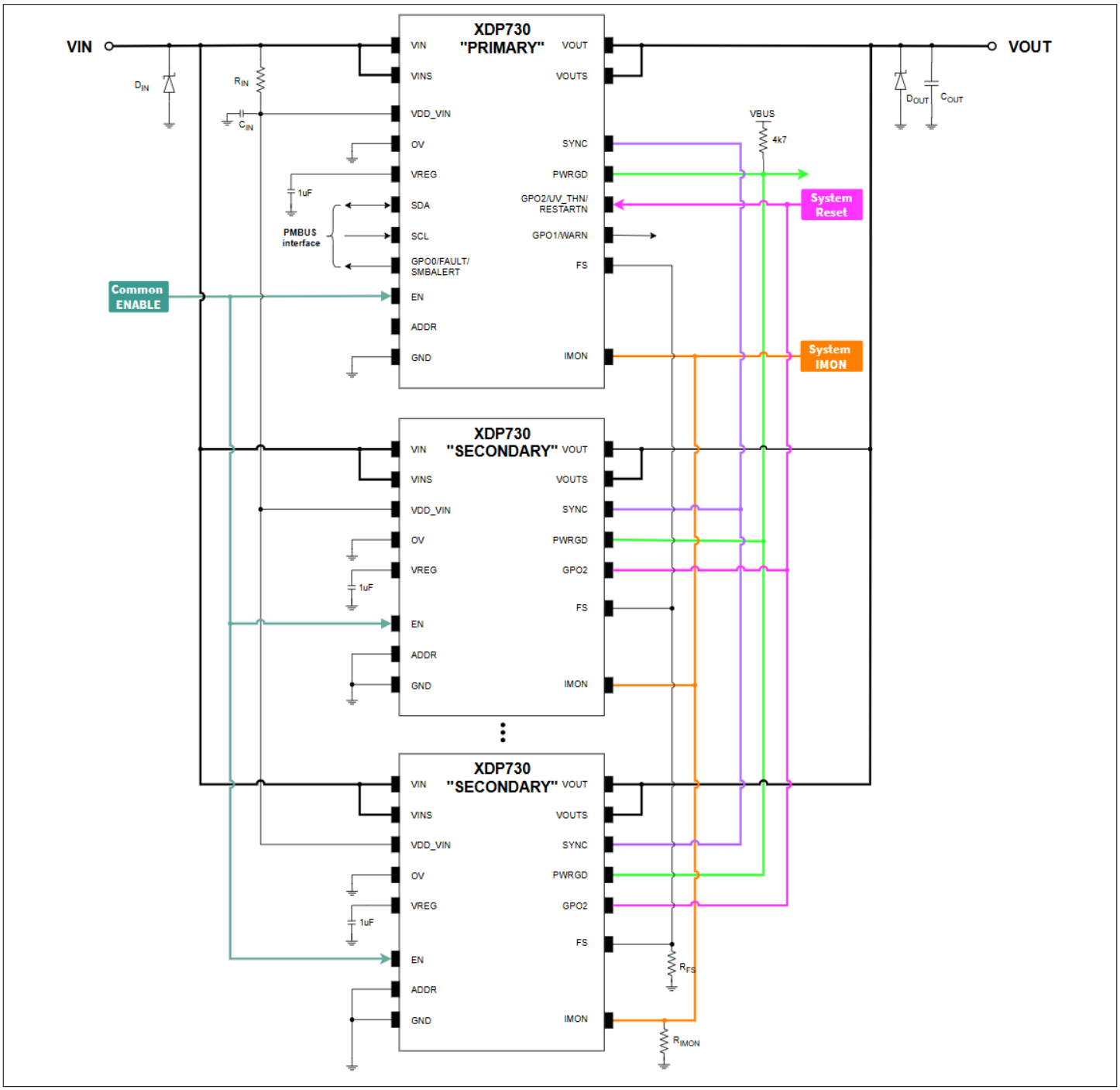


Figure 41 XDP730 typical application schematic (parallel operation)

The Figure 41 shows an example application schematic with multiple XDP730 devices in parallel. The following recommendations must be considered when designing such high-power systems.

- Connect the VDD_VIN, VIN, VOUT, EN, IMON, FS, GND and PWRGD pins of all the devices together.
- Each device must have a dedicated 1µF capacitor connected between its VREG and GND pins.
- IMON resistor must be calculated properly considering the total number of devices in parallel.
- ADDR pin of the SECONDARY devices must be tied to the GND pin.

- Connect all the GPO2 pins together with proper configuration and a single pull-up resistor, if the RESTART function is needed.
- Use proper TVS and/or Schottky diodes at the VIN and VOUT nets.

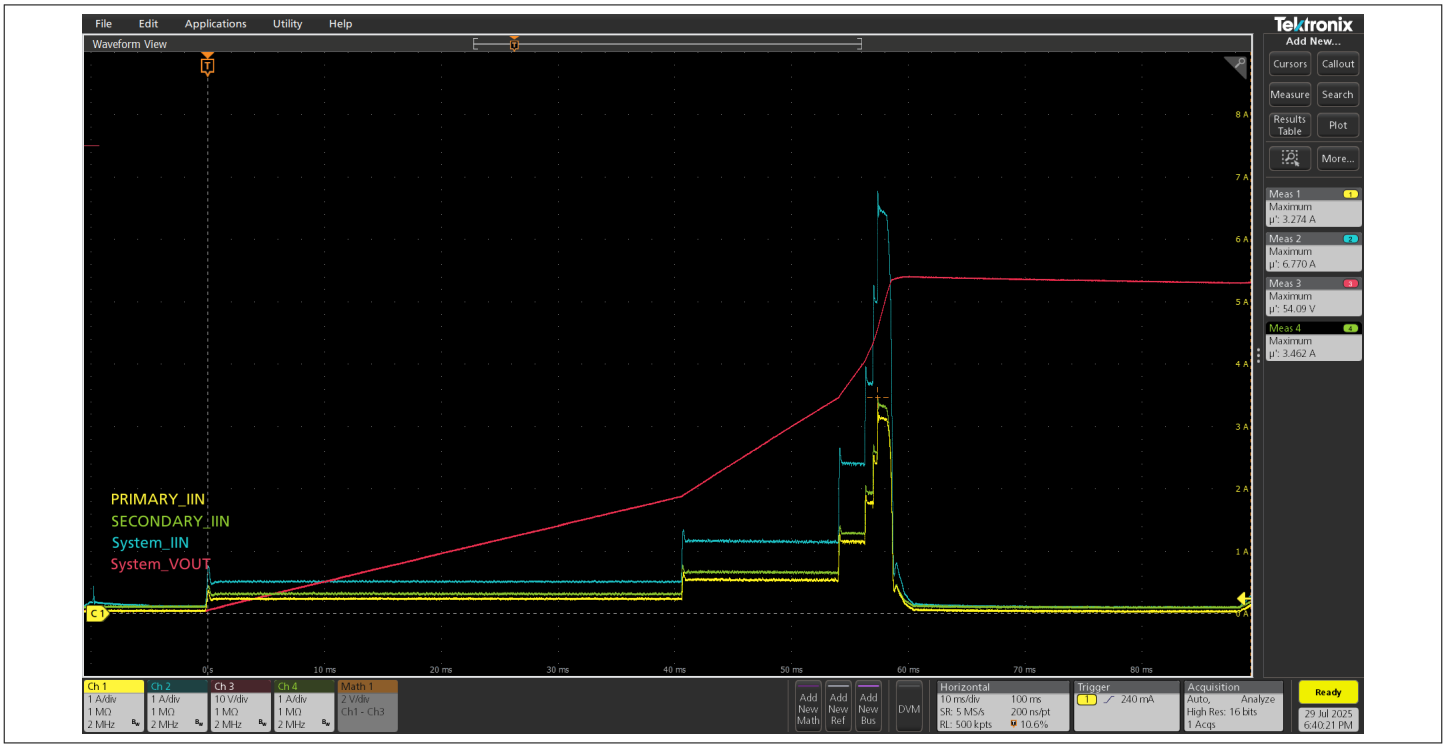


Figure 42 Parallel operation: Default turn-on

The Figure 42 shows a default turn-ON of two parallel connected XDP730-001 devices. As shown, the devices will start to turn-ON their MOSFETs almost at the same time because of the SYNC pins connection. Figure 43 shows the OV fault being independently triggered in the PRIMARY device. The OV fault in the PRIMARY leads to all the devices turning OFF their MOSFETs. In this case, the SECONDARY device does not trigger any fault as it is simply waiting for the PRIMARY device to release the SYNC pin.

Similarly, Figure 44 shows the OV fault being independently triggered in the SECONDARY device, which results in a SYNC fault being triggered in the PRIMARY device. Depending on the retry settings, the PRIMARY device handles the triggered SYNC fault. In this case, the retry cool down time is set to 4 s. Therefore, the PRIMARY device performs a successful retry attempt after 4 s as the fault in the SECONDARY is already released.

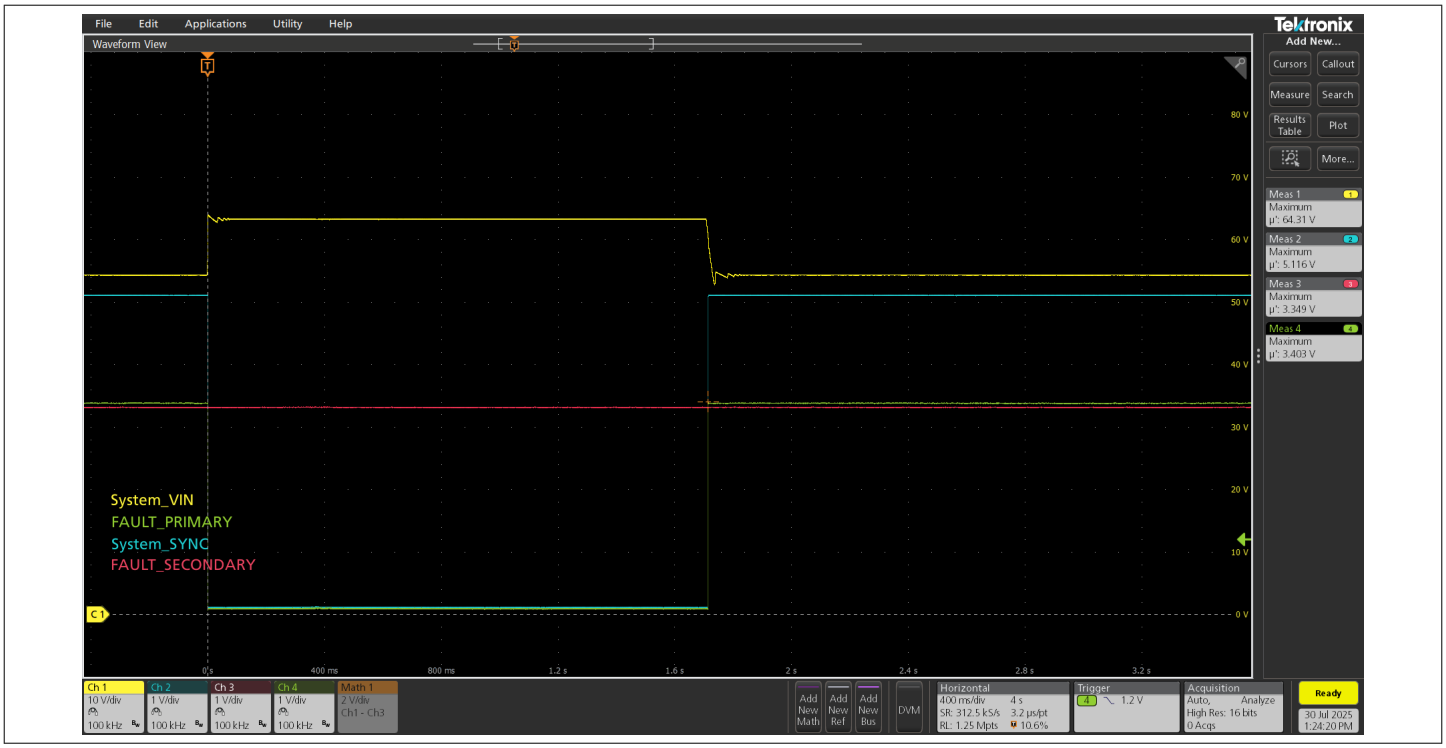


Figure 43 An input OV fault being triggered in PRIMARY device followed by a successful fault release

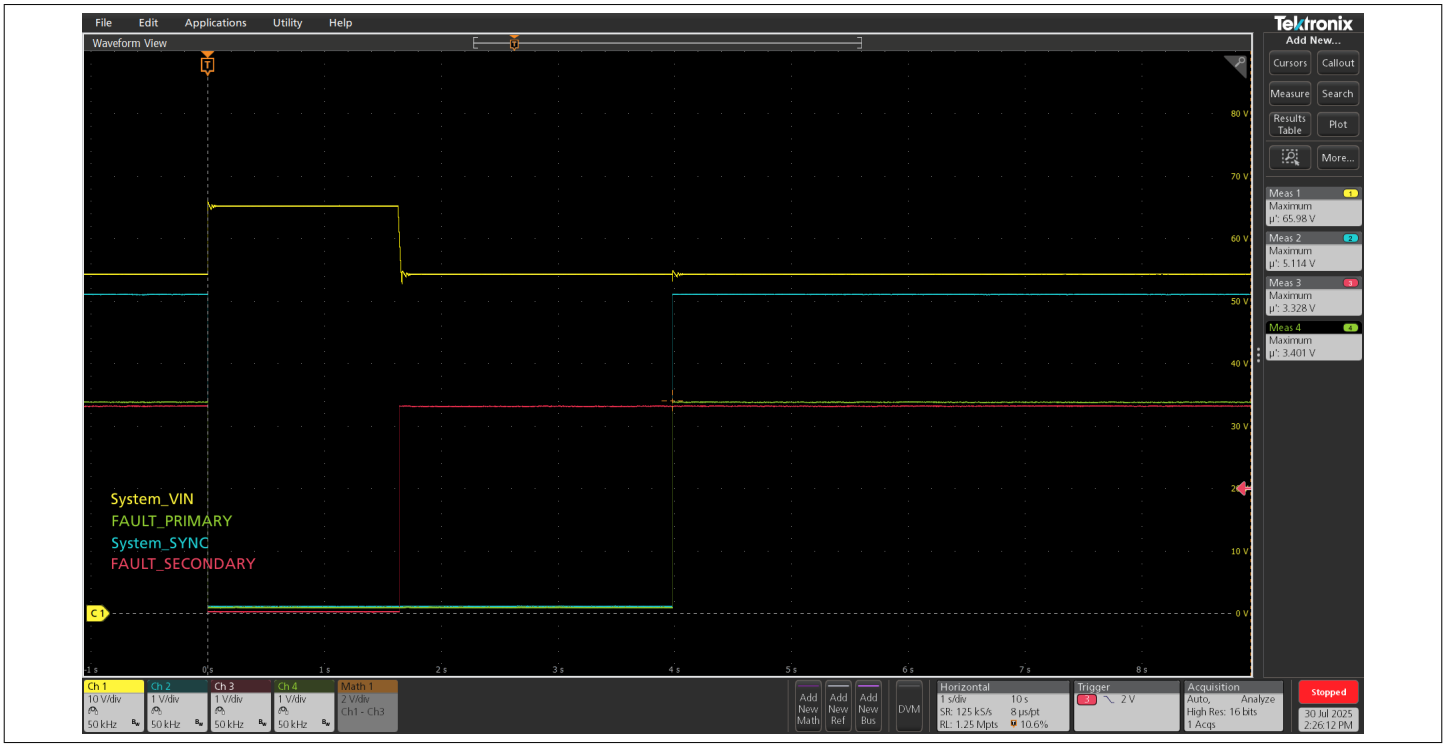


Figure 44 An OV fault being triggered in SECONDARY device resulting in a SYNC fault in PRIMARY device; Auto-retry enabled in PRIMARY with 4 s cool down time

4.3 Layout guidelines

The following guidelines shall be followed when designing the PCB for this device:

- VIN and VOUT pins (i.e. high-current carrying pins) must be properly sized to carry the necessary load current. Connect them to as much copper area as possible with thermal vias.

- Ceramic decoupling capacitors (~100 nF) are recommended at VIN and VOUT pins.
- An RC filter is recommended at the VDD_VIN pin with a minimum resistor value of 100 Ω. This is needed to support the surge immunity feature.
- A 1 µF capacitor is mandatory between the VREG pin and GND. It must be placed right next to the VREG pin.
- The GND pin must be connected to the PCB ground plane.
- If unused, the VINS and VOUTS pins must be connected to the nearest VIN and VOUT pins respectively.
- It is recommended to have a solid connection from the exposed pad to the VIN plane through many vias for effective thermal management of the device.
- Loading the SYNC pin must be avoided to minimize synchronization issues.
- Since the IMON pin resistor is essential for the current telemetry/protections, it is recommended to place it close to the IMON pin and avoid any nearby noisy signals.
- PMBus™ communication traces need a single-ended controlled impedance of 50 Ω. Therefore, their width must be adjusted accordingly.
- It is recommended to use TVS and/or Schottky diodes at VIN and VOUT pins to protect against voltage spikes.

4.4 PMBus direct format data conversion

This section gives an overview of converting PMBus direct format data into real-world values and vice-versa, using examples. The complete list of conversion coefficients/equations is already discussed in Chapter 2.13.3.

4.4.1 Voltage

Voltage levels/telemetry data conversion is straight forward. Let us consider the VIN_OV_FAULT_LIMIT as an example.

From Table 14, we know the coefficients associated with the voltage related commands:

m = 4653

b = 0

R = -2

The PMBus direct format code equivalent to 64 V is calculated using the following formula.

$$Y = \left(mX + b\right) \times 10^{R} \tag{7}$$

$$Y = \left(4653 \times 64 + 0\right) \times 10^{-2} \tag{8}$$

$$Y = 2978(in \quad decimal) = 0x0BA2 \tag{9}$$

So the value to be programmed in VIN_OV_FAULT_LIMIT, for 64 V input overvoltage level, is 0x0BA2.

Now, let us assume the value in the READ_VIN command is 0x08B9 = 2233 (in decimal). The following formula is used with the same coefficients to convert this data into Volt i.e. "real-world" value.

$$X = \frac{1}{m} \times \left(Y \times 10^{-R} - b\right) \tag{10}$$

$$X = \frac{1}{4653} \times \left(2233 \times 10^{-(-2)} - 0\right) \tag{11}$$

$$X = \sim 48V \tag{12}$$

4.4.2 Current

The load/MOSFET current is a bit tricky to convert from PMBus™ direct format to "real-world" value and vice-versa. Therefore, the equations shown in Chapter 2.13.3 must be readjusted.

Let us consider the IOUT_OC_WARN_LIMIT = 15 A as an example with the R_{IMON} = 2 kΩ and G_{IMON} = 20 µA/A.

From Table 14, we know the coefficients associated with the current related commands:

m = 24668

b = 0

R = -4

The PMBus™ direct format code equivalent to 15 A is calculated using the following formula.

$$Y = \left(mX + b\right) \times 10^{R} \tag{13}$$

where,

$$X = I_{OUT}(A) \times G_{IMON}(\mu A/A) \times R_{IMON}(k\Omega) \tag{14}$$

$$Y = \left(\left(24668 \times 15 \times 20 \times 2\right) + 0\right) \times 10^{-4} \tag{15}$$

$$Y = 1480(in \quad decimal) = 0x05C8 \tag{16}$$

So the value to be programmed in IOUT_OC_WARN_LIMIT in this example, for the 15 A overcurrent warning level, is 0x05C8.

Now, let us assume the value in the READ_IOUT command is 0x05A1 = 1441 (in decimal). The following formula is used with the same coefficients and "X" to convert this data into Ampere i.e. "real-world" value.

$$X = \frac{1}{m} \times \left(Y \times 10^{-R} - b\right) \tag{17}$$

where,

$$X = I_{OUT}(A) \times G_{IMON}(\mu A/A) \times R_{IMON}(k\Omega) \tag{18}$$

$$I_{OUT} = \frac{\left(Y \times 10^{-R}\right) - b}{m \times G_{IMON}(\mu A/A) \times R_{IMON}(k\Omega)} \tag{19}$$

$$I_{OUT} = \frac{\left(1441 \times 10^{-(-4)}\right) - 0}{24668 \times 20 \times 2} \tag{20}$$

$$I_{OUT} = \sim 14.60394A \tag{21}$$

4.4.3 Temperature

The temperature protection levels/telemetry data conversion is straight forward. Let us consider the OT_FAULT_LIMIT as an example.

From Table 14, we know the coefficients associated with the MOSFET temperature related commands:

m = 54

b = 22521

R = -1

The PMBus™ direct format code equivalent to 100°C is calculated using the following formula.

$$Y = \left(mX + b\right) \times 10^{R} \tag{22}$$

$$Y = \left(54 \times 100 + 22521\right) \times 10^{-1} \tag{23}$$

$$Y = 2792(in \quad decimal) = 0x0AE8 \tag{24}$$

So the value to be programmed in OT_FAULT_LIMIT, for 100°C MOSFET overtemperature level, is 0x0AE8.

Now, let us assume the value in the READ_TEMPERATURE_1 command is 0x0A00 = 2560 (in decimal). The following formula is used with the same coefficients to convert this data into °C i.e. "real-world" value.

$$X = \frac{1}{m} \times \left(Y \times 10^{-R} - b\right) \tag{25}$$

$$X = \frac{1}{54} \times \left(2560 \times 10^{-(-1)} - 22521\right) \tag{26}$$

$$X = \sim 57.018°C \tag{27}$$

4.4.4 Power

As the input power depends on the load/MOSFET current, it follows similar steps to convert PMBus™ direct format to "real-world" and vice-versa. Let us consider the PIN_OP_WARN_LIMIT as an example with the R_{IMON} = 2 kΩ, G_{IMON} = 20 µA/A and P_{IN} (i.e. VIN * IOUT) = 1000 W.

From Table 14, we know the coefficients associated with the power related commands:

m = 4486

b = 0

R = -1

The PMBus™ direct format code equivalent to 1000 W is calculated using the following formula.

$$Y = \left(mX + b\right) \times 10^{R} \tag{28}$$

where,

$$X = P_{IN}(W) \times G_{IMON}(\mu A/A) \times R_{IMON}(k\Omega) \times 10^{-3} \quad (29)$$

$$Y = \left(\left(4486 \times 1000 \times 20 \times 2 \times 10^{-3}\right) + 0\right) \times 10^{-1} \quad (30)$$

$$Y = 17944(in \quad decimal) = 0x4618 \quad (31)$$

So the value to be programmed in PIN_OP_WARN_LIMIT in this example, for the 1000 W overpower warning level, is 0x4618.

Now, let us assume the value in the READ_PIN command is 0x1500 = 5376 (in decimal). The following formula is used with the same coefficients and "X" to convert this data into Watt i.e. "real-world" value.

$$X = \frac{1}{m} \times \left(Y \times 10^{-R} - b\right) \quad (32)$$

where,

$$X = P_{IN}(W) \times G_{IMON}(\mu A/A) \times R_{IMON}(k\Omega) \times 10^{-3} \quad (33)$$

$$P_{IN} = \frac{\left(Y \times 10^{-R}\right) - b}{m \times G_{IMON}(\mu A/A) \times R_{IMON}(k\Omega) \times 10^{-3}} \quad (34)$$

$$P_{IN} = \frac{\left(5376 \times 10^{-(-1)}\right) - 0}{4486 \times 20 \times 2 \times 10^{-3}} \quad (35)$$

$$P_{IN} = \sim 299\,.\,5987W \quad (36)$$

4.4.5 Energy

Energy is calculated based on the 16-bit power, therefore, the same coefficients shall be used. Since energy is a product of power and time, it is also required to know the time between the samples.

From Table 14, we know the coefficients associated with the energy related commands:

m = 4486

b = 0

R = -1

Two samples are required for the conversion in four steps. Let us consider the two READ_EIN samples as shown in the following table:

Table 25 READ_EIN samples

	First sample		Second sample	
	in hex	**in decimal**	**in hex**	**in decimal**
SAMPLE_COUNT	0x1000	4096	0x3DC7	15815
ROLLOVER_COUNT	0x10	16	0xFF	255
ENERGY_COUNT	0x01FF	511	0x1FAC	8108

Step 1: Calculate the power difference between the samples using the following formula.

$$Power \quad difference = Append(ROLLOVER\_COUNT; \quad ENERGY\_COUNT)_{second\_sample} - Append(ROLLOVER\_COUNT; \quad ENERGY\_COUNT)_{first\_sample} \tag{37}$$

$$Power \quad difference = 0xFF1FAC - 0x1001FF \tag{38}$$

$$Power \quad difference = 0xEF1DAD = 15670701(in \quad decimal) \tag{39}$$

Step 2: Calculate the SAMPLE_COUNT difference between the samples using the following formula.

$$SAMPL\_COUNT \quad difference = SAMPLE\_COUNT_{second\_sample} - SAMPLE\_COUNT_{first\_sample} \tag{40}$$

$$SAMPL\_COUNT \quad difference = 0x3DC7 - 0x1000 = 0x2DC7 = 11719 \quad (in \quad decimal) \tag{41}$$

Step 3: Calculate the average power per sample using the following formula.

$$Average \quad power = \frac{Power \quad difference}{SAMPLE\_COUNT \quad difference} \tag{42}$$

$$Average \quad power = \frac{15670701}{11719} = 1337\left(in \quad decimal\right) \tag{43}$$

Step 4: Convert the calculated average power into the "X" value in Watt using the following formula.

$$X = \frac{1}{m} \times \left(Y \times 10^{-R} - b\right) \tag{44}$$

$$X = \frac{1}{4486} \times \left(1337 \times 10^{-(-1)} - 0\right) \tag{45}$$

$$Average \quad power(W) = X = \sim 2.98W \tag{46}$$

Step 5: Calculating the energy in Joule

The time between samples can either be measured or calculated. This device has an ADC conversion rate of 102.4 µs. This is also the time it takes to get a sample of energy, so the time between samples can be determined by multiplying the SAMPLE_COUNT difference with 102.4 µs.

$$Time\quad difference(s) = SAMPLE\_COUNT\quad difference \times 102.4\mu s \tag{47}$$

$$Time\quad difference\left(s\right) = 11719 \times 102.4 \times 10^{-6} = \sim 1.2s \tag{48}$$

Finally, now the energy can be calculated by multiplying average power with time difference as follows.

$$Energy(J) = Average\quad power(W) \times Time\quad difference(s) \tag{49}$$

$$Energy(J) = 2.98 \times 1.2 = \sim 3.576J \tag{50}$$

5 Package information

5.1 Ordering information

Table 26 Ordering information table

Basic part number	Orderable part number	Description
XDP730	XDP730-001	Positive input voltage 30 A eFuse IC with PMBus™.

5.2 Package outline

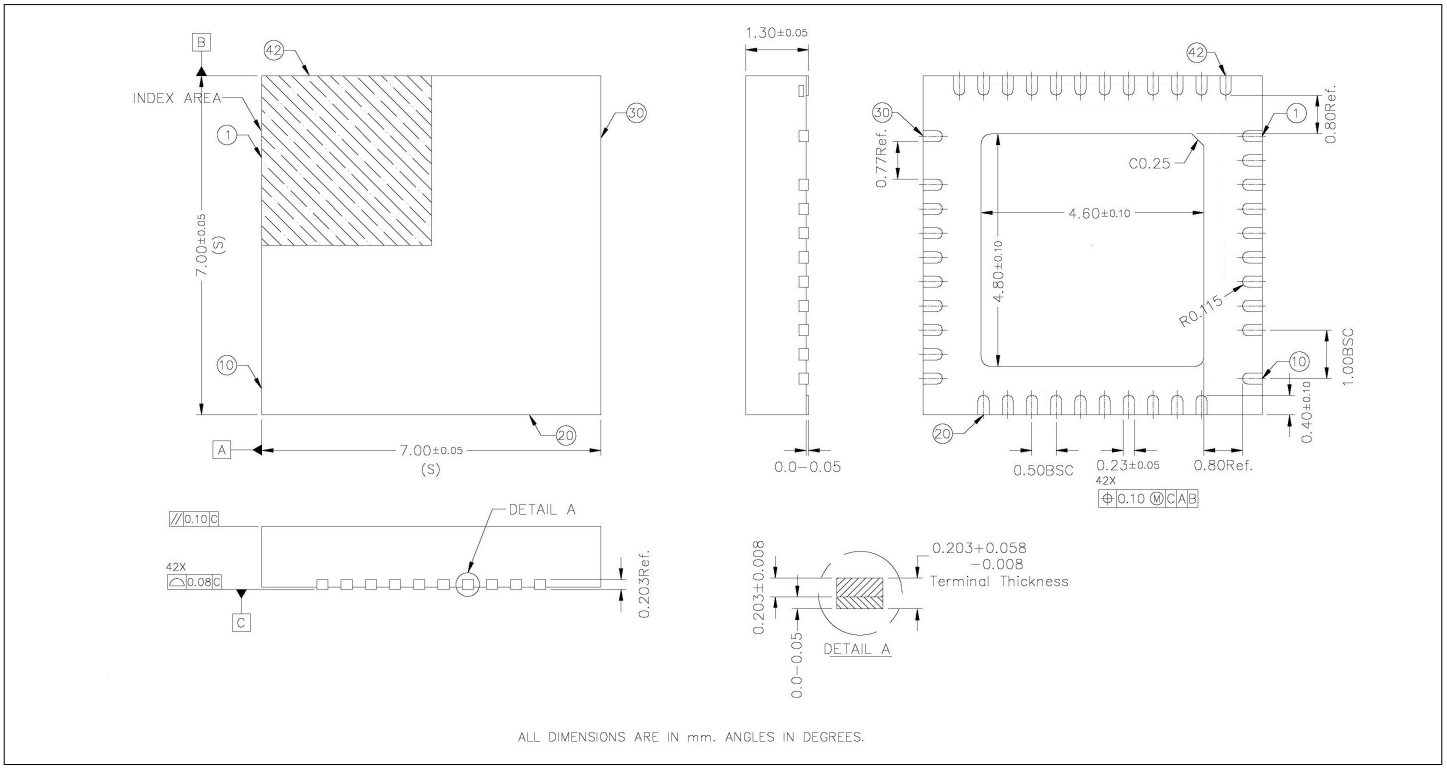


Figure 45 XDP730-001 package dimensions

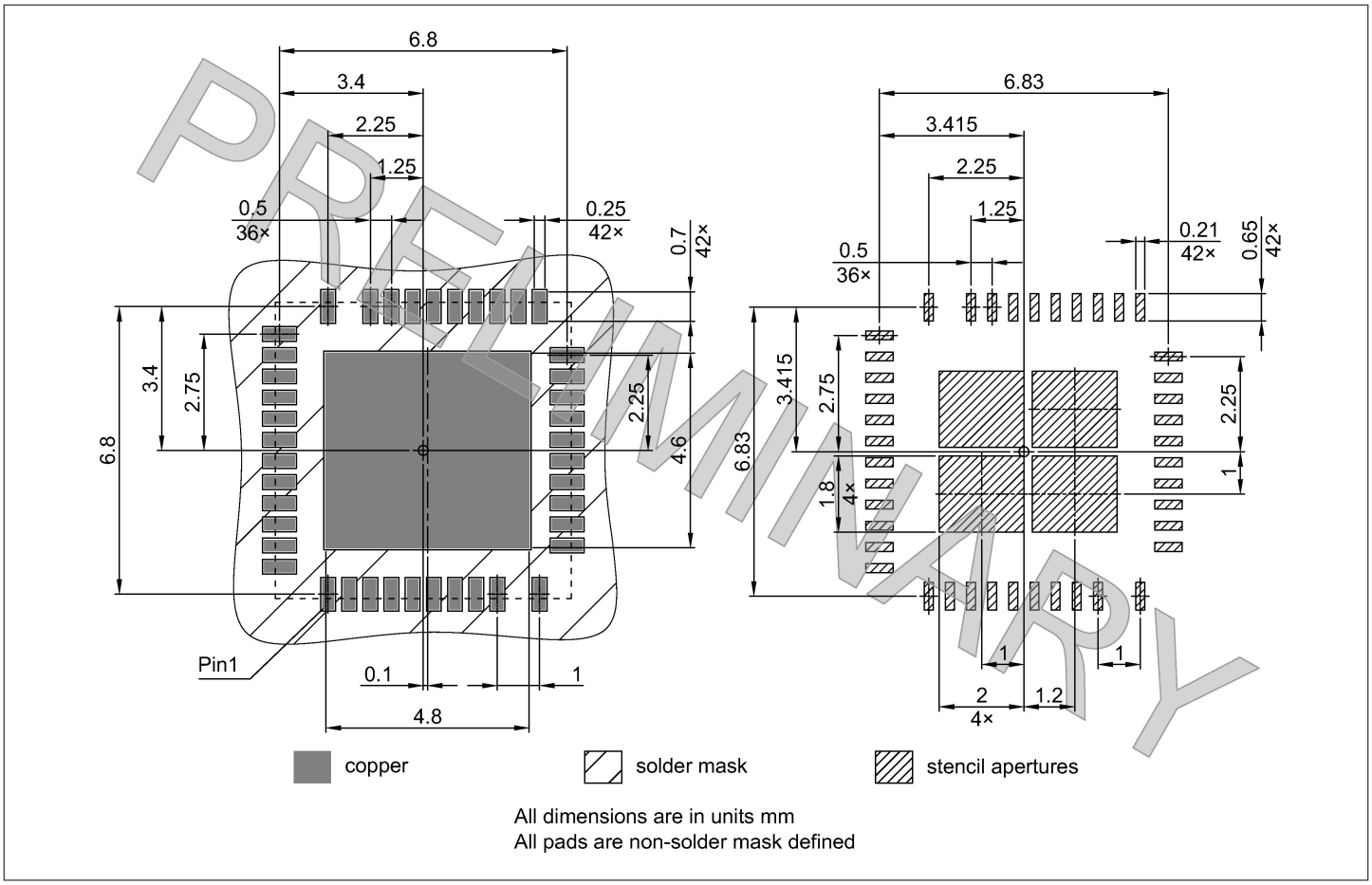
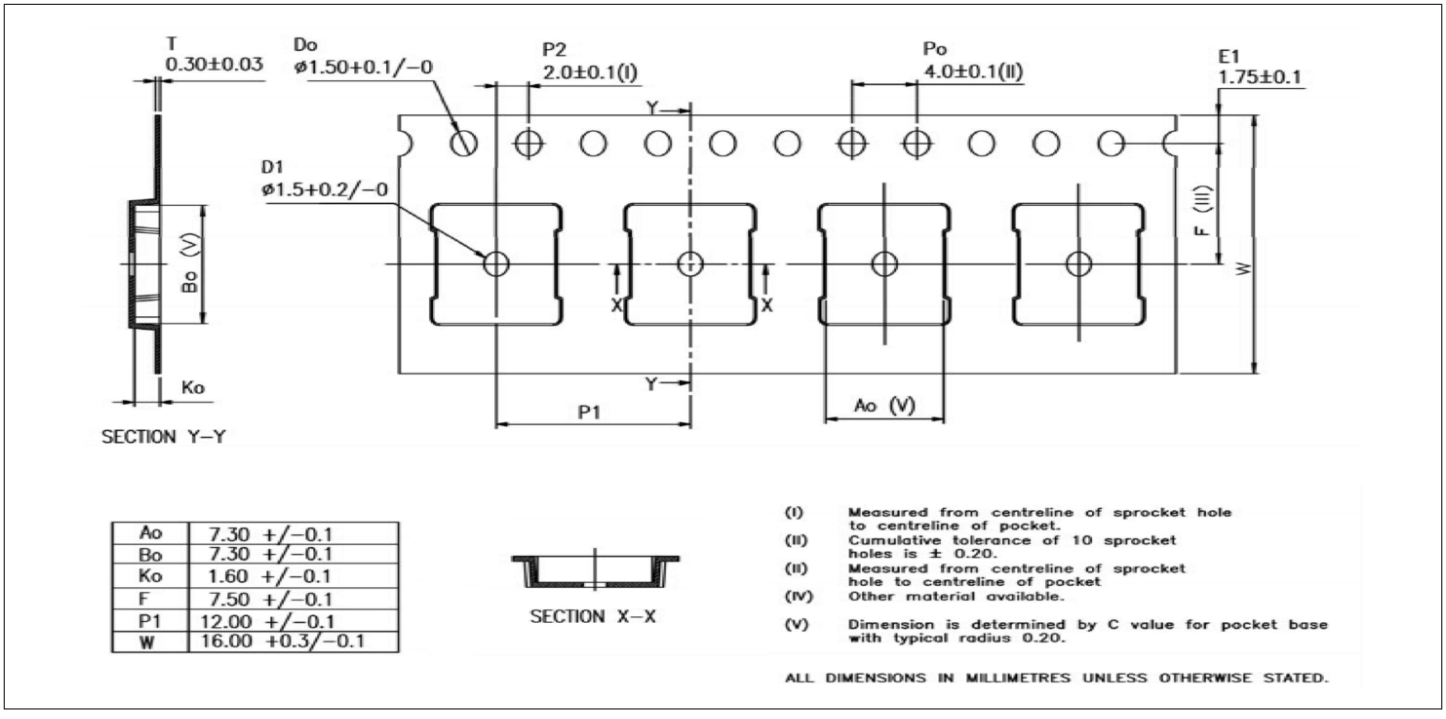


Figure 46 XDP730-001 recommended footprint



Ao	7.30 +/−0.1
Bo	7.30 +/−0.1
Ko	1.60 +/−0.1
F	7.50 +/−0.1
P1	12.00 +/−0.1
W	16.00 +0.3/−0.1

Figure 47 PG-LIQFN-42-1 package information

Green Product (RoHS compliant)

To meet the worldwide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). Further information on packages: https://www.infineon.com/packages

6 Revision history

Revision	Date	Notes (major changes since last revision)
0.96	2025-10-08	Seventh draft. (Document is restructured)
0.95	2025-09-29	Sixth draft. (Auto-Retry note is updated; Packing (Tape-Reel) information is added)
0.94	2025-08-29	Fifth draft. (Telemetry accuracies and MOSFET $R_{DS(on)}$ updated)
0.93	2025-08-20	Fourth draft.
0.92	2025-03-14	Third draft.
0.91	2025-03-07	Second draft.
0.9	2024-10-15	First draft.

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