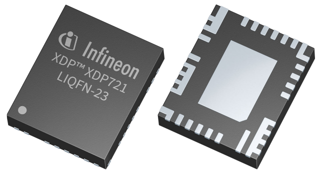
XDP™ XDP721/2

20 A eFuse without PMBus®



Features

- Wide input voltage range: 7 V to 80 V
- Integrated 100 V, ~3 mΩ OptiMOS™ FET with current sensor
- Controller and built-in GATE driver
- Maximum Continuous Current: up to 20 A
- Inrush current protection using digital SOA control with active FET SOA protection
- Parallel operation for higher current applications with active current sharing at start-up
- "Primary/standalone" or "secondary" device operation mode for stacking multiple eFuses
- Integrated die temperature sensors
- Analog current (IMON) reporting and monitoring with up to ± 1% accuracy
- Fast short circuit protection
- Fault response: auto-retry (XDP722) or latch-off (XDP721)
- Fault protections: input undervoltage, input overvoltage, output undervoltage, overcurrent, severe overcurrent, unsuccessful MOSFET turn-on, pre-charged output voltage (VDS), FET health, thermal shutdown, etc.
- Sequential turn-on capability
- IPC2221B and IPC9592B high-voltage compliant
- PG-LIQFN-23 lead, 6 mm x 5 mm package
- - 40°C to + 125°C operating junction temperature

Potential applications

- Fan tray/control applications
- Servers and datacenters
- Power distribution systems

Product validation

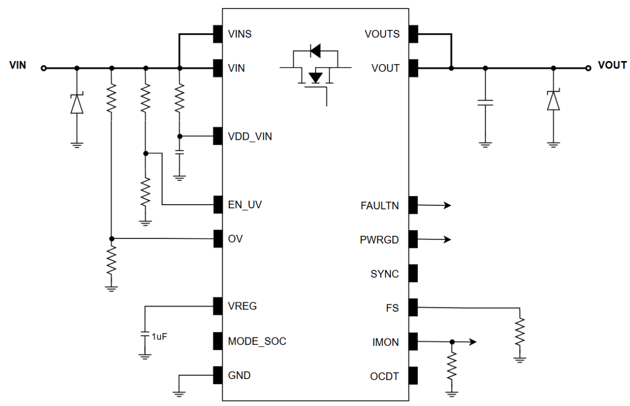
Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

XDP721 is a 20 A eFuse with integrated ~3 mΩ $R_{DS(on)}$ OptiMOS™ FET, current sensor, controller and a built-in GATE driver. It is an IPC2221B and IPC9592B HV standard compliant device that ensures reliable inrush current control and continuous system health monitoring. The digital SOA control with active SOA protection ensures that the integrated MOSFET always operates under safe conditions. When multiple XDP721 ICs are connected in parallel, the active current sharing during start-up maintains safety conditions in high-power systems. A simplified schematic is shown below for reference.

XDP721 reports analog current at the IMON pin for post-processing. It incorporates various system protections and generates appropriate protection responses depending on the incident's severity. This device comes in two variants depending on the fault response, i.e. auto-retry (XDP722) or latch-off (XDP721).

It is available in a 6 mm x 5 mm 23pin PG-LIQFN package and is specified over a - 40°C to + 125°C junction temperature range.



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1 Pin configuration

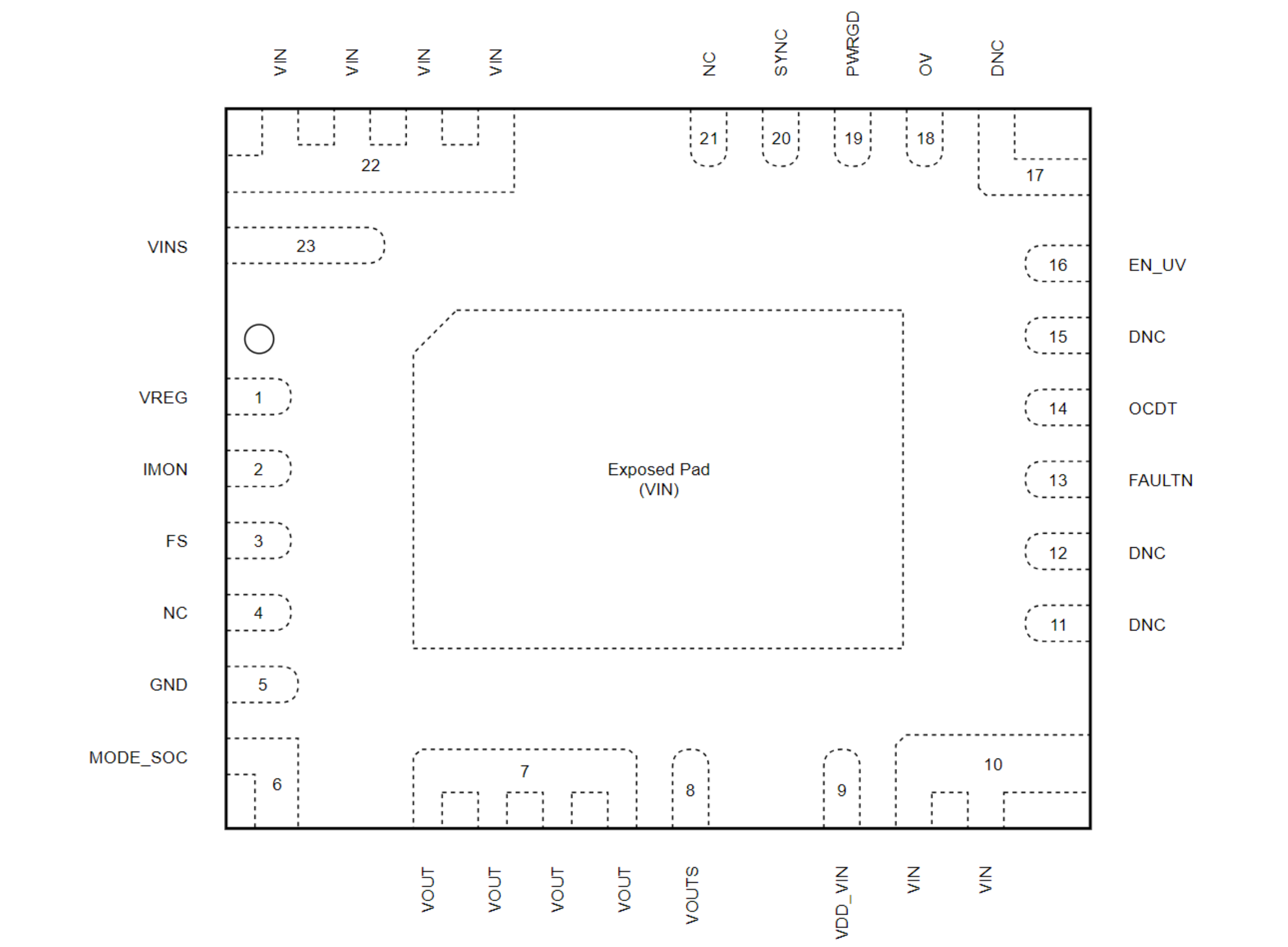


Figure 1 XDP721 device pinout (top view)

Table 1 XDP721 pinout

Pin #	Name	Type	Description	If unused, connect to
1	VREG	O	VREG (internal 5 V regulator) output pin. A 1 µF capacitor from this pin to GND is mandatory.	Connect a 1 µF capacitor from this pin to GND
2	IMON	IO	Analog current monitor pin. This pin reports/sources a current proportional to the monitored MOSFET current (IMON) level. This pin is also monitored for current protection levels. A resistor is mandatory from this pin to GND.	Resistor to GND
3	FS	I	Fail-Safe pin for turn-on fail safety. A resistor greater than 9.06 kΩ is recommended from this pin to GND.	Open (PRIMARY); Connect to the PRIMARY's FS pin at resistor to GND (SECONDARY)
4, 21	NC	-	Not connected pin.	-

(table continues...)

Table 1 **(continued) XDP721 pinout**

Pin #	Name	Type	Description	If unused, connect to
5	GND	-	Ground reference terminal (to be connected to system ground).	GND
6	MODE_SOC	I	Device mode and SOC configuration input pin It can be left open, tied to GND directly or through a resistor to configure the device mode and the severe overcurrent, i.e. short-circuit protection level.	Open
7	VOUT	O	Output voltage terminal.	VOUT
8	VOUTS	I	Output voltage sense pin.	VOUT
9	VDD_VIN	I	Power supply pin. A 100 Ω – 100 nF RC filter is recommended at this pin.	VIN
10, 22	VIN	I	Input voltage terminal.	VIN
11, 12, 15, 17	DNC	-	Do not connect pin.	Open
13	FAULTN	O	FAULTN open drain output pin. his pin asserts low when a fault has occurred.	Open
14	OCDT	I	Overcurrent deglitch timer input pin. This pin configures the OC deglitch, i.e. blanking time. Connect a resistor from this pin to GND, see details.	Open
16	EN_UV	I	Enable/input undervoltage pin. The MOSFET is turned on when $V_{EN\_UV} \geq V_{EN\_UV\_UTH}$. The UV fault is triggered if V_{EN_UV} level is lower than $V_{UV\_LTH\_P}$ (or $V_{UV\_LTH\_S}$).	Pull-up to VREG
18	OV	I	Input overvoltage pin. The OV fault is triggered if $V_{OV} > V_{OV\_UTH}$.	-
19	PWRGD	O	Power good open drain output pin. It is asserted high when VOUT has reached its final level i.e. steady state, the MOSFET is fully enhanced and no faults are detected.	Open
20	SYNC	IO	SYNC open drain pin with internal pull-up. This pin is used to synchronize multiple XDP72x devices connected in parallel. It is functionally similar to the FAULTN pin.	Open (PRIMARY); Connect to the PRIMARY's SYNC pin (SECONDARY)
23	VINS	I	Input voltage sense pin.	VIN
EP	VIN	I	Input voltage terminal.	VIN

2 Block diagram

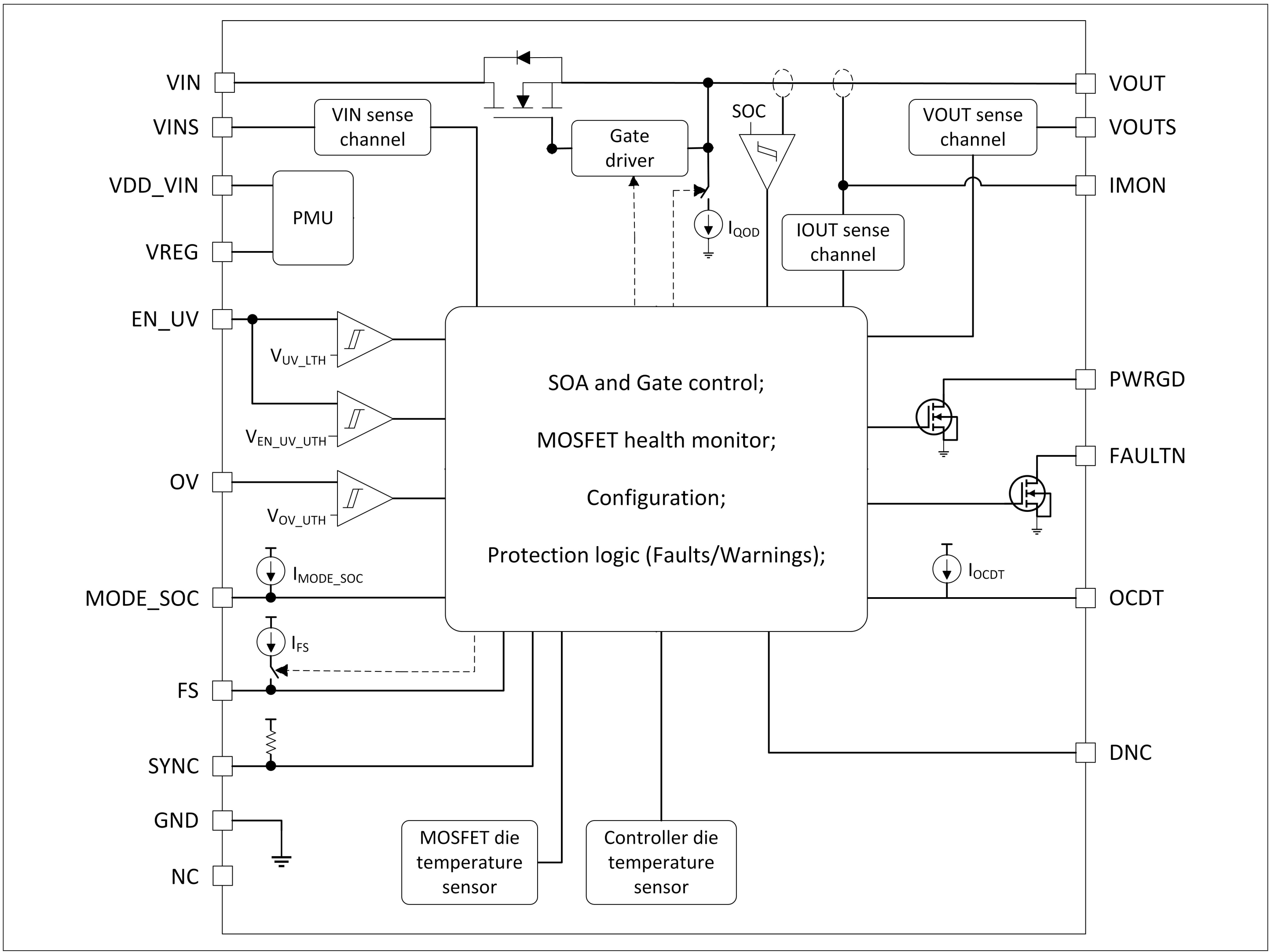


Figure 2 **XDP721/22 block diagram**

3 Functional description

XDP721 is a 20 A eFuse with integrated low $R_{DS(on)}$ OPTIMOS™ FET, current sensor, die temperature sensors, controller and a built-in GATE driver. The device becomes fully operational when the voltage on the VDD_VIN pin crosses 9 V. If there are no faults and the EN_UV pin is raised above $V_{EN\_UV\_UTH}$, then the enable deglitch timer (t_{EN_DG}) is initiated which allows the input supply on VIN pins to stabilize. The device waits until this timer has expired and then starts the MOSFET turn-on procedure. Its proprietary digital SOA control mechanism ensures that the inrush current never exceeds the safe operating limits of the MOSFET. The device establishes stable output voltage at VOUT pins after the MOSFET is successfully turned on. The PWRGD pin is used to signal the load/microcontroller that VOUT is ready.

The input voltage, current, output voltage, internal MOSFET temperature and internal controller temperature are constantly monitored by the device to ensure proper protection. It also reports a current proportional to the current flowing through the device on the IMON pin. There are many protections incorporated in this device to protect itself and the system load. These include input undervoltage, input overvoltage, overcurrent, severe overcurrent, overtemperature, thermal shutdown and MOSFET health checks to name a few. The FAULTN pin asserts low (active low) when a fault condition is triggered. There are two variants of this device (XDP721 and XDP722) with different fault responses. When a fault has occurred, the XDP721 will directly enter the latch-off state whereas the XDP722 will perform auto-retry.

This device has the ability to quickly discharge its output voltage. It is designed to address the ever-increasing power demands of the market. Multiple XDP72x devices can be connected in parallel to increase the system power. The SYNC pin and FS pin always ensure that all the devices in the chain are synchronized, and the main/PRIMARY device is alive in the system. A fault in any device will cause all the devices to turn off their MOSFETs, thus disconnecting the system load from the input supply. The PRIMARY device will then react accordingly whereas the SECONDARY devices will simply follow the PRIMARY device.

***Attention**: XDP722 can be considered as XDP721 with the Auto-Retry function. This document is valid for both the product variants.*

3.1 Configuration modes

In XDP72x, the MODE_SOC pin is used to configure two important parameters, namely the device mode of operation and the severe overcurrent (SOC) protection level. The Table 2 below shows the MODE_SOC pin configuration.

Table 2 Configuration of MODE_SOC pin

MODE_SOC pin voltage (V)	MODE_SOC pin resistance (kΩ)	Device mode	SOC level setting (A)
$V_{MODE\_SOC} > 2.8$ (Open)	Open	PRIMARY	22
$2.2 < V_{MODE\_SOC} \le 2.8$	24.9		33
$1.7 < V_{MODE\_SOC} \le 2.2$	19.6		44
$1.3 < V_{MODE\_SOC} \le 1.7$	15		55
$0.9 < V_{MODE\_SOC} \le 1.3$	11	SECONDARY	55
$0.6 < V_{MODE\_SOC} \le 0.9$	7.5		44
$0.3 < V_{MODE\_SOC} \le 0.6$	4.53		33
$V_{MODE\_SOC} \le 0.3$ (GND)	GND		22

Device mode configuration is extremely useful in parallelizing multiple XDP72x devices for high power designs. In order to turn-on its MOSFET, the SECONDARY device relies on the I_{FS} current from the PRIMARY device for failsafe check using the FS pin. The SECONDARY configured device will not have an independent auto-retry capability as it simply follows the PRIMARY device in the system. Refer Chapter 5 for high power design.

Note: *In a high power design, only the PRIMARY configured XDP722 will have the auto-retry fault response. See Chapter 3.9.2 for more details.*

3.2 Power-up sequence

When using XDP721 in an application, the main input power supply bus is connected to the VIN pins whereas the VDD_VIN pin is connected to the VIN through an RC filter. This RC filter helps to get a stabilized VDD_VIN level, which is the input supply to the device's controller section. When the VDD_VIN level rises above 7 V, the internal regulator VREG output is set to ~5 V level and all the analog/digital pins are released after a successful check. It is mandatory to have a 1 uF capacitor connected from the VREG pin to GND. Figure 3 shows a simplified XDP721 power-up sequence.

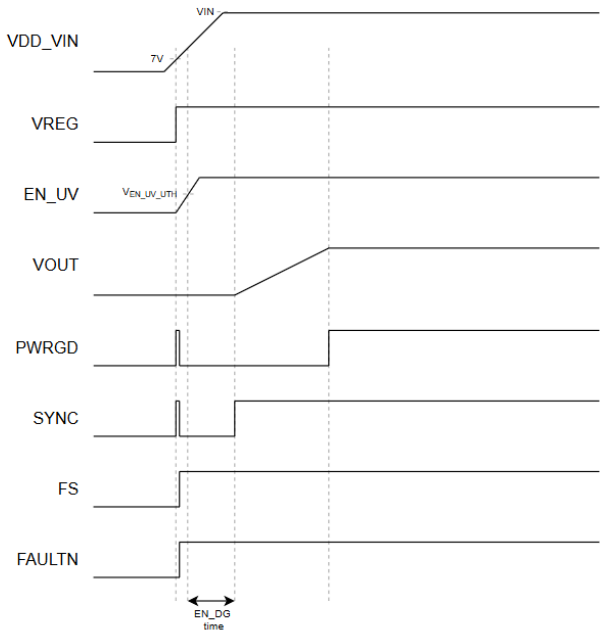


Figure 3 **XDP721 power-up sequence (PWRGD and FAULTN are pulled up to VREG)**

3.2.1 FailSafe

This device has a turn-on fail safety mechanism to ensure that the SECONDARY devices in the system will not turn-on their MOSFETs if the PRIMARY device is damaged. After a successful device power-up, the PRIMARY configured device will source I_{FS} current on its FS pin. A resistor from this pin to GND aids every device in the system to constantly sense the FS pin voltage (V_{FS}). Each device will only allow its MOSFET to turn-on if V_{FS} >= V_{FS_TH}, else it triggers SYNC fault.

***Note**:*
- *Every device has an internal pull-down resistor (R_{FS_PD}) at the FS pin.*
- *The device will enter LATCH-OFF state when a SYNC fault is triggered due to FS. It can only be released reliably, by performing a device power cycle.*

3.2.2 SYNC procedure

When multiple XDP72x devices are connected in parallel to increase system power, it becomes extremely crucial to properly synchronize them. This is achieved by connecting all the SYNC pins together. Every device has a SYNC pin with internal control and sense lines. At device power-up, the SYNC pin is internally held low by the device until all checks are successful. It is only released and pulled high once the enable deglitch timer has expired without any fault conditions. This way all the devices will turn-on their MOSFETs at the same time when SYNC goes high, provided all other turn-on conditions are present. When a fault is triggered, the device will pull its SYNC pin low based on the type of fault. This is seen by the other devices almost immediately, which forces them to turn-off their MOSFETs to protect the system. The SECONDARY configured device also performs a SYNC handshaking protocol to ensure that the PRIMARY device in the system is properly taking control over the SECONDARYs. If, for some reason, the PRIMARY device fails to respond within t_{SYNC_HSK} then the SECONDARY device will treat it as an unsuccessful SYNC handshaking and gets latched off.

Attention**: **SYNC pin is functionally similar to the FAULTN pin.

3.2.3 Enable and disable

The EN_UV pin is used to enable or disable the device output by controlling the MOSFET. There is an analog comparator at the EN_UV pin which senses its voltage. As shown in the table below, the MOSFET is allowed to turn-on if the voltage on this pin is higher than the threshold level i.e. $V_{EN\_UV\_UTH}$, along with mentioned conditions.

Table 3 MOSFET turn-on conditions

FS	SYNC	EN_UV	State of the MOSFET
V_{FS} >= V_{FS_TH}	H	V_{EN_UV} >= $V_{EN\_UV\_UTH}$	Active (can be ON / OFF due to fault)
V_{FS} < V_{FS_TH}	x	x	OFF
x	L	x	OFF
x	x	x	OFF
x	x	V_{EN_UV} < $V_{UV\_LTH\_x}$	OFF

The enable deglitch timer (t_{EN_DG}) is started when the EN_UV pin voltage rises above $V_{EN\_UV\_UTH}$. This timer protects the device from contact bouncing during hotswap events. In addition to enabling/disabling the device, the EN_UV pin can also be used to clear any faults using its HIGH-to-LOW transition as described in Chapter 3.9.2.2.

***Attention**: At power-up, the MOSFET can only be turned on when the EN_UV pin voltage is above the $V_{EN\_UV\_UTH}$ level and the OV pin voltage is below the V_{OV_LTH} level.*

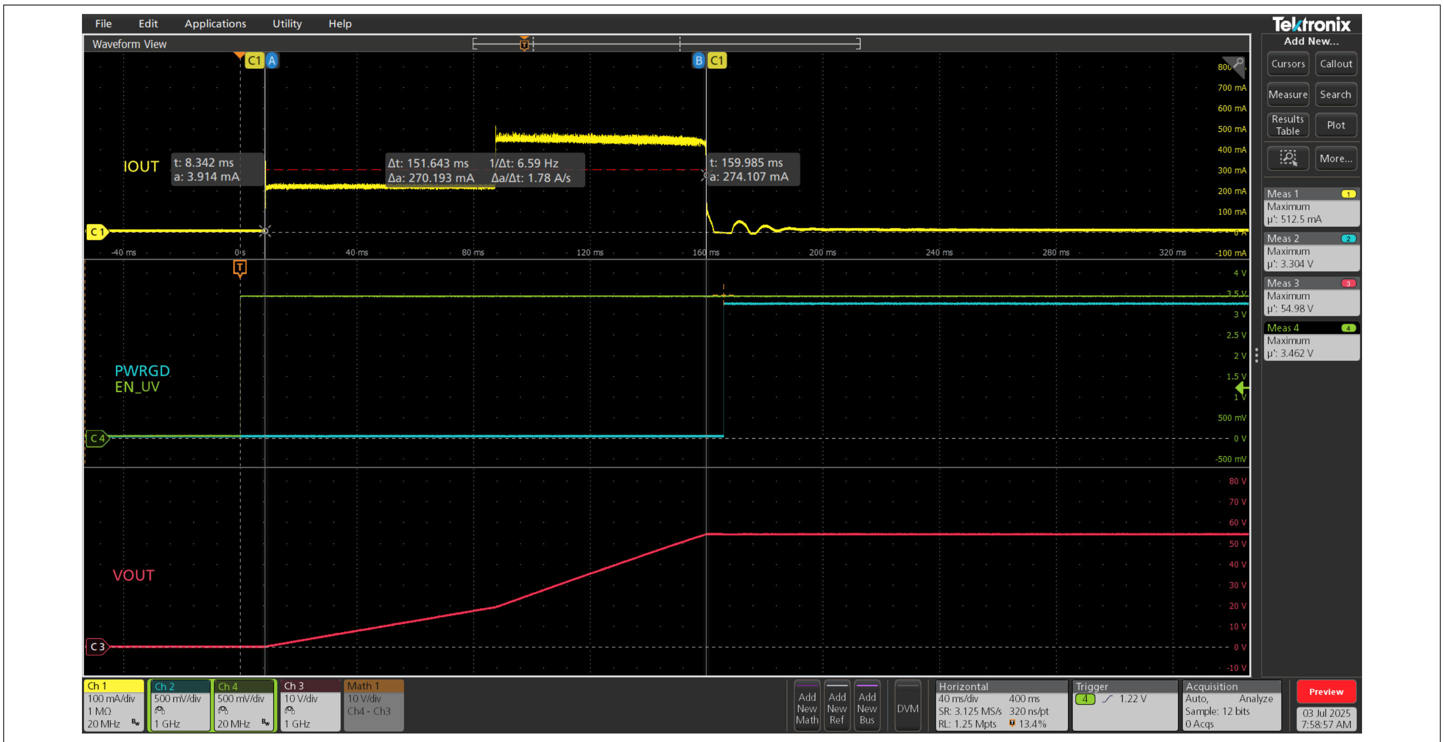


Figure 4 Default turn-on; C_{OUT} = 1 mF

3.2.3.1 Undervoltage function

Generally, every system that uses an eFuse is designed for a specific operating voltage range. The XDP721 has an undervoltage protection for monitoring the minimum input voltage. When the EN_UV pin voltage falls to/below $V_{UV\_LTH\_P}$ (or $V_{UV\_LTH\_S}$), the input undervoltage protection (UV) is triggered. The equation below can be used to calculate the values of the resistor divider network at the EN_UV pin as shown in Figure 5.

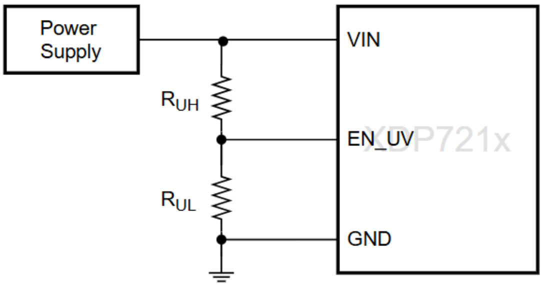


Figure 5 **Input undervoltage protection**

$$UV(V) = V_{UV\_LTH\_x}(V) \times \frac{R_{UH}(k\Omega) + R_{UL}(k\Omega)}{R_{UL}(k\Omega)} \quad (1)$$

where $V_{UV\_LTH\_x}$ is the input undervoltage threshold ($V_{UV\_LTH\_P}$ or $V_{UV\_LTH\_S}$) in volt and UV is the desired undervoltage limit in Volt.

***Note**: At power-up, the UV detection begins only after the EN_UV pin voltage (V_{EN_UV}) has crossed the fault level (i.e. $V_{UV\_LTH\_x}$) and the EN_DG timer has expired for the first time.*

3.2.3.2 Overvoltage function

Similar to input undervoltage, the XDP721 has input overvoltage protection for monitoring the maximum input voltage. When the OV pin voltage rises to/above V_{OV_UTH}, the input overvoltage protection (OV) is triggered. The equation below can be used to calculate the values of the resistor divider network at the OV pin as shown in Figure 6.

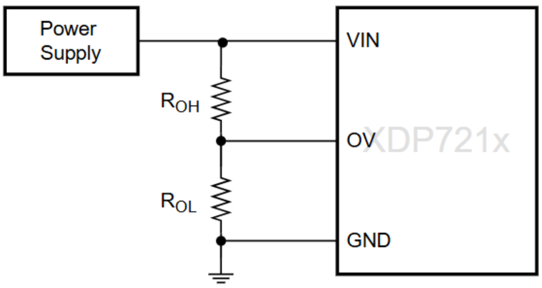


Figure 6 **Input overvoltage protection**

$$OV(V) = V_{OV\_UTH}(V) \times \frac{R_{OH}(k\Omega) + R_{OL}(k\Omega)}{R_{OL}(k\Omega)} \quad (2)$$

where V_{OV_UTH} is the input overvoltage threshold in Volt and OV is the desired overvoltage limit in Volt.

In a PRIMARY configured device, there is an additional "backup" on-chip overvoltage (OVIN) limit set to 80 V, to protect the device against bad design or OV setting.

3.3 Inrush current control

The main purpose of an eFuse is to minimize the inrush current during hotswap events, especially in high-availability systems such as servers, data centers, etc. Most eFuses in the market use soft-start, i.e. dvdt method of inrush current control. Although this approach is relatively simple to implement in eFuse, it is not completely safe for the MOSFET. During MOSFET turn-ON, the current can easily go beyond the safe operating area (SOA) limits due to the linear dvdt start-up method, which can damage the MOSFET. Therefore, we at Infineon use our proprietary “Digital SOA control” approach for the inrush current control as shown in Figure 7. This approach keeps the MOSFET in the SOA during the turn-ON procedure and is simple to configure from the user's perspective.

The SOA control loop consists of a closed loop system that senses the input voltage, output voltage and the current flowing through the MOSFET internally. The device calculates the MOSFET's V_{DS} by subtracting VOUT from VIN i.e. V_{DS} = VIN - VOUT, and regulates the MOSFET's current according to the SOA/control loop limits. This regulation is achieved by adjusting the MOSFET's V_{GS}.

Thus, current limitation delays the charging of the output capacitor, significantly reducing the inrush current at start-up while keeping the MOSFET safe at all times.

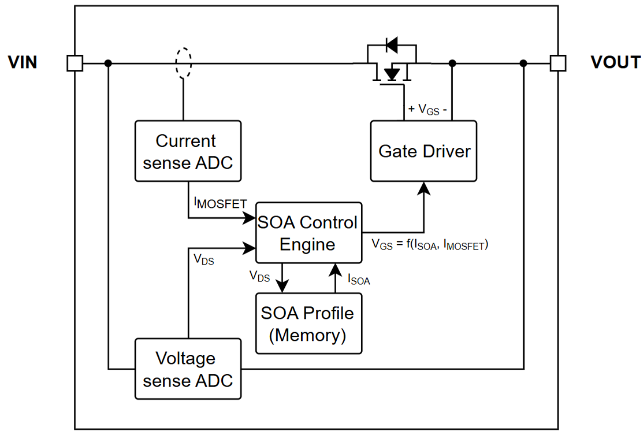


Figure 7 Digital SOA based inrush current control

Figure 8 shows the internal MOSFET's SOA chart with the maximum allowed start-up current limit (I_{START_ILIM}). The severe overcurrent i.e. short circuit limit ($I_{SOC\_STARTUP}$) at start-up is also shown in the Figure 8. It provides a fast response in case the inrush current reaches a critical level.

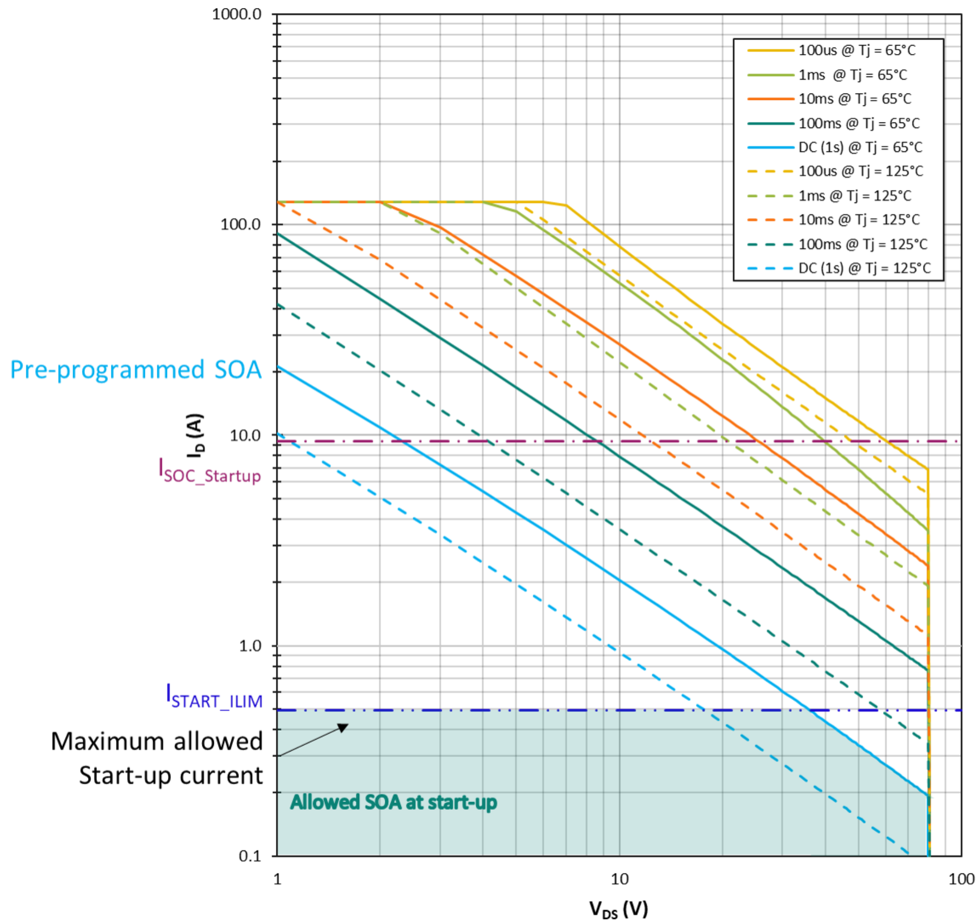


Figure 8 MOSFET's SOA chart during start-up

The SOA is digitally stored as a look-up table with 80 values, corresponding to V_{DS} = 1 V to 80 V. Each entry represents the MOSFET's current allowed for that V_{DS} level and has a resolution of 0.5 A. As an example, let us consider the inrush current control in a typical 54 V input application.

- Before the MOSFET is turned on, there is 54 V at the input and 0 V at the output with respect to ground. As the output capacitor is discharged at the start-up, V_{DS} = 54 V.
- The device starts charging the output capacitor by regulating the MOSFET. As shown in Figure 9, the control loop allows an I_{SOA} = 0.25 A at 54 V.
- As the capacitor charges, the V_{DS} of the MOSFET starts to reduce which allows more current to flow through the MOSFET as per the control loop limits.
- When V_{DS} reaches ~35 V, the allowed MOSFET current will be increased to ~0.495 A i.e. I_{START_ILIM}.

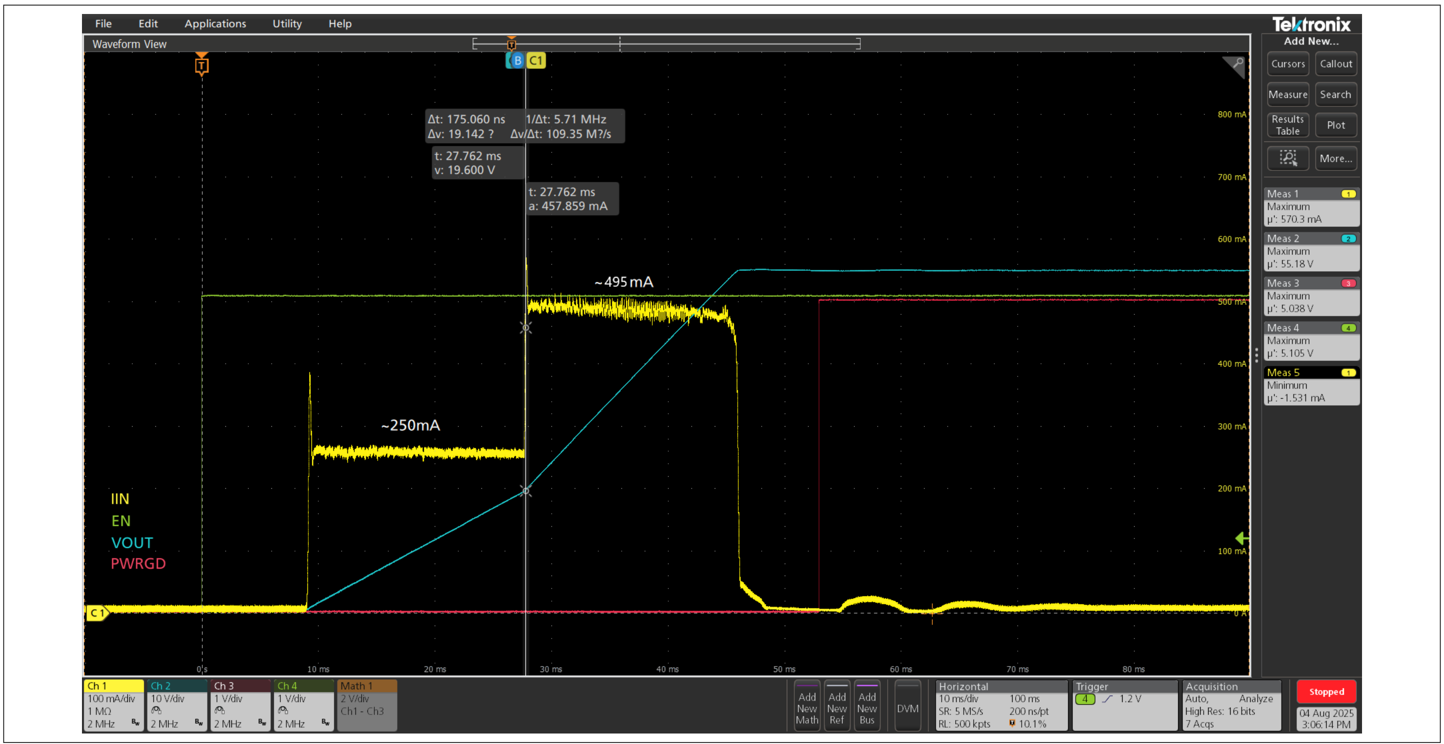


Figure 9 **Inrush control for C_{OUT} = 270 µF**

3.4 Current limit settings

XDP721 has multiple current protection levels for maximum flexibility/configurability. This includes a fixed start-up current limit (I_{START_ILIM}), two overcurrent limits (via IMON pin and back-up overcurrent limit) and a severe overcurrent limit (via MODE_SOC pin).

Since overcurrent and severe overcurrent protections are triggered during steady-state operation of the MOSFET, the Figure 10 must be referred to configure these fault limits correctly.

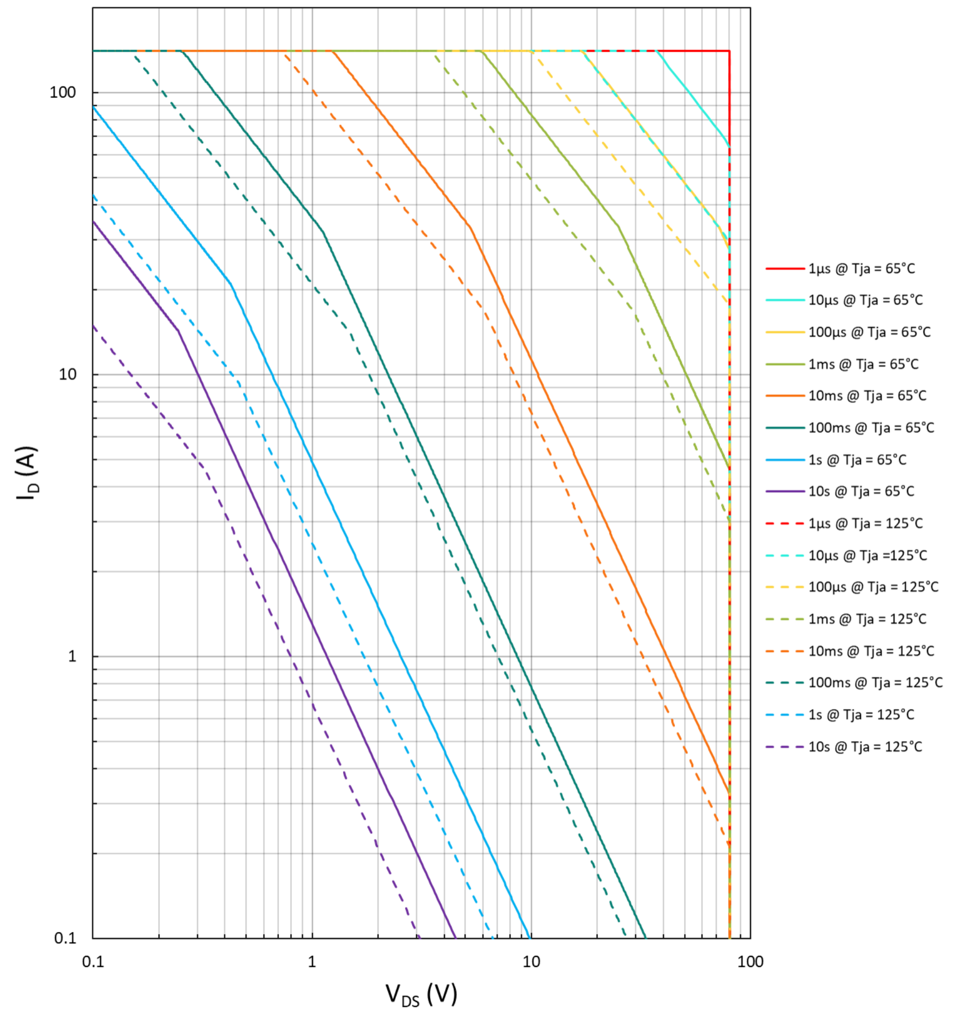


Figure 10 **MOSFET's SOA chart during ON state i.e. steady-state operation**

3.4.1 Start-up current setting

In this device, the start-up current limit (I_{START_ILIM}) is fixed to ~495 mA. This start-up current limit is only considered during inrush control i.e. MOSFET turn-on procedure. It is disregarded as soon as the steady state is reached.

During MOSFET turn-on, the XDP721 allows the current to flow through the device as per the MOSFET's allowed SOA limits until its VDS drops to ~35 V. Thereafter, the start-up current is limited to 495 mA as shown in Figure 8.

3.4.2 Overcurrent setting

After a successful turn-on, the device reaches steady state and activates the overcurrent (OC) protection along with the continuous current reporting on its IMON pin with a gain of G_{IMON}. In a PRIMARY configured device, the system overcurrent protection is triggered if the IMON pin voltage (V_{IMON}) reaches the reference threshold (V_{SYS_OC}) level. The IMON resistor required to generate the system overcurrent protection can be calculated using the following equation (3).

$$R_{IMON}(\Omega) = \frac{V_{SYS\_OC}(V)}{G_{IMON}(\mu A/A) \times 10^{-6} \times I_{SYS\_OC}(A)} \quad (3)$$

where G_{IMON} is the IMON gain, V_{SYS_OC} is the reference fault threshold and I_{SYS_OC} is the desired overcurrent limit.

It is possible to add some deglitch/delay time to the system overcurrent detection using the OCDT pin, as shown in the table below.

Table 4 Configuration of OCDT pin

OCDT pin voltage (V)	OCDT pin resistance (kΩ)	Description (OC deglitch time in ms)
$V_{OCDT} > 2.8$ (Open)	Open	0
$2.2 < V_{OCDT} \leq 2.8$	12.4	0.5
$1.7 < V_{OCDT} \leq 2.2$	9.76	1
$1.3 < V_{OCDT} \leq 1.7$	7.5	2
$0.9 < V_{OCDT} \leq 1.3$	5.49	4
$0.6 < V_{OCDT} \leq 0.9$	3.74	10
$0.3 < V_{OCDT} \leq 0.6$	2.32	20
$V_{OCDT} \leq 0.3$ (GND)	GND	50

There is also a local/backup overcurrent limit (I_{BKP_OC}) to protect the device if the system overcurrent protection is not set properly. This local overcurrent protection has a fixed fast deglitch/delay time (t_{BKP_OC}).

Note:
- *Overcurrent protection using the IMON pin i.e. system overcurrent level, is only possible in a PRIMARY configured device.*
- *Local/Backup overcurrent level triggers the Overcurrent protection, irrespective of the device mode.*

3.4.3 Severe overcurrent setting

During short circuit (i.e. surge or high di/dt current) events, the current flowing through the MOSFET may reach a dangerous level which can critically damage the system load. The device has a fast comparator to protect against such severe overcurrent (SOC) incidents. It can quickly respond by turning off the MOSFET with a strong pull-down current. The complete SOC response time from the moment it is detected till the MOSFET is turned off is t_{SOC_DG}. As mentioned in Chapter 3.1 section, the SOC protection level is configured using the MODE_SOC pin setting.

Note: *The SOC level during the MOSFET turn-on procedure is fixed to $I_{SOC\_STARTUP}$.*

3.5 Power good (PWRGD)

A power good (PWRGD) pin is available in this device which can be used as a flag or to control the system load. It is asserted i.e. pulled high when the device reaches steady state to indicate that the MOSFET is fully enhanced ($V_{GS} >$ 7.8 V and $V_{DS} <$ 1.0 V) and there are no fault conditions. When a fault is triggered, the MOSFET is turned off and this pin is de-asserted i.e. pulled low. It will also be de-asserted if the MOSFET turn on conditions, shown in Table 3 are not met. This device has a 5 ms deglitch time (t_{PWRGD}) for PWRGD pin assertion and 0 ms for de-assertion.

3.6 Thermal protection

Thermal protection is an important feature in any eFuse as it indicates and protects the device (and system load) against thermal instability. The device has two levels of thermal protection thanks to the dedicated temperature sensors in the MOSFET and controller. The MOSFET overtemperature protection is triggered when its temperature reaches T_{OT}. Additionally, the controller's thermal shutdown protection is triggered when the controller's die temperature reaches T_{TSD}. When a temperature protection is triggered in the device, it will at least keep the MOSFET turned off until the device cools down below the protection limit minus hysteresis.

3.7 MOSFET power down

The MOSFET turn-off can be triggered automatically due to a fault or manually by the user by removing the EN_UV signal. The MOSFET is generally turned off using I_{GATE_SPD} pull-down current except for OVIN and SOC fault events. Since OVIN and SOC events are critical for the device and the system load, a strong/fast pull-down current I_{GATE_FPD} is used for turning off the MOSFET immediately to avoid V_{DS} overshoots.

3.8 Quick output discharge

The device has an output discharge feature to quickly discharge the output capacitor (C_{OUT}) at the VOUT pin using an internal current source I_{QOD} to GND. This helps to quickly remove the residual charge left on the C_{OUT}. The QOD feature is activated when the user turns off the MOSFET using the EN_UV pin. A fixed deglitch timer t_{QOD} is started when the MOSFET is turned off. The current source I_{QOD} is activated only after the deglitch timer has expired. The output discharge is automatically deactivated after $t_{QOD\_Discharge}$ time has elapsed. It can be immediately deactivated if any of the following conditions exist.

- MOSFET is turned ON
- VOUT < 2 V
- Fault condition occurred (except for UV fault)

This feature can elevate the device temperature due to the increased power dissipation from the internal current source. Therefore, the QOD is disabled if the thermal protections are triggered.

3.9 Protections

3.9.1 Faults

This device incorporates many protections that ensure safe operation of the device and system load in different scenarios. The FAULTN pin will be pulled low and the MOSFET is turned off when a fault is triggered. The FAULT pin remains low for a minimum of t_{FAULT_MIN} regardless of the duration of the actual fault condition. This ensures that the user (or system microcontroller) can properly detect the FAULTN pin reporting. The FAULTN pin is released after the fault condition is removed.

There are priorities assigned to each fault. If a high-priority fault is triggered while processing a lower-priority fault, then the device will immediately start processing the higher-priority fault. The device will resume the lower-priority fault process only after the high-priority fault serving is finished. If multiple faults with the same priority are triggered at the same time, then the device will act on a first-come-first-serve basis.

Table 5 below provides an overview of when a fault's detection and processing are active.

Table 5 Faults overview table

Fault name and priority*1	State of the device						Fault availability*2
	Power-up phase	Standby phase	Start-up phase (i.e. MOSFET Turn-on)	Steady state	Fault phase	Latch-off	
SGD (1)	-	X	-	-	X	-	P/S
SGS (1)	-	-	X*3	-	-	-	P/S
SOC (2)	-	-	X	X	X	-	P/S
VDS (3)	-	X*4	-	-	-	-	P
OT (3)	-	X	X	X	-	-	P/S
TSD (3)	-	X	X	X	-	-	P/S

(table continues...)

Table 5 (continued) Faults overview table

Fault name and priority*1	State of the device						Fault availability*2
	Power-up phase	Standby phase	Start-up phase (i.e. MOSFET Turn-on)	Steady state	Fault phase	Latch-off	
OVIN (4)	-	X	X	X	X	-	P
OV (5)	-	X	X	X	X	-	P/S
UV (6)	-	X	X	X	X	-	P/S
WD (7)	-	-	X	-	-	-	P/S
OC (7)	-	-	-	X	-	-	P/S
SYNC (8)	-	X	X	X	-	-	P/S

Attention: ***1): Fault priority level decreases as we go down the table.***
2): Indicates the device configuration, P = PRIMARY and S = SECONDARY.
3): Right at the point when the watchdog timer expires.
4): Detection is active after first power-up phase.

3.9.1.1 Damaged MOSFET faults

This device comes with three internal MOSFET checks to mainly determine if there are any shorted pins in the MOSFET.

Shorted MOSFET Gate-Drain (SGD) fault

This fault checks if the Gate and Drain terminals of the MOSFET are shorted. It is triggered if:

- At power-up after $t_{SGD\_FLT\_DG}$ expires, the MOSFET's V_{GS} goes above 1 V.
- Or, after the device enters the FAULT or STANDBY state and activates any gate pull-down, the MOSFET's V_{GS} does not go below 1 V within $t_{FLT\_PD\_GATE}$.

When this fault is triggered, the device will turn off its MOSFET and get latched off. The fault is released only through the latch-off release procedure.

Shorted MOSFET Gate-Source (SGS) fault

If the MOSFET is not able to turn on within the watchdog time (t_{WD}) and its V_{GS} is below 1 V then the SGS fault will be issued. When this fault is triggered, the device will turn off its MOSFET and get latched off. The fault is released only through the latch-off release procedure.

Pre-charged output voltage (VDS) fault

This fault is enabled only in a PRIMARY configured device as shown in Table 5. It is detected during the device power-up after the enable deglitch timer (t_{EN_DG}) has expired for the first time. The V_{DS} level of the MOSFET is measured using the VINS and VOUTS pins i.e. V_{DS} = VIN - VOUT. This fault is released if the V_{DS} voltage of the MOSFET exceeds the fault level (V_{VDS_F}) or the output voltage is lower than 2 V.

3.9.1.2 Voltage faults

System input undervoltage (UV) fault

As mentioned in Chapter 3.2, the input voltage sensing is performed using the analog comparator at the EN_UV pin. The fault is triggered when the EN_UV pin voltage drops to/below $V_{UV\_LTH\_P}$ or $V_{UV\_LTH\_S}$. This fault is released when the sensed voltage rises to/above the $V_{EN\_UV\_UTH}$ level.

To avoid any false triggering of the UV fault during device power-up, the UV detection starts only after the fault level is crossed and the t_{EN_DG} has expired for the first time.

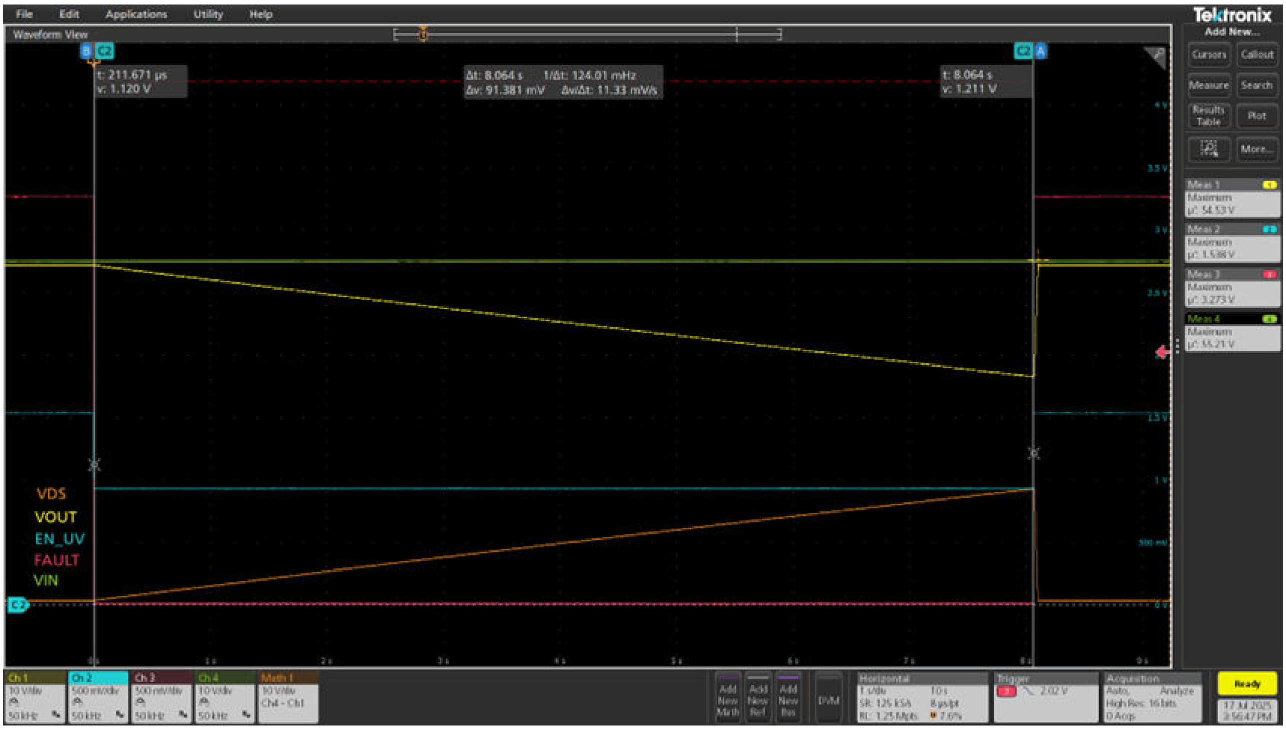


Figure 11 **Input UV fault being triggered followed by a successful fault release**

System input overvoltage (OV) fault

For OV fault, the input voltage is sensed using the analog comparator at the OV pin. The OV fault is triggered when the OV pin voltage rises to/above V_{OV_UTH}. This fault is released when the sensed voltage drops to/below the V_{OV_LTH} level.

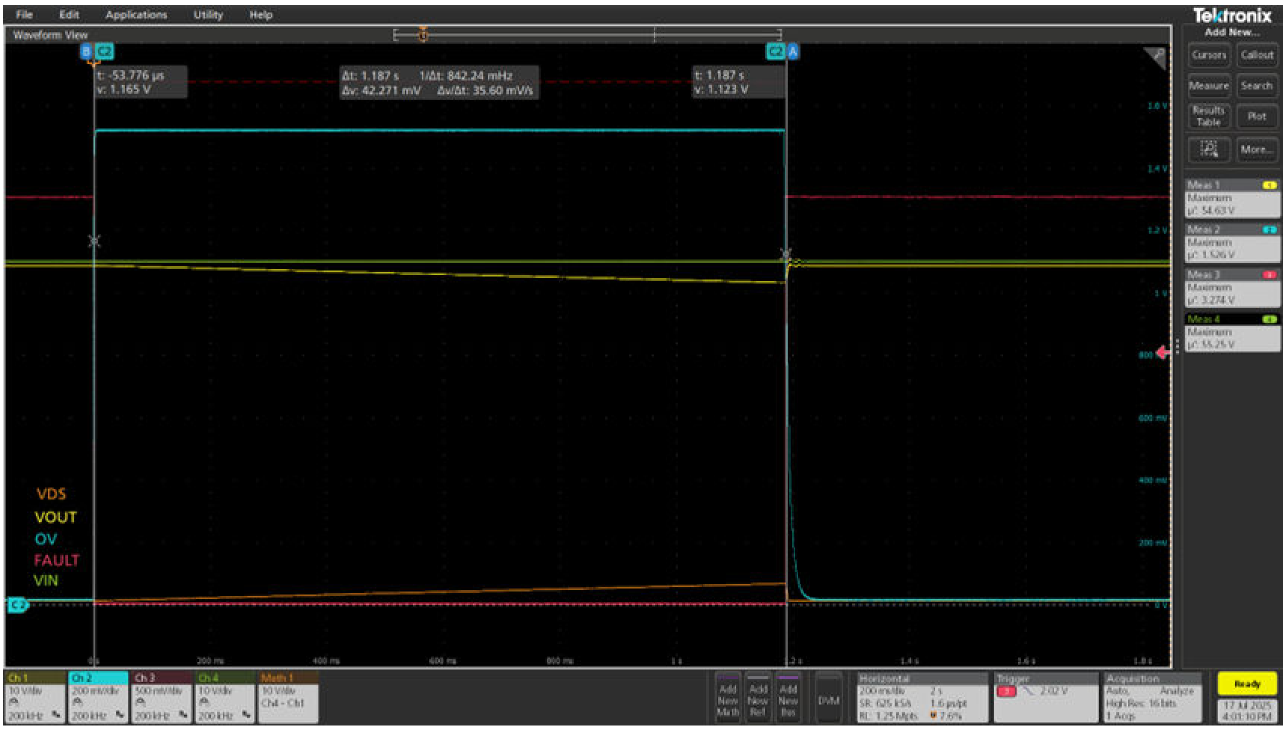


Figure 12 **Input OV fault being triggered followed by a successful fault release**

On-chip input overvoltage (OVIN) fault

This fault acts as a backup to the OV fault and it is enabled only in a PRIMARY configured device as shown in Table 5. If the VINS pin voltage rises to/above the V_{OVIN} level, the OVIN fault is triggered and the MOSFET is immediately turned off with a strong/fast pull-down current. This fault is released when the input voltage drops to/below the V_{OVIN} minus hysteresis i.e. V_{OVIN_HYS}.

3.9.1.3 Current faults

Overcurrent (OC) fault

As mentioned in Chapter 3.4, the OC condition can be detected in two ways through system OC (using IMON pin) and local OC.

When the IMON pin voltage reaches the fault reference threshold level V_{SYS_OC}, the deglitch timer t_{OCDT} configured using the OCDT pin is initiated. If the V_{IMON} drops below the fault level minute hysteresis (10% of fault level) before this timer expires, then the device continues normal operation otherwise the OC fault is triggered.

Alternatively, when the current through the MOSFET rises to/above the back-up/local current level I_{BKP_OC}, the deglitch timer t_{BKP_OC} is initiated. If the current through the MOSFET drops below the back-up fault level before this timer expires, the device continues normal operation otherwise the OC fault is triggered.

When the OC fault is triggered, the MOSFET is turned off with a regular pull-down and the device will follow the retry settings depending on the device variant.

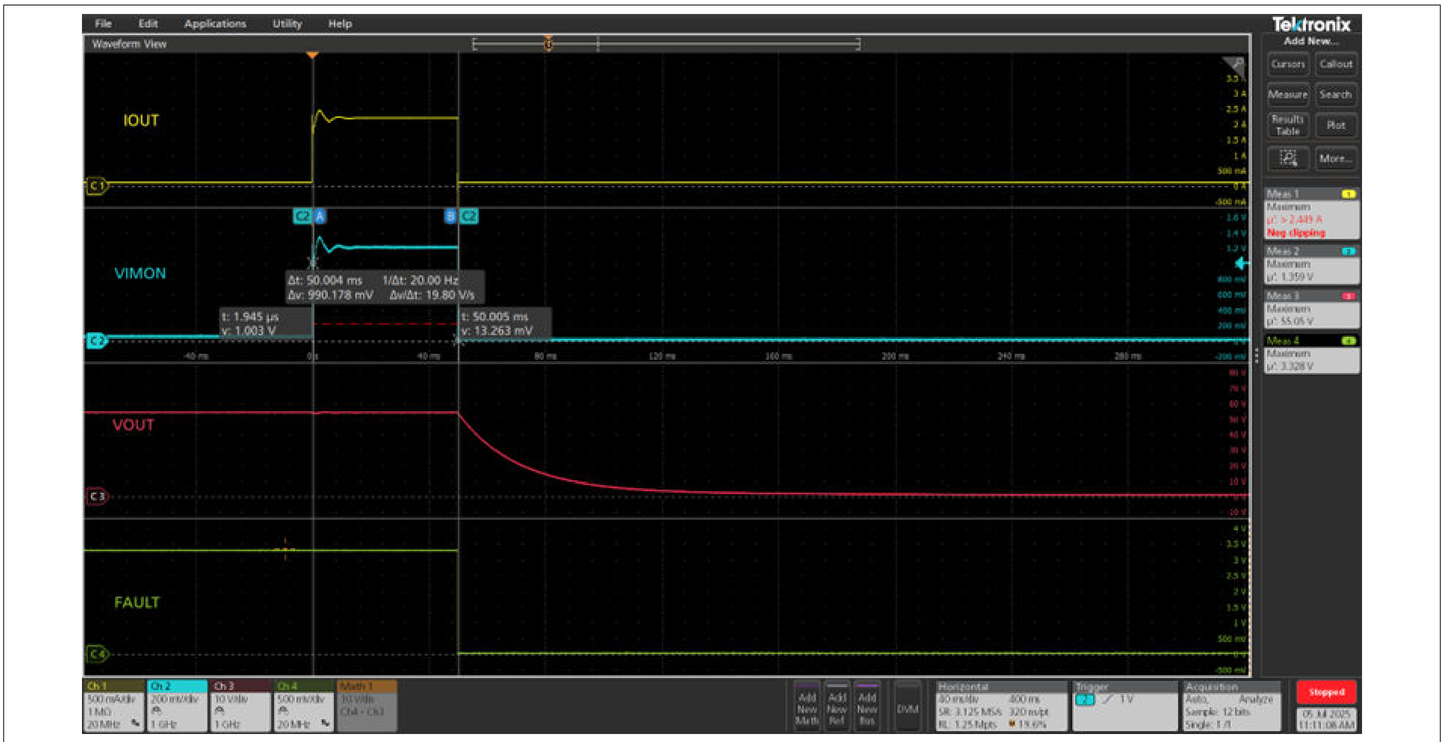


Figure 13 Overcurrent fault being triggered after 50 ms of V_{IMON} reaching ~1.0025 V; R_{IMON} = 27.5 kΩ

Severe overcurrent (SOC) fault

When the current flowing through the MOSFET rises to/above the SOC fault level configured using the MODE_SOC pin setting, the SOC fault is triggered.

Since it is a critical fault, the MOSFET is turned off immediately with a strong/fast pull-down when the SOC fault is triggered and the device will follow the retry settings depending on the device variant.

***Note**: During MOSFET turn-on, the SOC level is fixed to $I_{SOC\_STARTUP}$*

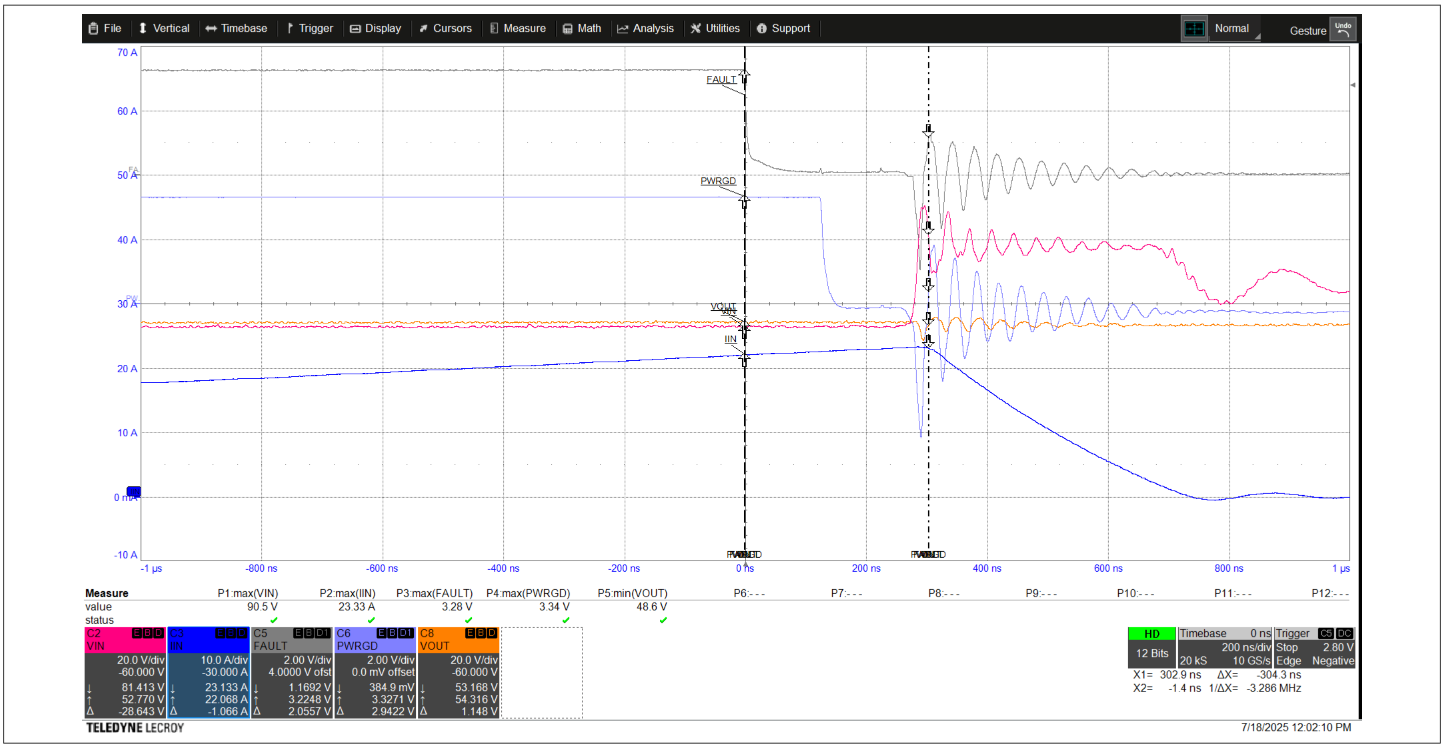


Figure 14 **Severe overcurrent fault (22 A) being triggered followed by a fast MOSFET turn-off within ~400 ns**

3.9.1.4 Thermal faults

MOSFET overtemperature (OT) fault

This fault depends on the temperature sensed inside the MOSFET. If the MOSFET's temperature rises to/above the fault level T_{OT}, the OT fault is triggered. As a result, the MOSFET is turned off with a regular pull-down current. The device waits until the MOSFET is completely turned off and its temperature drops below the fault level minus hysteresis (T_{OT_HYS}). After this waiting period, the device will follow the retry settings depending on the device variant.

Controller thermal shutdown (TSD) fault

The TSD fault relies on the temperature sensed inside the controller. If the controller's temperature rises to/above the fault level T_{TSD}, the TSD fault is triggered. As a result, the MOSFET is turned off with a regular pull-down current. The device waits until the MOSFET is completely turned off and the controller's temperature drops below the fault level minus hysteresis (T_{TSD_HYS}). After this waiting period, the device will follow the retry settings depending on the device variant.

3.9.1.5 Power-up faults

Unsuccessful MOSFET start-up, i.e. watchdog (WD) fault

As soon as the MOSFET turn-on procedure is initiated, the timer t_{WD} is initiated. If the MOSFET is not fully enhanced (i.e. V_{DS} < 1 V and V_{GS} > 7.8 V) before the timer expires, the WD fault is triggered. As a result, the MOSFET is turned off with a regular/slow pull-down current and the device will follow the retry settings depending on the device variant.

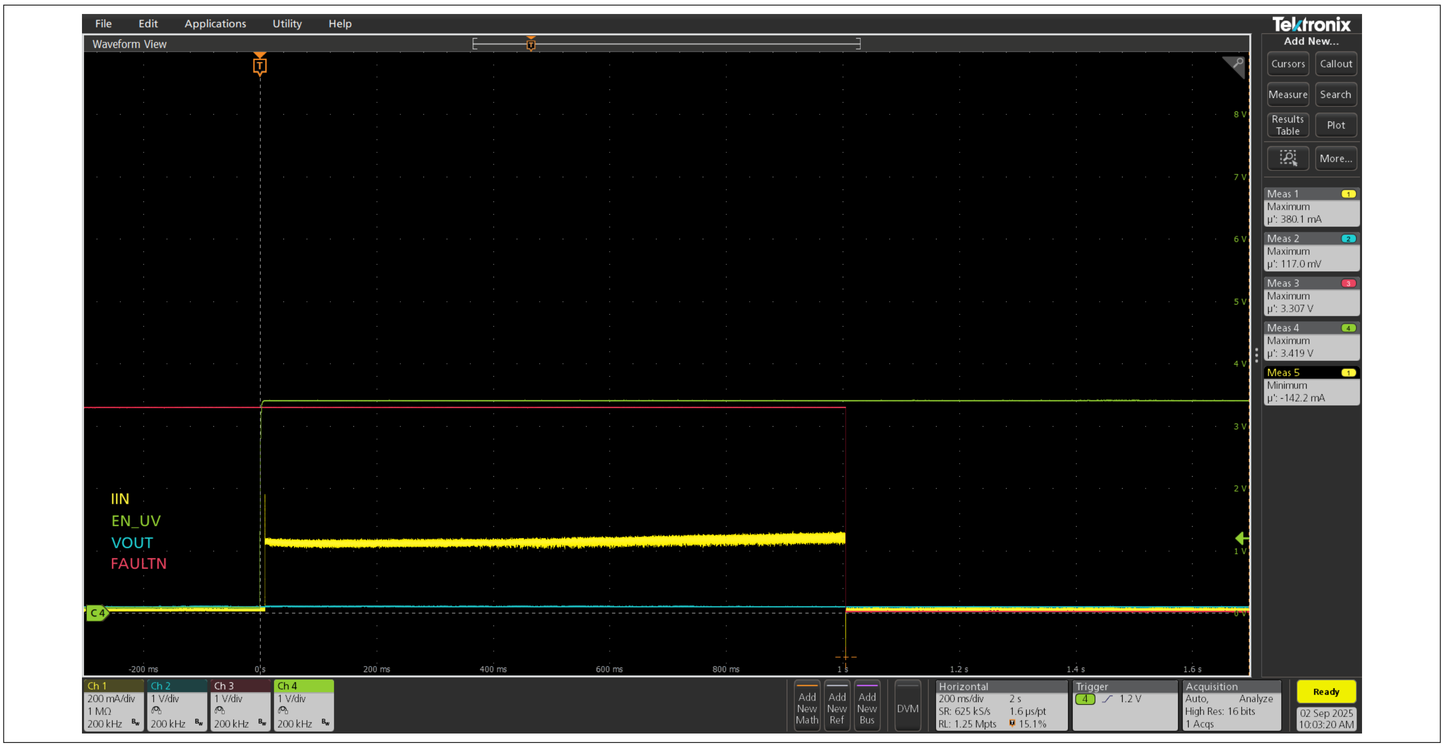


Figure 15 **Start-up into short protection triggers watchdog (WD) fault after 1 s**

3.9.1.6 Internal protection fault

SYNC Fault

This fault is used to synchronize all the devices in a high-power system. The SYNC fault is triggered in the device if,

- Failsafe check is unsuccessful i.e. $V_{FS} < V_{FS\_TH}$
- Or, the SYNC pin is externally pulled LOW

The device will turn off its MOSFET with a regular pull-down and follow the retry settings depending on the device variant.

VREG fault

If, at any point in time, the VREG pin voltage goes below 4.1 V then the device will trigger an automatic power-on reset which resets the volatile memory. This fault is not reported to the user.

3.9.2 Fault response

This device is available in two variants depending on the fault response type, i.e. XDP721 (latch-off) and XDP722 (auto-retry). There are a total of six major faults that can trigger the auto-retry/latch-off response from the device. These include unsuccessful MOSFET start-up, overcurrent, severe overcurrent, MOSFET overtemperature, thermal shutdown and synchronization faults. It must be noted that the auto-retry function is only possible in a PRIMARY configured XDP722-001 device. The SECONDARY device (XDP721 or XDP722) will simply follow the PRIMARY device with the help of its SYNC pin connection.

3.9.2.1 Auto-retry (XDP722)

When a retry-based fault is triggered, the PRIMARY configured XDP722-001 will keep retrying an infinite number of times until the MOSFET is turned on or the device is power cycled. Before every retry attempt, the device will wait for a cool-down period (t_{COOLD}). During this period, the device keeps its MOSFET turned off and ignores the fault release prompt i.e. EN_UV pin toggling. After the cool-down has expired, the device will attempt to turn-on the MOSFET if all the other turn-on conditions shown in Table 3 are met and no fault conditions exist.

3.9.2.2 Latch-off (XDP721)

The XDP721 (and a SECONDARY configured XDP722) will get directly latched off if any of the retry-based faults are triggered. After latch-off, the device will continue to:

- keep its MOSFET turned off
- latch the state of the PWRGD and FAULTN pins

Latch-off release:

The device will get unlatched using:

- EN_UV pin toggling (HIGH-to-LOW transition)
- Or, device power cycle

If either of these methods is used, the device will:

- de-assert/release the PWRGD and FAULTN pins
- proceed to MOSFET turn-on attempt if all the turn-on conditions shown in Table 3 are present

4 General product characteristics

4.1 Absolute maximum ratings

Attention**: **Absolute maximum ratings are not subject to production test, specified by design.

Table 6 Absolute maximum ratings

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to GND unless otherwise specified, positive currents are flowing into the pin, $T_A = 25°C$.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltage at VDD_VIN, VIN, VINS, VOUT and VOUTS pins	$V_{VDD\_VIN\_DC}$, V_{VIN_DC}, V_{VINS}, V_{VOUT_DC}, V_{VOUTS}	-0.3	-	80	V	-
Voltage at VOUT and VOUTS pins	V_{VOUT_DC}, V_{VOUTS}	-1	-	80	V	-
Voltage transients at VDD_VIN, VIN, VINS, VOUT and VOUTS pins	$V_{VDD\_VIN\_AC}$, V_{VIN_AC}, V_{VINS_AC}, V_{VOUT_AC}, V_{VOUTS_AC}	-0.3	-	100	V	For 500 ms maximum
Voltage transients at VOUT and VOUTS pins	V_{VOUT_AC}, V_{VOUTS_AC}	-5	-	100	V	• -5 V during MOSFET OFF condition, for transients up to 5 µs • 100 V for 500 ms maximum
Voltage slew rate at VDD_VIN, VIN, VINS, VOUT and VOUTS pins	SR_{VDD_VIN}, SR_{VIN}, SR_{VINS}, SR_{VOUT}, SR_{VOUTS}	-	-	80	V/µs	The RC filter (100 Ω/100 nF or etc.) on the VDD_VIN pin is recommended, especially for high voltage applications. An output cap (10 µF min) limits a slew rate on the VOUT pin.
Output voltage at VREG pin	V_{VREG}	-0.3	-	6	V	-
Digital pins output voltage (FAULTN, SYNC, PWRGD)	V_{FAULTN}, V_{SYNC}, V_{PWRGD}	-0.3	-	6	V	-
Digital pins input voltage (SYNC)	V_{SYNC}	-0.3	-	6	V	-
Analog pins input voltage (MODE_SOC, EN_UV, OV, FS)	V_{MODE_SOC}, V_{EN_UV}, V_{OV}, V_{FS}	-0.3	-	6	V	-
IMON pin voltage	V_{IMON}	-0.3	-	3.3	V	-

(table continues...)

Table 6 **(continued) Absolute maximum ratings**

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to GND unless otherwise specified, positive currents are flowing into the pin, T_A = 25°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction Temperature range	T_J	-40	-	150	°C	-
Storage Temperature range	T_S	-55	-	150	°C	-

4.2 Functional range

Table 7 **Functional and performance ranges description**

Absolute voltage range at VDD_VIN (V)	MOSFET	VREG
0 ≤ VDD_VIN < 7	Off (passive pull-down)	Off
7 ≤ VDD_VIN < 9	Limited operation: - Off (active pull-down); - limited SOA regulation depending on gate driver supply; - On/enhancement is not guaranteed (but ≥ 4.5 V)	5.0 V (typ.)
9 ≤ VDD_VIN ≤ 80	Full operation: - Off (active pull-down); - full SOA regulation; - On/enhancement (typ. 10.5 V)	

Table 8 **Recommended operating range**

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to GND unless otherwise specified, positive currents are flowing into the pin, T_A = 25°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage at VDD_VIN pin	V_{VDD_VIN}	7	-	80	V	-
Supply voltage at VDD_VIN pin to enable all features	$V_{VDD\_VIN\_EN}$	9	-	80	V	Refer Chapter 4.2.
Supply voltage filter resistor	R_{VDD_VIN}	100	-	-	Ω	-

(table continues...)

Table 8 (continued) Recommended operating range

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to GND unless otherwise specified, positive currents are flowing into the pin, T_A = 25°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage at VIN pin	V_{VIN}	7	-	80	V	-
Voltage at VINS, VOUTS and VOUT pins	V_{VINS}, V_{VOUTS}, V_{VOUT}	0	-	80	V	-
Maximum output current	I_{OUT_MAX}	-	20	-	A	-
Digital pins output voltage (FAULTN, SYNC, PWRGD)	V_{FAULTN}, V_{SYNC}, V_{PWRGD}	0	-	5.5	V	-
Digital pins input voltage (SYNC)	V_{SYNC}	0	-	5.5	V	-
IMON pin voltage	V_{IMON}	0	-	1.35	V	-
Analog pins input voltage (MODE_SOC, EN_UV, OV, FS, OCDT)	V_{MODE_SOC}, V_{EN_UV}, V_{OV}, V_{FS}, V_{OCDT}	0	-	5.5	V	-
Junction temperature range	T_J	-40	-	125	°C	-

4.3 Thermal characteristics

Attention: ***Thermal data is not subject to production test, specified by design.***

Table 9 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance junction-to-case (bottom)	$R_{\Theta JC\_Bot}$	-	6.5	-	K/W	PCB simulation setup as described in Table 10.
Thermal resistance junction-to-case (top)	$R_{\Theta JC\_Top}$	-	22.9	-	K/W	PCB simulation setup as described in Table 10.
Thermal resistance junction-to-ambient	$R_{\Theta JA}$	-	25.6	-	K/W	PCB simulation setup as described in Table 10.

Table 10 PCB characteristics for thermal simulation

		λ_{therm} [W/m-K]
Metalization	JEDEC 2s2p (JESD 51-7, JESD 51-5)	388
Cooling Area [mm²]	none	388

Note:
- *Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.*
- *This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org*

4.4 ESD robustness

Attention: ***ESD robustness data is not subject to production test, specified by design.***

Table 11 ESD robustness

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ESD robustness HBM	V_{ESD_HBM}	-2000	-	+2000	V	Human Body Model sensitivity as per ANSI/ESDA/JEDEC JS-001
ESD robustness CDM	V_{ESD_CDM}	-500	-	+500	V	Charge device model sensitivity as per ANSI/ESDA/JEDEC JS-002

4.5 Electrical characteristics

Attention: ***Electrical parameters are subject to production test, unless otherwise noted.***

Table 12 Electrical characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDD_VIN and VIN						
Supply voltage at VDD_VIN and VIN pins	V_{VDD_VIN}, V_{VIN}	7	54	80	V	-
Current consumption	I_{VDD}	-	7.4	9.5	mA	VDD_VIN supply current; MOSFET is fully ON (IOUT = 0 A)
VINS and VOUTS						
VINS pin input current	I_{VINS}	-	34	-	µA	At VINS = 54 V
VOUTS pin input current	I_{VOUTS}	-	34	-	µA	At VOUTS = 54 V
VDS fault limit	V_{VDS_F}	-	10	-	V	(1) For V_{DS} = VIN - VOUT

(table continues...)

Table 12 (continued) Electrical characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Enable/Input Undervoltage (EN_UV)						
EN_UV pin upper threshold	$V_{EN\_UV\_UTH}$	1.14	1.2	1.26	V	-
EN_UV pin lower threshold	V_{EN_LTH}	0.76	0.8	0.84	V	Output is disabled; MOSFET is turned off
EN_UV pin lower threshold (Primary)	$V_{UV\_LTH\_P}$	1.07	1.12	1.17	V	Input UV fault is triggered
EN_UV pin lower threshold (Secondary)	$V_{UV\_LTH\_S}$	0.95	1	1.05	V	Input UV fault is triggered
Input overvoltage (OV) protection						
OV pin upper threshold	V_{OV_UTH}	1.13	1.164	1.2	V	Input OV fault is triggered
OV pin lower threshold	V_{OV_LTH}	1.09	1.123	1.156	V	Input OV fault is released
On-chip input overvoltage (OVIN) protection						
OVIN fault limit	V_{OVIN}	-	80	-	V	(1) On-chip overvoltage (OVIN) fault is triggered
OVIN fault hysteresis	V_{OVIN_HYS}	-	5	-	V	(1)
VREG						
Output voltage	V_{REG}	4.7	5.0	5.3	V	7 V ≤ VDD_VIN < 80 V
VREG bypass capacitor	C_{VREG}	-	1	-	µF	(1) For V_{REG} = 5 V
Current capability	I_{REG}	-	-	1	mA	(1) To supply external load
Power MOSFET						
On resistance	$R_{DS(on)}$	-	3	3.7	mΩ	-
Fast pull-down current	I_{GATE_FPD}	-	1	-	A	(1) For SOC and OVIN faults
Slow pull-down current	I_{GATE_SPD}	-	1250	-	µA	(1) For faults (except SOC, OVIN)
Start-up current						
Start-up current limit	I_{START_ILIM}	-	495	-	mA	(1)
Overcurrent protection						
System OC reference voltage limit	V_{SYS_OC}	-	1.0025	-	V	(1) OC fault is triggered when V_{IMON} >= V_{SYS_OC}
Backup/Local OC fault limit	I_{BKP_OC}	-	44	-	A	(1)

(table continues...)

Table 12 (continued) Electrical characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Short circuit protection						
SOC fault limit (Primary)	I_{SOC_P}	- - - - -	- 22 33 44 55	- - - - -	A	(1) Set via MODE_SOC pin; Refer Table 2
SOC fault limit (Secondary)	I_{SOC_S}	- - - - -	- 22 33 44 55	- - - - -	A	(1) Set via MODE_SOC pin; Refer Table 2
Start-up SOC fault limit	$I_{SOC\_STARTUP}$	-	9.375	-	A	(1) Only during inrush current control
MODE_SOC						
Pin sense current at device power-up	I_{MODE_SOC}	93	100	107	µA	-
OCDT						
Pin sense current at device power-up	I_{OCDT}	186	200	214	µA	-
IMON						
IMON gain	G_{IMON}	-	18.2	-	µA/A	-
IMON signal reporting accuracy	$IMON_{ACC}$	-1 -3 -5	- - -	+1 +3 +5	%	(1) IOUT = 10 A; IOUT = 5 A; IOUT = 2 A
IMON operating voltage	V_{IMON}	-	-	1.35	V	(1)
PWRGD and FAULTN						
Output low voltage	V_{OL_PG}	-	-	0.4	V	At 10 mA
Input Low Voltage	V_{IL_PG}	-	-	0.8	V	-
Input High Voltage	V_{IH_PG}	2	-	-	V	-
Leakage current	I_{PG}	-	-	5	µA	At 5.5 V; output is HiZ.
FS						
FS pin sense current	I_{FS}	37	40	43	µA	Only in PRIMARY configured device
FS pin threshold voltage	V_{FS_TH}	0.27	0.3	0.33	V	-

(table continues...)

Table 12 (continued) Electrical characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
FS pin pull-down resistor	R_{FS_PD}	0.8	1	1.2	MΩ	[1]
Quick output discharge (QOD)						
QOD current source	I_{QOD}	14	21	31	mA	0°C ≤ T_J ≤ 125°C
MOSFET on-chip overtemperature (OT) protection						
OT fault limit	T_{OT}	-	130	-	°C	[1]
OT hysteresis	T_{OT_HYS}	-	15	-	°C	[1]
Controller on-chip thermal shutdown (TSD) protection						
TSD fault limit	T_{TSD}	-	145	-	°C	[1]
TSD hysteresis	T_{TSD_HYS}	-	10	-	°C	[1]
Retry						
Retry counter	*RC*	-	infinite	-	-	[1] Allowed retry attempts in XDP722

***Note**:* *(1) Not tested in production, specified by design.*

4.6 Timing characteristics

***Attention**: Timing parameters are subject to production test, unless otherwise noted.*

Table 13 Timing characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Enable/input undervoltage (EN_UV) pin						
EN_UV pin deglitch time	$t_{EN\_UV\_D}$	6.5	10	13.5	µs	Input filter before processing the signal.
EN insertion delay	t_{EN_DG}	-	8	-	ms	[1]
Input Overvoltage (OV) protection						
OV pin deglitch time	t_{OV_DG}	6.5	10	13.5	µs	Input filter before processing the signal.
OVIN detection time	t_{OVIN_DET}	-	-	2.0	µs	[1]
PWRGD						
PWRGD assertion deglitch time	t_{PWRGD}	-	5	-	ms	[1] From MOSFET fully enhanced till PWRGD is pulled high

(table continues...)

Table 13 (continued) Timing characteristics

VDD_VIN - GND = 54 V, VIN - GND = 54 V, VINS is tied to VIN, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fault timers						
SGD fault deglitch time	$t_{SGD\_FLT\_DG}$	28.8	32	35.2	µs	[1]
Time for any gate discharge in fault state	$t_{FLT\_PD\_GATE}$	9	10	11	ms	[1]
Fault strong pull down activation time for fast gate discharge	$t_{FLT\_PD\_FAST}$	13.5	15	16.5	µs	[1]
Fault reaction time	$t_{FLT\_GATE\_OFF}$	-	0.3	1.0	µs	[1] From fault triggered to activation of MOSFET's gate turn-off.
FAULT pin hold time	t_{FAULT_MIN}	20	-	-	µs	[1] At C_L= 50 pF; External pull-up resistor of 10 kΩ.
Retry Cool Down time	t_{COOLD}	-	2	-	s	[1] Only for XDP722
Turn-on watchdog timer	t_{WD}	-	1	-	s	[1] Maximum allowed time for MOSFET turn-on.
System OC (IMON) deglitch timer	t_{OCDT}	- - … -	- 0 … 50	- - … -	ms	[1] Set via OCDT pin; Refer Table 4
Backup/local OC deglitch time	t_{BKP_OC}	-	200	-	µs	[1]
SOC fault response time	t_{SOC_DG}	300	400	800	ns	[1]
QOD						
QOD deglitch time	$t_{QOD\_Deglitch}$	-	6	-	ms	[1] It is started when the MOSFET is turned off.
QOD discharge time	$t_{QOD\_Discharge}$	-	1000	-	ms	[1] It is started when the QOD is activated.
SYNC						
SYNC handshaking timeout	t_{SYNC_HSK}	-	10	-	µs	[1]

***Note**: (1) Not tested in production, specified by design.*

5 Application information

5.1 Standalone operation

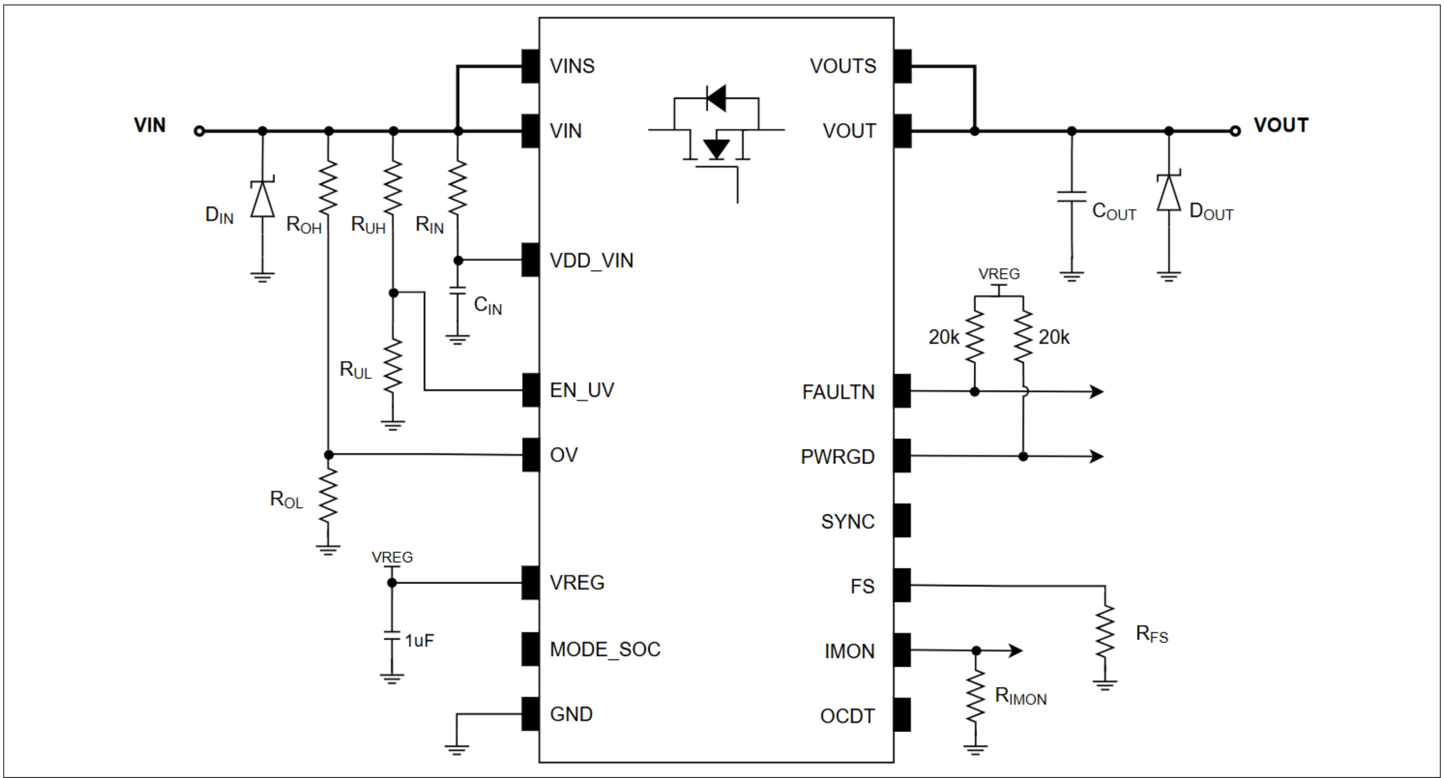


Figure 16 **XDP721 typical application schematic (standalone eFuse)**

5.2 Parallel operation

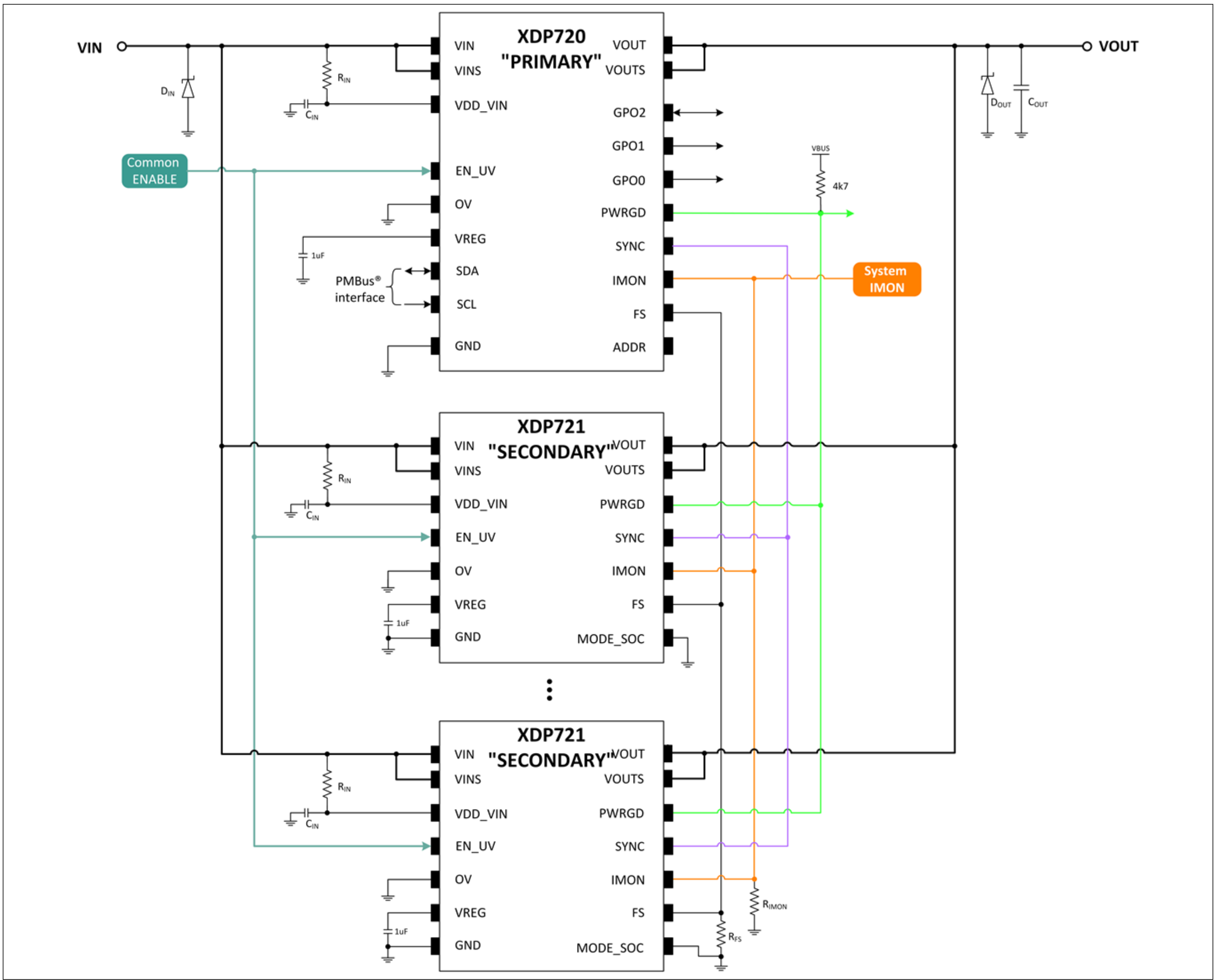


Figure 17 XDP720/XDP721 typical application schematic (parallel operation)

The Figure 17 shows an example application schematic with one XDP20 (PRIMARY) and multiple XDP21 devices in parallel. The following recommendations must be considered when designing such high-power systems.

- Connect the VDD_VIN, VIN, VOUT, EN_UV, OV, IMON, FS, GND and PWRGD pins of all the devices together.
- Each device must have a dedicated 1 µF capacitor connected between its VREG and GND pins.
- IMON resistor must be calculated properly considering the total number of devices in parallel.
- ADDR pin or MODE_SOC pin of the SECONDARY connected XDP72x devices must be tied to the GND pin.
- If only XDP720-001 devices are connected in parallel, then connect all the GPO2 pins together with proper configuration and a single pull-up resistor to use the hardware RESTART pin function.
- Use proper TVS and/or Schottky diodes at the VIN and VOUT nets.

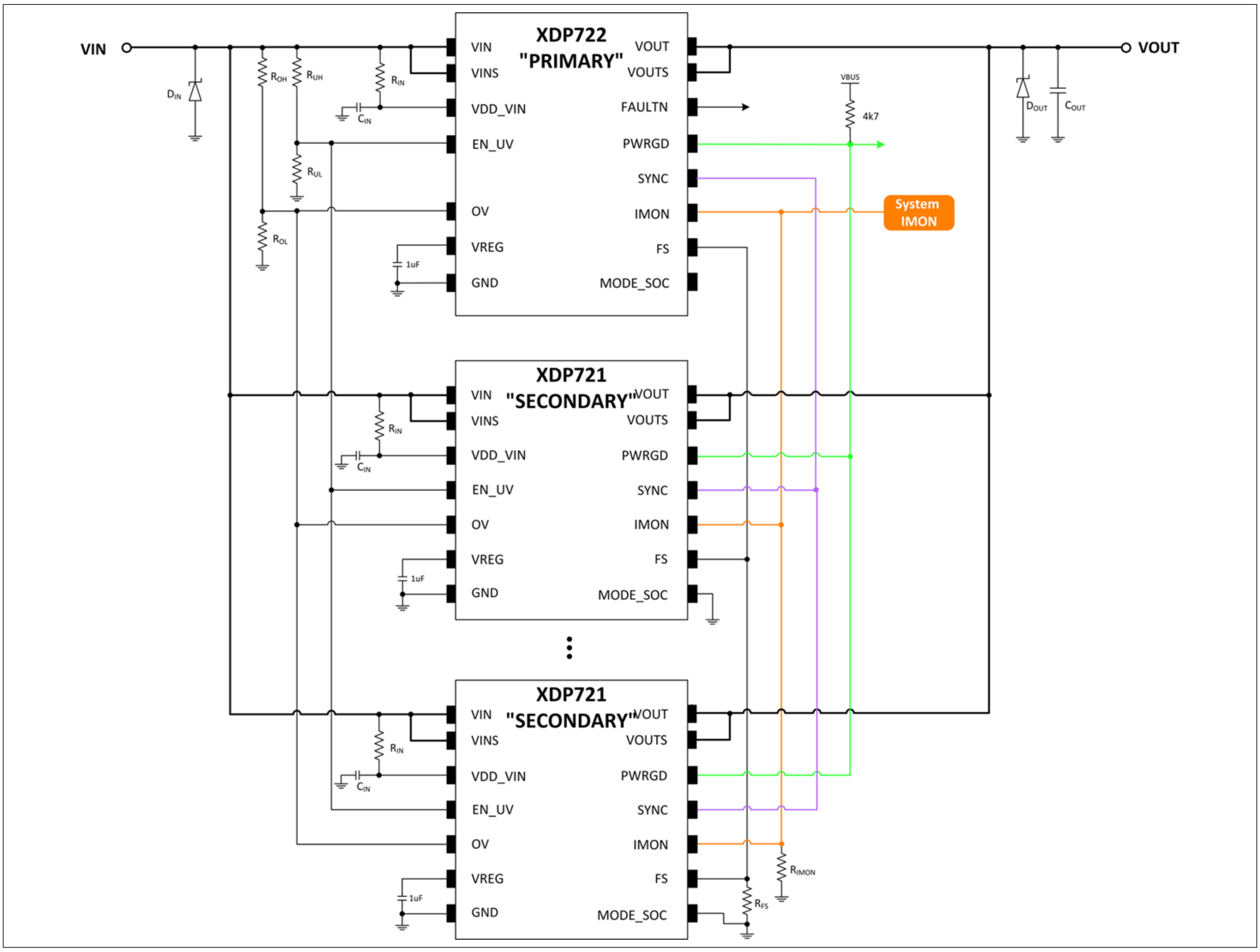


Figure 18 **XDP722/XDP721 typical application schematic for non-PMBus® application**

Figure 18 shows a typical application where PMBUS is not required. In such cases, based on the fault response needed, either XDP722 or XDP721 can be connected as the PRIMARY device in the parallel operation.

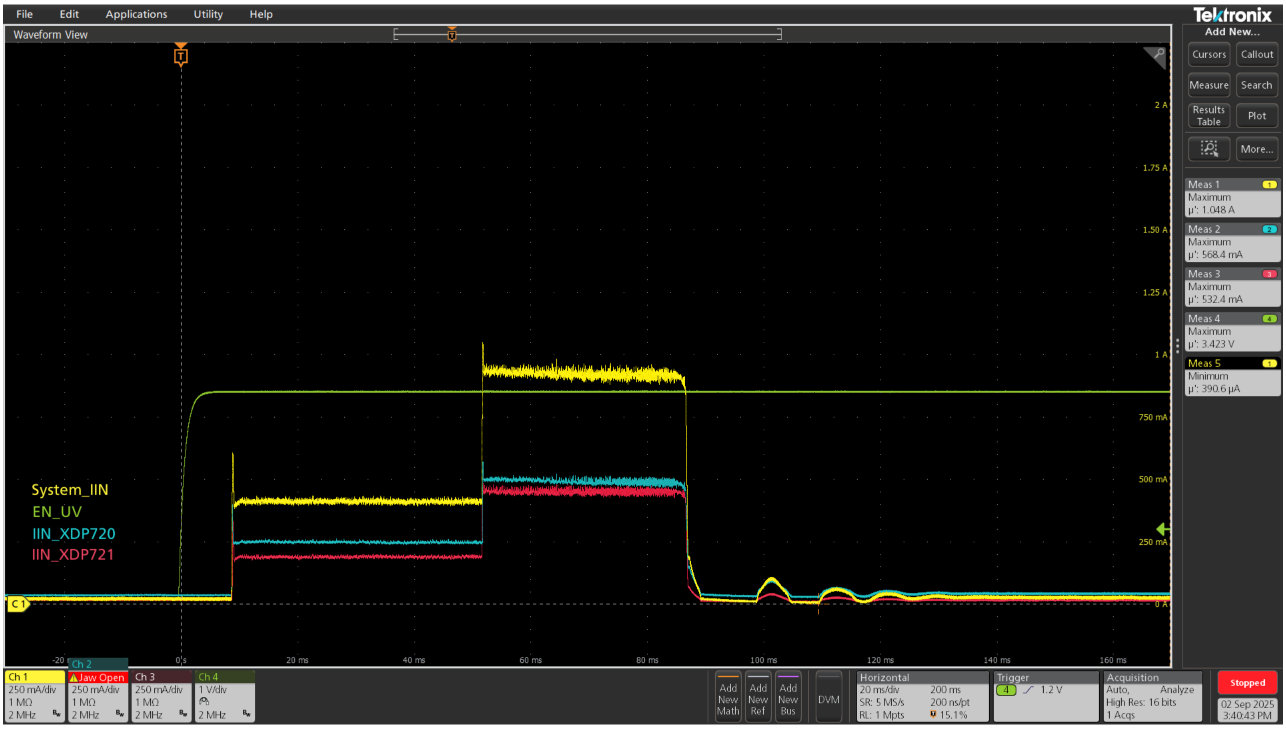


Figure 19 **Parallel operation (XDP720 + XDP721): Turn-on**

The Figure 19 shows the turn-ON of two parallel connected XDP72x-001 devices (XDP720-001 as PRIMARY and XDP721-001 as SECONDARY). As shown, the devices will start to turn-ON their MOSFETs almost at the same time because of the SYNC pins connection. Figure 20 shows the OV fault being independently triggered in the PRIMARY device. The OV fault in the PRIMARY leads to all the devices turning OFF their MOSFETs. In this case, the SECONDARY device does not trigger any fault as it is simply waiting for the PRIMARY device to release the SYNC pin.

Similarly, Figure 21 shows the OV fault being independently triggered in the SECONDARY device, which results in a SYNC fault being triggered in the PRIMARY device. Depending on the retry settings, the PRIMARY device handles the triggered SYNC fault. In this case, the retry cool down time is set to 4 s in the XDP720-001 device. Therefore, the PRIMARY device performs a successful retry attempt after 4 s as the fault in the SECONDARY is already released.

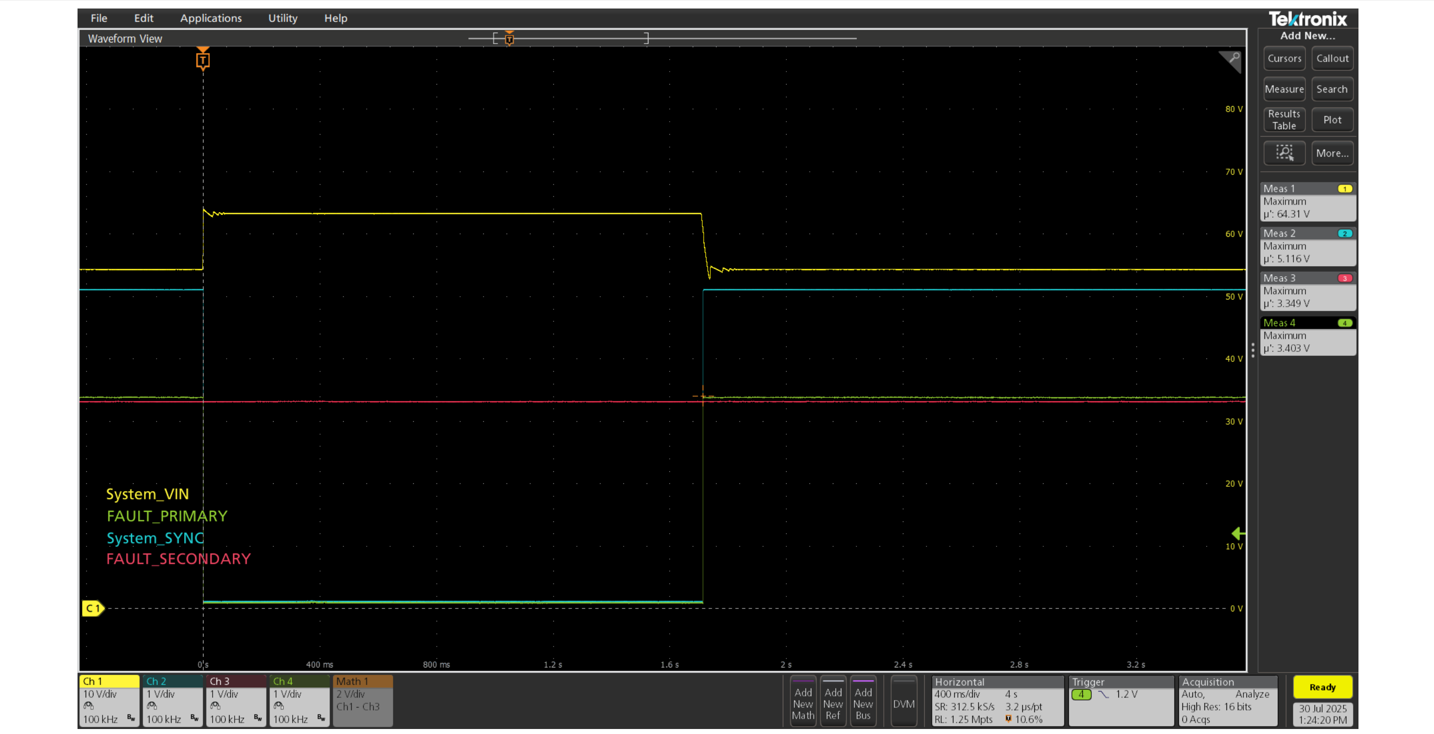


Figure 20 **An input OV fault being triggered in PRIMARY device followed by a successful fault release**

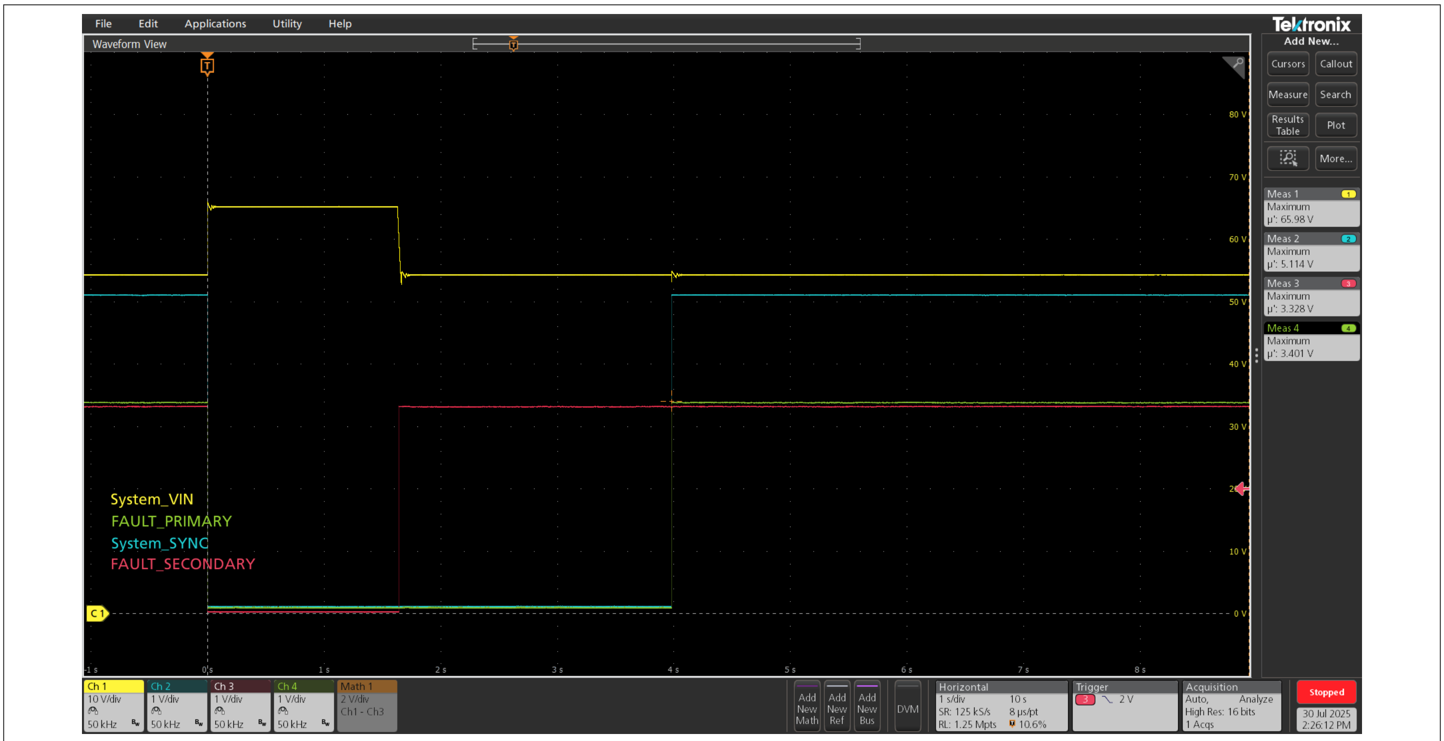


Figure 21 **An OV fault being triggered in SECONDARY device resulting in a SYNC fault in PRIMARY device; Auto-retry enabled in PRIMARY with 4 s cool down time**

5.3 Layout guidelines

The following guidelines shall be followed when designing the PCB for this device:

- VIN and VOUT pins (i.e. high-current carrying pins) must be properly sized to carry the necessary load current. Connect them to as much copper area as possible with thermal vias.

- Ceramic decoupling capacitors (~100 nF) are recommended at VIN and VOUT pins.
- An RC filter is recommended at the VDD_VIN pin with a minimum resistor value of 100 Ω.
- A 1 µF capacitor is mandatory between the VREG pin and GND. It must be placed right next to the VREG pin.
- The GND pin must be connected to the PCB ground plane.
- If unused, the VINS and VOUTS pins must be connected to the nearest VIN and VOUT pins respectively.
- It is recommended to have a solid connection from the exposed pad to the VIN plane through many vias for effective thermal management of the device.
- Resistor divider networks at EN_UV and OV pins shall be placed close to the device for faster response.
- Loading the SYNC pin must be avoided to minimize synchronization issues.
- Since the IMON pin resistor is essential for the current protections, it is recommended to place it close to the IMON pin and avoid any nearby noisy signals.
- It is recommended to use TVS and/or Schottky diodes at VIN and VOUT pins to protect against voltage spikes.

6 Package information

6.1 Ordering information

Table 14 Ordering information table

Basic part number	Orderable part number	Description
XDP721	XDP721-001	Positive input voltage 20 A eFuse IC with latch-off
XDP722	XDP722-001	Positive input voltage 20 A eFuse IC with auto-retry (i.e. XDP721-001 and auto-retry function)

6.2 Package outline

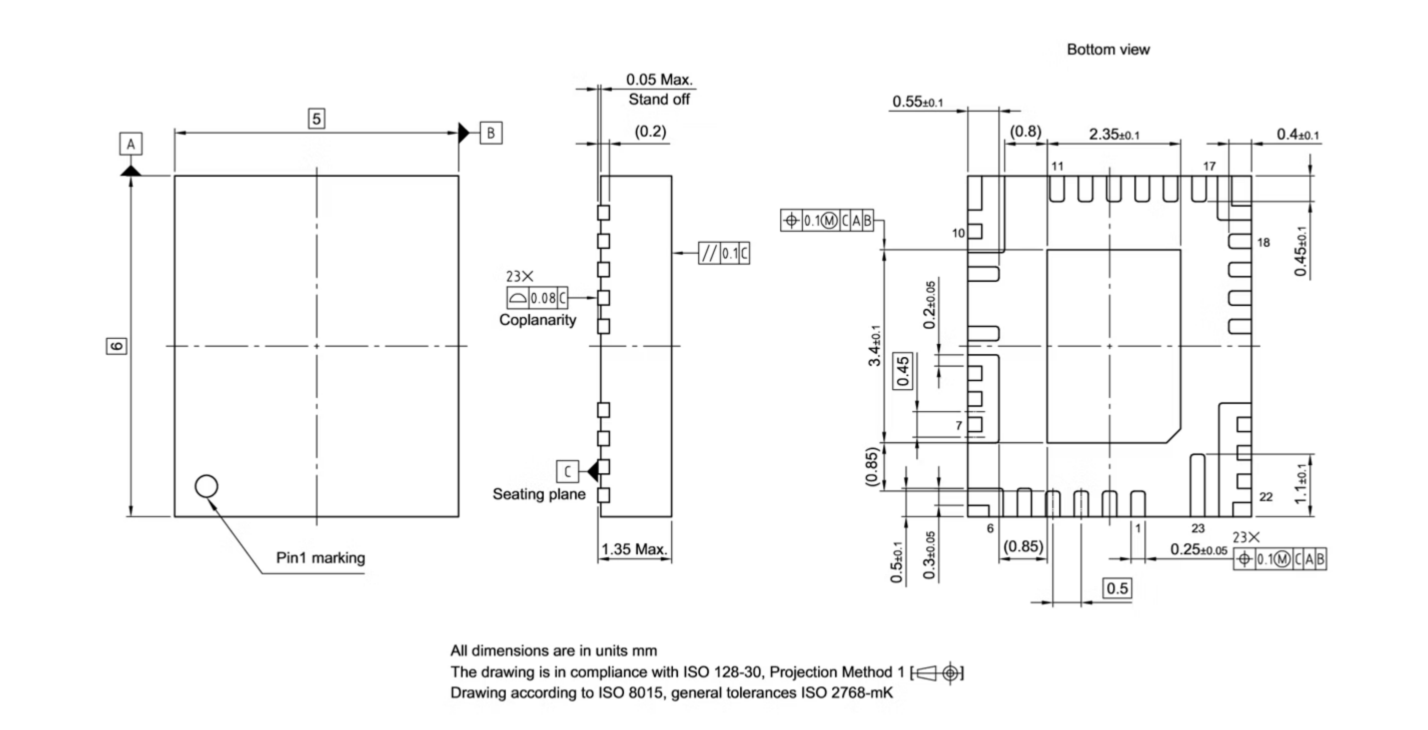


Figure 22 XDP72x-001 package dimensions

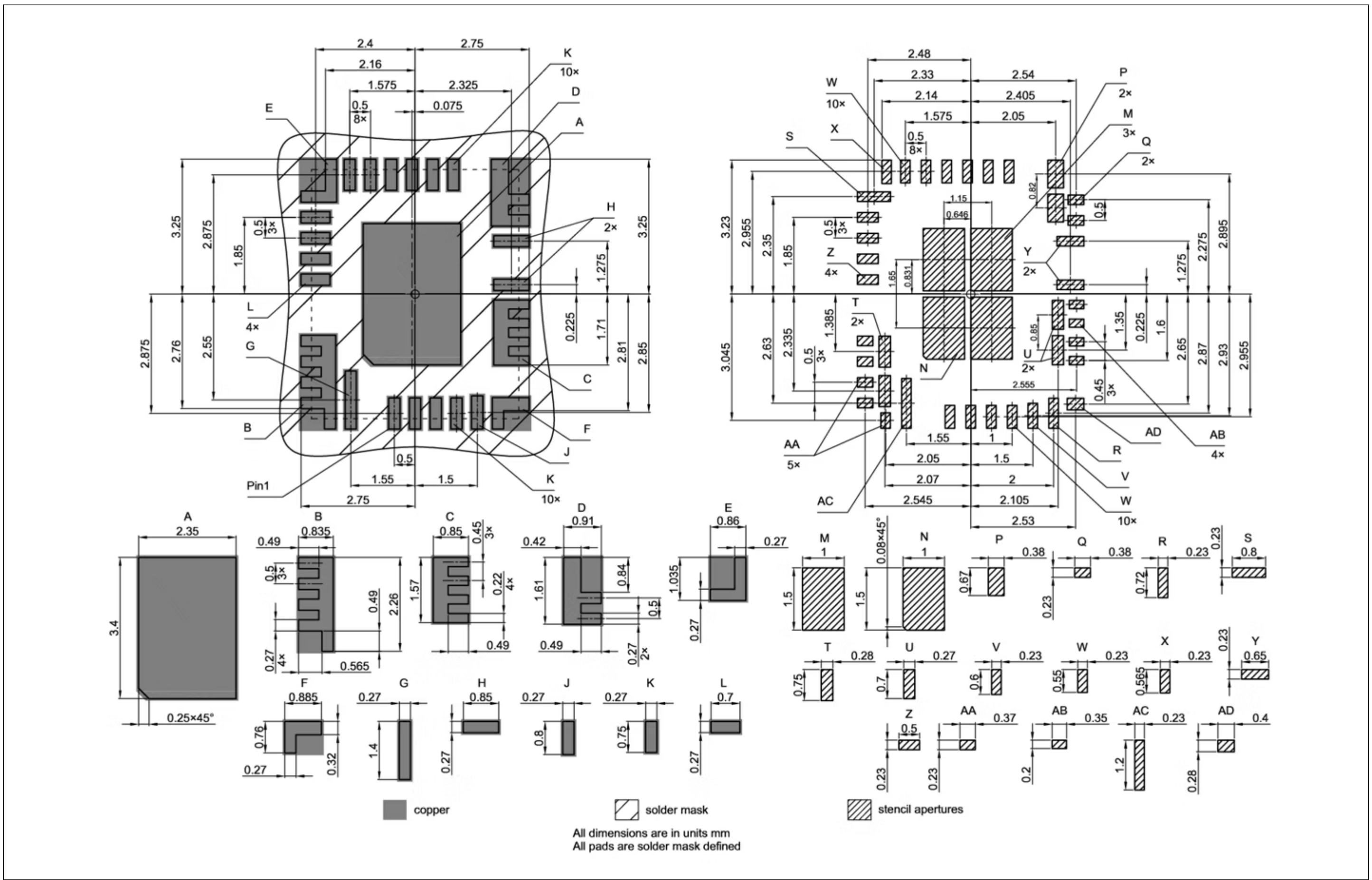
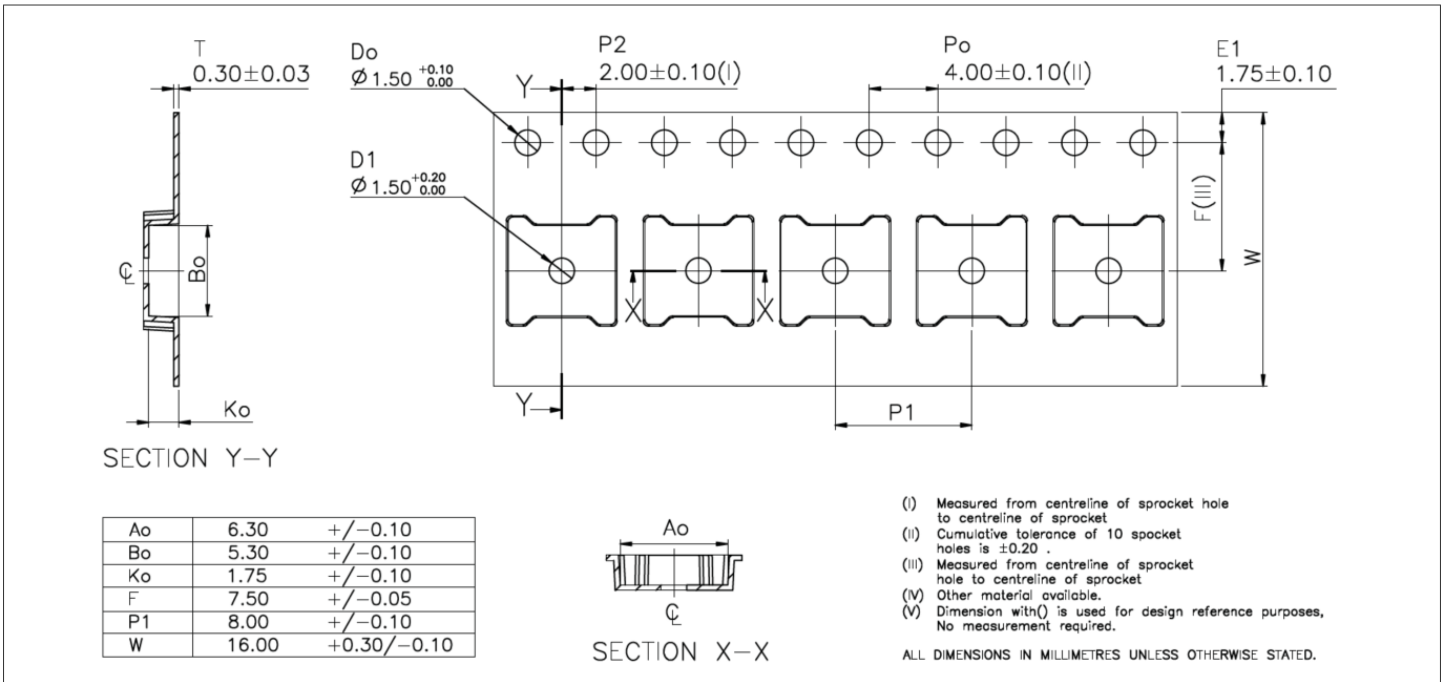


Figure 23 **XDP72x-001 recommended footprint**



Ao	6.30	+/−0.10
Bo	5.30	+/−0.10
Ko	1.75	+/−0.10
F	7.50	+/−0.05
P1	8.00	+/−0.10
W	16.00	+0.30/−0.10

Figure 24 **PG-LIQFN-23-1 package information**

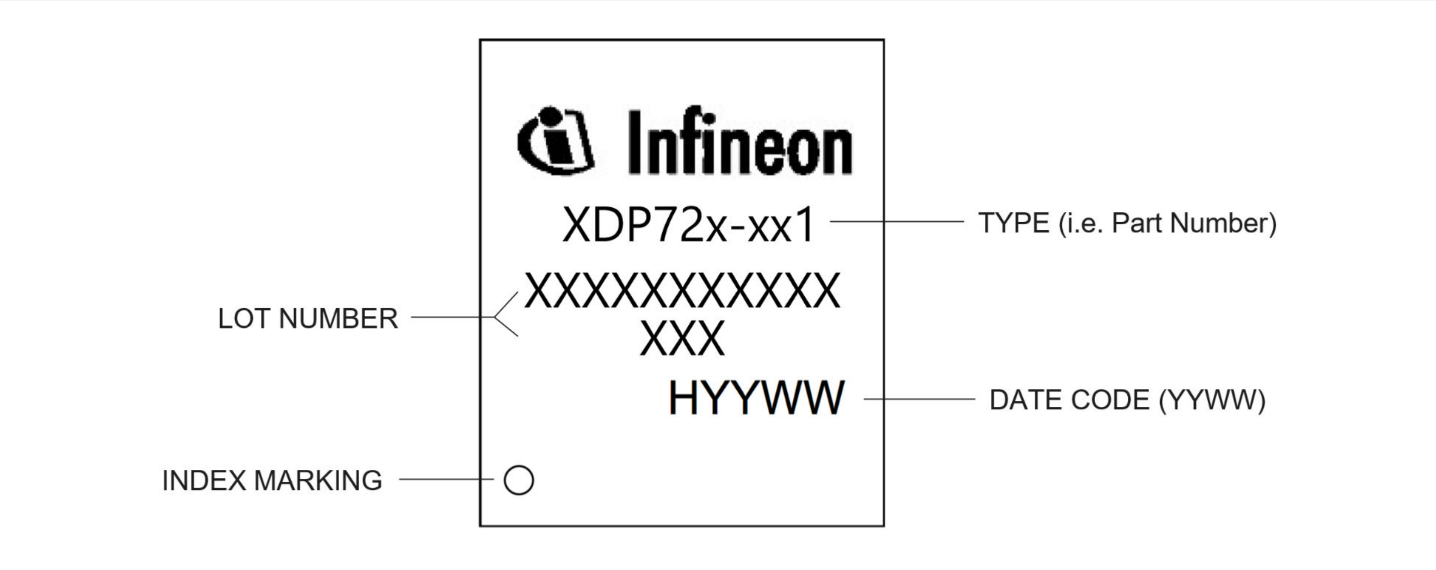


Figure 25 **XDP72x-xx1 package marking**

Green Product (RoHS compliant)

To meet the worldwide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). Further information on packages: https://www.infineon.com/packages

7 Revision history

Revision	Date	Notes (major changes since last revision)
1.0	2026-06-12	First release.

Trademarks

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