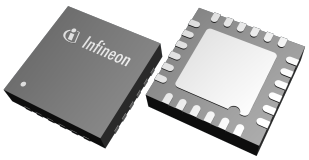
## Digital power supply controller for PWM and PFM applications



### Features

- Digital controller assisted high performance analog front ends and fully programmable ARM® Cortex™-M0 processor
  - 100 MHz clock, 32-bit, 64 kB OTP, 32 kB RAM, 80 kB ROM
- High performance, low latency digital hardware control loop for single rail up to two phases
- High-speed voltage sense
  - 100 MHz 11-bit ADC with 1.25 mV/LSB
  - Up to 2.1 V differential voltage range
  - 200 MHz edge detection comparator
- High-speed current sense
  - 100 MHz 9-bit ADC with 1 mV/LSB
  - Configurable symmetrical positive and negative input voltage range or asymmetrical input
- 6 high resolution Digital Pulse Width Modulated (DPWM) remappable outputs
  - 78.125 ps pulse width resolution
  - Adjustable dead times between pairs for both rising and falling edges with 1.25 ns or 2.5 ns resolution
  - Frequency range: 50 kHz to 2 MHz with 5 ns resolution
- 2 high-speed inputs for external fault shutdown or PWM edge control
- PWM edge alignment
  - Trailing, leading, and dual-edge modulation
- Configurable feedback control
  - Voltage mode, peak current mode
- Configurable modulation methods
  - Pulse-width modulation, phase shift modulation, frequency modulation
- Up to 11 GPIO pins
- Synchronization with external clock
- 4-channel, 10-bit, 0.926 Msps general-purpose ADC
  - 2.34 mV/LSB, input voltage range 2.4 V
- Communication peripherals
  - 1 MHz $I^2C$/PMBus®, full duplex SPI, full duplex UART
- 24-pin VQFN package
- Operating temperature: -40 ˚C to 125 ˚C

### Potential applications

- Isolated/non-isolated DC-DC PWM converters
- LLC converters
- Intermediate bus converters for datacenter/computing system
- Power supplies for telecom infrastructure/brick modules

### Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

### Description

The XDPP1140 and XDPP1148 are digital power supply controllers for AC/DC and DC/DC power converters. References to XDPP114x in this document apply to both the XDPP1140 and XDPP1148 versions of the product, while references to XDPP1140 or XDPP1148 specifically refer to the referenced version of the product. The main difference between these two product versions is that the XDPP1140 contains two voltage sense (VS) inputs and one current sense (IS) input while the XDPP1148 contains one VS input and two IS inputs.

## Description

The controller has high performance analog front end, a unique architecture with optimized power-processing digital blocks, and built-in ready to use firmware that minimizes firmware development effort. The state machine based configurable control loop architecture supports various modes of operation including PWM and PFM modulation, voltage mode and peak current mode control.

The XDPP114x includes a 32-bit, 100 MHz ARM® Cortex™-M0 RISC microcontroller sub-system that can be used for enhanced control, real-time monitoring, configuration of peripheral, and managing communications. It also allows firmware-based customization and implementation of housekeeping functions such as sequencing, blackbox data recording and interfacing.

The core power control functions are implemented by dedicated hardware or firmware pre-programmed in the ROM, allows fast time to market. Additional programs can be stored and executed out of the nonvolatile memory OTP and RAM. Developers have full control of their application and firmware. System designers can develop and compile their customized firmware in any commonly used ARM™ based develop environment.

The XDPP114x supports PMBus® 1.4 subsets and includes UART, SPI and I2C communication interfaces. PMBus® command set is runtime programmable, which allows config the commands on the fly.

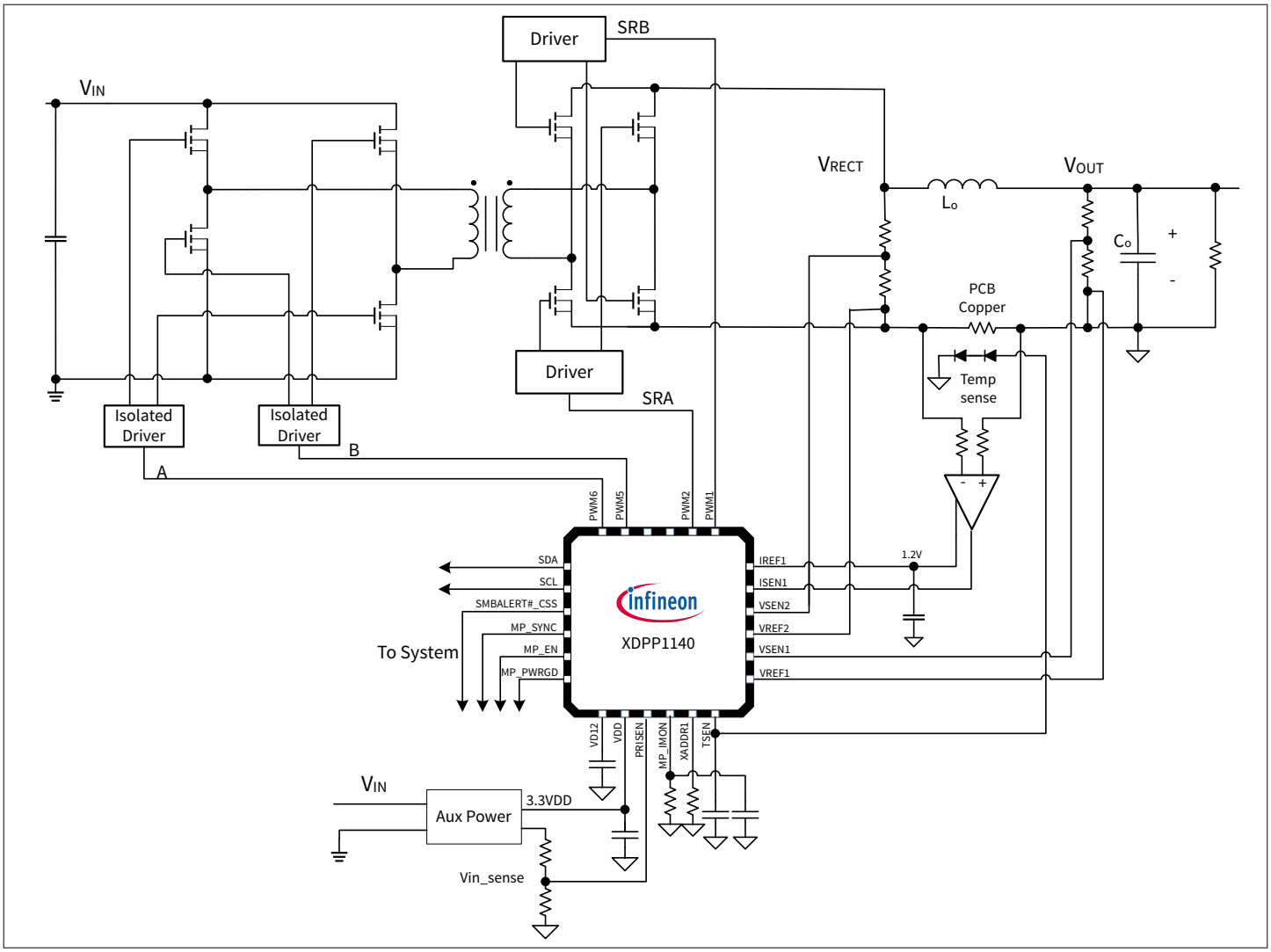
The XDPP114x supports many commonly used AC-DC and DC-DC topologies such as, LLC, hard-switched full bridge and half bridge, phase shifted full bridge, active clamp forward, non-isolated buck, buck-boost, boost, interleaved buck, interleaved buck-boost, and interleaved boost topologies.

The application diagram shows the XDPP1140 controller in a full-bridge to full-bridge converter.

Application specific features includes:

- Soft start with pre-bias (non-resonant topologies)
- Feed-forward compensation for PWM topologies
- Active current sharing
- LLC features
  - Hybrid soft start: PWM or phase-shift at the maximum frequency and frequency sweep
  - Adaptive SR turn-off based on $V_{DS}$ sensing
  - Light load operation including:
    - Burst mode at the maximum frequency
    - Diode emulation (DE) mode
    - Phase Shift duty cycle reduction at the maximum frequency for full-bridge LLC
- High efficiency and light load management
  - Burst mode (except ACF topology)
  - Phase dropping (interleave topologies)
- Flux balancing
- Phase current balancing
- Configurable non-linear PID and Fast Transient Response (FTR)
- Feature rich fault protections
  - Programmable over and under voltage protection (OVP, UVP) thresholds and response
  - Programmable over and under current protection (OCP, UCP) thresholds and response
  - Programmable fast over-current protection and short circuit protection
  - Programmable over and under temperature protection (OTP, UTP) thresholds and hysteresis
  - Programmable positive/negative peak current limit threshold
  - Internal and external temperature sensor
  - Feedback open loop protection
  - Programmable blanking time

**Description**




| Base part number | Package type | Standard pack form and Qty | | Application | Orderable part number |
|---|---|---|---|---|---|
| XDPP1140-100C | VQFN (24) 4 mm x 4 mm | Tape & Reel | 5000 | Single phase topologies, supports flux balancing | XDPP1140100CXUMA1 |
| XDPP1148-100C | | | | Single phase or interleaved topologies, supports current balancing between phases | XDPP1148100CXUMA1 |

# Table of contents

# 1 Block diagram

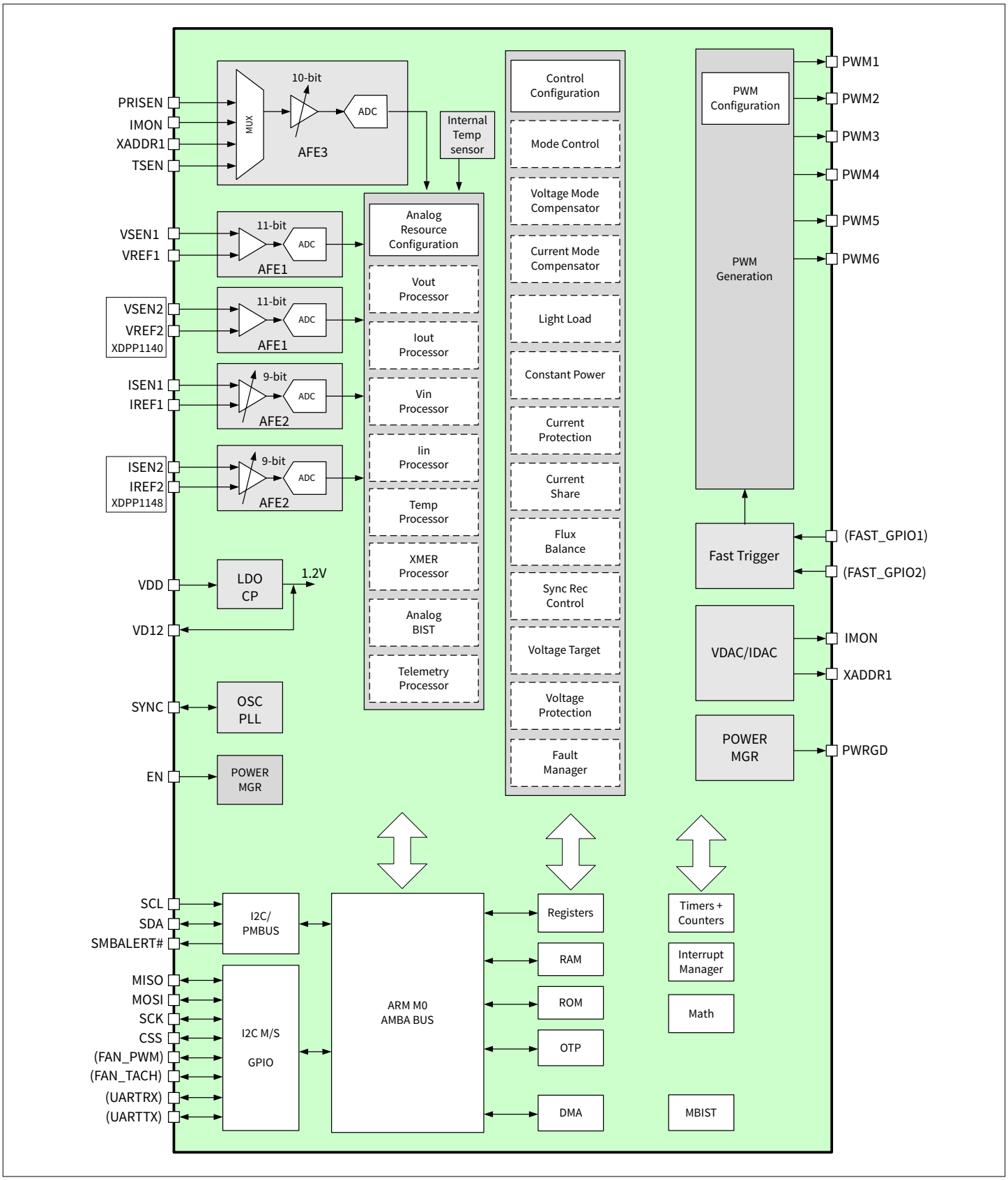



**Figure 1 Block diagram**

# 2 Product selection table

**Table 1 Product selection table**

| Feature | XDPP1140-100C | XDPP1148-100C | XDPP1188-200C |
|---|---|---|---|
| ARM M0 core processor | 100 MHz | 100 MHz | 100 MHz |
| High resolution DPWM outputs (78.125ps resolution) | 6 | 6 | 8 |
| Number of voltage sense ADC | 2 | 1 | 2 |
| Number of current sense ADC | 1 | 2 | 2 |
| General-purpose ADC channels | 4 | 4 | 4 |
| OTP | 64 kB | 64 kB | 64 kB |
| RAM | 32 kB | 32 kB | 32 kB |
| ROM | 80 kB | 80 kB | 80 kB |
| DPWM switching frequency | Up to 2 MHz | Up to 2 MHz | Up to 2 MHz |
| SPI serial bus | Yes | Yes | Yes |
| UART | Yes | Yes | Yes |
| PMBus® | Yes | Yes | Yes |
| Watchdog | Yes | Yes | Yes |
| On chip oscillator | Yes | Yes | Yes |
| Sync in and sync out functions | Yes | Yes | Yes |
| Temperature sense inputs | 1 | 1 | 1 |
| Total GPIO (general-purpose I/O pins) | 11 | 11 | 13 |
| Package offering | PG-VQFN-24-20 (4x4 $mm^2$) | PG-VQFN-24-20 (4x4 $mm^2$) | PG-VQFN-40-13 (5x5 $mm^2$) |

# 3 Pin configuration and functions

## 3.1 XDPP1140-100C package

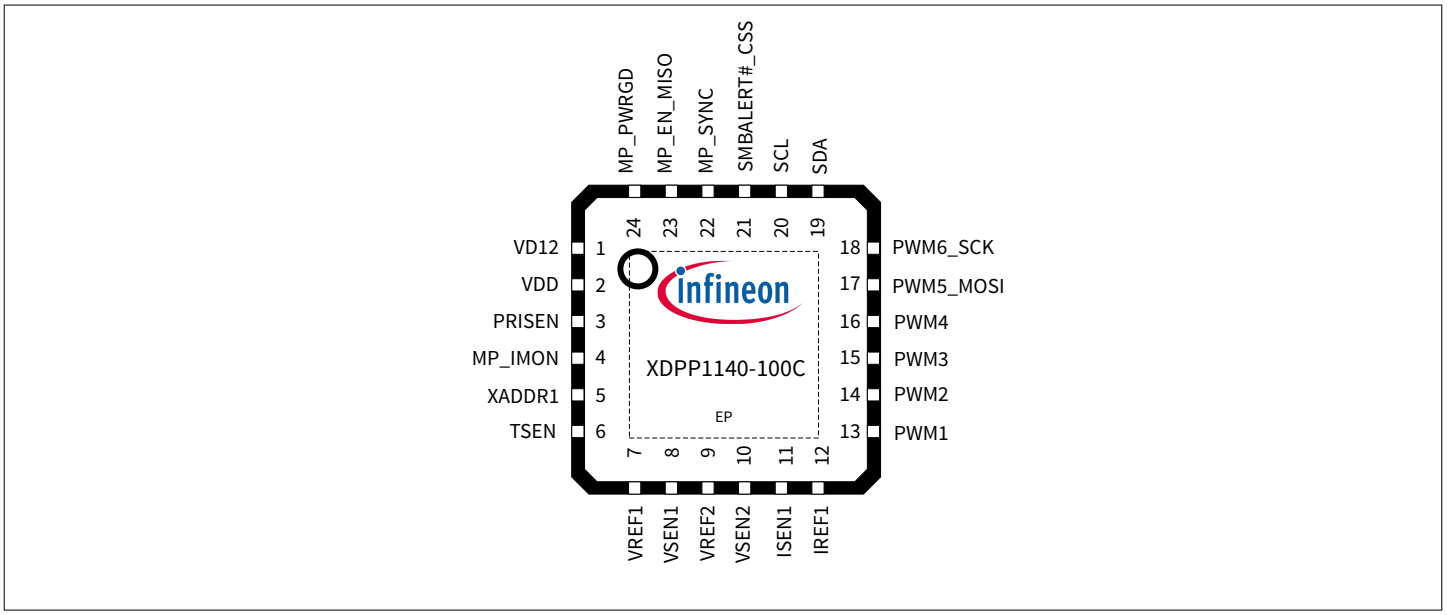



**Figure 2 XDPP1140-100C pin assignment**

**Table 2 XDPP1140-100C pin definition**

| Pin No. | Name | Primary assignment | Alternate assignment | Configurable GPIO |
|---|---|---|---|---|
| 1 | VD12 | 1.2 V supply bypass | – | – |
| 2 | VDD | 3.3 V main supply input | – | – |
| 3 | PRISEN | Primary voltage sensing input | GPA1 | – |
| 4 | MP_IMON | Output current monitor | GPA2/SYNC/FAN1_TACH/Fault/ Fast_GPI2/EN | Yes |
| 5 | XADDR1 | Address 1 | GPA3 | – |
| 6 | TSEN | Temperature sensing input | GPA4 | – |
| 7 | VREF1 | Differential voltage sensing 1, negative input | – | – |
| 8 | VSEN1 | Differential voltage sensing 1, positive input | – | – |
| 9 | VREF2 | Differential voltage sensing 2, negative input | – | – |
| 10 | VSEN2 | Differential voltage sensing 2, positive input | – | – |
| 11 | ISEN1 | Differential current sensing, positive input | – | – |

**(table continues...)**

**Table 2 (continued) XDPP1140-100C pin definition**

| Pin No. | Name | Primary assignment | Alternate assignment | Configurable GPIO |
|---|---|---|---|---|
| 12 | IREF1 | Differential current sensing, negative input | – | – |
| 13 | PWM1 | PWM1 output | SYNC/Fast_GPI1 | Yes |
| 14 | PWM2 | PWM2 output | SYNC/Fast_GPI2 | Yes |
| 15 | PWM3 | PWM3 output | SYNC/Fast_GPI1/FAN1_TACH | Yes |
| 16 | PWM4 | PWM4 output | SYNC/Fast_GPI2/FAN1_PWM | Yes |
| 17 | PWM5_MOSI | PWM5 output | SYNC/UARTRX/Fast_GPI1/ SPI_MOSI | Yes |
| 18 | PWM6_SCK | PWM6 output | SYNC/UARTTX/Fast_GPI2/ SPI_SCK | Yes |
| 19 | SDA | $I^2C$ serial data line | – | – |
| 20 | SCL | $I^2C$ serial clock line | – | – |
| 21 | SMBALERT#_CSS | SMBALERT line | SYNC/Fault/CSS | Yes |
| 22 | MP_SYNC | Synchronization input/output | FAN1_PWM/Fast_GPI1/Fault | Yes |
| 23 | MP_EN_MISO | Enable/sleep control | SYNC/SPI_MISO | Yes |
| 24 | MP_PWRGD | Power good output | SYNC | Yes |
| – | EP (exposed pad) | Ground | – | – |

## 3.2 XDPP1148-100C package

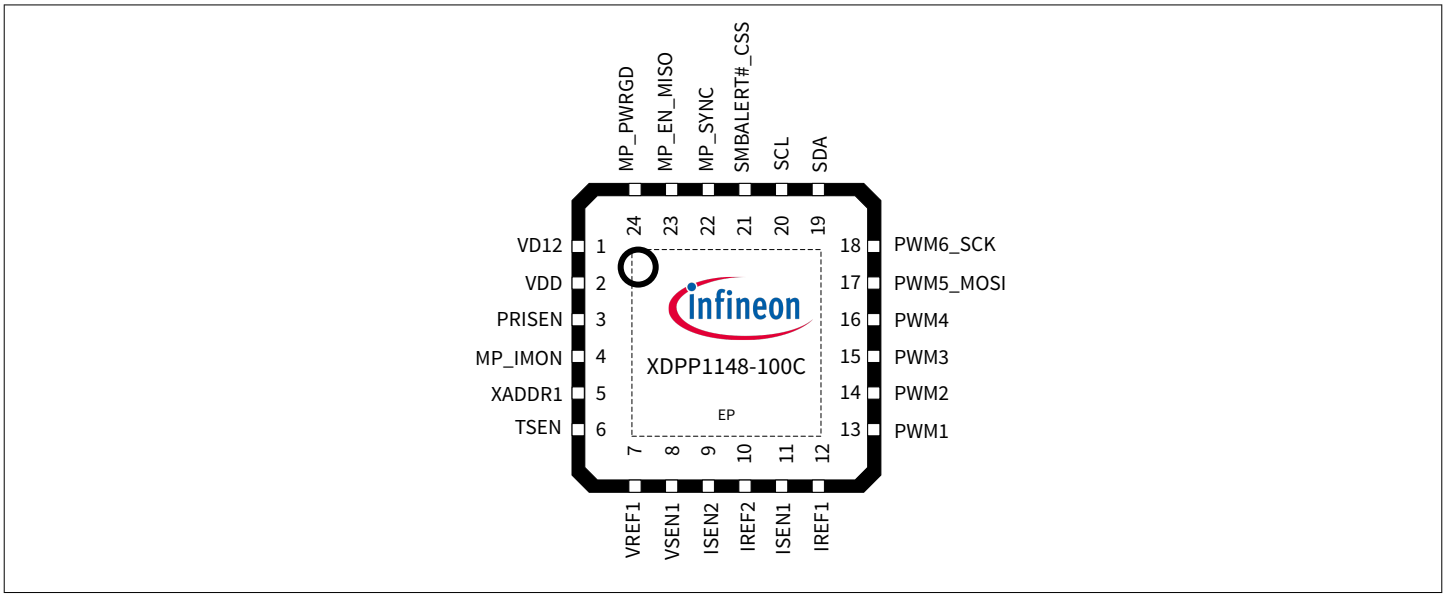



**Figure 3 XDPP1148-100C pin assignment**

**Table 3 XDPP1148-100C pin definition**

| Pin No. | Name | Primary assignment | Alternate assignment | Configurable GPIO |
|---|---|---|---|---|
| 1 | VD12 | 1.2 V supply bypass | – | – |
| 2 | VDD | 3.3 V main supply input | – | – |
| 3 | PRISEN | Primary voltage sensing input | GPA1 | – |
| 4 | MP_IMON | Output current monitor | GPA2/SYNC/FAN1_TACH/Fault/ Fast_GPI2/EN | Yes |
| 5 | XADDR1 | Address 1 | GPA3 | – |
| 6 | TSEN | Temperature sensing input | GPA4 | – |
| 7 | VREF1 | Differential voltage sensing, negative input | – | – |
| 8 | VSEN1 | Differential voltage sensing, positive input | – | – |
| 9 | ISEN2 | Differential current sensing of phase 2, positive input | – | – |
| 10 | IREF2 | Differential current sensing of phase 2, negative input | – | – |
| 11 | ISEN1 | Differential current sensing of phase 1, positive input | – | – |
| 12 | IREF1 | Differential current sensing of phase 1, negative input | – | – |
| 13 | PWM1 | PWM1 output | SYNC/Fast_GPI1 | Yes |
| 14 | PWM2 | PWM2 output | SYNC/Fast_GPI2 | Yes |
| 15 | PWM3 | PWM3 output | SYNC/Fast_GPI1/FAN1_TACH | Yes |
| 16 | PWM4 | PWM4 output | SYNC/Fast_GPI2/FAN1_PWM | Yes |
| 17 | PWM5_MOSI | PWM5 output | SYNC/UARTRX/Fast_GPI1/ SPI_MOSI | Yes |
| 18 | PWM6_SCK | PWM6 output | SYNC/UARTTX/Fast_GPI2/ SPI_SCK | Yes |
| 19 | SDA | $I^2C$ serial data line | – | – |
| 20 | SCL | $I^2C$ serial clock line | – | – |
| 21 | SMBALERT#_CSS | SMBALERT line | SYNC/Fault/CSS | Yes |
| 22 | MP_SYNC | Synchronization input/output | FAN1_PWM/Fast GPI1/Fault | Yes |
| 23 | MP_EN_MISO | Enable/sleep control | SYNC/SPI_MISO | Yes |
| 24 | MP_PWRGD | Power good output | SYNC | Yes |
| – | EP (exposed pad) | Ground | – | – |

Notes:

**1.** EP is the metal pad under the chip

**2.** SDA, SCL, SMBALERT#_CSS are open drain I/O pins

3. All digital GPIO pins are 3.3 V CMOS; the outputs are programmable to be CMOS or open drain
4. GPA: general-purpose analog input pin

# 4 Functional description

## 4.1 Introduction

The XDPP114x is a flexible, feature-rich digital controller, optimized for isolated and non-isolated dc-to-dc converters. The XDPP114x is designed to enable flexibility and provide excellent digital control for all the major fixed frequency topologies: pulse-width modulated (PWM) half-bridge (HB), PWM full-bridge (FB), PWM phase-shift full-bridge (PSFB), active clamp forward (ACF), non-isolated buck, boost and buck-boost. It also works for resonant LLC topologies including half-bridge (HB) LLC, full-bridge (FB) LLC, phase-shift full-bridge (PSFB) LLC. The XDPP1148 supports interleaved operation of buck, boost and buck-boost.

The features that require fast response are implemented by state machine in hardware and can be configured over the $I^2C$ port. These features include:

- Digital PID loop filter and compensation
- Pre-bias startup
- Feed-forward compensation
- Non-linear PID fast transient
- Active current sharing
- Current balancing between two phases
- Flux balancing of full-bridge converter
- Burst operation in light load
- Phase shedding

The fault protections are implemented in hardware for the shortest delay time. The fault thresholds, thresholds hysteresis and fault count are configurable. The fault response is managed by firmware for flexibility. The industry standard PMBus® interface also provides access to the monitoring and system control functions.

The integrated ARM® Cortex® -M0 microcontroller and built-in non-volatile memory provide extensive programming and customization of functions such as, the frequency dithering, GPIO signal timing, soft start timing and sequencing, dynamic dead time, and blackbox data recording.

### 4.1.1 ARM® Cortex™ –M0 core

The controller embeds the smallest ARM processor – the ARM® Cortex™-M0 processor. It is a high performance 32-bit processor with low gate count, minimal power requirements, and reduced code footprint. It is an optimized interrupt controller, allows to be used in hard real-time applications. The ARM® Cortex™ -M0 processor clock frequency $f_{CLK}$ is 100 MHz.

### 4.1.2 Memories

The controller has 80 kB boot ROM that contains the initial firmware startup routines for PMBus® communication. This boot ROM is executed after power-on-reset checks. The controller also supports customization of the boot program by allowing an alternative boot routine to be executed from the one-time programmable (OTP) nonvolatile memory (NVM). Control registers can be reprogrammed in the field via the serial communication ($I^2C$) bus and stored into the OTP NVM. For run time data storage and scratchpad memory, a 32 kB RAM is available.

### 4.1.3 Communication ports

The controller provides $I^2C$, SPI, and UART communication ports.

#### 4.1.3.1 I2C/PMBus®

All operating parameters in the controller are configurable via the $I^2C$ serial interface (SDA, SCL). The SDA, SCL support two logic levels, 3.3 V and 1.8 V. By default, the controller uses 3.3 V logic. The controller supports all three $I^2C$ speeds: standard (100 kHz), fast (400 kHz) and fast mode plus (1 MHz) operating frequency.

The controller is compliant to PMBus® Power System Management Protocol Specification, revision 1.4.1. The $I^2C$/PMBus® interface allows configuration of the controller as well as monitoring fault status, voltage, current, power, and temperature telemetry.

### 4.1.3.2 SPI

SPI is a high-speed communication protocol that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the controller at a programmed bit-transfer rate of up to 5 MHz. The SPI port supports two logic levels, 3.3 V and 1.8 V. For 3.3 V output, the SPI pins can be configured as CMOS (push-pull) or open-drain output. For 1.8 V logic, it must be configured as open-drain output and use external pull-up.

The controller supports both slave and master mode. Since the SPI is typically used for communication between the controller and external peripherals, such as shift registers, SPI EPROMs and analog-to-digital converters, it should be configured as master in these applications. On the other hand, it should be configured as slave when receiving control from another controller in the system.

### 4.1.3.3 UART

A full duplex Universal Asynchronous Receiver/Transmitter (UART) interface is included in the controller. The baud rate, word size, buffer depth are configurable through registers. A loop back feature can also be setup for firmware verification.

The UARTTX and UARTRX pins are configured using assigned GPIO pins. See Table 6 for the list of GPIO pins and their pre-defined functions.

### 4.1.3.4 Address offset

The base address of $I^2C$ and PMBus® is configured by firmware registers **addr_pin_i2c_address_offset** and **addr_pin_pmbus_address_offset**. By default, the base address of $I^2C$ is 0x10, and the base address of PMBus® is 0x40. Address offset can be added to the base address to differentiate multiple controllers that have the same configuration (base address) in the system. The controller uses XADDR1 pin for $I^2C$/PMBus® address offset by connecting a resistor from the XADDR1 to ground. This offset decoding is enabled by default.

The controller supports 16-valent or 8-valent address table as shown in Table 4 and Table 5. The bit [1] of firmware register **addr_pin_xv** configs the xvalent selection between 16-valent and 8-valent. To properly set the addresses, resistors with 1% tolerance or better must be used. The resistor values are designed for E12 series for system cost saving. The XADDR1 resistor measurement only takes place during controller initialization. On-the-fly modification of the address offset is not supported. The configuration must be stored in OTP memory and only takes effect after reboot.

**Table 4 $I^2C$/PMBus® address offset of 16-segment decode**

| XADDR1 resistor to GND (1%) | Address offset |
|---|---|
| 680Ω | 0x00 |
| 1 kΩ | 0x01 |
| 1.5 kΩ | 0x02 |
| 2.2 kΩ | 0x03 |
| 3.3 kΩ | 0x04 |
| 4.7 kΩ | 0x05 |
| 6.8 kΩ | 0x06 |
| 10 kΩ | 0x07 |
| 15 kΩ | 0x08 |
| 22 kΩ | 0x09 |
| 33 kΩ | 0x0A |
| 47 kΩ | 0x0B |
| 68 kΩ | 0x0C |

**(table continues...)**

**Table 4 (continued) I²C/PMBus® address offset of 16-segment decode**

| XADDR1 resistor to GND (1%) | Address offset |
|---|---|
| 100 kΩ | 0x0D |
| 150 kΩ | 0x0E |
| 220 kΩ | 0x0F |

**Table 5 I²C/PMBus® address offset of 8-segment decode**

| XADDR1 resistor to GND (1%) | Address offset |
|---|---|
| 10 kΩ | 0x00 |
| 22 kΩ | 0x01 |
| 33 kΩ | 0x02 |
| 47 kΩ | 0x03 |
| 68 kΩ | 0x04 |
| 100 kΩ | 0x05 |
| 150 kΩ | 0x06 |
| 220 kΩ | 0x07 |

### 4.1.4 GPIO

The XDPP114x provides up to 11 general-purpose input outputs (GPIOs). All GPIO pins are shared with multiple alternative functions. The GPIO configuration is programmed by the function register of each GPIO pin. The GPIO polarity is configurable. When configured as an output pin, the MP_IMON, MP_EN, PWM5_MOSI and PWM6_SCK pins can choose output buffer as CMOS output (push-pull) or open-drain output. All other GPIO pins can be configured as CMOS or emulated open-drain output.

The GPIO configuration is only loaded during initialization. Modifications to GPIO registers need to be stored in OTP and only takes effect after reboot or FW reset.

**Table 6 GPIO and I²C/SPI multi-purpose pin functions**

| Name | Function 0 | Function 1 | Function 2 | Function 3 | Function 4 | Function 5 | Function 6 | Function 7 |
|---|---|---|---|---|---|---|---|---|
| MP_IMON | A:IMON | GPIO[3] | GPIO[11] | IO:SYNC | I:FAN1_TACH | O:GENERIC_FAULT | I:FAST_GPI2 | GPIO[0] (EN) |
| PWM1 | O:PWM1 | GPIO[5] | GPIO[13] | IO:SYNC | – | – | I:FAST_GPI1 | – |
| PWM2 | O:PWM2 | GPIO[7] | GPIO[15] | IO:SYNC | – | – | I:FAST_GPI2 | – |
| PWM3 | O:PWM3 | GPIO[6] | GPIO[14] | IO:SYNC | I:FAN1_TACH | – | I:FAST_GPI1 | – |
| PWM4 | O:PWM4 | GPIO[2] | GPIO[10] | IO:SYNC | O:FAN1_PWM | – | I:FAST_GPI2 | – |
| PWM5 | O:PWM5 | GPIO[3] | GPIO[11] | IO:SYNC | I:UARTRX | I:S_MOSI | I:FAST_GPI1 | O:M_MOSI |

**(table continues...)**

**Table 6 (continued) GPIO and I²C/SPI multi-purpose pin functions**

| Name | Function 0 | Function 1 | Function 2 | Function 3 | Function 4 | Function 5 | Function 6 | Function 7 |
|---|---|---|---|---|---|---|---|---|
| PWM6 | O:PWM6 | GPIO[4] | GPIO[12] | IO:SYNC | O:UARTTX | I:S_SCK | I: FAST_GPI2 | O:M_SCK |
| SMBALERT#_CSS | IO:SMBALERT_N | GPIO[6] | GPIO[14] | IO:SYNC | O:GENERIC_FAULT | I:S_CSS | – | O:M_CSS |
| MP_SYNC | – | GPIO[7] | GPIO[15] | IO:SYNC | O: FAN1_PWM | O: GENERIC_FAULT | I: FAST_GPI1 | – |
| MP_EN_MISO | GPIO[0] (EN) | GPIO[10] | GPIO[8] | IO:SYNC | – | O:S_MISO | – | I:M_MISO |
| MP_PWRGD | GPIO[1] (PWRGD) | GPIO[12] | GPIO[9] | IO:SYNC | – | – | – | – |

Notes:

1. Analog functions prefixed with "A:"
2. Digital input prefixed with "I:", output prefixed with "O:", input/output prefixed with "IO:"
3. All GPIOs are input/output; the "IO:" prefix is omitted
4. Input priority by lowest pin number (e.g., if MP_IMON and PWM6_SCK are both programmed to SYNC, the input is taken from MP_IMON due to its lower pin number)

### 4.1.5 Register map

The controller is configured by application specific parameter settings loaded into control registers. Direct I²C register access is disabled by default. Instead, it is achieved via PMBus®. The MFR_REG_WRITE, MFR_REG_READ and the MFR_AHB_ADDRESS commands are used write and read control registers. The access to register map is supported by the XDP Designer GUI without extra steps.

The control registers are not pre-programmed at the factory. Control registers should be programmed in each specific application and stored into the on-chip nonvolatile memory (NVM), which is then downloaded to the control registers during initialization of the controller as it powers up. The controllers support multiple reprogramming cycles which is easily accomplished with the XDP Designer GUI or System Programmer software.

The controller also supports storing multiple configurations in the NVM. It can store up to 16 configurations, and these configurations can be reprogrammed if needed.

## 4.2 Analog blocks and subsystems

### 4.2.1 Power supply

Operating from a single +3.3 V (VDD) supply to the controller, an on-chip low drop-out (LDO) regulator generates an internal +1.2 V voltage at VD12 pin. Both VDD and VD12 pin should have 1 µF + 0.1 µF ceramic bypass capacitors for noise filtering. Place the bypass capacitors as close as possible to VDD and VD12 pins. Do not apply voltage to or ground VD12 pin. VD12 pin can be used as 1.2 V reference of the current sense input, but not intend to drive a load.

The controller can enter sleep mode to reduce quiescent current and system standby power. The sleep mode current consumption is $I_{DD\_sleep}$. It is capable wakeup from sleep mode after $t_{wake}$. If sleep mode is not desired, it can be disabled and allows faster response to the EN input. The EN logic can be configured to be active-high or active-low.

### 4.2.2 Oscillator and PLL

An internal oscillator running at $f_{OSC}$ is incorporated in the controller for pulse-wdith modulation (PWM)/pulse-frequency modulation (PFM) generator, which is generally referred to as PWM in the rest of the document. The frequency programming resolution is 5 ns. With a 6-bit interpolator, the controller offers high PWM resolution of 78.125 ps. Using a 12-bit time-based period and frequency control, the maximum supported pulse width is 20.48 µs

(4096 x 5 ns). This sets the minimum switching frequency to approximately 50 kHz. The maximum switching frequency is 2 MHz. For LLC topologies, the frequency modulation resolution is 2.5 ns.

A typical LLC frequency modulation waveform is shown in Figure 4. The top axis shows the compensated error signal (that is, PID output). The second axis shows the resulting PWM waveform of even cycle, followed by the PWM of odd cycle. Lower PID output corresponds to higher switching frequency. The signals on the next two axes are PWM outputs which have hatched lines indicating where the deadtimes are applied. The bottom two axes are the secondary SR PWM waveforms which follow primary PWM with a maximum on-time limit.

A typical PWM generation waveform is shown in Figure 5. The top axis shows the analog behavioral waveforms of a dual-edge modulator ($V_{mod}$) and the compensated error signal (that is, PID output). The second axis shows the resulting PWM waveform. The signals on the bottom four axes have hatched lines indicating where the deadtimes are applied.

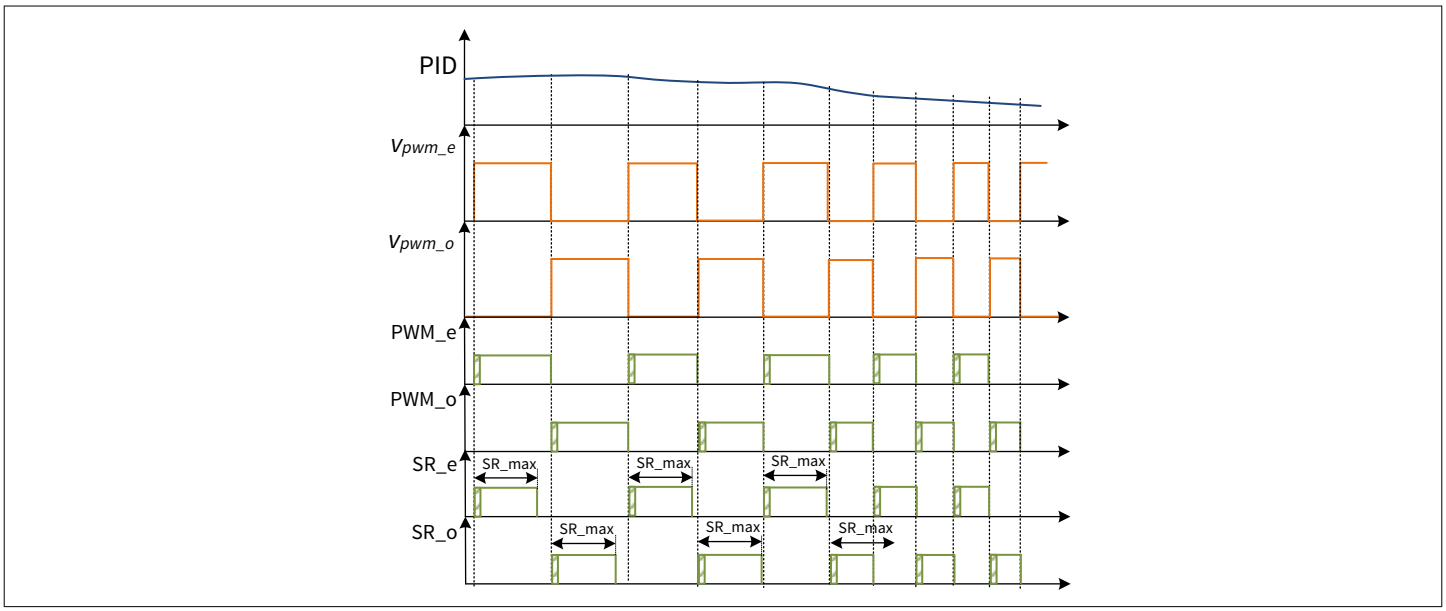



**Figure 4 PFM generation of LLC topology**

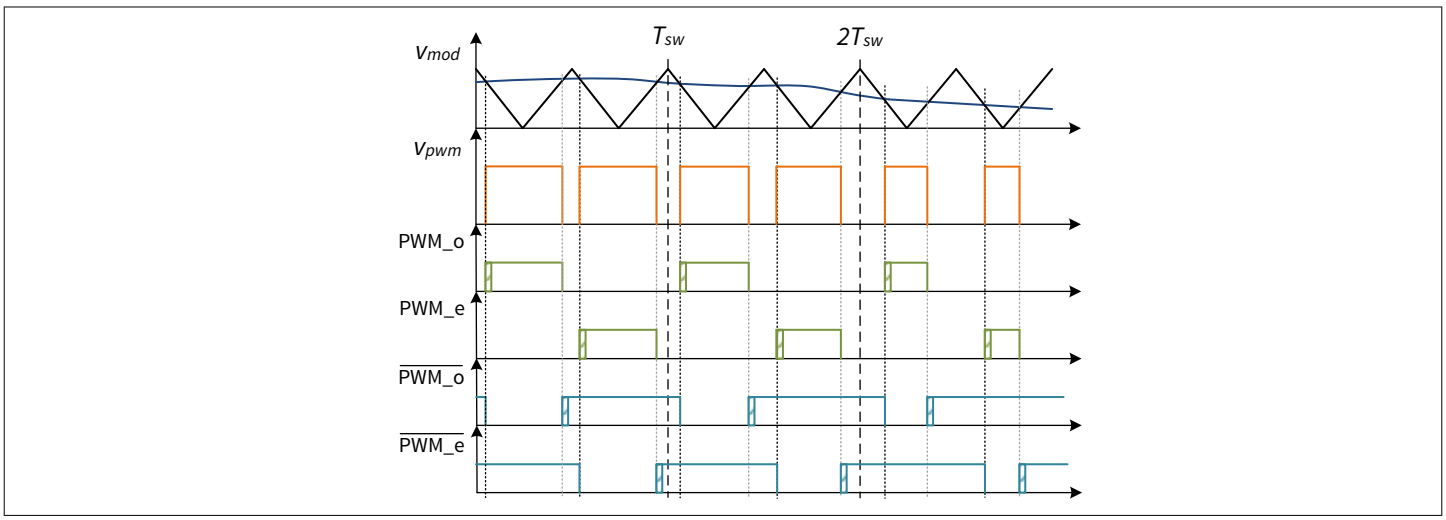



**Figure 5 PWM Generation of PWM topology**

Deadtime refers to the amount of time between the turning-off of one switch and the turning-on of another switch where both are off to prevent unintentional short circuit conditions. The standard way of implementing deadtime is to use leading edge-blanking. Each PWM generator is capable of blanking the rising edge by a programmable amount. The controller supports two sets of deadtime resolutions and ranges: 0-318.75 ns in 1.25 ns increments or 0-637.5 ns in 2.5 ns increments. The controller also supports adjusting the falling edge of each PWM if required. The value of deadtime can be modified on-the-fly during normal operation to allow efficiency optimization.

The PWM outputs are 3.3 V CMOS signals which are set to high impedance during reset, configuration, and initialization. The PWM outputs that are mapped to a loop to drive MOSFETs is pulled to the state defined in the configuration after firmware completed the initialization. The PWM off-state level can be set to low or high. By default, the PWM off-state is low and all the PWMs that are mapped to a loop stay low during shutdown.

The multi-purpose MP_SYNC pin can be configured as an input to allow synchronization to an external clock signal, or as an output to provide a clock that other controllers synchronize to. Any GPIO pin can be configured as SYNC function. When SYNC pin is configured as an input, the PLL receives a periodic signal. The input signal period is limited to ±12.5% of the programmed switching period to lock the sync clock. Once locked, the controller can remain in sync for a maximum of ±25% of the programmed switching period. The SYNC output signal is a square wave with the rising edge aligned with PWM signal per topology and type of modulation. For LLC topologies, the SYNC output follows the real-time switching frequency and has a fixed pulse width.

#### 4.2.2.1 The 3rd ramp

Besides the two standard oscillator ramps that generate PWM outputs for up to two phases, the controller also provides a third ramp (ramp2). The frequency of the third ramp can be configured independently and different from the two standard ramps (ramp0 and ramp1). It can also be synchronized to ramp0 or external frequency if desired. The third ramp is not associate with any closed-loop control thus only supports open-loop operation. The rising and falling edges of the third ramp can be programmed independently by FW patch.

With the third ramp, a single controller can drive a regulated (closed-loop) stage and an open-loop stage.

### 4.2.3 Voltage sense AFE1

The XDPP1140 offers two dedicated high-speed voltage analog-to-digital converters (ADC) as analog front end (AFE1), while the XDPP1148 offers one dedicated high-speed VADC. The voltage sense AFE1 can be used as voltage sense processor (VSP) or rectified voltage sense processor (VRSP).

The major functions of the VSP and its associated blocks are:

- Voltage ADC full rate interface to the digital domain
- Voltage ADC gain and offset trim (digital trim)
- Voltage scaling (external resistor divider)
- Input or output voltage computation (configurable input or output sense)
- Over/under voltage protection comparators and fault
- Fast transient (FTR) mode and FTR exit comparators
- Burst mode and burst mode exit comparators

The VRSP and its associated blocks have the following functions in addition to the above:

- 200 MHz edge comparator with digital de-glitcher
- Measure $V_{RECT}$ voltage of the even and odd half cycles of bridge topologies
- Measure $V_{RECT}$ voltage on the even cycle for non-bridge topologies
- Average the measured even and odd $V_{RECT}$ voltage
- Flux balancing circuit
- Input voltage processing

The simplified VSADC block diagram is shown in Figure 6

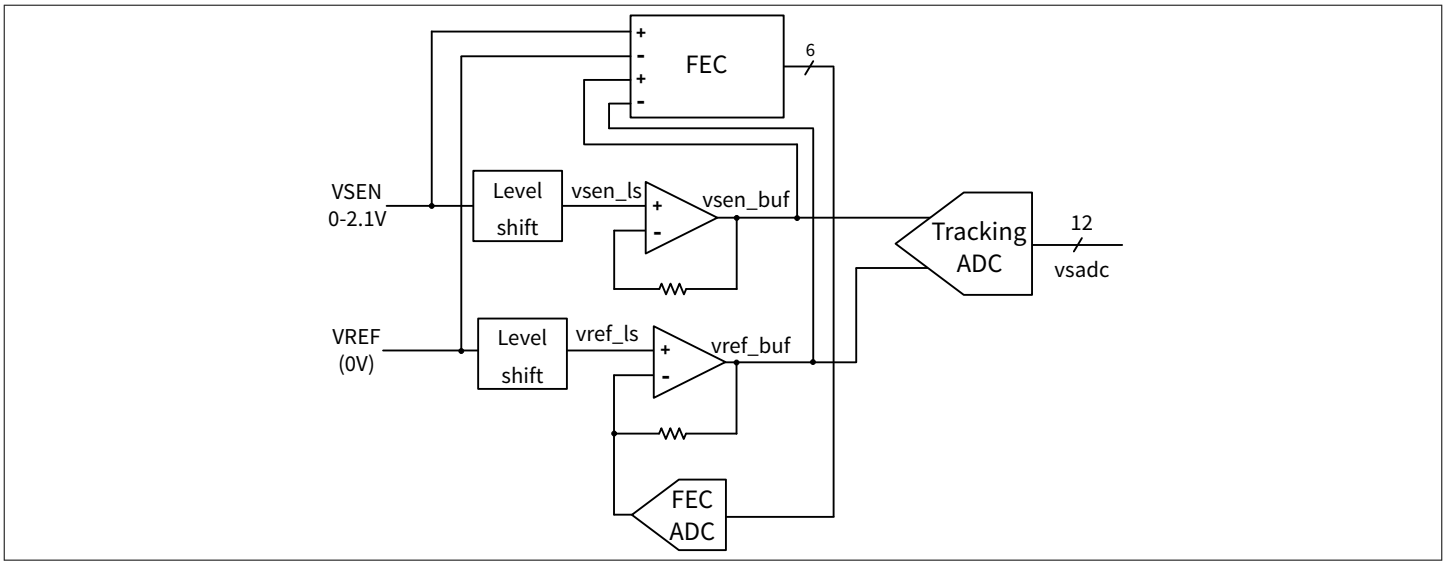



**Figure 6 Voltage sense ADC block diagram**

The level shifters allow wide input voltage range, 0.0 to 2.1 V, as well as providing a high input impedance. The unity gain buffers provide additional drive strength to the tracking ADC input stage. The front end offset compensator (FEC) is to reduce the effects of temperature, stress and lifetime offset-drift in the AFE.

The simplified block diagram of the tracking ADC is shown in Figure 7. The summing amplifier amplifies the difference between the buffered differential sensed voltage and the DAC output voltage.

The output of the summing amplifier drives the comparator whose output determines the size and direction of the next step for the tracking integrator. The tracking integrator output represents the analog-to-digital converted sensed voltage. It is also used to drive the DAC whose output is summed in the summing amplifier.

Tracking ADC resolution is 12 bits with an input referred LSB weight of 1.25 mV. Note that the AFE input range is restricted to maximum of 2.1 V, meaning only the lower 11 bits of the ADC output are actually used. For output voltage sensing, 3-bit modulation is added to the reference voltage to achieve 156.25 µV resolution. The voltage sense input has a nominal input impedance of 1 MΩ. The ADC is clocked at 100 MHz and a voltage sense front-end amplifier process the voltage at 50 MHz. There is no need for anti-alias filter, but it is advantageous to add a high bandwidth external RC filter network to attenuate high frequency noise in the voltage sense lines. This RC filter should cause minimal impact on the phase margin of the feedback loop.

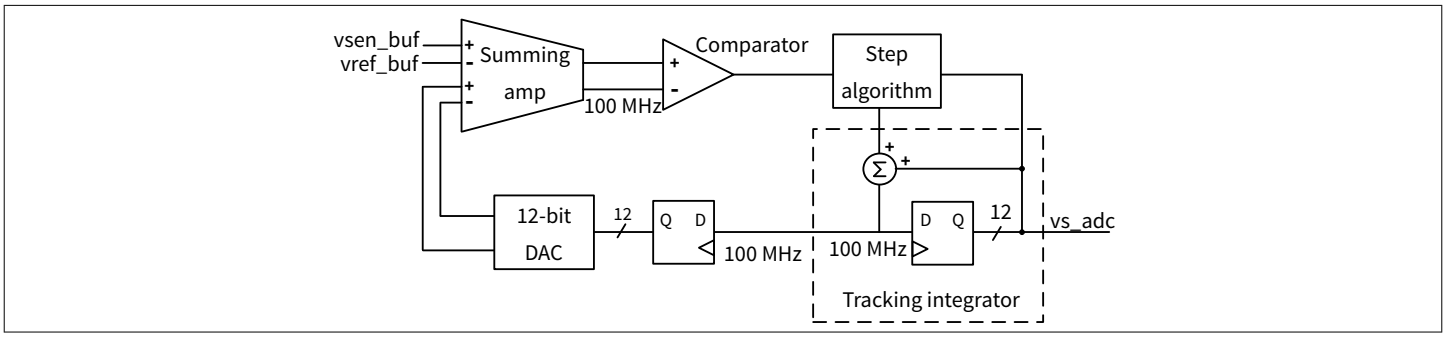



**Figure 7 Tracking ADC block diagram**

The VRSP is responsible for controlling the VSEN1 or VSEN2 ADC when they are used to measure the rectified voltage waveform ($V_{RECT}$). $V_{RECT}$ sensing is often used to sense the input voltage indirectly from the secondary side of the transformer. Figure 8 illustrates how sampling of the $V_{RECT}$ waveform is achieved. Noise has been added to the sensed $V_{RECT}$ waveform at VSENx pin to highlight the importance of sampling window timing. The AFE1 has an edge detector running with 200 MHz clock. It detects the rising and falling edges of $V_{RECT}$ waveform, whose output is shown as $T_{detect}$ in Figure 8. After the rising edge is detected, a programmable blanking window is added. This blanking window should be configured to be longer than the duration of voltage spikes and ringing, with a minimum recommended value of 250 ns for the tracking ADC to settle. After the blanking window, the sampling of the rectified voltage starts, shown as the $T_{sample}$ waveform. The comparator for the VSEN ADC is prepositioned to the value of the last cycle to

minimize the time required for the ADC to properly track the voltage. The sampling window ends when the associated PWM signal goes low.

The input voltage is calculated based on $V_{RECT}$ sensed voltage, $V_{RECT}$ resistor divider scale and the transformer turns ratio. Faults and warnings including input overvoltage and undervoltage can be detected by the VRSP when it is being used for input voltage sensing.

The timing of the rising and falling edges of the rectified voltage waveform, along with the magnitude, is used for transformer protection, that is, in full-bridge voltage mode converter, volt-second flux balancing. To avoid waveform and timing distortion, it is not recommended to add any filter to the input of VSEN when it is used for $V_{RECT}$ sensing.

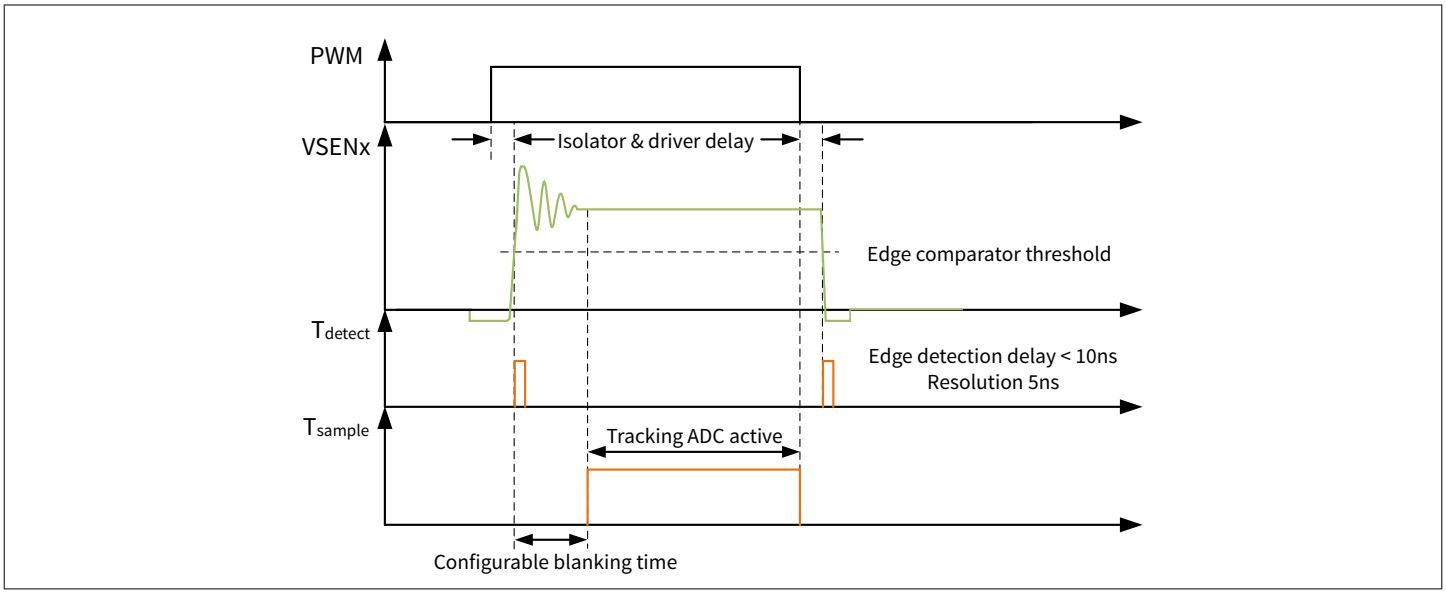



**Figure 8 Timing of $V_{RECT}$ sensing**

### 4.2.4 Current sense AFE2

The XDPP1140 offers one dedicated high-speed differential current sense ADC as AFE2, while the XDPP1148 offers two current sense ADCs. The current sense AFE2 is designed to sense current via low ohmic sense resistor or PCB copper trace, as well as through current sense transformer for primary current. The ISADC (ISEN1, ISEN2) is 9-bit ADC. It operates at 100 MHz and provides fast short-circuit protection (SCP). The resolution of the current sense ADC is 1 mV/LSB. The typical reference level (voltage at IREF pin) is 1.2 V.

The controller supports both primary and secondary current sense. When sensing primary current through a current transformer, symmetric positive and negative input voltage range (± 256 mV) is enabled. This feature does not require rectifying the signal, thus simplifying the external circuit. When sensing secondary current, a configurable digital offset can be used to adjust the voltage level at 0 A, thus increasing the effective positive input voltage range. The maximum digital offset voltage is 252 mV.

The simplified block diagram of the current sense ADC is shown in Figure 9.

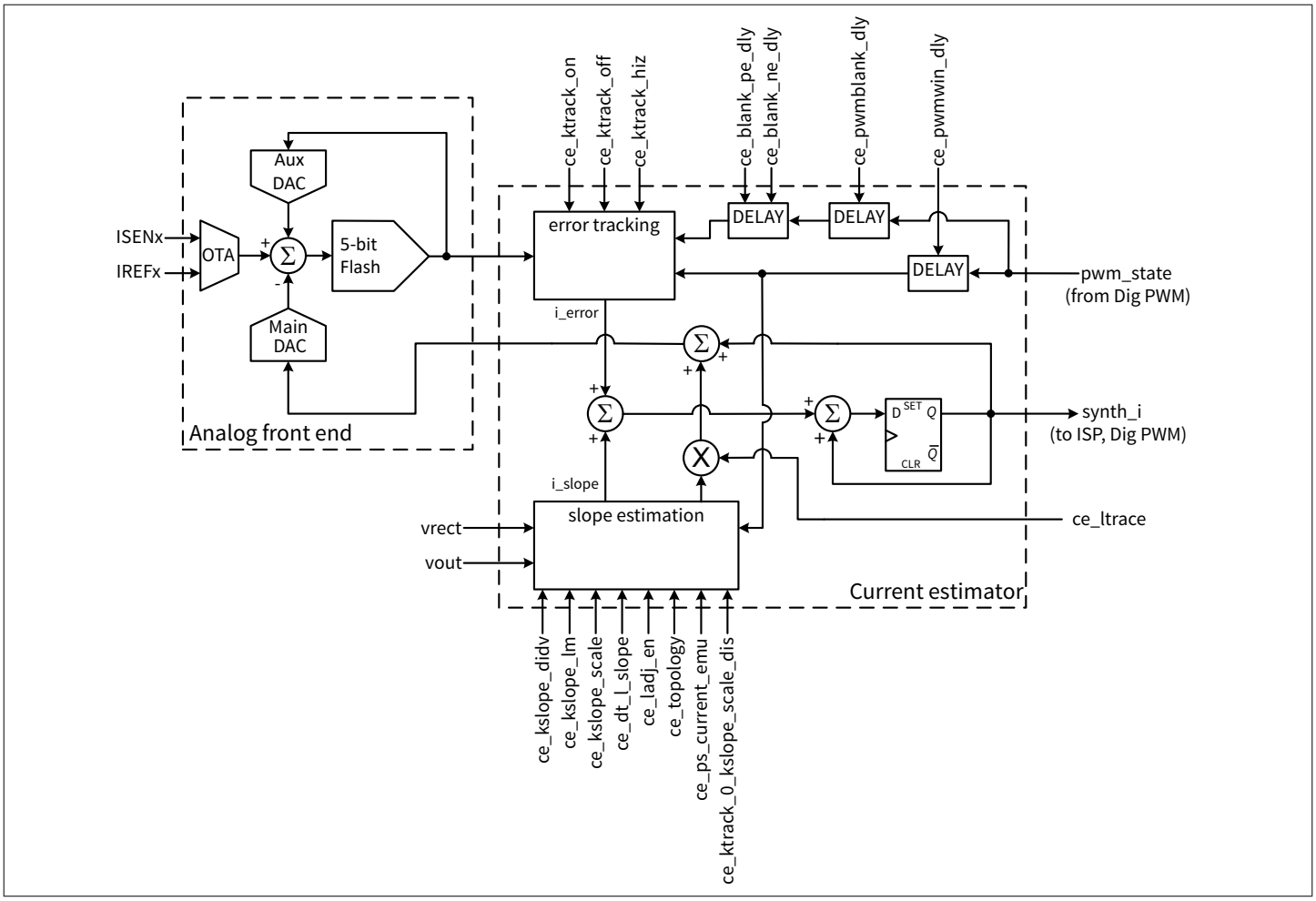



**Figure 9 Simplified block diagram of the current sense ADC**

For PWM topologies, the current estimator provides a digital reconstruction of the secondary side inductor current or the primary side current, depending on the configuration. The shape of this current is obtained through slope estimation function. Based on the state of the PWM, the controller continuously predicts the current. The result of the prediction is combined with the actual measured current to be processed by the controller. Hence, the noise in the measurement can be filtered out without losing the valuable ripple current information.

The current estimator supports compensation of the following non-idealities associated with typical current sense schemes:

- The voltage step induced by the parasitic inductance of the current sense resistor
- Output inductance variation with output current
- Leading and falling edge blanking time for noise rejection after PWM toggles
- Propagation delay of the current sense circuitry

For LLC topologies, the current estimator circuit is bypassed. The output of the current sense block purely relies on ADC measurement. The ADC is capable of tracking sinusoidal current waveform with slew rate up to 1.6 mV/ns.

If PCB copper trace is used for current sensing, temperature compensation should be considered to improve the accuracy. The controller continuously monitors the temperature and uses this information to compensate for resistance changes over temperature. The built-in temperature coefficient is 0.39%/°C for copper material. Custom temperature coefficient can be implemented using FW patch.

The controller provides several mechanisms for improving the current sense accuracy. To reduce the switching noise, leading edge and trailing edge blanking times are implemented at PWM transitions. In addition, the controller takes multiple current measurements and the results are averaged over every switching cycle. Furthermore, the controller supports compensation of the parasitic inductance of current sense resistor.

The polarity of the current sense can be configured. When inverted, the current estimator is disabled and the current sense relies solely on the ADC. The default configuration is non-inverted.

The major functions of the ISP and its associated blocks are:

- Current ADC full rate interface to the digital domain
- Current ADC gain and offset trim (digital trim)
- Current scaling
- Output current computation
- Output current shunt temperature compensation
- Output over/under current protection comparators and fault
- Input current computation
- Input over current protection comparators and fault
- Cycle-by-cycle peak current limit

### 4.2.5 General-purpose AFE3

The general-purpose ADC AFE3, also referred to as telemetry ADC (TS ADC), is a 10-bit, high-speed ADC. The resolution of the general-purpose ADC is 2.344 mV, with a sampling frequency of 0.926 MHz. The general-purpose ADC block consists of 8 channels with 4 channels externally accessible through pins PRISEN, MP_IMON, TSEN and XADDR1 as shown in Figure 10. It can be configured to digitize voltage, impedance, and temperature.

The conversion sequence of the channels can be customized or set to auto sequencing per mux control registers **ts_muxctrl1**, **ts_muxctrl2**, **ts_muxmode**.

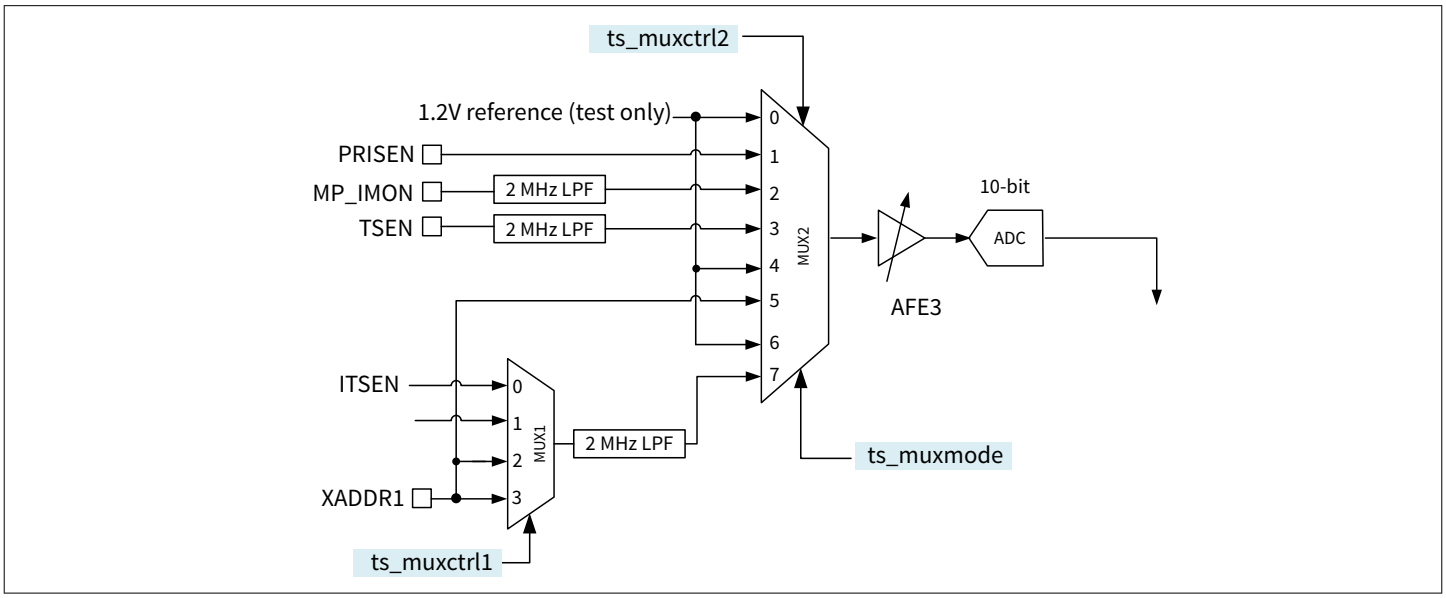



**Figure 10 Telemetry ADC block diagram**

#### 4.2.5.1 IMON and active current sharing

The IMON pin has an internal current source digital-to-analog converter (DAC) for representing the output current. A current proportional to the output current is sourced from IMON pin. This can be used for output current monitor, and for active current sharing between multiple parallel modules. The IMON current DAC (IDAC) is 6-bit DAC with a range of 0 to 640 µA. There is 4-bit accumulated dithering that drives an extra LSB input to the DAC for extra resolution (total 6+4 bit). The gain of the current source is configurable which allows to scale the current source per application. At no load, the source current is 160 µA. Current lower than 160 µA indicates negative output current.

For active current sharing, it is necessary to connect a 2.2 kΩ precision resistor ($R_{ishare}$) between IMON and a GPIO pin. The GPIO pin is used as a switch to disconnect the $R_{ishare}$ when the converter is not in regulation such as in off state or in fault shutdown. When the converter is in regulation and the current sharing is active, the GPIO pin connects the $R_{ishare}$ to ground, thus closing the circuit for the current source DAC at IMON pin and creating a voltage proportional to

the output current. The IMON pins of each converter are connected together, referred to as the Ishare bus. The voltage of Ishare bus represents the average current of all converters.

Each converter compares its own output current with the average current and adjust its target output voltage accordingly to reduce the error. To prevent oscillation, a dead zone is applied to the current sharing function. When the error current is less than the dead zone, current sharing is inactive. At full load, the IMON voltage is 1.408 V (640 µA x 2.2 kΩ); and at 0 A load, the IMON voltage is 0.352 V (160 µA x 2.2 kΩ).

To smooth the IDAC dithering ripple, it is suggested to put at least 1 nF capacitor between IMON pin and ground. The controller has an internal low pass filter to config the bandwidth for current sharing.

The controller provides both positive and negative clamps to voltage adjustment during active current sharing. This guard bands the output voltage in a safe range. If the output voltage reaches the clamping level and the current error is still larger than the dead zone, the current share fault is reported.

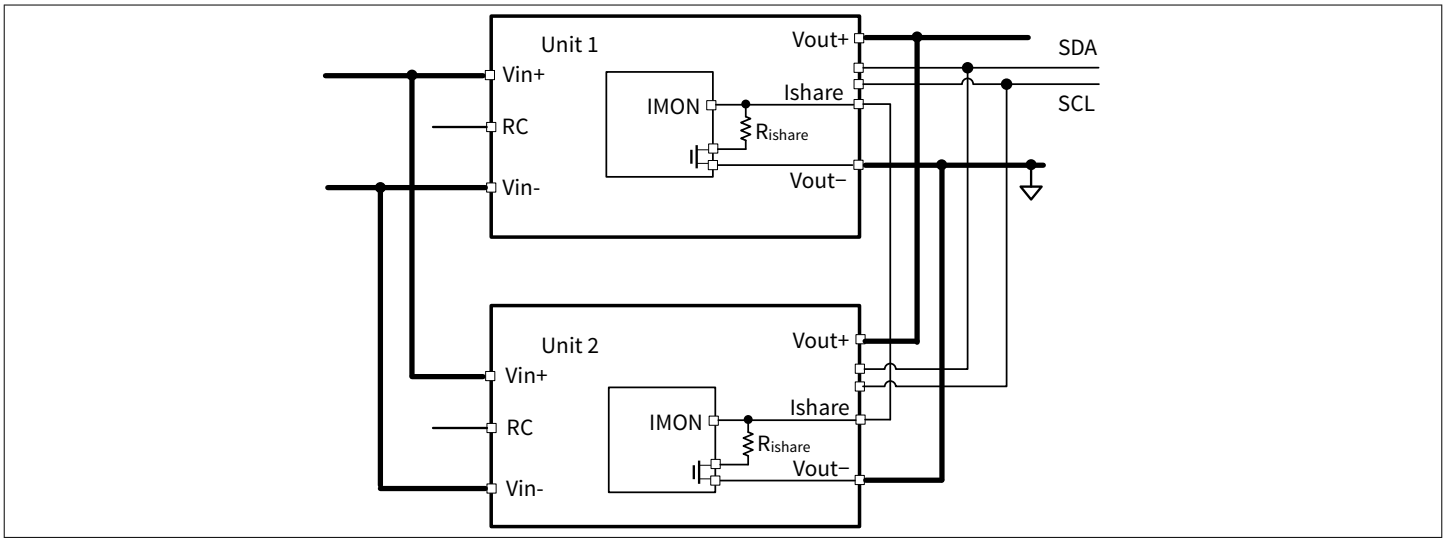



**Figure 11 Parallel module current sharing diagram**

### 4.2.5.2 Temperature sense

The controller supports both external and internal temperature sensing for protection and monitoring. External temperature sensing is achieved with a temperature sensor connected between TSEN and ground. The supported temperature sensor includes diodes, NTC and PTC. When using diodes, it is recommended to use two in series to provide better resolution. The temperature sensor should be placed close to and tightly coupled to the element of interest, for instance, the power stage components or the current sense resistor.

Figure 12 shows the TSEN pin connected to two diodes in series to ground for temperature sense. It can also be configured to use NTC thermistor by replacing the series diodes with a 47 kΩ NTC in parallel with a 12 kΩ resistor. The NTC-based temperature sense is backward compatible with the XDPP1100-Q024 solutions. The temperature is sensed by injecting a 100 µA current and measuring the voltage on TSEN. The temperature is used to effectively compensate for the temperature coefficient of the current sense element and to provide over temperature protection. If the temperature sensor is not required, the TSEN pin must be tied to GND.

When using two-diode voltage drop or $V_{BE}$ for temperature sensing, the offset and gain can be adjusted for the actual diode used. Customized temperature lookup table is also supported if other temperature sense device is preferred, such as PTC thermistor.

A decoupling capacitor is recommended and should be placed between the TSEN pin and GND next to the controller.

The internal temperature sensor is a proportional to absolute temperature (PTAT) voltage generated within the controller die which reflects the junction temperature.

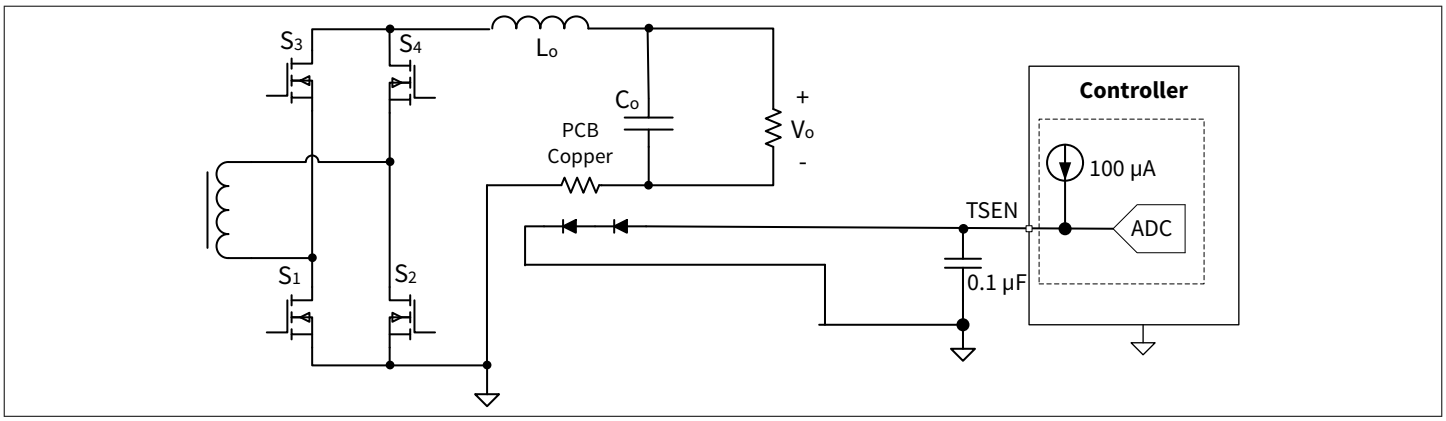



**Figure 12 Example temperature sensing diagram**

### 4.2.5.3 PRISEN

PRISEN can be used to sense primary voltage for input voltage telemetry and feed-forward control. For isolated topologies, the input voltage is sensed at the primary side and fed to the device through an isolated amplifier or auxiliary transformer. The ADC has a sample rate of 0.926 MHz, and is shared with three other inputs (TSEN, IMON, and XADDR1). Compared to using VSEN for input voltage sensing (Chapter 4.2.3), the response of PRISEN is slower. This affects feed-forward and fault detection.

The PRISEN and VSEN voltage sensing can be combined for best system performance. The controller allows to configure the input voltage source for telemetry and feed-forward independently. Using PRISEN for input voltage telemetry allows continuous input voltage monitoring in off-state and pre-startup protections, while using $V_{RECT}$ sensing through VSEN for fast feed-forward response and flux balancing.

## 4.2.6 Fast trigger input

The controller has up to 2 fast trigger inputs (GPI1 and GPI2), which can be used as external fault for shutdown control; or for special timing control such as the SR timing of LLC topologies.

In addition to IMON and SYNC, any PWM pin can be configured as the fast trigger input, as shown in Table 6.

## 4.2.7 Fast fault output

The fast fault output can be assigned to MP_IMON, MP_SMBALERT# or MP_SYNC pin. This is shown as GENERIC_FAULT in Table 6. The output changes polarity when a loop or common fault is triggered. The typical response time from fault triggering to the fault pin reporting is $t_{FSF}$. The list of fault and fault mask bit assignment are described in Chapter 4.4. To enable the fast fault pin responding to a particular fault, set the assigned bit of the **fault_gpio_mask_loop** or the **fault_gpio_mask_com** to 1.

# 4.3 Control loop and subsystems

## 4.3.1 State diagram

The state diagram is shown in Figure 13.

Controller operation is initialized by a power-on UVLO circuit. During controller configuration, the content of the OTP NVM is downloaded onto the control registers. At the same time, the GPIO pins are held in high impedance (Hi-Z) state.

During the Initialization state, the controller measures the internal and external temperatures, input and output voltage, and executes various calibration routines. Prior to completing the initialization state, the controller performs the external resistor (XADDR1) measurements to set the I²C/PMBus® addresses. Once a valid address has been determined, communication with the controller can be established via the I²C bus.

After the Initialization process, the controller enters the inactive state. The controller verifies that the following conditions are satisfied before initiating the system:

1. Valid VDD: The voltage applied to VDD must exceed VDD UVLO rising threshold ($V_{DD\_rising}$) for the internal power valid signal to be asserted. Otherwise, a VDD UVLO fault is issued.
2. No faults are asserted that are defined in the programmed shutdown mask.
3. Enable is asserted if the ON_OFF_CONFIG is set to “respond to EN pin”. It is recommended that EN be asserted only after VDD, $V_{IN}$ and other power supplies for the power stages are ready.
4. TSEN input and the internal temperature are within operation range.

Once the above startup conditions are satisfied, the controller waits for a programmable period of time (PMBus® command TON_DELAY) before attempting soft start and ramping up the output voltage.

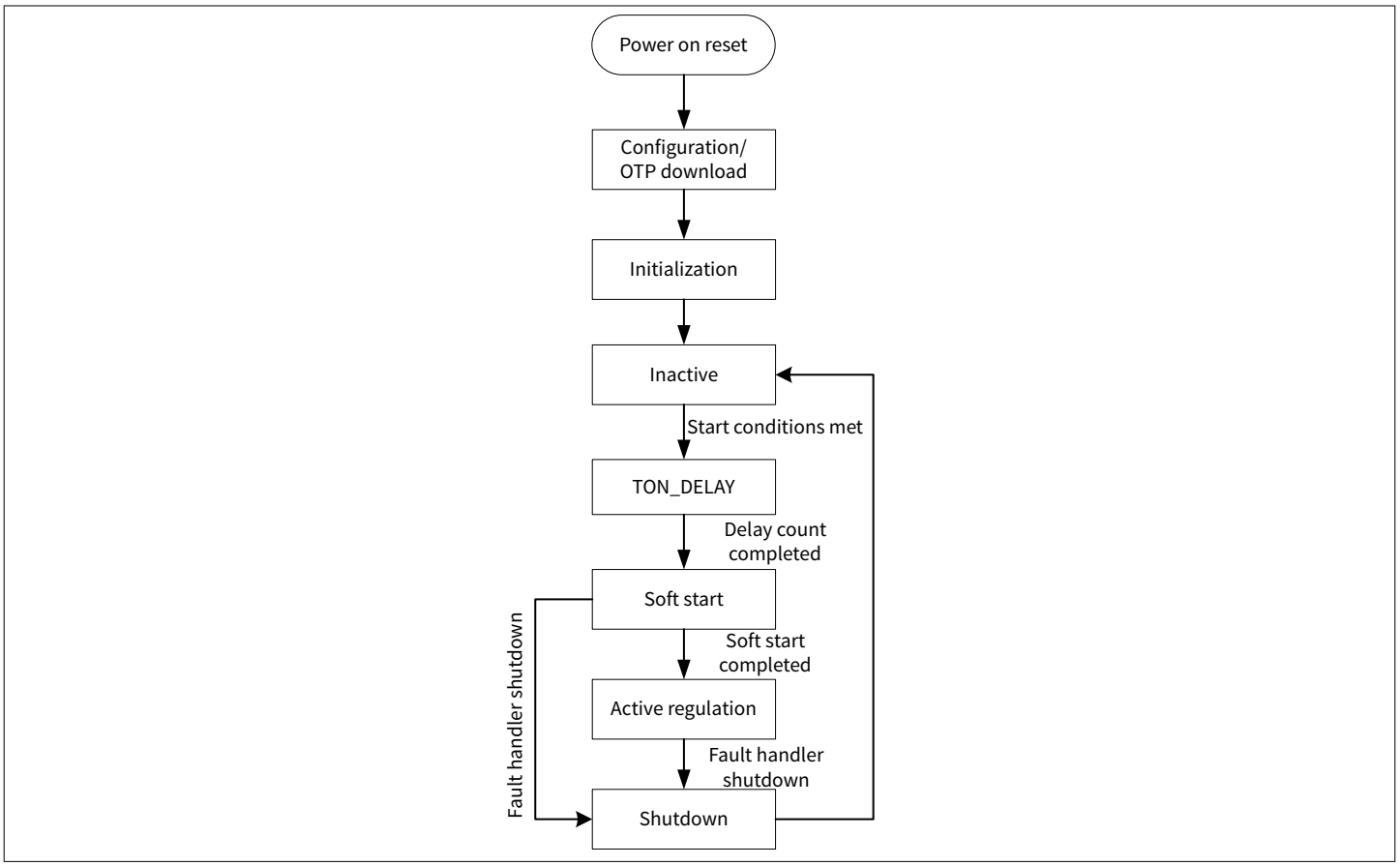



**Figure 13 State diagram**

## 4.3.2 Soft start

### 4.3.2.1 Soft start for non-resonant topologies

For non-resonant topologies, prior to entering the active regulation state, the controller performs a controlled, monotonic soft start ramp of the output voltage. At the beginning of soft start, the controller performs a pre-bias measurement of the output voltage. The controller can disable synchronous rectifier PWM output signals (DE, diode emulation mode) so that the converter does not sink current from the pre-biased output. The diode emulation mode in soft start can be configured using PMBus® command FW_CONFIG_REGULATION.

The soft start is performed by actively regulating the output voltage to an internal reference voltage which is digitally ramped up from the measured pre-biased voltage to the final target value. The target output voltage, ramp rate, turn-on rise time, as well as the number of turn-on trials can be configured during a soft start ramp.

The transition from diode rectification (DE) to synchronous rectification (SR) is seen by the control loop as a load release. To avoid voltage glitch, the control loop can reset the PID accumulated error and use the feed-forward duty cycle when the SR PWMs are enabled.

The controller can also gradually increase the duty cycle of SR PWMs, from a configurable minimum pulse width to the full pulse width. See SR soft turn-on in Chapter 4.3.20.

When the converter completes the initial output voltage ramp to the target output voltage, it enters the active regulation state. The power good signal PWRGD is asserted indicating the output voltage is within the regulation window.

### 4.3.2.2 Soft start for LLC topologies

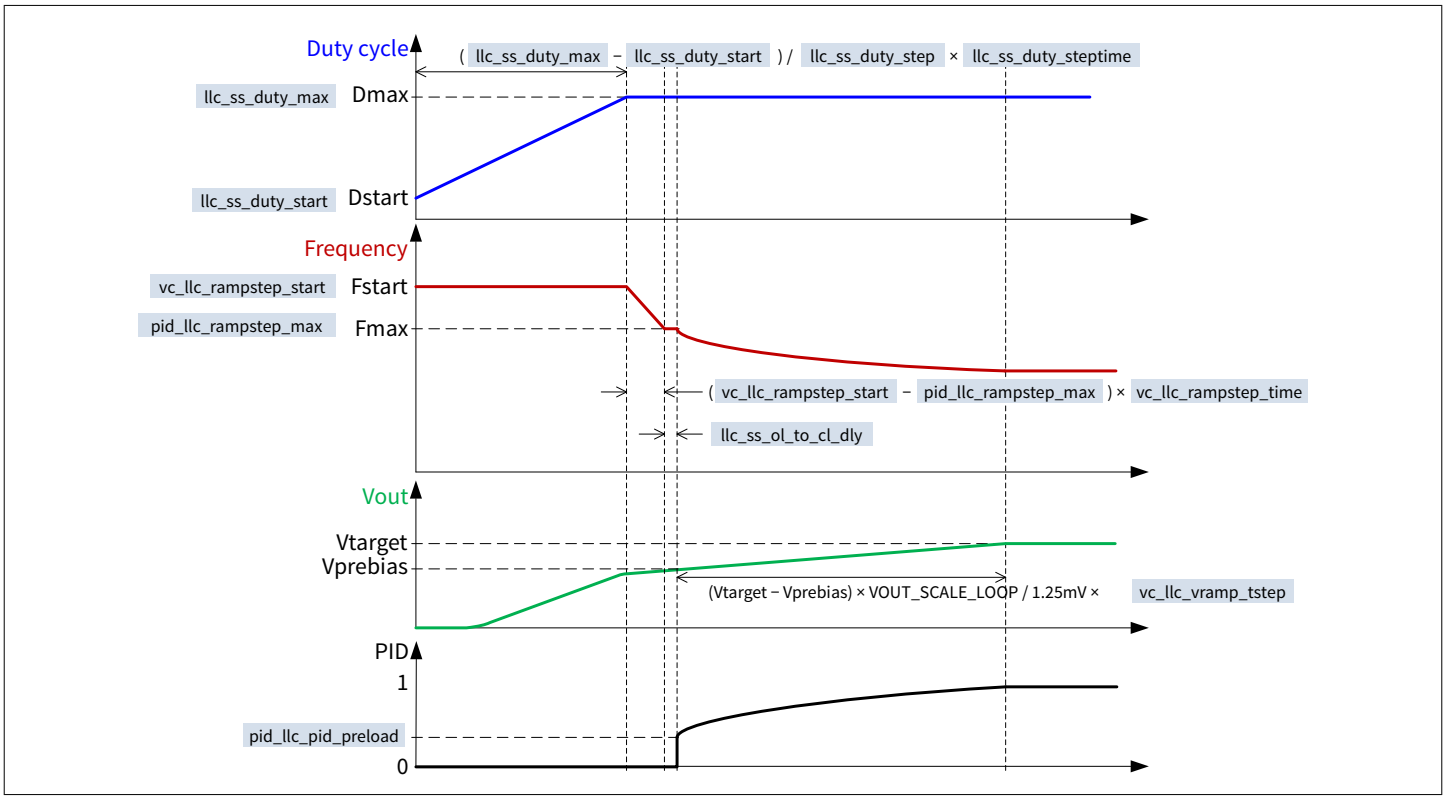



**Figure 14 Typical soft start sequence of LLC topologies**

As illustrated in Figure 14, the soft start of LLC converter includes three stages. During the first stage, duty cycle is ramped up from Dstart to Dmax, while switching at the soft-start initial switching frequency Fstart. The start and end duty cycles, the ramp time, as well as the initial switching frequency are configurable. After the duty cycle reaches maximum, the converter enters the second stage where the duty cycle stays at maximum, and the switching frequency ramps from Fstart to the maximum switching frequency Fmax. The Fmax can be set different from the Fstart. When the Fstart is higher than the Fmax, the frequency ramp time can be configured. If the Fstart is equal or lower than the Fmax, the second stage is skipped. An optional delay is also implemented before the start of the third stage.

In the third stage, the closed-loop voltage regulation starts. The voltage reference of the control loop ramps from the measured pre-bias to the final target voltage at a configurable slew rate, and the switching frequency is modulated automatically by the control loop.

## 4.3.3 Shutdown

The shutdown state can be entered from either soft start or active regulation states through intervention (de-asserting EN) or through a detected fault. Example fault condition includes: over temperature (OT), over current (OC), input under voltage (VIN UV), input over voltage (VIN OV), output over voltage (VOUT OV), and flux balance fault.

The controller supports two selectable shutdown options in response to de-assertion of EN. The first option is a closed-loop shutdown where the controller ramps down the output voltage at a configurable slew rate. The second option is a hot-shutdown (Hi-Z) response, where the output stage power FETs are immediately switched off. If immediate shut-down is required, the PMBus® command TOFF_DELAY should be set to 0 ms. For cases where the shutdown is caused by a fault, the resultant shutdown response is always Hi-Z.

Once shutdown has occurred, firmware handles the subsequent responses, including latched shutdown, a finite or infinite retry mode.

### 4.3.4 Voltage mode control (VMC)

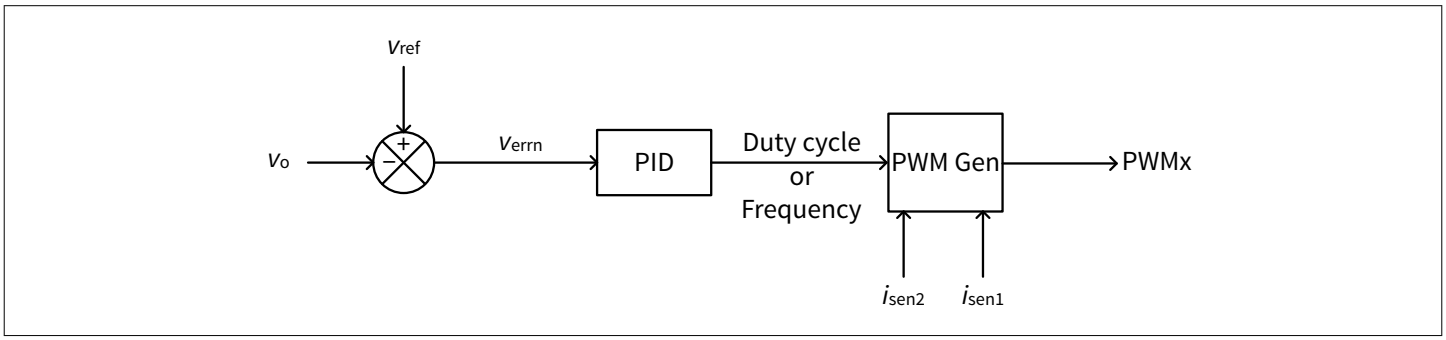



**Figure 15 Voltage mode control loop**

Voltage mode control (VMC) is the most fundamental control mode supported by the controller and is shown in Figure 15. The output voltage is compared to its target voltage ($V_{ref}$) to generate an error voltage that is fed into the PID compensation network. The output of the PID is used by the PWM Gen block to create the required signals for the given topology.

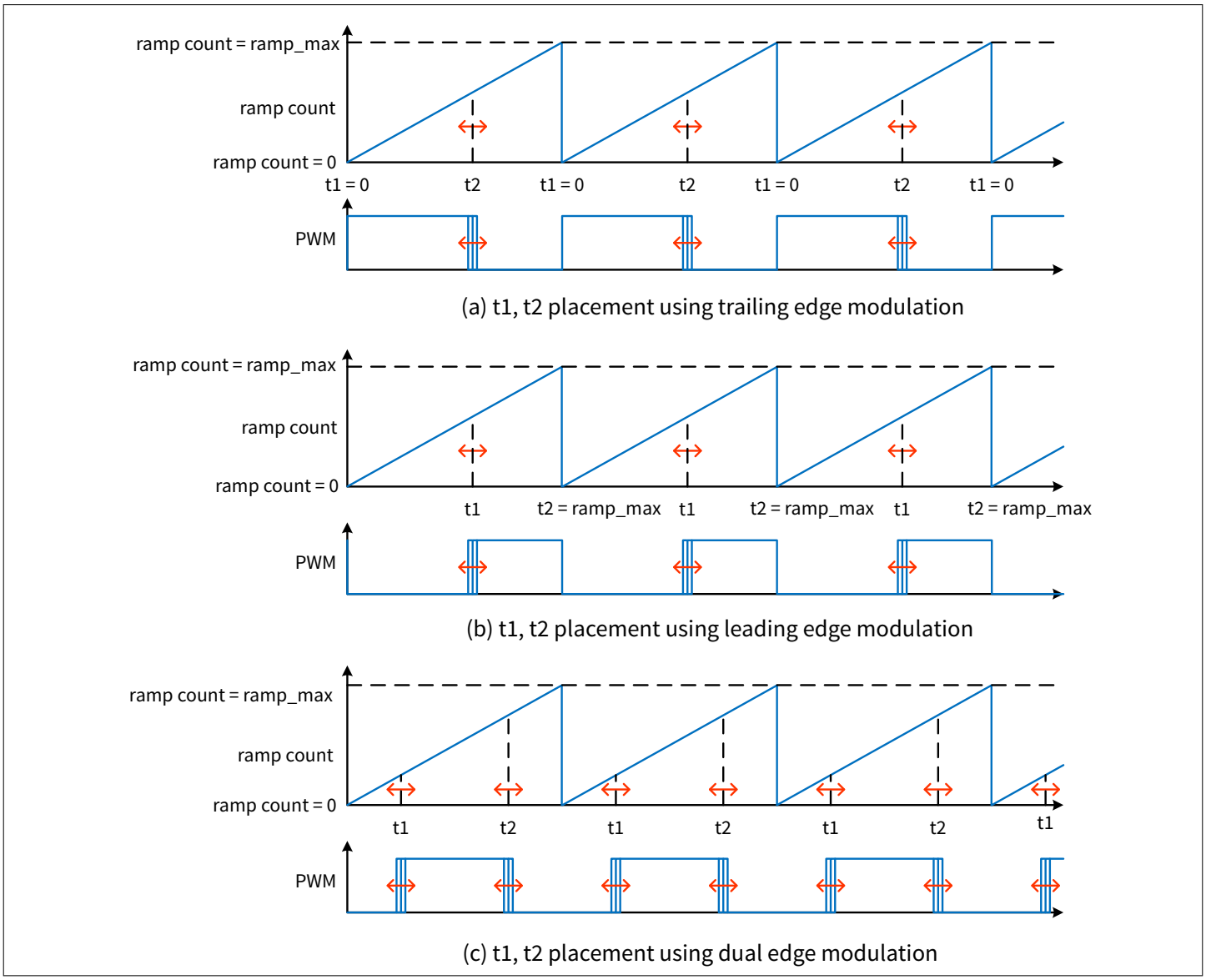



**Figure 16 Modulation schemes and t1 and t2 placement: (a) TE, (b) LE and (c) DE**

VMC supports trailing edge (TE) modulation, leading edge modulation (LE), and dual edge modulation (DE) for non-resonant topologies as shown in Figure 16. It only supports trailing edge modulation for LLC topologies.

TE modulation, shown in Figure 16(a), has a fixed leading edge and a modulated trailing edge. LE modulation, shown in Figure 16(b), has a fixed trailing edge and a modulated leading edge. DE modulation, shown in Figure 16(c), has both leading and trailing edges modulated.

### 4.3.5 Peak current mode control (PCMC) for non-resonant topologies

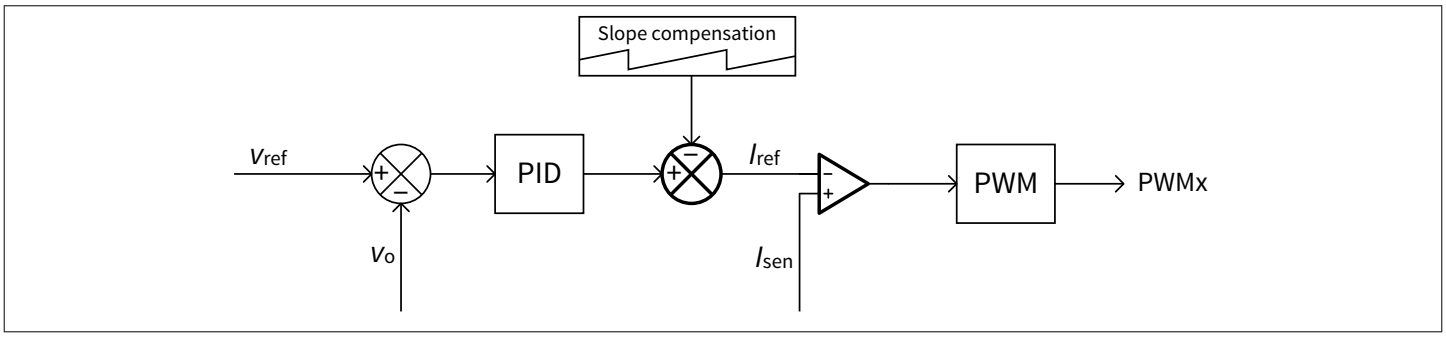



**Figure 17 Peak current mode control loop**

In peak current mode control (PCMC), the current is sensed and compared to a threshold ($I_{ref}$), creating the PWM signal. The compensated error voltage defines $I_{ref}$. The controller supports both primary side and secondary side PCMC. To implement primary side PCMC, the sensed current is the primary device current and is typically fed across the isolation barrier by a current transformer or an isolation amplifier. For secondary side PCMC, the sensed current is the output (inductor) current. Only non-resonant topologies support PCMC.

With PCMC, the derivative portion of the compensator network is not needed, leaving only a PI for the compensation network.

The slope compensation is implemented to avoid subharmonic oscillation when duty cycle is greater than 50%. The slope of the compensation ramp is configurable from $V_O/L$ to $8V_O/L$.

During startup and controlled shutdown when the duty cycle is very low, the primary current signal is very small. It is recommended to set a minimum pulse width instead of skipping the pulse.

PCMC only supports trailing edge modulation.

### 4.3.6 PID and control loop

The control loop implements a fixed frequency, digital PID compensator. The effective transfer function of the PID compensator is given by:

$$H_{PID}(z) = \left[ \left(K_p + K_d\left(1 - z^{-1}\right)\right)\left(\frac{K_{fp2}}{1 - \left(1 - K_{fp2}\right)z^{-1}}\right) + \frac{K_i}{1 - z^{-1}} \right]\left[\frac{K_{fp1}}{1 - \left(1 - K_{fp1}\right)z^{-1}}\right]z^{-1} \quad (1)$$

The locations of the poles and zeroes are determined by the digital loop coefficients Kp, Ki, Kd, and Kfp, which are the PID (proportional, integral, derivative) and low pass filter pole terms, respectively. It creates the equivalent of type III compensation network. In current mode control, phase lead is not required, so the derivative term Kd should be zeroed out by setting the **pid_kd_index_1ph** to 0.

Two extra sets of coefficients of Kp, Ki, Kd can be used to set non-linear loop compensation when the error voltage exceeds customized thresholds in the negative or positive directions.

For non-resonant topologies, the output of the digital PID compensator is converted to a PWM pulse using a digital dual-edge pulse width modulator. The maximum duty cycle limit is programmable up to 99.5%. In addition to using the PID compensator for regulation, the controller has nonlinear control mechanisms such as fast transient response (Chapter 4.3.12, Chapter 4.3.13), and input voltage feed-forward (Chapter 4.3.14), to minimize voltage excursions during transient events. For LLC topologies, the PID output controls the switching frequency. See additional information in Chapter 4.3.7.

### 4.3.7 Frequency modulation (LLC)

Frequency modulation is commonly used for closed-loop LLC topologies. When enabled by register **llc_mode**, the PID output is used to control the rate (step size) of the internal ramp, which in turn determines the switching frequency. As shown in Figure 18, the minimum (Fmin) and maximum (Fmin + Fgain) frequencies are configurable. Optionally, the clamps for max and min frequencies (Fmax and Fmin_clamp) are also configurable.

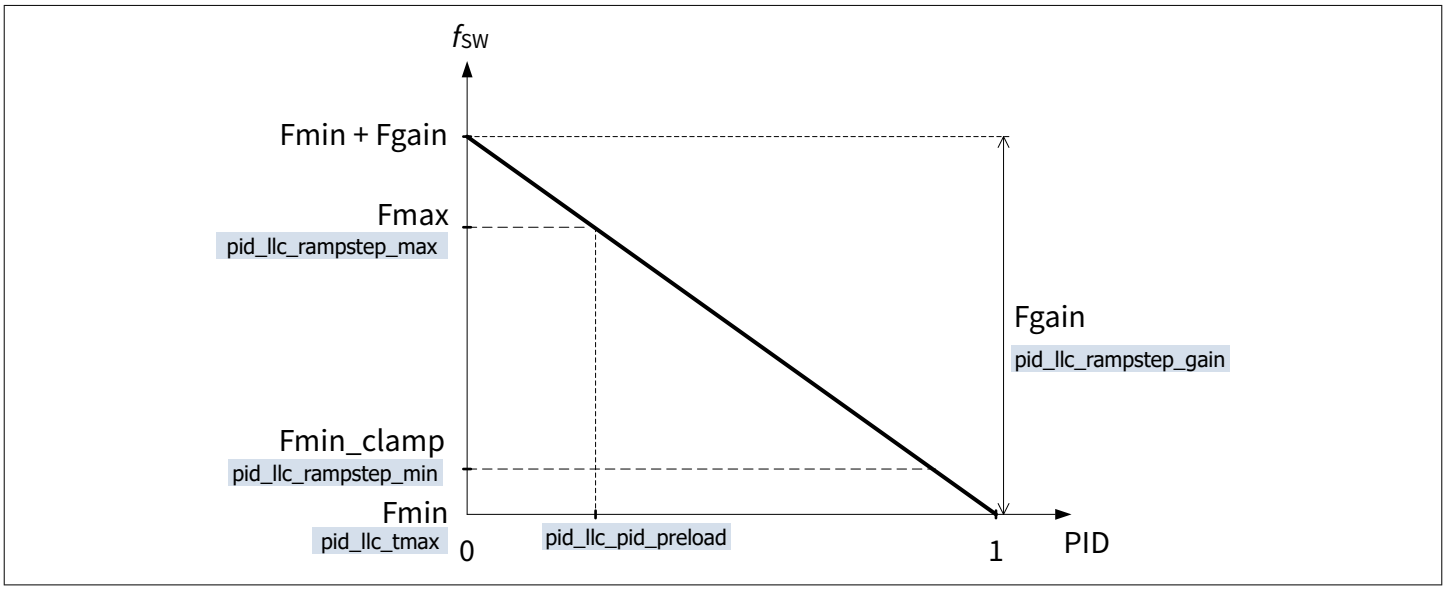



**Figure 18 PID output controls ramp stepsize in frequency modulation**

### 4.3.8 Full-bridge LLC with phase shift

In addition to frequency modulation, phase shift can also be applied in LLC topologies with full-bridge primary. This can be useful to improve the light load performance and/or regulation range. When enabled, after reaching Fmax, PID output controls the duty cycle instead of the frequency, as shown in Figure 19. The reduction of duty cycle is effectively the increase of phase shift, given that the PWMs for primary are assigned according to the phase-shift full-bridge LLC topology, shown in Figure 20.

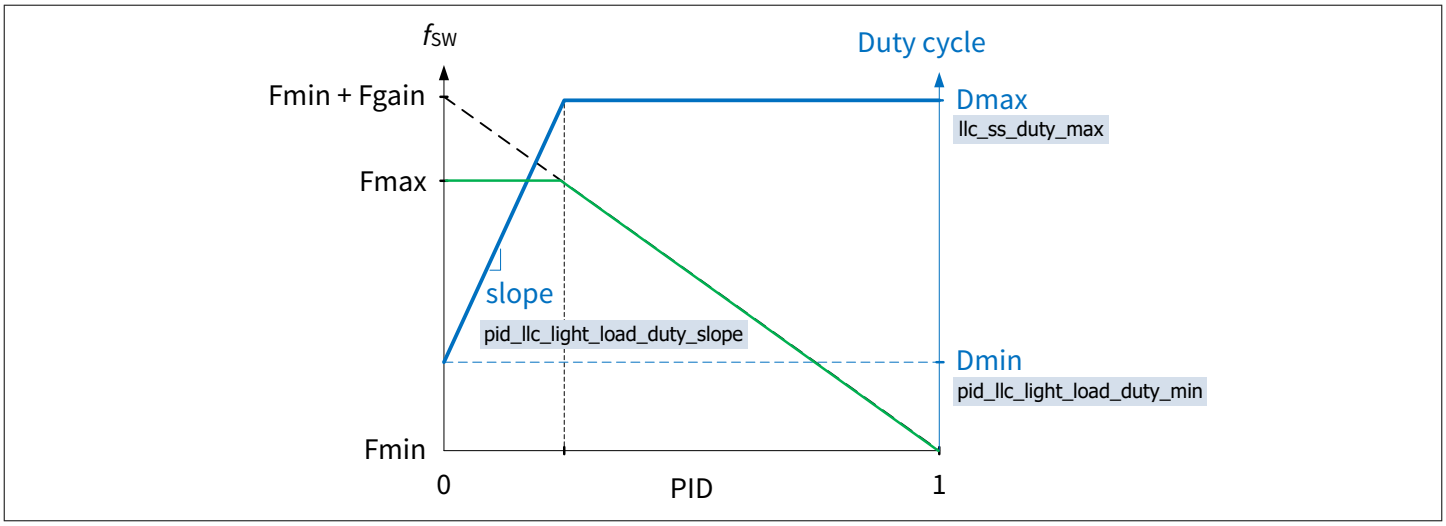



**Figure 19 Phase shift control after reaching maximum frequency**

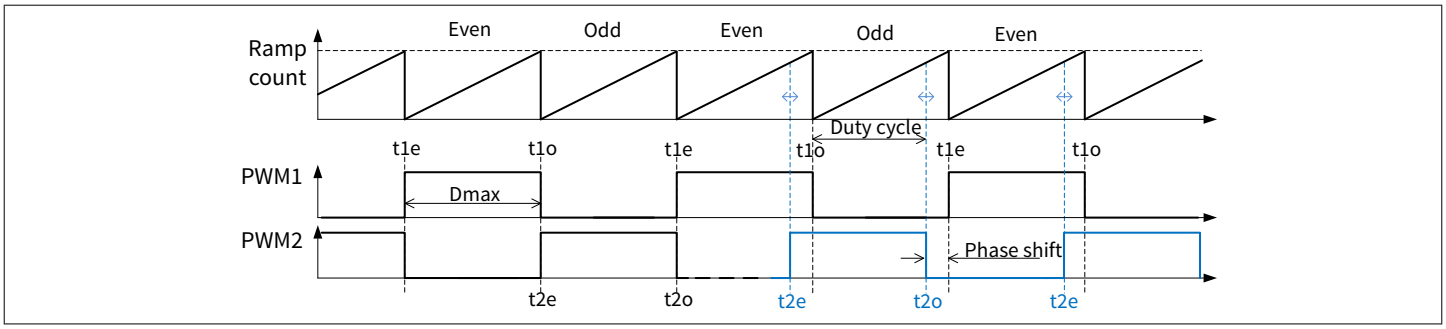



**Figure 20 Phase shift full-bridge LLC primary PWM timing**

## 4.3.9 LLC SR timing control

### 4.3.9.1 Fixed SR maximum on-time

The turn-on of SR PWM is aligned with primary PWM rising edge, with configurable delay using dead time. The turn-off of SR PWM has two scenarios depending on the switching frequency, as shown in Figure 21.

(a) when the switching frequency (fsw) is lower than the resonant frequency (fres), the maximum SR on-time is limited to the half of the resonant period. The exact turn-off time can be adjusted to allow additional diode conduction time or compensate for primary dead time and isolator delay.

(b) when the switching frequency is equal or higher than the resonant frequency, the SR turn-off is aligned with primary PWM falling edge.

The resonant frequency is a parameter that is defined by user based on the system design.

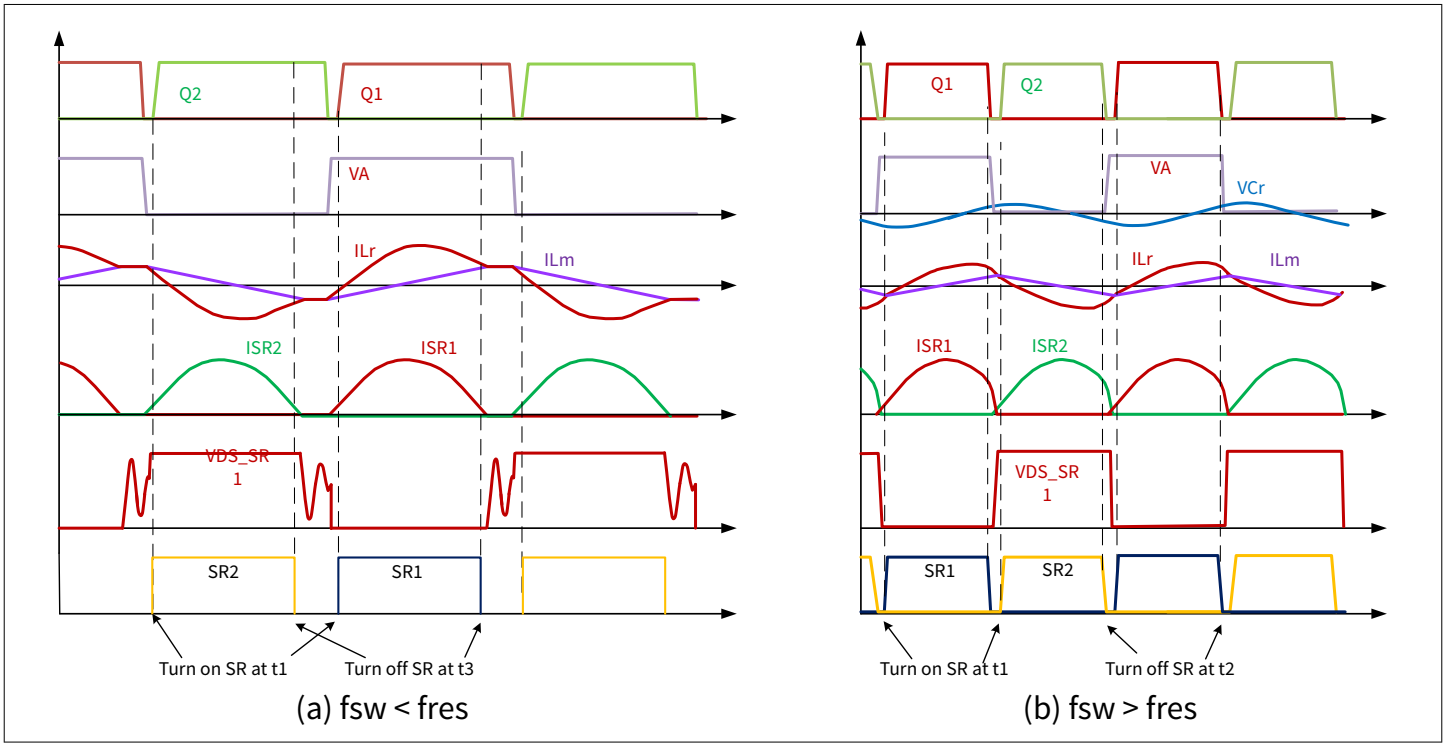



**Figure 21 LLC typical waveforms with SR timing control: (a) below resonance fsw < fres, and (b) above resonance fsw > fres**

### 4.3.9.2 Adaptive SR maximum on-time

When the switching frequency is lower than the resonant frequency, the maximum on-time of SR can be dynamically adjusted. This adaptive SR timing control is achieved by sensing the SR $V_{DS}$ voltage. An example $V_{DS}$ sensing circuit is shown in Figure 22. The $V_{DS}$ voltage is first level-shifted and clamped by a small signal MOSFET (such as BSS123N),

and sent to a comparator with threshold configurable by the resistor divider. The comparator measures the SR body diode conduction time and generates corresponding pulses. As shown in Figure 23, the measured half resonant period (½Tres) corresponds to the duration between the rising edges of the first body diode conduction pulse before the SR PWM turning on, and the falling edge of the second body diode conduction pulse after the SR PWM turning off. This signal is connected to the fast GPI input and is processed by the controller to dynamically adjust the maximum SR on-time.

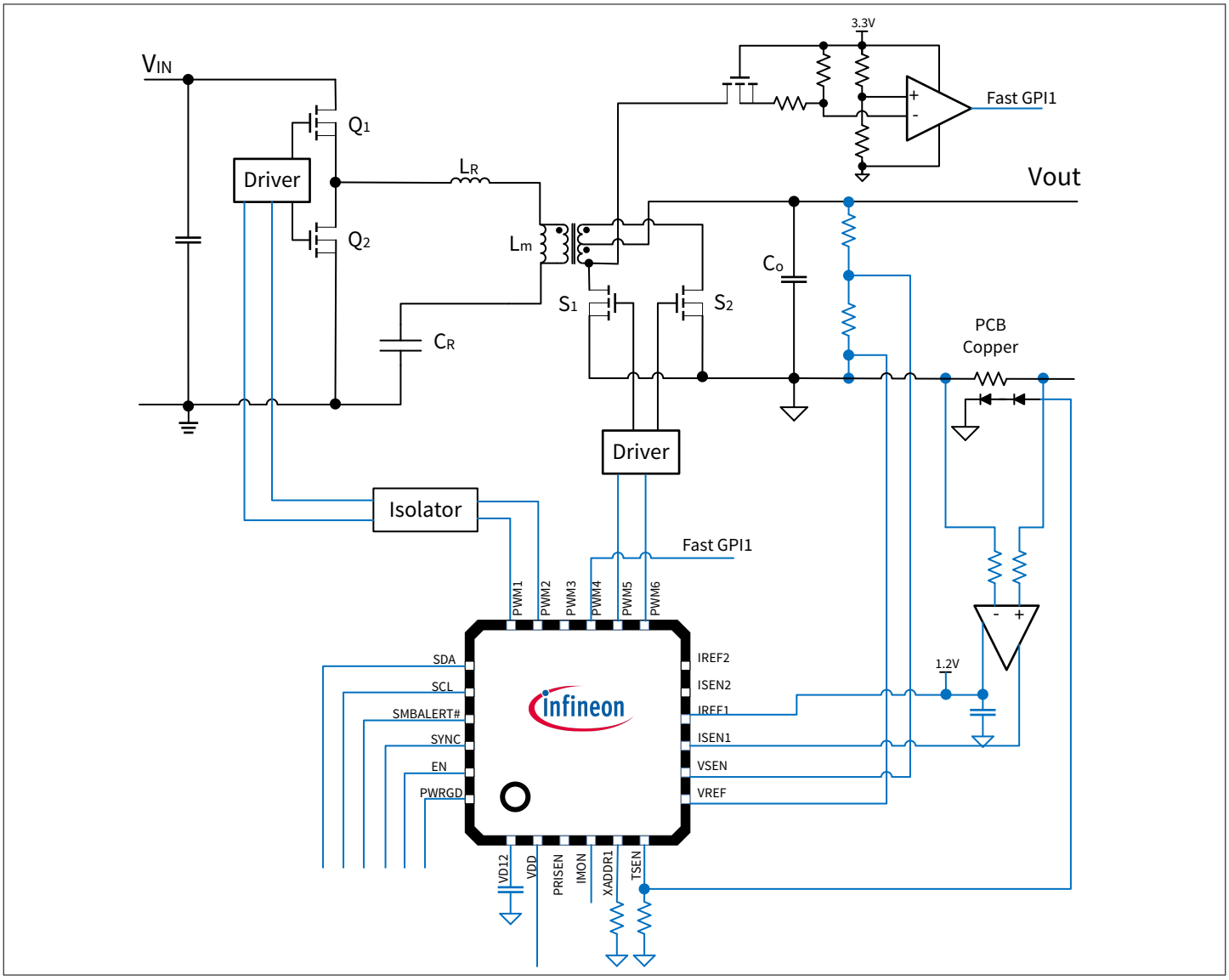



**Figure 22 Example LLC with $V_{DS}$ sensing circuit**

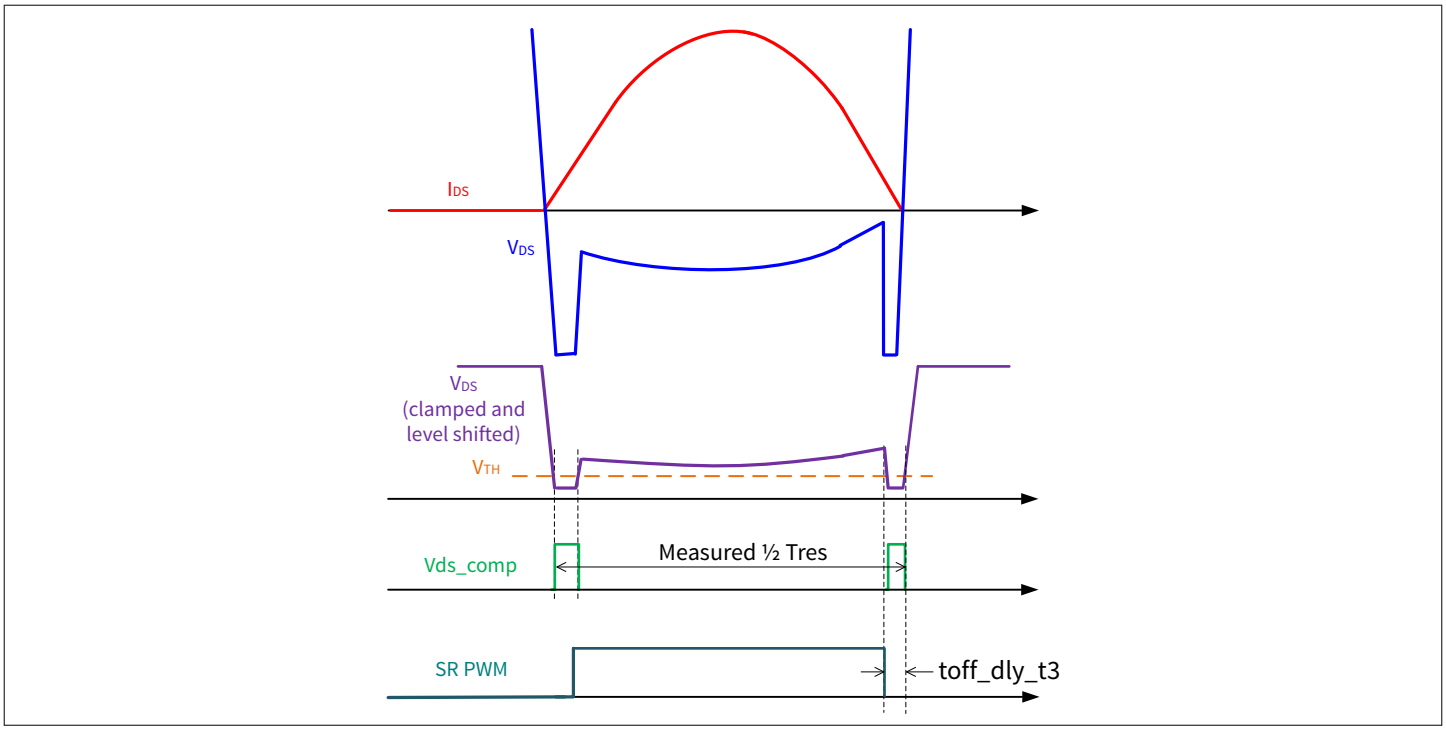



**Figure 23 Typical SR $V_{DS}$ sensing and fast GPI1 waveforms for fsw < fres**

## 4.3.10 Load-line (droop)

The controller supports PMBus® command VOUT_DROOP in LINEAR11 format. The droop is used for current sharing purpose when multiple converters are connected in parallel. The output voltage drop is equal to the product of the output current and the defined droop resistance.

The multi-segment droop can be implemented for emulating constant current and constant power operation. Multi-segment droop is a type of non-linear droop that allows different droop resistance under different load current. If the load-line resistor is set high, output voltage sags quickly when the current exceeds the set threshold, which imitate constant current (CC) or constant power (CP) operation.

Figure 24 illustrates the behavior of multi-segment load-line. The load-line value of $R_{LL,neg}$ is used when the output current $I_o$ is less than zero. This helps current sharing between paralleling modules. $R_{LL,1}$ is the regular droop resistance defined by VOUT_DROOP. From $I_{thr\_seg2}$ to $I_{thr\_seg3}$, $R_{LL,2}$ is used to emulate constant current operation. From $I_{thr\_seg3}$ to the overcurrent shut down threshold $I_{OCFault}$, $R_{LL,3}$ is used for emulate CP operation. $I_{OCFault}$ equals to the IOUT_OC_FAULT_LIMIT.

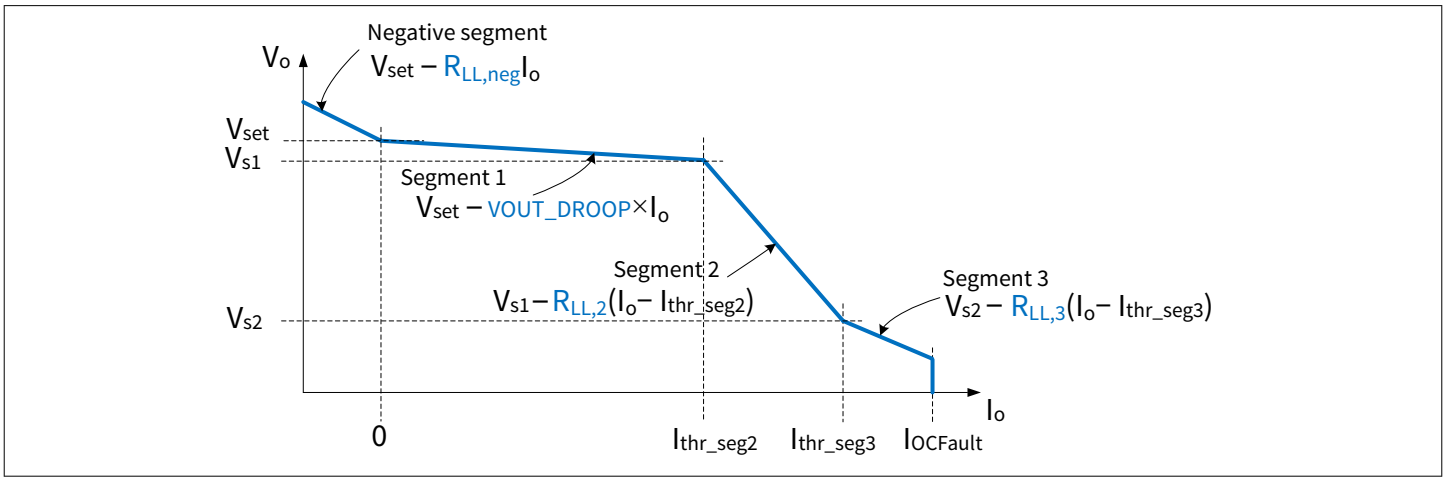



**Figure 24 Load-line implementation example for over-current protection**

### 4.3.11 AC droop

For applications that cannot tolerate the DC voltage drop introduced by the load-line at heavy loads, the controller can still provide some load-line benefits with its AC droop feature. Instead of adding droop to the DC target voltage, the AC droop temporarily adds this load-line offset through a programmable band-pass filter. As a result, the load-line is only applied at mid-band, and is blocked at either low or high load transient frequencies.

### 4.3.12 Fast transient response (FTR) for bridge topologies

The controller supports fast transient response for half-bridge and full-bridge topologies. Upon the detection of a positive load transient, the controller effectively saturates the rectified voltage by changing the switching period from $T_{sw}$ to $2T_{on}$ where $T_{on}$ is the product of the duty cycle and the switching period. As the duty cycle varies with the input voltage, the operating frequency during the transient is also dependent on the input voltage.

Transient detection is achieved by output error voltage $V_{err}$. When the error voltage and its slope are higher than the configured thresholds, the controller enters FTR. The example FTR waveforms for bridge topologies are shown in Figure 25. The output voltage $V_o$ starts to recover after a few FTR cycles when the current in the output inductor is higher than the load current. To avoid overshoot, the controller should ideally exit FTR before $V_o$ returning to the target. The FTR exit condition also consists of voltage threshold and slope. When the error voltage and its slope are lower than the configured thresholds, the controller exits FTR, upon which the controller completes the present FTR cycle and resumes switching period back to $T_{sw}$, and the linear control loop takes over to continue regulation.

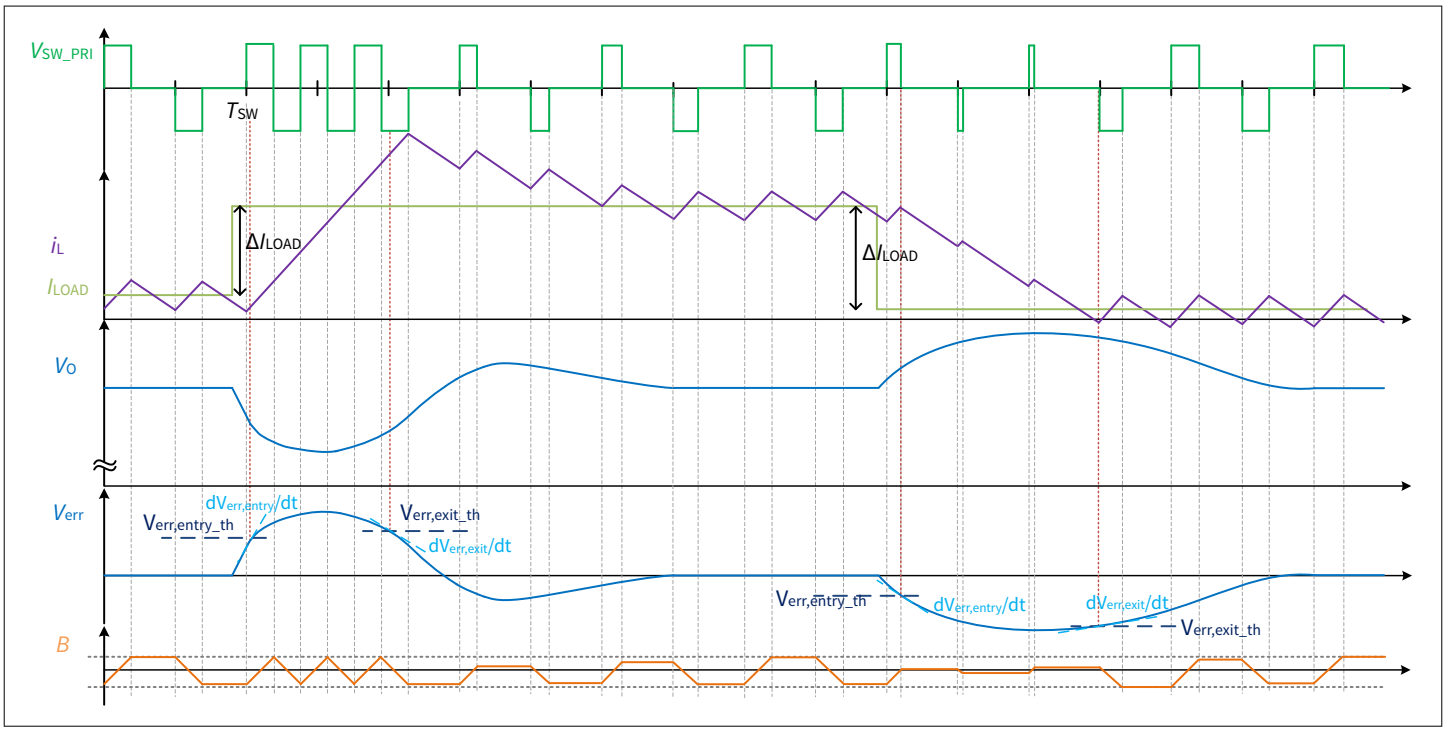



**Figure 25 Fast transient response waveforms of bridge topology**

### 4.3.13 Fast transient response (FTR) for buck topology

The triggering of FTR of a buck topology is the same as the bridge topologies. When enabled, instead of changing the frequency during the FTR, the buck FTR changes the duty cycle/pulse width instead. The magnitude and slope of the error voltage of the output $V_{err}$ is monitored. The FTR function increases the duty cycle during a positive load transient to reduce output undershoot. The duty cycle of FTR is configurable.

The overshoot fast transient response (OVS FTR) function reduces the pulse width during a negative load transient to reduce output overshoot. The PWM pulse width in OVS FTR jumps to the minimum pulse width defined by PMBus® command MFR_MIN_PW.

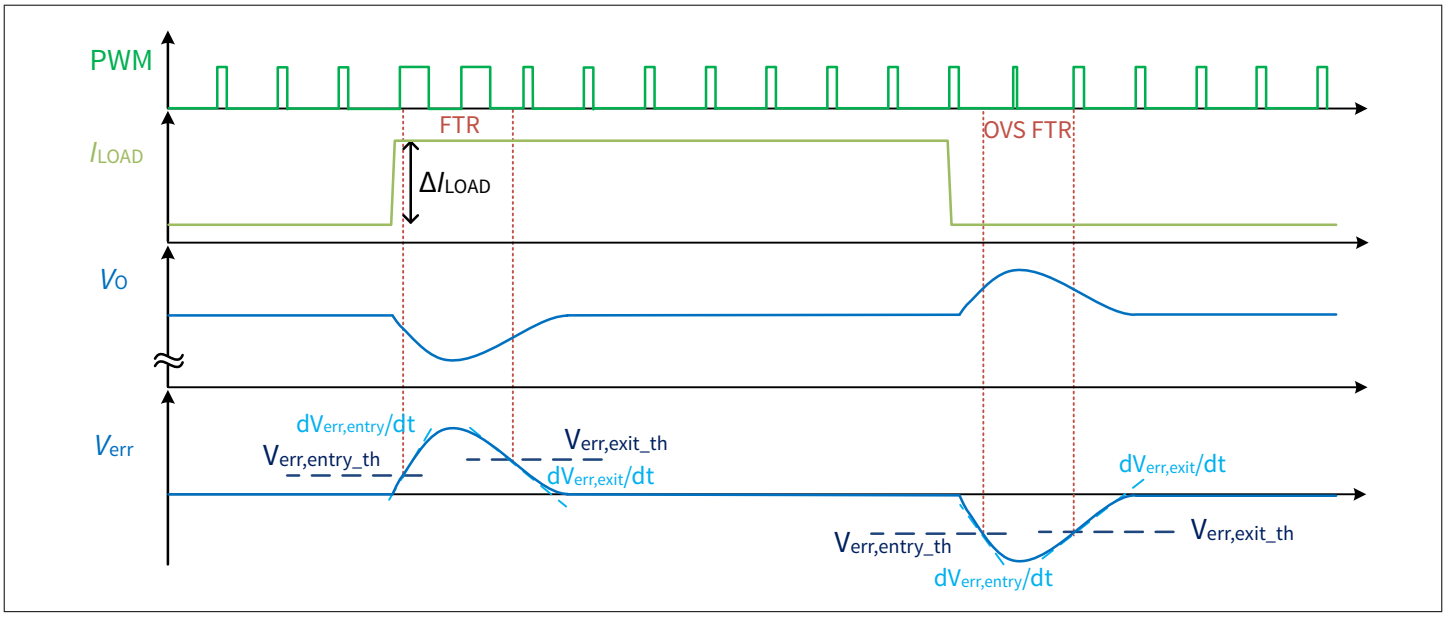



**Figure 26 Fast transient response waveforms of buck topology**

### 4.3.14 Input voltage feed-forward

Input voltage feed-forward involves using input and output voltage measurements to set the nominal duty cycle for the given conditions. Upon sensing a change of the input voltage, the controller quickly compensates the duty cycle. During an input voltage transient, feed-forward response is much faster than output linear control loop. In an isolated converter with controller placed at the secondary side, fast and accurate $V_{RECT}$ sensing is critical to achieve high performance feed-forward.

The following input voltage sensing sources are available to the controller for feed-forward computation:

- Sensed $V_{IN}$ or $V_{RECT}$ on the VSENx input
- Sensed $V_{IN}$ on the PRISEN input (Telemetry sense $V_{IN}$)
- Firmware override

Feed-forward duty cycle calculation varies with topology, as defined in the equations below. The input voltage is measured, while target output voltage ($V_{o,target}$) and turns ratio are controller settings.

$$D_{HB} = \frac{2N \times V_{o,target}}{V_{IN}} \quad (2)$$

$$D_{FB,ACF} = \frac{N \times V_{o,target}}{V_{IN}} \quad (3)$$

$$D_{buck} = \frac{V_{o,target}}{V_{IN}} \quad (4)$$

$$D_{buck\text{-}boost} = \frac{V_{o,target}}{V_{IN} + V_{o,target}} \quad (5)$$

$$D_{\text{boost}} = \frac{V_{\text{o,target}} - V_{\text{IN}}}{V_{\text{o,target}}} \quad (6)$$

HB: half-bridge, FB: full-bridge, ACF: active clamp forward, N: transformer turns ratio $N_p$:$N_s$

### 4.3.15 Current balancing

Current balancing is required for interleaved topologies. The circuit receives the cycle-averaged current from the ISEN1 and ISEN2 inputs. The difference between these current inputs is computed and used as the input to a PI compensator. The compensator output adjusts the duty cycle of the ramp0 PWM, up to ±25%.

An enable threshold is applied to current balancing. Current balancing only activates when the total current is higher than the enable threshold, which has the option of 0 A, 3 A and 5 A.

### 4.3.16 Current sharing

Current sharing refers to balancing the current of individual power supplies that provide a common output voltage. One way to implement current sharing is to use IMON (Chapter 4.2.5.1), shown in Figure 11 where the Ishare pin of each converter are connected together. The IDAC generates a current proportional to the load current of the module. The sum of the currents creates a voltage across the resistor that is measured by the TS ADC and used to identify the error current and make adjustments. Current sharing is a slow loop (for example, 1/10 of voltage loop bandwidth).

The second method of current sharing is passive and uses load-line (Chapter 4.3.10).

### 4.3.17 Flux balancing

In full-bridge (FB) converters, timing mismatch can cause the applied volt-second across the transformer during one half cycle to be greater than that during the other half cycle. This places a DC voltage across the transformer core, leading to saturation, also known as “flux walkaway”.

The controller supports flexible flux balancing methods, including volt-second, voltage only and time only balance. The controller uses the rectified voltage ($V_{RECT}$) for voltage and timing measurement. The high-speed edge comparator has 5 ns resolution for accurate timing measurement. The measured error between each half cycle is fed to a PI compensator for duty cycle adjustment. This adjustment is applied to odd half cycles.

The maximum duty cycle correction is configurable with a resolution of 0.09766%. To avoid adjustment error in DCM operation, or when part of the inductor current becomes negative, the flux balancing can be disabled with a configurable output current threshold. The flux balancing is disabled in burst mode.

Failure to achieve flux balance within a programmable number of cycles generates a fault. More details of flux balancing and flux balance fault protection can be found in the application note.

### 4.3.18 Burst mode

#### 4.3.18.1 Burst mode for non-resonant topologies

To increase light load efficiency, the controller supports burst mode. For non-resonant topologies (except ACF topology), when the load current falls below the burst entry current threshold, the controller enters burst mode operation. All PWMs stop switching when entering burst mode (burst-off interval). Switching is resumed when output voltage drops below an error threshold level (burst-on interval). This error threshold defines the output voltage ripple in burst mode. The PID output is frozen at the value prior to burst mode entry. Thus, during burst-on interval, the controller effectively works in constant on-time mode. All SR PWMs are turned off during burst mode. The frequency of the PWM bursts is the same as the normal switching frequency. The number of burst pulses during burst-on interval is configurable, from one to 16 pulses.

The controller exits burst mode when the burst-off interval is less than half of the switching period. In other words, two burst-on events happen next to each other. If enabled, it can also exits burst mode when the output current exceeds the burst exit threshold. Additionally, a large transient can also trigger burst mode exit if configured.

During burst mode, a different low pass filter is used for output current telemetry, typically configured to a lower band width compared to the normal filter to smooth out the ripple.

Example burst mode waveforms for non-resonant topologies are shown in Figure 27.

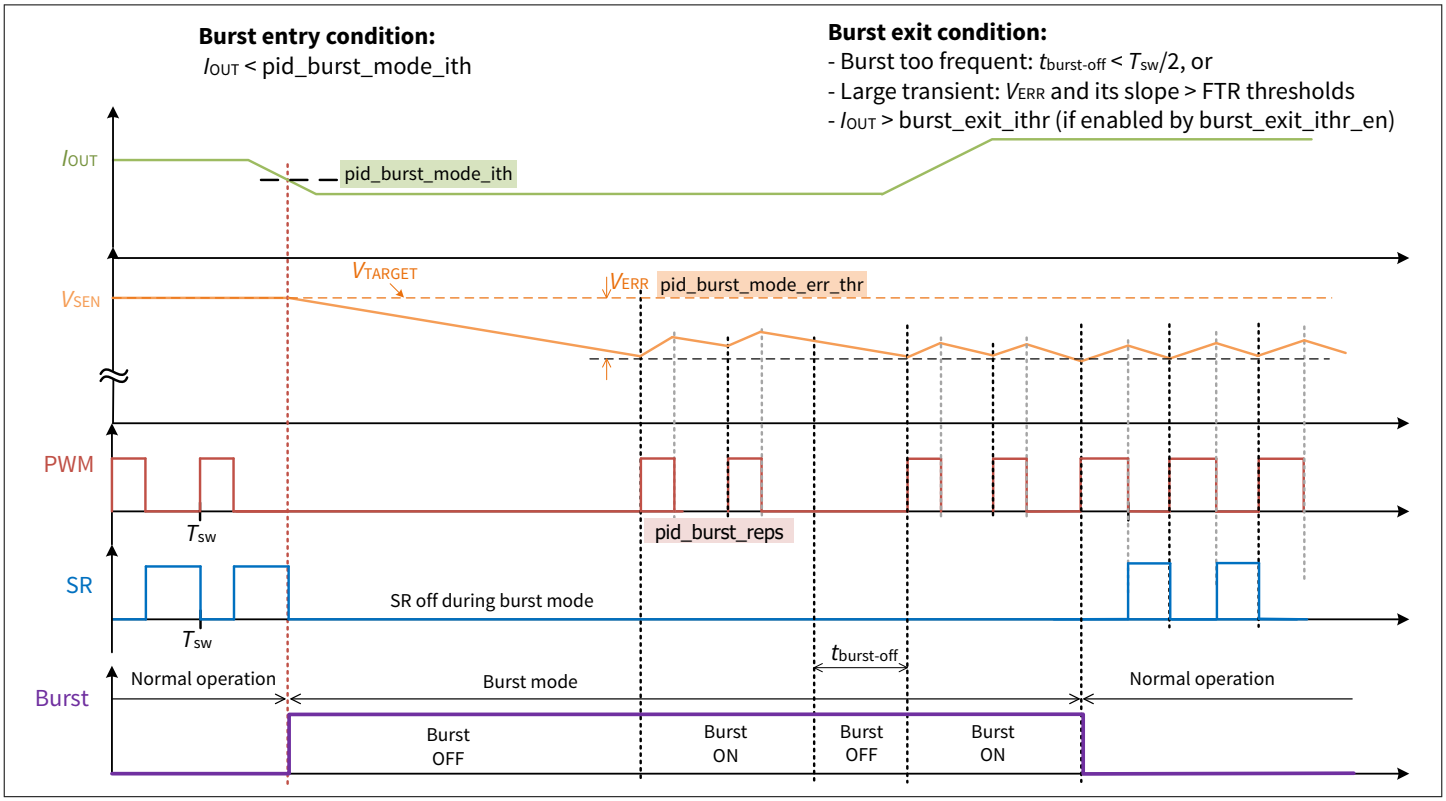



**Figure 27 Example burst mode waveforms for non-resonant topologies**

### 4.3.18.2 Burst mode for LLC topologies

For LLC topologies, at high input voltage and light load, the switching frequency $f_{SW}$ increases towards the maximum frequency Fmax. The converter enters burst mode if the $f_{SW}$ reaches the Fmax and the output voltage error is at maximum allowed threshold. The burst entry condition can also be based on load current (light load) with configurable threshold. In burst mode, SR PWMs can be configured to be on or off. All PWMs stop (burst-off) until the sensed output voltage drops below a threshold, then the PWMs resume (burst-on) for a defined number of switching cycles. After that, all PWMs stop and the burst-off/burst-on cycle repeats.

In burst mode, the switching frequency is frozen at the value right before burst entry, typically Fmax. Before burst mode entry, the last PWM pulse changes to half of the normal pulse width (1/4 $T_{SW}$). This ensures the primary magnetizing current and resonant current are nearly zero during the burst-on to burst-off transition. The first burst-on pulse is also half of the normal pulse width so that the magnetizing current keeps the same slope and direction.

The exit of burst mode occurs when the control loop reduces switching frequency as the load increases, or when a large voltage error is detected due to load transient. Figure 28 illustrates the typical waveforms for LLC burst mode operation.

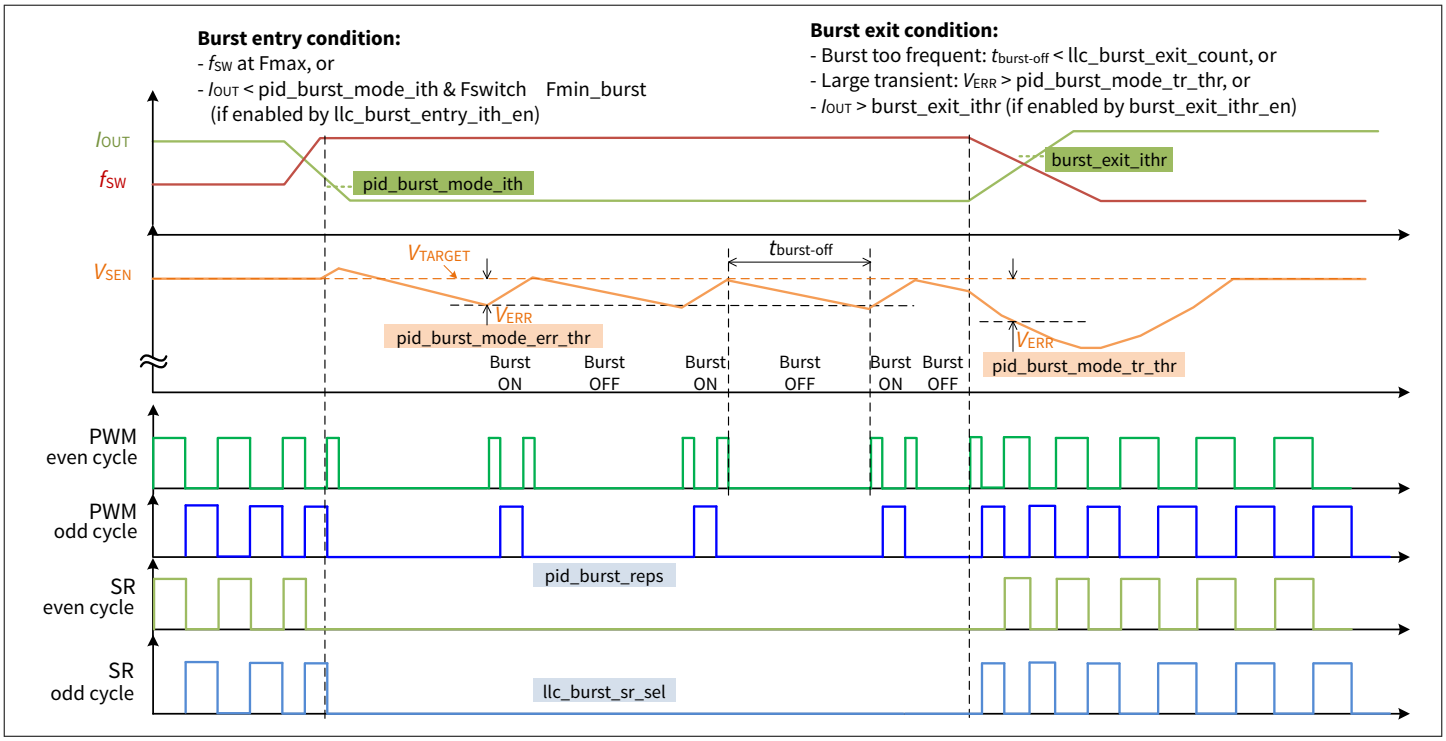



**Figure 28 Example burst mode waveforms for LLC topologies**

## 4.3.19 Phase shedding

For interleaved topologies, the controller supports automatic phase shedding at light load. When the output current falls below the phase dropping threshold, the controller drops one phase. When the output current rises above the phase adding threshold, the controller adds the other phase back.

## 4.3.20 SR soft turn-on

The SR PWMs can be disabled during pre-bias startup or in light load DE mode to avoid negative current in the SR MOSFETs. The SR PWMs are usually enabled at the end of soft-start or DE mode exit. For non-resonant PWM topologies, the controller supports different behaviors for SR turn-on as shown in Figure 29:

- Immediate turn-on. The SR PWM starts normally
- Initially in phase with primary PWM. The SR PWM starts in phase with the corresponding primary PWM for a few switching cycles. Then, the falling edge is extended to the normal SR falling edge while the rising edge still aligned with primary. After a few more switching cycles, the SR PWM switches normally
- Gradually increase duty cycle. The pulse width of the SR PWM increases gradually from the minimum to the full duty cycle in a few steps.

For LLC topologies, only immediate turn-on is supported.

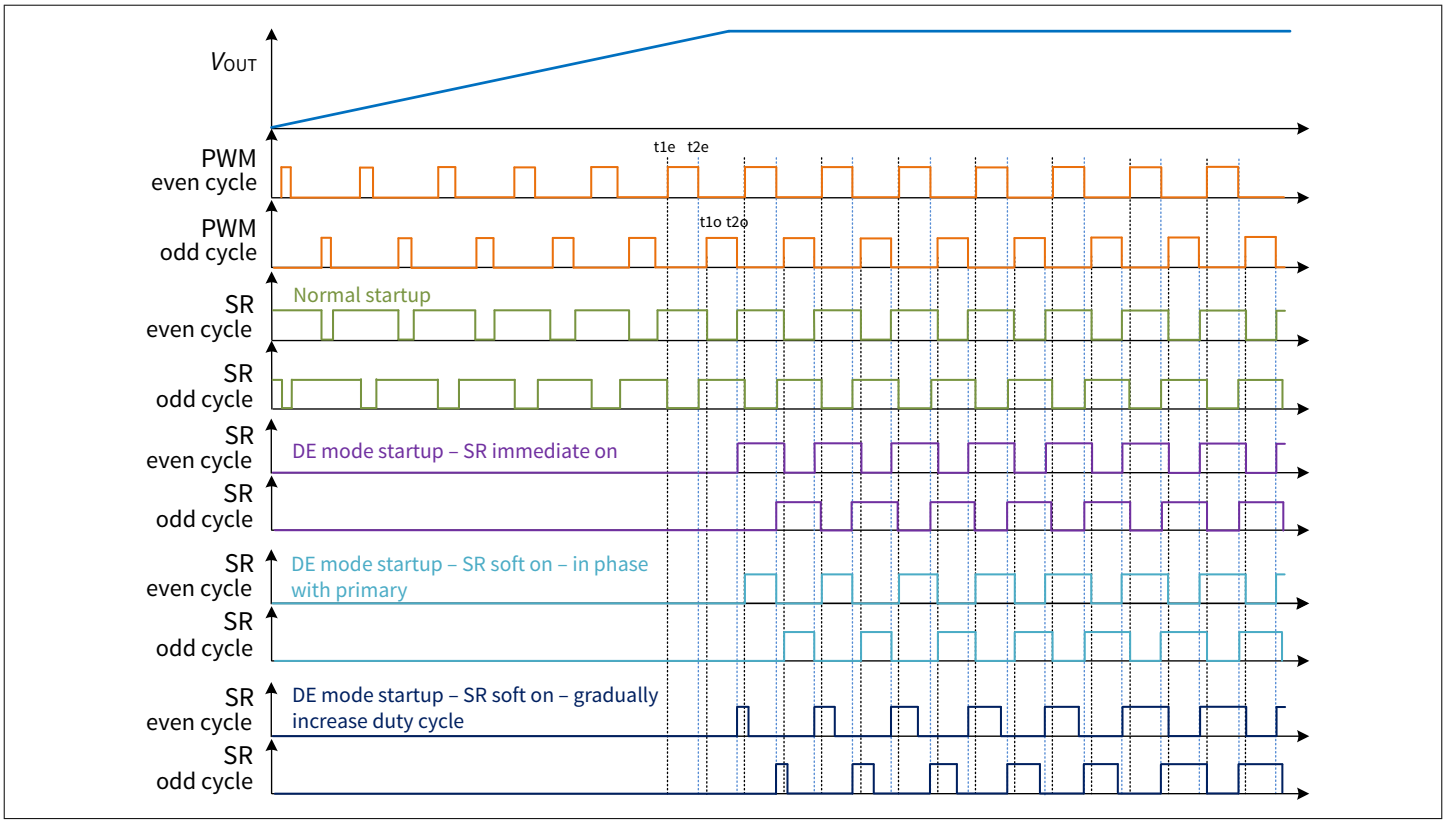



**Figure 29 Example SR turn-on behaviors of PWM bridge topologies in DE startup**

## 4.4 Protection and fault

The fault protection system has the following functions:

- Controller VDD under-voltage lock out (VDD UVLO)
- Input under/over-voltage protection (VIN_UV/VIN_OV)
- Input over current protection (IIN_OC)
- Input over power warning (PIN_OP)
- Output under/over-voltage protection (VOUT_UV/VOUT_OV)
- Output under/over-current protection (IOUT_UC/ IOUT_OC)
- Output over power warning (POUT_OP)
- Pulse-by-pulse peak current limit protection (PCL)
- Short circuit protection (SCP)
- Internal/external temperature protection (OT/ UT)
- Flux balance fault
- Sync fault
- Current sharing fault
- SMBALERT#
- Configuration (CRC) failure
- I2C communication failure

The hardware protection block diagram is shown in Figure 30. The controller implements all the fault protections without the need of external comparators.

The list of hardware fault, FW fault and common fault are shown in Table 7, Table 8, and Table 9. Setting the bit to 1 disables the corresponding fault.

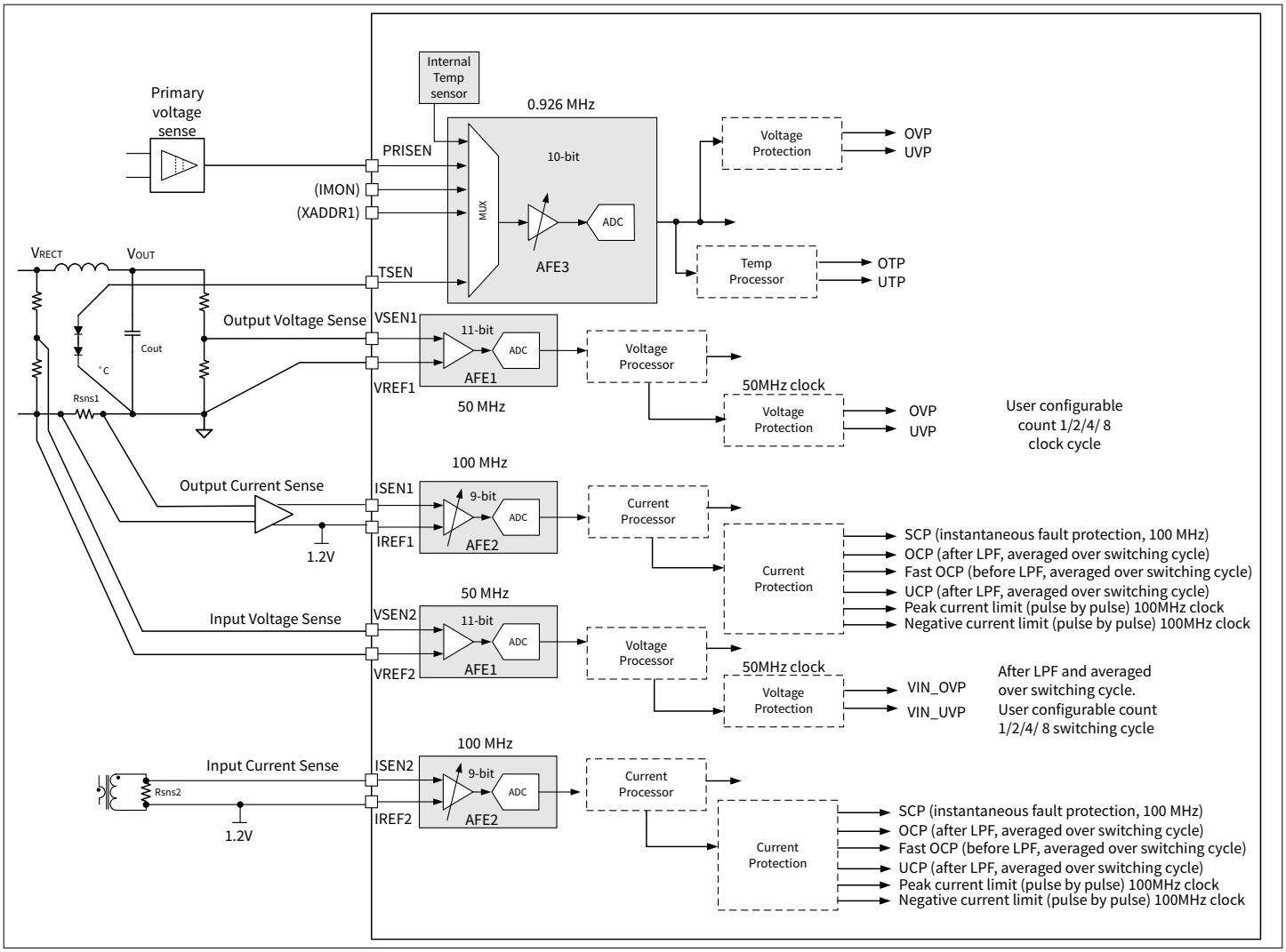



**Figure 30 Protection block diagram**

**Table 7 Hardware fault mask bit assignment by fault_enable_mask_loop_hw_loop0**

| Bit | Fault | Bit | Fault |
|---|---|---|---|
| 0 | Reserved | 1 | VOUT_OV_FAULT |
| 2 | VOUT_OV_WARN | 3 | VOUT_UV_FAULT |
| 4 | VOUT_UV_WARN | 5 | IOUT_OC_LV_FAULT |
| 6 | VIN_OV_FAULT | 7 | VIN_OV_WARN |
| 8 | VIN_UV_FAULT | 9 | VIN_UV_WARN |
| 10 | MFR_IOUT_OC_FAST | 11 | IOUT_OC_FAULT |
| 12 | IOUT_CONSTANT_CURRENT | 13 | IOUT_OC_WARN |
| 14 | IOUT_UC_FAULT | 15 | IIN_OC_FAULT |
| 16 | IIN_OC_WARN | 17 | OT_FAULT |
| 18 | OT_WARN | 19 | UT_FAULT |
| 20 | UT_WARN | 21 | Reserved |

**(table continues...)**

**Table 7 (continued) Hardware fault mask bit assignment by fault_enable_mask_loop_hw_loop0**

| Bit | Fault | Bit | Fault |
|---|---|---|---|
| 22 | VDD_UVLO_FAULT | 23 | SYSTEM_RESET_EVENT |
| 24 | EXTERNAL_FAULT | 25 | ISP0_SCP_FAULT |
| 26 | ISP1_SCP_FAULT | 27 | CURRENT_SHARE_FAULT |
| 28 | SYNC_FAULT | 29 | ANALOG_OVP |
| 30 | VOUT_MAX_MIN_WARN | 31 | FW_FAULT_PIN_SET |

**Table 8 Firmware fault mask bit assignment by fault_enable_mask_loop_fw_loop0**

| Bit | Fault | Bit | Fault |
|---|---|---|---|
| 0 | Reserved | 1 | COMMON_FAULT |
| 2 | TON_MAX_FAULT | 3 | TOFF_MAX_WARN |
| 4 | VIN_INSUFFICIENT | 5 | PIN_OP_WARN |
| 6 | POUT_OP_WARN | 7 | ESTIMATED_IIN_OC_FAULT |
| 8 | ESTIMATED_IIN_OC_WARN | 9 | INVALIDATED_CORRUPTED_SNAPSHOT |
| 10-31 | Unused | | |

**Table 9 Common fault mask bit assignment by fault_enable_mask_loop_common**

| Bit | Fault | Bit | Fault |
|---|---|---|---|
| 0 | Reserved | 1 | ISEN1 tracking fault |
| 2 | ISEN2 tracking fault | 3 | Flux balance fault |
| 4 | ISEN1 PCL fault | 5 | ISEN2 PCL fault |
| 6 | VSEN open fault | 7 | LLC burst mode warning |
| 8 | LLC open loop warning | 9 | Reserved |
| 10 | POR VDDA fault | 11-31 | Unused |

# 5 Electrical characteristics

## 5.1 Absolute maximum ratings

Subjecting the controller to stresses above those listed in absolute maximum rating (Table 10) may cause permanent damage. These are absolute stress ratings only and functional operation is not implied or recommended at these or any other conditions in excess of those given in the recommended operating conditions sections of this specification. Exposure to absolute maximum ratings for extended periods may adversely affect the operation and reliability.

**Table 10 Absolute maximum ratings**

| Parameter | Symbol | Values | | | Unit | Note or condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| VDD supply voltage | $V_{DD}$ | -0.3 | – | 4.0 | V | Instantaneous voltage. See Note [1)] below |
| VDD supply voltage | $V_{DD}$ | -0.3 | – | 3.7 | V | Continuous voltage |
| VSEN1, VSEN2 input voltage | $V_{VSENx}$ | -0.3 | – | 3.7* | V | *The lesser of 3.7 V or $V_{DD}$ + 0.2 V |
| VREF1, VREF2 input voltage | $V_{VREFx}$ | -0.3 | – | 0.5 | V | – |
| ISEN1, ISEN2, IREF1, IREF2 input voltage | $V_{ISENx}$, $V_{IREFx}$ | -0.3 | – | 3.7* | V | *The lesser of 3.7 V or $V_{DD}$ + 0.2 V |
| VD12 current | $I_{VD12}$ | -1 | – | 1 | mA | Do not drive VD12 pin |
| All other pins input voltage | $V_{PIN}$ | -0.3 | – | 3.7* | V | *The lesser of 3.7 V or $V_{DD}$ + 0.2 V |
| Operating junction temperature | $T_J$ | -40 | – | 150 | °C | – |
| Storage temperature | $T_{STG}$ | -65 | – | 150 | °C | – |

1) The absolute maximum $V_{DD}$ supply voltage is 4.0 V with the conditions that the junction temperature range is maintained between -40°C ≤ $T_J$ ≤ +125°C and the product is not operated at the absolute maximum $V_{DD}$ supply voltage for more than 24 hours cumulatively over the lifetime of the product.

## 5.2 ESD and MSL rating

**Table 11 ESD and MSL ratings**

| Symbol | Descripion | Value | Unit |
|---|---|---|---|
| $ESD_{HBM}$ | Human Body Model sensitivity as per EIA/JEDEC standard EIA/JS-001 | 2000 | V |
| $ESD_{CDM}$ | Charged Device Model sensitivity as per JEDEC standard JS-002 | 1000 | V |
| *MSL* | Moisture Sensitivity Level as per IPC/JEDEC J-STD-020E | MSL2 | – |

## 5.3 Thermal characteristics

**Table 12 Thermal characteristics**

| Parameter | Symbol | Values | | | Unit | Note or condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction to ambient | $R_{thJA\_0}$ | – | 53.5 | – | K/W | JEDEC 2s2p, no airflow. Note 1) |
| Thermal resistance, junction to ambient | $R_{thJA\_200}$ | – | 36.9 | – | K/W | JEDEC 2s2p, 200 lfm airflow. Note 1) |
| Thermal resistance, junction to ambient | $R_{thJA\_500}$ | – | 30.3 | – | K/W | JEDEC 2s2p, 500 lfm airflow. Note 1) |
| Thermal resistance, junction to case (bottom) | $R_{thJC\_B}$ | – | 3.6 | – | K/W | Note 1) |
| Thermal resistance, junction to case (top) | $R_{thJC\_T}$ | – | 33.1 | – | K/W | Note 1) |

1) Not subject to production test - specified by design

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org

## 5.4 Recommended operating conditions

**Table 13 Recommended operating conditions**

The recommended operating conditions are shown for which the DC electrical characteristics are valid.

| Parameter | Symbol | Values | | | Unit | Note or condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply voltage | $V_{DD}$ | 2.97 | 3.3 | 3.63 | V | – |
| Junction temperature | $T_J$ | -40 | 25 | 125 | °C | – |

## 5.5 Electrical characteristics

**Table 14 Electrical characteristics**

$V_{DD}$ = 2.97 V to 3.63 V, 1 µF capacitor from VDD pin to GND, 1 µF capacitor from VD12 pin to GND, $T_J$ = -40°C to 125°C unless otherwise specified. Positive current flows into the pin.

| Parameter | Symbol | Values | | | Unit | Note or condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **Power supply** | | | | | | |
| Supply current | $I_{DD0}$ | – | 8 | – | mA | In off mode, telemetry disabled |
| Supply current | $I_{DD1}$ | – | 21 | – | mA | 4 PWMs switching at 250 kHz |
| Supply voltage UVLO rising threshold | $V_{DD\_rising}$ | – | 2.78 | 2.95 | V | – |
| Supply voltage UVLO falling threshold | $V_{DD\_falling}$ | 2.5 | 2.7 | – | V | – |
| Supply voltage UVLO hysteresis | $V_{DD\_hyst}$ | – | 80 | – | mV | – |
| Supply current, sleep mode | $I_{DD\_sleep}$ | – | 1 | – | mA | Not regulating, clocks stopped, peripherals disabled, responsive to sleep pin. Note [1)] |
| Wakeup time from sleep mode | $t_{wake}$ | – | 150 | – | µs | Toggling of sleep pin as wakeup event. Measured from the wakeup event to the first instruction executed by the CPU. Note [1)] |
| **Voltage ADC AFE1** | | | | | | |
| Input differential voltage range | $V_{VSENx\text{-}VREFx}$ | 0.25 | – | 2.1 | V | Note [1)] |
| Error voltage digital resolution | $V_{RES1}$ | – | 1.25 | – | mV | Note [1)] |
| Input impedance | $R_{EA1}$ | – | > 1 | – | MΩ | Note [1)] |
| Sample rate | $f_{ADC1}$ | – | 100 | – | MHz | – |
| VS ADC accuracy | $A_{AD1\_1}$ | -1 | – | 1 | % | Setpoint 1.6 V to 2.1 V. Note [2)] |
| VS ADC accuracy | $A_{AD1\_2}$ | -1 | – | 1 | % | Setpoint 1.2 V, Note [2)] |
| VS ADC accuracy | $A_{AD1\_3}$ | -1.5 | – | 1.5 | % | Setpoint 0.8 V, Note [2)] |
| VS ADC accuracy | $A_{AD1\_3}$ | -2.3 | – | 2.3 | % | Setpoint 0.5 V, Note [2)] |

**(table continues...)**

**Table 14 (continued) Electrical characteristics**

$V_{DD}$ = 2.97 V to 3.63 V, 1 µF capacitor from VDD pin to GND, 1 µF capacitor from VD12 pin to GND, $T_J$ = -40°C to 125°C unless otherwise specified. Positive current flows into the pin.

| Parameter | Symbol | Values | | | Unit | Note or condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| VS ADC accuracy | $A_{AD1\_5}$ | – | ±0.45 | – | % | Setpoint 1.6 V to 2.1 V, $T_J$ = 25°C, $V_{DD}$ = 3.3 V, Typ. = 3σ, Note 2) |
| VS ADC accuracy | $A_{AD1\_6}$ | – | ±0.45 | – | % | Setpoint 1.2 V, $T_J$ = 25°C, $V_{DD}$ = 3.3 V, Typ. = 3σ, Note 2) |
| VS ADC accuracy | $A_{AD1\_7}$ | – | ±0.8 | – | % | Setpoint 0.8 V, $T_J$ = 25°C, $V_{DD}$ = 3.3 V, Typ. = 3σ, Note 2) |
| VS ADC accuracy | $A_{AD1\_8}$ | – | ±1.15 | – | mV | Setpoint 0.5 V, $T_J$ = 25°C, $V_{DD}$ = 3.3 V, Typ. = 3σ, Note 2) |
| **Current ADC AFE2** | | | | | | |
| Input differential voltage range | $V_{ISENx\text{-}IREFx}$ | -256 | – | 256 | mV | – |
| IREF pin voltage range | $V_{IREFx}$ | 1.0 | 1.2 | 1.32 | V | Note 1) |
| Error voltage digital resolution | $V_{RES2}$ | – | 1 | – | mV | Note 1) |
| Input impedance | $R_{EA2}$ | – | > 1 | – | MΩ | Note 1) |
| IS ADC offset | $V_{OFFSET2}$ | -2.5 | – | 2.5 | LSB | – |
| Sample rate | $f_{ADC2}$ | – | 100 | – | MHz | – |
| Tracking slew rate | $dV_{ISEN}/dt$ | – | – | 1.6 | mV/ns | Note 1) |
| IS ADC accuracy | $A_{AD2\_1}$ | – | ±4 | – | % | ±100 mV differential input, Typ. = 3σ |
| IS ADC accuracy | $A_{AD2\_2}$ | – | ±2.2 | – | % | ±256 mV differential input, Typ. = 3σ |
| **General-purpose ADC AFE3** | | | | | | |
| Input voltage range | $V_{ADC3\_IN}$ | 0 | – | 2.4 | V | Note 1) |
| Error voltage digital resolution | $V_{RES3}$ | – | 2.344 | – | mV | Note 1) |
| Input impedance | $R_{EA3}$ | – | > 1 | – | MΩ | Note 1) |
| TS ADC offset error | $V_{OFFSET3}$ | -2 | – | 2 | LSB | $V_{ADC3\_IN}$ = 1.2 V, TS ADC LSB = 2.344 mV |

**(table continues...)**

**Table 14 (continued) Electrical characteristics**

$V_{DD}$ = 2.97 V to 3.63 V, 1 µF capacitor from VDD pin to GND, 1 µF capacitor from VD12 pin to GND, $T_J$ = -40°C to 125°C unless otherwise specified. Positive current flows into the pin.

| Parameter | Symbol | Values | | | Unit | Note or condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Sample rate | $f_{ADC3}$ | – | 0.926 | – | MHz | – |
| TS ADC gain error | $A_{ADC3\_1}$ | -1 | – | 1 | % | $V_{ADC3\_IN}$ = 0.3 V to 2.1 V |
| TS ADC accuracy | $V_{ADC3\_1}$ | -16 | – | 16 | mV | $V_{ADC3\_IN}$ = 0.15 V |
| TS ADC accuracy | $A_{ADC3\_2}$ | -4.5 | – | 4.5 | % | $V_{ADC3\_IN}$ = 0.3 V |
| TS ADC accuracy | $A_{ADC3\_3}$ | -2 | – | 2 | % | $V_{ADC3\_IN}$ = 0.6 V |
| TS ADC accuracy | $A_{ADC3\_4}$ | -1 | – | 1 | % | $V_{ADC3\_IN}$ = 1.2 V, 2.1 V and 2.4 V |
| **IMON DAC** | | | | | | |
| Output current range | $I_{DAC}$ | -640 | – | 0 | µA | Note [1] |
| Output current resolution | $I_{RES}$ | – | 10 | – | µA | Note [1] |
| DAC accuracy | $A_{DAC}$ | -3 | – | 3 | % | $I_{DAC}$ = -100 µA |
| **XADDR1** | | | | | | |
| Output current range | $I_{XADDR1}$ | -640 | – | 0 | µA | Note [1] |
| **GPIO: IMON, EN** | | | | | | |
| Low-level output voltage | $V_{OL}$ | – | – | 0.4 | V | $I_{OL}$ = 5 mA |
| High-level output voltage | $V_{OH}$ | 2.6 | – | – | V | $I_{OH}$ = -5 mA |
| Low-level input voltage | $V_{IL}$ | – | – | 1.0 | V | Note [3] |
| High-level input voltage | $V_{IH}$ | 2.1 | – | – | V | Note [3] |
| Leakage current | $I_{OZ}$ | -1 | – | 1 | µA | – |
| **GPIO: PWM1-6, PWRGD, SYNC** | | | | | | |
| Low-level output voltage | $V_{OL}$ | – | – | 0.4 | V | $I_{OL}$ = 5 mA |
| High-level output voltage | $V_{OH}$ | 2.6 | – | – | V | $I_{OH}$ = -5 mA |

**(table continues...)**

**Table 14 (continued) Electrical characteristics**

$V_{DD}$ = 2.97 V to 3.63 V, 1 µF capacitor from VDD pin to GND, 1 µF capacitor from VD12 pin to GND, $T_J$ = -40°C to 125°C unless otherwise specified. Positive current flows into the pin.

| Parameter | Symbol | Values | | | Unit | Note or condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Low-level input voltage | $V_{IL}$ | – | – | $0.3V_{DD}$ | V | – |
| High-level input voltage | $V_{IH}$ | $0.7V_{DD}$ | – | – | V | – |
| Leakage current | $I_{OZ}$ | -1 | – | 1 | µA | – |
| **SDA, SCL, SMBALERT** | | | | | | |
| Low-level output voltage | $V_{OL}$ | – | – | 0.4 | V | $I_{OL}$ = 20 mA |
| Low-level input voltage | $V_{IL}$ | – | – | 1.0 | V | Configured as 3.3 V CMOS |
| High-level input voltage | $V_{IH}$ | 2.1 | – | – | V | Configured as 3.3 V CMOS |
| Low-level input voltage | $V_{IL}$ | – | – | 0.6 | V | Configured as 1.8 V CMOS |
| High-level input voltage | $V_{IH}$ | 1.35 | – | – | V | Configured as 1.8 V CMOS |
| Leakage current | $I_{OZ}$ | -1 | – | 1 | µA | – |
| Pin capacitance | $C_{PIN}$ | – | 1.5 | – | pF | Note [1)] |
| **System performance** | | | | | | |
| Processor master clock | $f_{CLK}$ | – | 100 | – | MHz | – |
| Internal oscillator frequency | $f_{OSC1}$ | 195 | 200 | 205 | MHz | $T_J$ = 25°C |
| Internal oscillator frequency | $f_{OSC2}$ | 190 | 200 | 210 | MHz | -40°C < $T_J$ < 125°C |
| Switching frequency | $f_{SW}$ | 50 | – | 2000 | kHz | PWM. Note [1)] |
| Switching period programming resolution | $t_{RES1}$ | – | 5 | – | ns | Note [1)] |

**(table continues...)**

**Table 14 (continued) Electrical characteristics**

$V_{DD}$ = 2.97 V to 3.63 V, 1 µF capacitor from VDD pin to GND, 1 µF capacitor from VD12 pin to GND, $T_J$ = -40°C to 125°C unless otherwise specified. Positive current flows into the pin.

| Parameter | Symbol | Values | | | Unit | Note or condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Switching period regulation resolution | $t_{RES2}$ | – | 2.5 | – | ns | Note [1] |
| Synchronization frequency range | $k_{SYNC}$ | -12.5 | – | 12.5 | % | With respect to switching period. Note [1] |
| **Temperature sensor** | | | | | | |
| Input voltage range | $V_{TSEN}$ | 0 | – | 2.4 | V | Note [1] |
| Output bias current | $I_{TSEN}$ | – | -100 | – | µA | Sourcing current to measure external $V_{BE}$, NTC or PTC resistor. Can be disabled |
| Internal temperature sensor accuracy | $T_{ERR}$ | – | ±5 | – | ˚C | Note [1] |
| **Fast GPIO** | | | | | | |
| Fast GPI response time | $t_{FSD1}$ | – | 50 | – | ns | From fast GPI input rising/falling edge to PWM rising/falling edge (synchronization), with zero programmed deadtime. Note [1] |
| Fast GPI response time | $t_{FSD2}$ | – | 150 | – | ns | From fast GPI input rising edge to PWM falling edge (PWM disable/shutdown) with zero programmed deadtime. Note [1] |
| Minimum input pulse width | $t_{FPW}$ | 25 | – | – | ns | Note [1] |
| Fast fault output response time | $t_{FSF}$ | – | 50 | – | ns | From fault triggering to rising/falling edge of fast fault output pin. Note [1] |

1) Not subject to production test - specified by design and/or characterization
2) Production minimum and maximum limits verified at 0.5V, 0.8V, 1.2V, 1.6V. Full range not subject to production test
3) EN pin voltage cannot linger between the $V_{IL}$ and $V_{IH}$ thresholds. The EN pin is intended to operate as a switch with the pin voltage either above or below the thresholds

# 6 Package Information

To meet the worldwide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

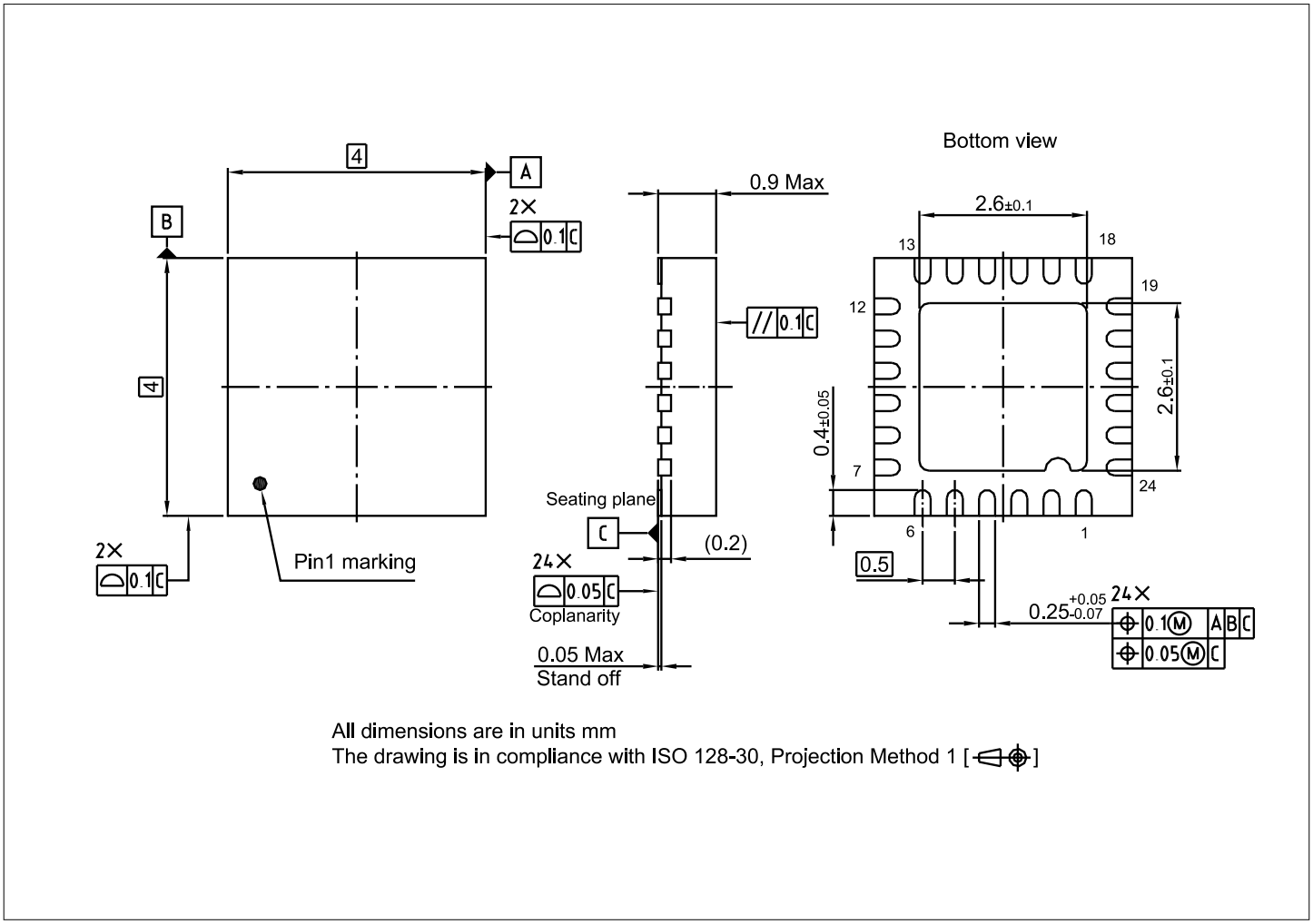



**Figure 31 Package dimensions PG-VQFN-24-20**

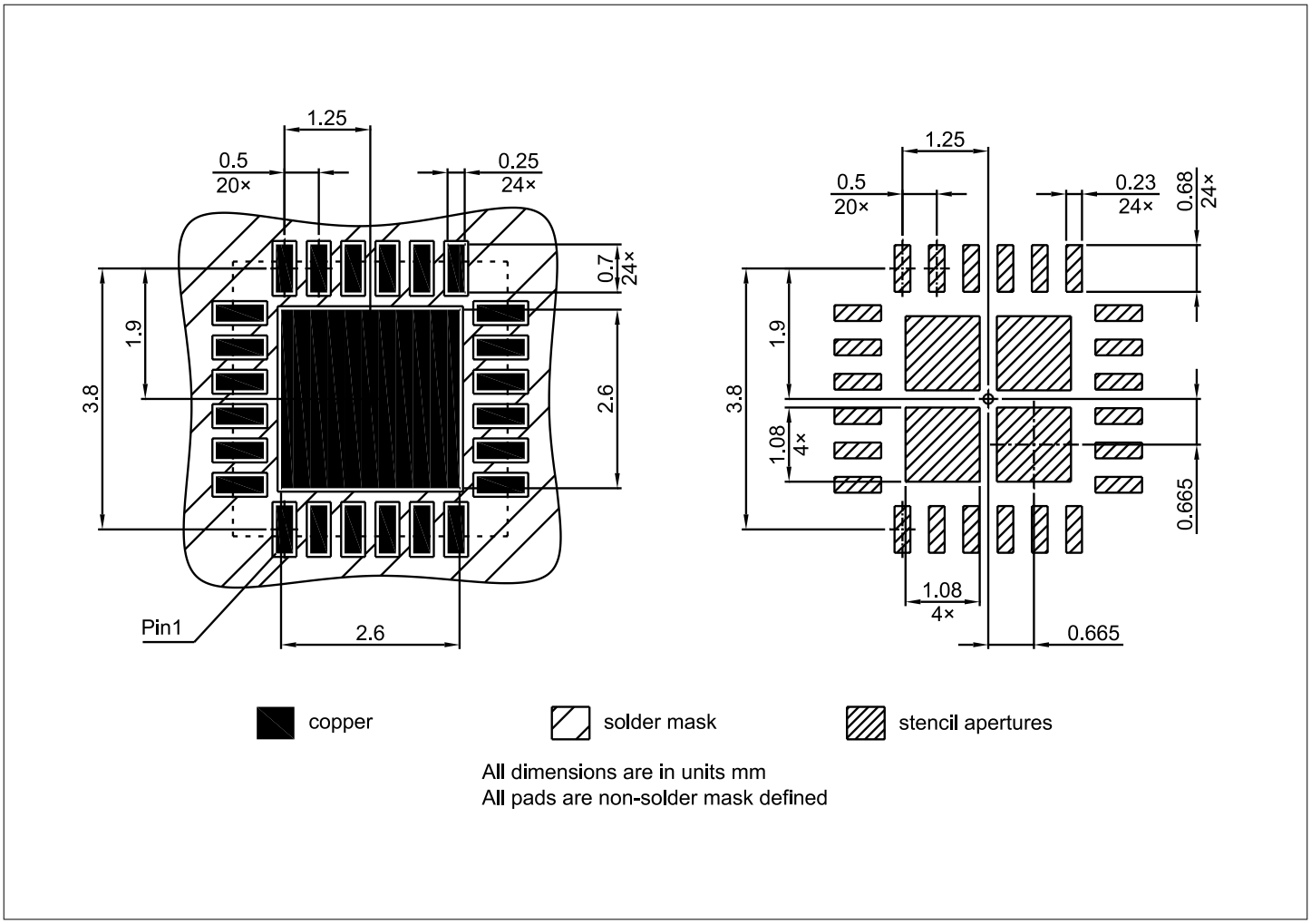



**Figure 32 Recommended footprint**

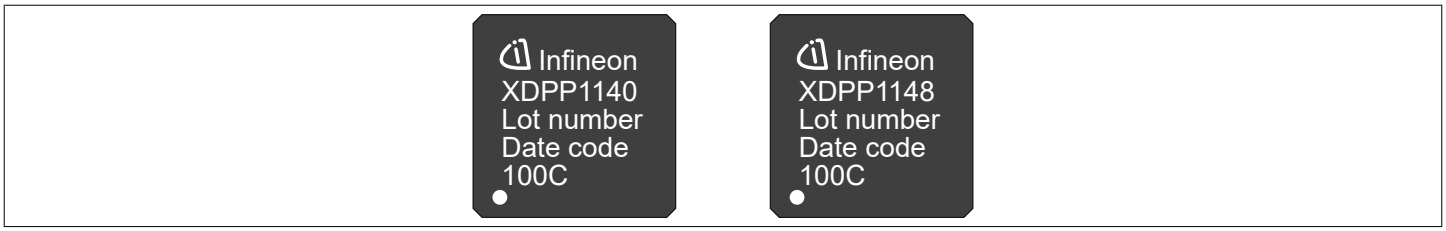



**Figure 33 Package marking**

Examples of Lot number and Date code:
Lot number: 1YUS1ANNB03
Date code: H2018B03
The B03 at the end of date code is the last 3 digits of the lot number.

# 7 Revision History

**Table 15 Revision History**

| Document version | Date of release | Description of changes |
|---|---|---|
| Rev. 1.0 | 2026-01-21 | Initial release |

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