Wireless charging IC (WLC) transmitter – 25 W with integrated USB Type-C PD controller

General description

WLC1125 is a highly integrated, programmable wireless power transmitter controller that enables solutions as per latest Qi standard, which ensures higher energy efficiency and faster charging. WLC1125 supports Qi2.x charging profile such as magnetic power profile (MPP) protocol, extended power profile (EPP) protocol, and basic power profile (BPP) protocol. In addition to this, WLC1125 also supports proprietary power delivery extensions. WLC1125 comes with integrated USB Type-C Power Delivery (PD) controller and is also compliant with the latest USB Type-C and PD specifications. WLC1125 is a programmable wireless power transmitter controller for 25 W charging applications.

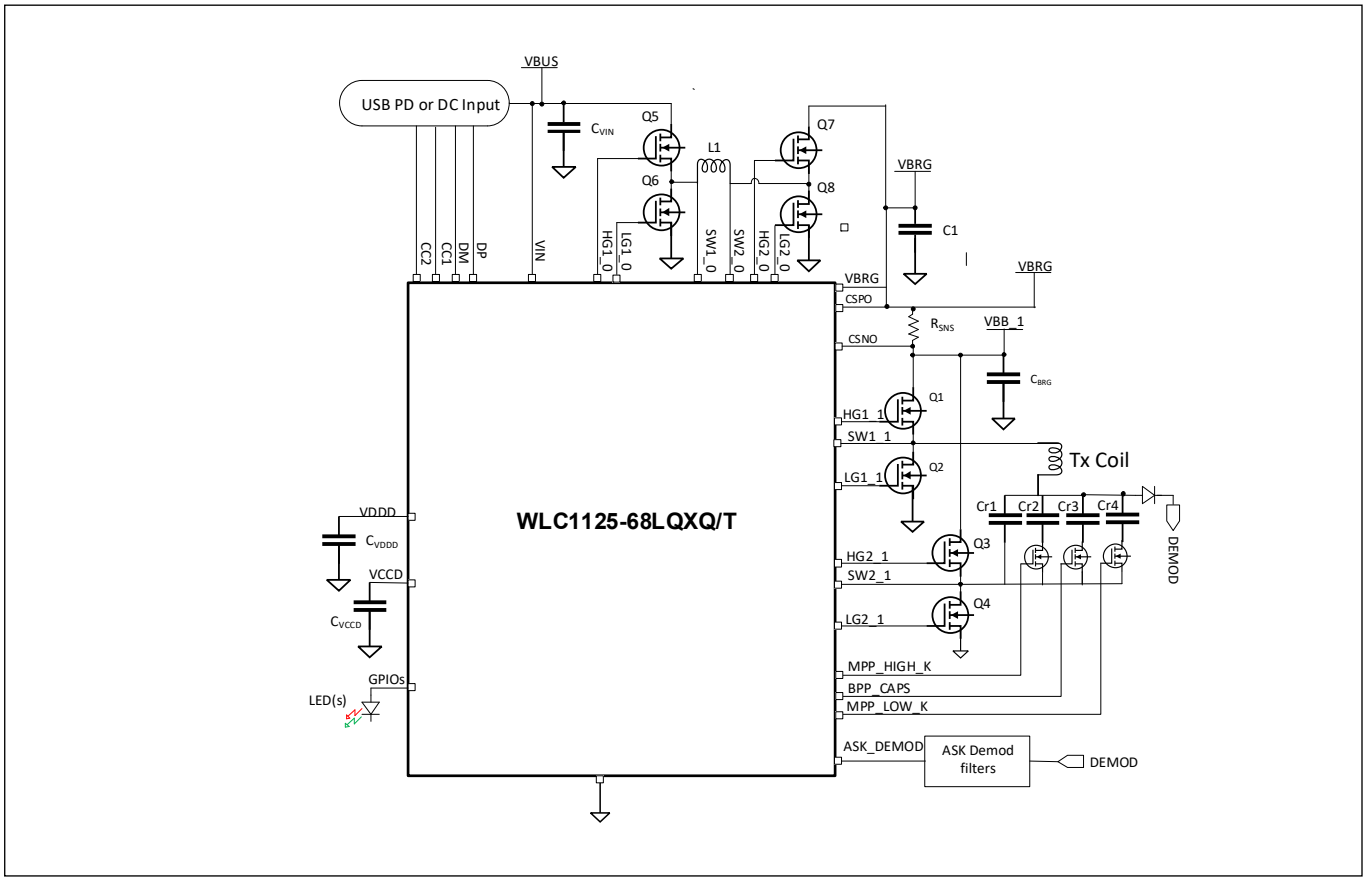
WLC1125 has integrated gate drivers for the buck-boost and inverter power supplies that are necessary for Qi2.x wireless transmitter applications. WLC1125 supports a wide input voltage range and offers many programmable features for creating distinct wireless transmitter solutions.

WLC1125 is a highly programmable wireless power transmitter and integrated USB-PD sink solution with an on-chip 32-bit Arm® Cortex®-M0 processor, 128 KB flash, 16 KB RAM, and 32 KB ROM that allows for convenient configuration changes for customization and tuning of important parameters such as FOD. It also includes various analog and digital peripherals such as ADC, PWMs, and timers. The inclusion of a fully programmable MCU with analog and digital peripherals enables scalable wireless transmitter solutions.

Features

- Enables Qi2.x compliant transmitter
- Integrated USB-PD controller
  - Supports USB-PD 3.x version
- Integrated buck-boost controller for inverter VBRG
- Integrated gate drivers for buck-boost converter and inverter
- Integrated Q factor detection
- Integrated FSK modulator
- Wide input voltage range: 4.5 V-24 V
- Communication ports: I^2C, UART
- **Protection**
  - Overcurrent protection (OCP), overvoltage protection (OVP)
  - Supports over-temperature protection through integrated ADC circuit and internal temperature sensor
- **Temperature range**
  - –40°C to +105°C extended industrial temperature range
- **Package**
  - 68-pin QFN 8.0 × 8.0 × 0.65 mm, LD68B 5.7 × 5.7 mm EPAD

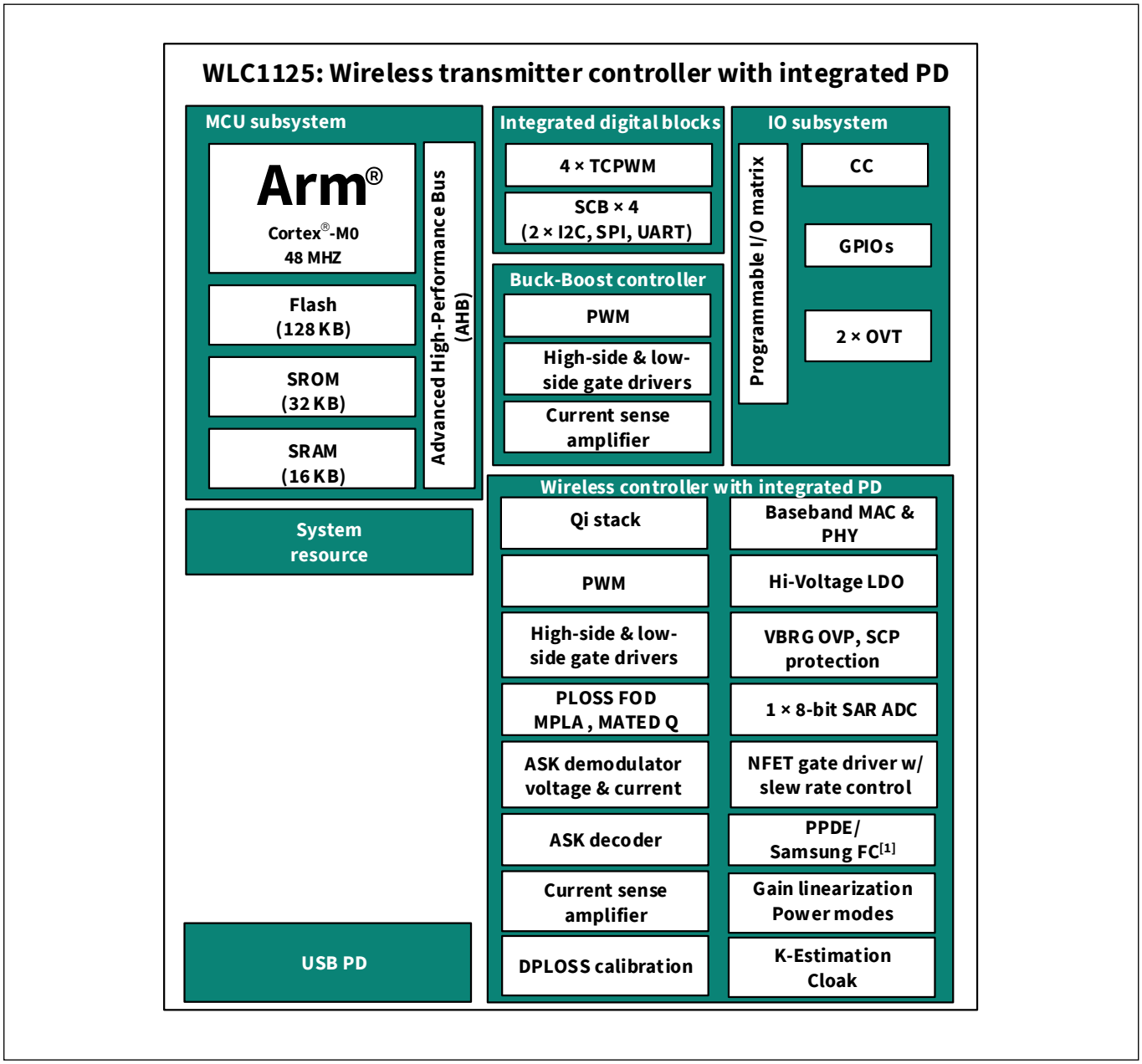
Application diagram



Potential applications

- Wireless charging pads for MPP, EPP, and BPP
- Smart speakers
- Portable accessories
- Furniture and home goods
- Docking stations
- High speed charging support

Logic block diagram



Note
1. Customers need to acquire their own licensing for Samsung FC.

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1 Application diagram for 25 W Qi2.x transmitter solution

Figure 1 illustrates a typical application of WLC1125 for 25 W, Qi2.x wireless power transmitter solution with MPP1 coil. The input power to the system is through Type-C PD sink or DC power supply input, powering the buck-boost converter with MPP1-based Qi transmitter coil. The buck-boost converter powers the full bridge inverter which in turn drives the MPP1 transmitter coil. The WLC1125 controls the inverter bridge voltage (VBRG) using the buck-boost converter to regulate the power flow to the transmitter coil powering the receiver. A dual Opamp is used for converting the amplitude shift key (ASK) modulated power signal into binary signal. WLC1125 uses a digital logic for decoding the binary signals. The Authentication IC is interfaced over I2C for authentication requirements as per Qi2.x.

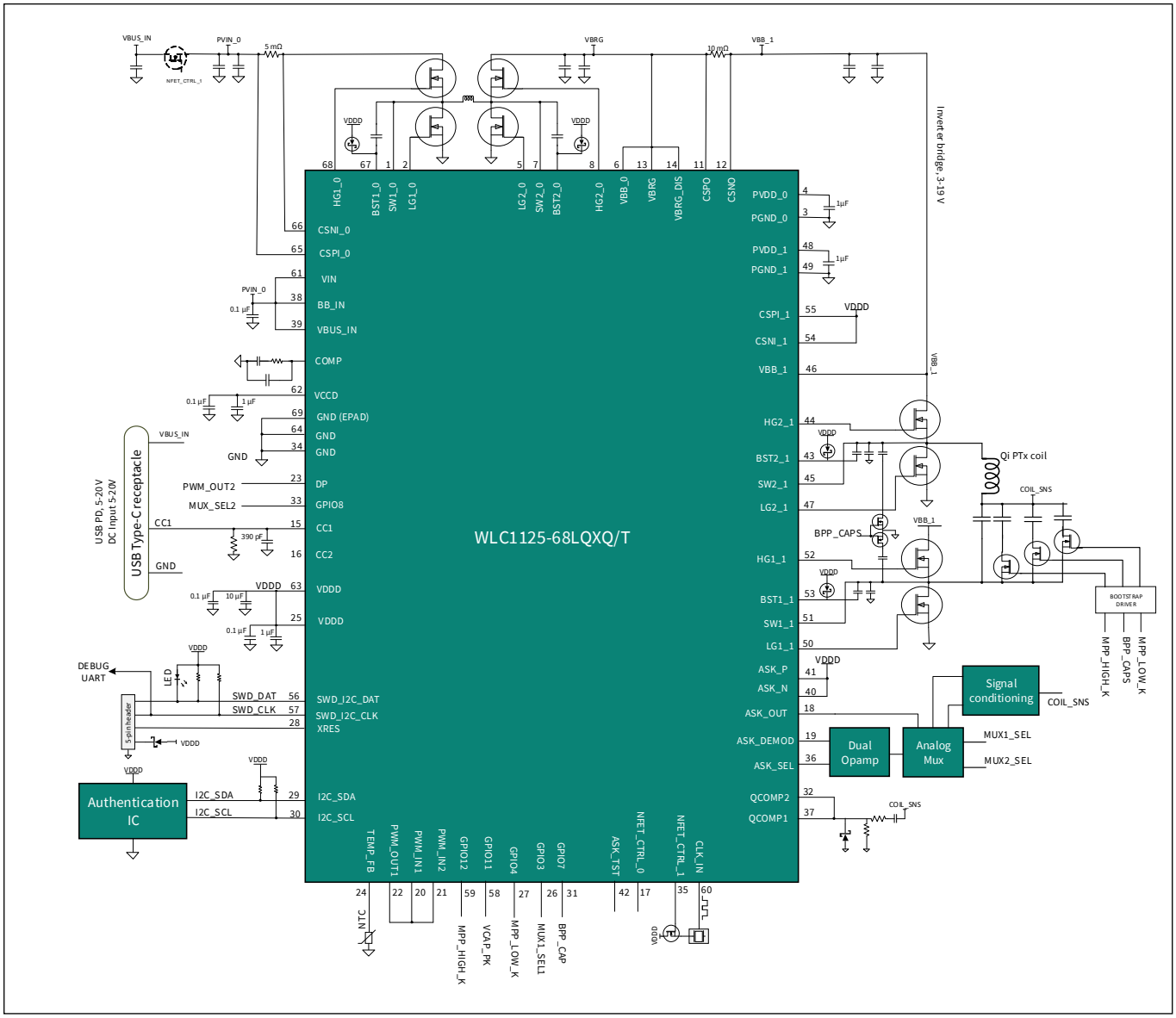


Figure 1 Application diagram for 25 W Qi2.x transmitter solution

2 Pin information

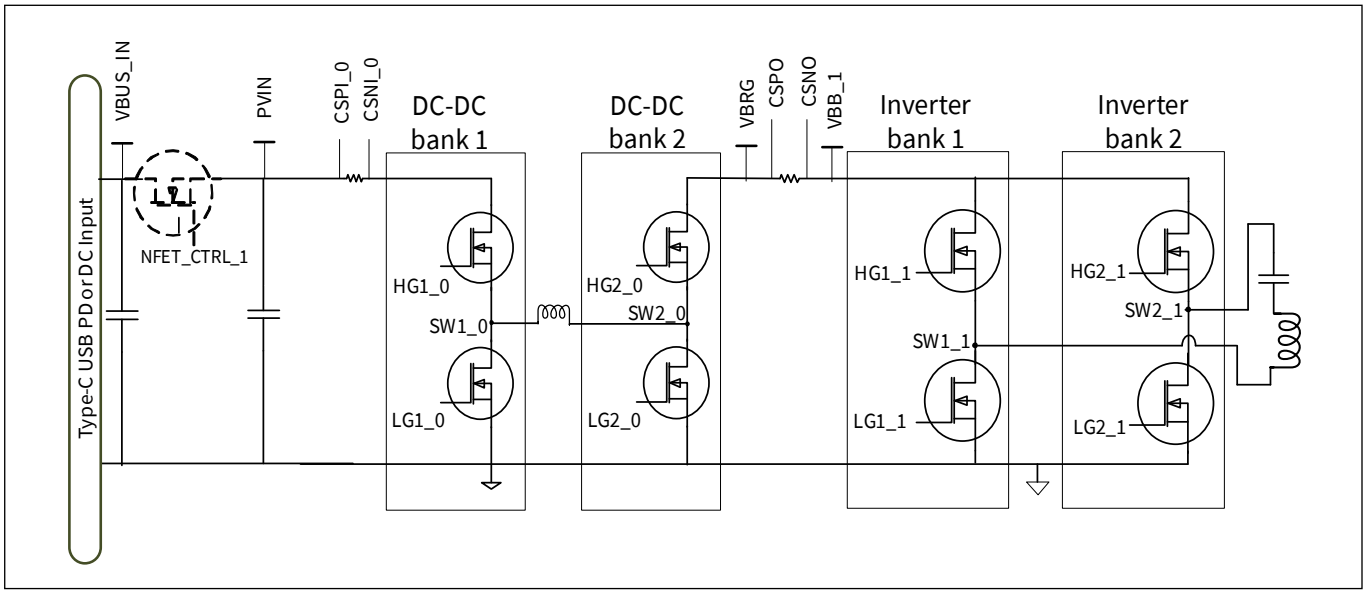


Figure 2 WLC1125 key pin mapping with buck-boost and inverter power supplies[2]

Table 1 WLC1125 pinouts

Pin#	Pin name	Pin function for 25 W MPP, or EPP application firmware	Pin description
1	SW1_0		Switching Node of DC-DC bank 1 (see **Figure 2**) and also used for programmable zero current detection (ZCD) of buck low-side gate driver. Connect this pin to the switch node (inductor). Use a short and wide trace to minimize the inductance and resistance of this connection.
2	LG1_0		Gate driver output for low-side FET of DC-DC bank 1. Connect this pin to the gate of low side FET. Use a wide trace to minimize inductance of this connection
3	PGND_0		Gate drive GND for DC-DC (Bank 1 and 2). Connect this GND directly to PCB ground plane and exposed pad (E-PAD).
4	PVDD_0		Supply for low-side gate driver of DC-DC bank 1 and 2. Connect to VDDD. Use 1 µF and 0.1 µF bypass capacitors as close as possible to the pin of WLC1125.
5	LG2_0		Gate driver output for low-side FET of DC-DC bank 2. Connect this pin to the gate of low side FET. Use a wide trace to minimize inductance of this connection.
6	VBB_0		Pin connects the output of the buck-boost converter and also for programmable reverse current protection (RCP) with high-side FET of DC-DC bank 2. Connect this pin to the boost sync (high-side) FET's drain. Use a dedicated (Kelvin) trace for this connection.

Note
2. See **Figure 2** for an overview of key WLC1125 pin mapping to power input, current sense and gate drivers of buck, and inverter power supplies.

Table 1 WLC1125 pinouts *(continued)*

Pin#	Pin name	Pin function for 25 W MPP, or EPP application firmware	Pin description
7	SW2_0		Switching node of DC-DC bank 2 (see **Figure 2**) and also its connection for reverse current protection (RCP) of high-side gate driver of DC-DC bank 2. Connect this pin to the switch node (inductor). Use a short and wide trace to minimize the inductance and resistance of this connection.
8	HG2_0		High-side gate driver output of DC-DC bank 2. Connect this pin to gate of high side FET. Use a wide trace to minimize inductance of this connection.
9	BST2_0		Node between Bootstrap capacitor and diode for high-side gate driver of DC-DC bank 2. Connect Schottky diode from VDDD to BST2_0. Also, connect a bootstrap capacitor (Recommended 0.1 µf) from this pin to SW2_0.
10	COMP		Error amplifier (EA) output for Buck Boost controller. Connect the RC compensation network to GND.
11	CSPO		Non Inverting input of current sensing amplifier of inverter bridge input sense current. Connect to positive terminal of the output current sense resistor (VBB_0).
12	CSNO		Inverting input of current sensing amplifier of inverter bridge input sense current. Connect to negative terminal of the current sense resistor.
13	VBRG		Feedback pin for buck-boost output voltage. Connect this pin to buck-boost output and before current sense resistor of inverter bridge.
14	VBRG_DIS		Connect this to VBRG. Used as weak discharge of VBRG.
15	CC1		Type-C connector configuration channel 1. Connect directly to the CC1 pin on the port's Type-C connector Also connect a 390-pF capacitor to ground.
16	CC2		Type-C connector configuration channel 2. Connect directly to the CC2 pin on the port's Type-C connector Also connect a 390-pF capacitor to ground.
17	NFET_CTRL_0		NFET gate driver output. Float this pin if it is not used.
18	ASK_OUT		Filtered ASK output from inverter input current.
19	ASK_DEMOD		Input for ASK signal decoding. Connect external ASK comparator output to this pin. Short this pin to pin-36 (ASK_SEL).
20	GD_OVR_HB_1	PWM_IN1	Inverter gate driver input signal for inverter bank 1. Short this pin to pin-23 (DP/GPIO1/PWM_OUT2).
21	GD_OVR_HB_2	PWM_IN2	Inverter gate driver input signal for inverter bank 2. Short this pin to pin-22 (PWM_OUT1).
22	PWM_OUT1		PWM input to inverter bank 1. Short this pin to pin-21 (PWM_IN2).
23	DP/GPIO1	PWM_OUT2	PWM input to inverter bank 2/ default USB D+ / configurable GPIO Short this pin to pin-20 (PWM_IN1). IC does not support USB data transmission on this pin.
24	DM/GPIO2	TEMP_FB	Default USB D- / configurable GPIO. IC does not support USB data transmission on this pin. Input pin for temperature from NTC for Qi2.x application.
25	VDDD		VDDD 5 V LDO output from VIN. Connect a ceramic bypass capacitor (recommended value 1 µF) from this pin to GND close to the IC. Also, connect this pin directly to pin 63.

Table 1 WLC1125 pinouts *(continued)*

Pin#	Pin name	Pin function for 25 W MPP, or EPP application firmware	Pin description
26	GPIO3	MUX_SEL1	Used GPIO for MUX1 selection. Select the ASK Input through MUX1 either Voltage or Phase
27	GPIO4	MPP_LOW_K	Output to select MPP resonance capacitor based on mated coil coupling K.
28	XRES		External reset – active low, internally pulled-up (~6 kΩ). Float this pin if it is not used.
29	GPIO5/SCB0	I2C_SDA	Use for interfacing as master, with Authentication IC I2C SDA. The pin is configured for open drain connection, connect an external pull-up resistor. Float this pin if it is not used.
30	GPIO6/SCB0	I2C_SCL	Used for interfacing with Authentication IC I2 C SCL The pin is configured for open drain connection, connect an external pull-up resistor. Float this pin if it is not used.
31	GPIO7/SCB1	BPP_CAP	GPIO used for selection of BPP resonance capacitor based on mated coil coupling.
32	QCOMP2		Q-factor based foreign object detection (FOD) pre-charge measurement input for frequency counting. Short this pin to pin 37 (QCOMP1).
33	GPIO8	MUX_SEL2	Used GPIO for Mux2 selection. Select the ASK Input through MUX2 either (voltage or phase) or current.
34	GND		Ground. Connect directly to the E-PAD and to ground plane.
35	NFET_CTRL_1		NFET gate driver output. Use to Drive NFET for inrush control. Float this pin if it is not used.
36	ASK_SEL		Use as input for ASK signal decoding. Short this pin to pin-19 (ASK_DEMOD).
37	QCOMP1		Q-factor based FOD pre-charge measurement input for peak voltage detect. Short this pin to pin 32 (QCOMP2).
38	BB_IN		Input voltage to buck-boost (DC-DC) controller. Connect to USB Type-C connector's VBUS pin. In case of EMI Filter Added to USB, connect pin after EMI Filtered voltage.
39	VBUS_IN		Input voltage to buck-boost (DC-DC) controller. Connect to USB Type-C connector's VBUS pin. In case of EMI Filter Added to USB, connect Pin after EMI Filtered Voltage.
40	ASK_N	DNU3	Negative input of ASK voltage sensing signal input to internal amplifier. Pullup this PIN to VDDD for Qi2.x Application.
41	ASK_P	DNU4	Positive input of ASK voltage sensing signal input to internal amplifier. Pullup this PIN to VDDD for Qi2.x Application.
42	ASK_TST		ASK voltage sensing comparator output. Float this pin if it is not used.
43	BST2_1		Node between Bootstrap capacitor & diode for high-side gate driver of inverter bank 2. Connect Schottky diode from VDDD to BST2_1. Also, connect a bootstrap capacitor (recommended 0.1 µf) from this pin to SW2_1.
44	HG2_1		High-side gate driver output of Inverter bank 2 Connect this PIN to Gate of high side FET. Use a wide trace to minimize inductance of this connection.

Table 1 WLC1125 pinouts *(continued)*

Pin#	Pin name	Pin function for 25 W MPP, or EPP application firmware	Pin description
45	SW2_1		Switching node of inverter bank 2 (see **Figure 2**) and also its connection for reverse current protection (RCP) of high-side Gate driver of inverter bank 2. Connect this pin to the switch node (inductor). Use a short and wide trace to minimize the inductance and resistance of this connection.
46	VBB_1		Inverter input voltage sense. Connect to inverter input voltage, after the current sense resistor. Use a dedicated (Kelvin) trace for this connection.
47	LG2_1		Gate driver output for Low Side FET of inverter bank 2 Connect this pin to the gate of low side FET. Use a wide trace to minimize inductance of this connection.
48	PVDD_1		Supply for low-side gate driver of inverter bank 1 and 2. Connect to VDDD. Use 1 µF and 0.1 µF bypass capacitors as close as possible to the pin of WLC1125.
49	PGND_1		Gate drive GND for inverter (bank 1 and 2). Connect this GND directly to PCB ground plane and Exposed pad (E-PAD).
50	LG1_1		Gate driver output for Low Side FET of Inverter bank 1 Connect this PIN to the gate of low side FET. Use a wide trace to minimize inductance of this connection.
51	SW1_1		Switching node of inverter bank 1 (see **Figure 2**) and also used for programmable zero current detection (ZCD) of buck low-side gate driver. Connect this pin to the switch node (inductor).Use a short and wide trace to minimize the inductance and resistance of this connection.
52	HG1_1		High-side gate driver output of Inverter bank 1. Connect this PIN to Gate of high side FET. Use a wide trace to minimize inductance of this connection.
53	BST1_1		Node between Bootstrap capacitor & diode for high-side gate driver of inverter bank 1. Connect Schottky diode from VDDD to BST1_1. Also, connect a bootstrap capacitor (recommended value of 0.1 µf) from this pin to SW1_1.
54	CSNI_1	DNU1	Negative input of input current sense amplifier for inverter. For Qi2.x pulled up this pin VDDD or Pvin.
55	CSPI_1	DNU2	Positive input of input current sense amplifier for inverter. For Qi2.x pulled up this pin VDDD or Pvin.
56	GPIO9/SCB3/SWD_DAT	SWD_I2C_DAT	Use for I2C/SWD register access or programming/configurable GPIO.
57	GPIO10/SCB3/SWD_CLK	SWD_I2C_CLK	Use for I2C/SCL register access or programming/configurable GPIO.
58	GPIO11/SCB3	VCAP_PK	Configurable GPIO. Use to measure Resonance Cap Peak voltage.
59	GPIO12/SCB3	MPP_HIGH_K	Output to select MPP Resonance capacitor based on Mated Coil Coupling K.
60	GPIO13	CLK_IN	Configurable GPIO. Qi2.x use as input for external clock from Crystal.
61	VIN		4.5V–24V input supply. Connect a decoupling capacitor (recommended value 0.1 µF) from this pin to GND close to this pin.
62	VCCD		1.8 V Core LDO output. Connect a decoupling capacitor (recommended value 0.1 µF) from this pin to ground. DO not connect this pin to avoid loading.

Table 1 WLC1125 pinouts *(continued)*

Pin#	Pin name	Pin function for 25 W MPP, or EPP application firmware	Pin description
63	VDDD		5 V LDO output. Connect a ceramic bypass capacitor (recommended value 10µF) from this pin to GND close. to the IC. Also, connect this pin directly to pin 62.
64	GND		Ground. Connect directly to the E-PAD and to ground plane.
65	CSPI_0		Positive input to current sense amplifier (DC-DC). Connect to the positive terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
66	CSNI_0		Negative input to current sense amplifier (DC-DC). Connect to the negative terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
67	BST1_0		Node between bootstrap capacitor and diode for high-side gate driver of DC-DC bank 1. Connect Schottky diode from VDDD to BST1_0. Also, connect a bootstrap capacitor (Recommended 0.1uf) from this pin to SW1_0.
68	HG1_0		High-side gate driver output of DC-DC bank 1. Connect this PIN to Gate of high side FET. Use a wide trace to minimize inductance of this connection.
	EPAD		Exposed ground pad. Connect directly to pins 34 and 64.

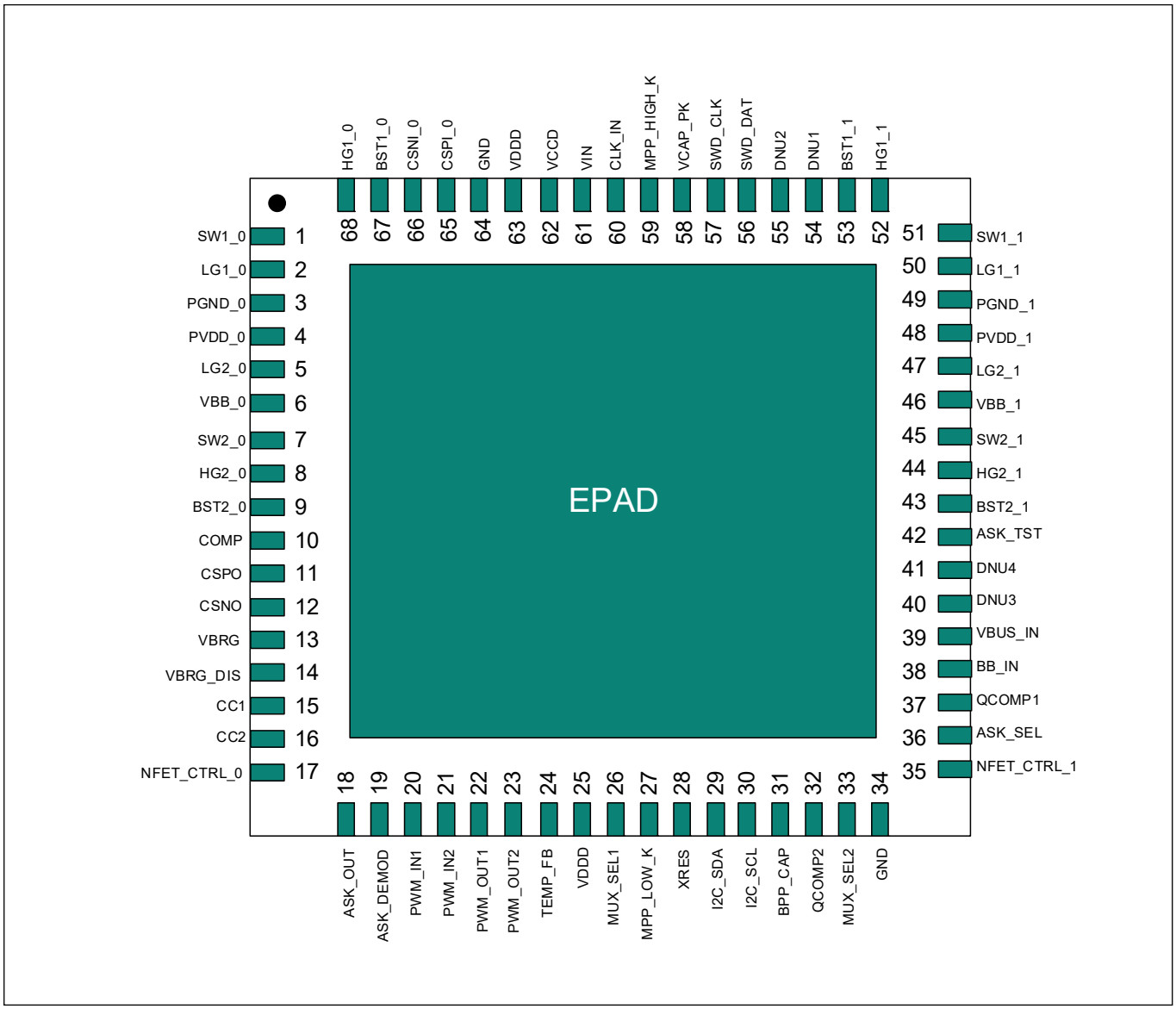


Figure 3 WLC1125 68-QFN pinout

3 Electrical specifications

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[3]

Exceeding maximum ratings may shorten the useful life of the device.

All specifications are valid for -40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Parameter	Description	Min	Typ	Max	Unit	Description
VIN	Maximum input supply voltage	–	–	40	V	–
VDDD, PVDD	Maximum supply voltage relative to VSS			6		
VBUS	Max VBRG_DIS (P0/P1) voltage relative to VSS			24		
CC_0, ASK_SEL	Max voltage on CC and ASK_SEL pins			24		
QCOMP1	Max voltage on QCOMP1 pins	–0.7		24		Current limited to 1 mA for –0.7 V minimum specification.
QCOMP2	Input to QCOMP2	–0.7		VDDD + 0.5		
GPIO	Inputs to GPIO	–0.5		VDDD + 0.5		–
IGPIO	Maximum current per GPIO	–25		25	mA	
IGPIO_INJECTION	GPIO injection current, Max for VIH > VDDD, and Min for VIL < VSS	–0.5		0.5		Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge (ESD) human body model (HBM)	2000		–	V	Applicable for all pins except CC1_0, CC2_0, ASK_SEL, QCOMP1 pins.
ESD_HBM_CC	ESDHBM for CC1 and CC2 pins for both ports	1100				Only applicable to CC1_0, CC2_0, ASK_SEL, QCOMP1 pins
ESD_CDM	ESD charged device model	500				Charged device model ESD
LU	Pin current for latch-up	–100		100	mA	–
TJ	Junction temperature	–40		125	°C	

Note

3. Usage above the absolute maximum conditions listed in **Table 2** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 3 Pin based absolute maximum ratings

Pin#	Pin name	Pin function for 25 W MPP, or EPP application firmware	Absolute minimum (V)	Absolute maximum (V)
1	SW1_0		–0.7	35
2	LG1_0[4]		–0.5	PVDD+0.5
3	PGND_0		–0.3	0.3
4	PVDD_0		–0.3	VDD
5	LG2_0[4]		–0.5	PVDD+0.5
6	VBB_0		–0.3	24
7	SW2_0		–0.3	24
8	HG2_0 (w.r.t SW2_0)[4, 5]		–0.5	PVDD+0.5
9	BST2_0 (w.r.t SW2_0)[4, 5, 6]		0	PVDD+0.5
10	COMP[4]		–0.5	PVDD+0.5
11	CSPO		–0.3	24
12	CSNO		–0.3	24
13	VBRG		–0.3	24
14	VBRG_DIS		–0.3	24
15	CC1		–0.5	24
16	CC2		–0.5	24
17	NFET_CTRL_0		–0.5	32
18	ASK_OUT[4]		–0.5	PVDD+0.5
19	ASK_DEMOD[4]		–0.5	PVDD+0.5
20	GD_OVR_HB_1[4]	PWM_IN1	–0.5	PVDD+0.5
21	GD_OVR_HB_2[4]	PWM_IN2	–0.5	PVDD+0.5
22	PWM_OUT1[4]		–0.5	PVDD+0.5
23	DP/GPIO1[4]	PWM_OUT2	–0.5	PVDD+0.5
24	DM/GPIO2[4]	TEMP_FB	–0.5	PVDD+0.5
25, 63	VDDD		–0.3	6
26	GPIO3[4]	MUX_SEL1	–0.5	PVDD+0.5
27	GPIO4[4]	MPP_LOW_K	–0.5	PVDD+0.5
28	XRES[4]		–0.5	PVDD+0.5
29	GPIO5/SCB0[4]	I2C_SDA	–0.5	PVDD+0.5
30	GPIO6/SCB0[4]	I2C_SCL	–0.5	PVDD+0.5
31	GPIO7/SCB1[4]	BPP_CAP	–0.5	PVDD+0.5
32	QCOMP2[4, 7]		–0.7	PVDD+0.5
33	GPIO8[4]	MUX_SEL2	–0.5	PVDD+0.5
34,64	GND		–0.3	0.3
35	NFET_CTRL_1		–0.5	32
36	ASK_SEL		–0.5	24
37	QCOMP1[7]		–0.7	24

Notes
4. Max voltage cannot exceed 6 V.
5. Max absolute voltage w.r.t GND must not exceed 40 V.
6. Min absolute voltage w.r.t GND must not be lower than –0.3 V.
7. Current limited to 1mA for –0.7 V minimum specification only.

Table 3 Pin based absolute maximum ratings *(continued)*

Pin#	Pin name	Pin function for 25 W MPP, or EPP application firmware	Absolute minimum (V)	Absolute maximum (V)
38	BB_IN		–0.3	24
39	VBUS_IN		–0.3	24
40	ASK_N		–0.3	24
41	ASK_P		–0.3	24
42	ASK_TST[4]		–0.5	PVDD+0.5
43	BST2_1 (w.r.t SW2_1)[4, 5, 6]		0	PVDD+0.5
44	HG2_1 (w.r.t SW2_1)[4, 5]		–0.5	PVDD+0.5
45	SW2_1		–0.7	24
46	VBB_1		–0.3	24
47	LG2_1[4]		–0.5	PVDD+0.5
48	PVDD_1		–0.3	VDDD
49	PGND_1		–0.3	0.3
50	LG1_1[4]		–0.5	PVDD+0.5
51	SW1_1		–0.7	35
52	HG1_1 (w.r.t SW1_1)[4, 5]		–0.5	PVDD+0.5
53	BST1_1 (w.r.t SW1_1)[4, 5, 6]		0	PVDD+0.5
54	CSNI_1	DNU1	–0.3	40
55	CSPI_1	DNU2	–0.3	40
56	GPIO9/SCB3/SWD_DAT[4]	SWD_I2C_DAT	–0.5	PVDD+0.5
57	GPIO10/SCB3/SWD_CLK[4]	SWD_I2C_CLK	–0.5	PVDD+0.5
58	GPIO11/SCB3[4]	VCAP_PK	–0.5	PVDD+0.5
59	GPIO12/SCB3[4]	MPP_HIGH_K	–0.5	PVDD+0.5
60	GPIO13/CLK_IN[4]	CLK_IN	–0.5	PVDD+0.5
61	VIN		–0.3	40
62	VCCD		–0.3	2
65	CSPI_0		–0.3	40
66	CSNI_0		–0.3	40
67	BST1_0 (w.r.t SW1_0)[4, 5, 6]		0	PVDD+0.5
68	HG1_0 (w.r.t SW1_0)[4, 5]		–0.5	PVDD+0.5
	EPAD		–0.3	0.3

Notes
4. Max voltage cannot exceed 6 V.
5. Max absolute voltage w.r.t GND must not exceed 40 V.
6. Min absolute voltage w.r.t GND must not be lower than –0.3 V.
7. Current limited to 1mA for –0.7 V minimum specification only.

3.2 Device-level specifications

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

3.3 DC specifications

Table 4 DC specifications (Operating conditions)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#1	VIN	Input supply voltage	4.5	–	24	V	–
SID.PWR#2	VDDD	VDDD output voltage range	4.6		5.5		5.5 V < VINS < 24 V; Max load = 150 mA
SID.PWR#3	VDDD_MIN	VDDD dropout voltage	VIN - 0.2		–		4.5 V < VIN < 5.5 V; Max load = 20 mA
SID.PWR#20	VBRG	VBRG_0 output range	3		22		VIN > VBRG
SID.PWR#5	VCCD	VCCD output voltage	–	1.8	–		–
SID.PWR#25	IDD_ACT48M	Operating quiescent current at 0.4 MHz switching frequency		87		mA	TA = 25°C, VIN = 12 V. CC IO in transmit or receive, no I/O sourcing current, No VCONN load current, CPU at 48 MHz, buck and inverter ON, 3-nF gate driver capacitance.

3.3.1 CPU

Table 5 CPU specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#4	FCPU	CPU input frequency	–	–	48	MHz	External 43.935 MHz clock is required for MPP mode of operation.
SYS.XRES#5	TXRES	External reset pulse width	5	–	–	µs	
SYS.FES#1	T_PWR_RDY	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	

3.3.2 GPIO

All specifications are valid for -40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 6 GPIO specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
GPIO DC specifications							
SID.GIO#9	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × VDDD	–	–	V	CMOS input
SID.GIO#10	V_{IL_CMOS}	Input voltage LOW threshold	–		0.3 × VDDD		
SID.GIO#7	V_{OH}	Output voltage HIGH level	VDDD – 0.6		–		IOH = –4mA
SID.GIO#8	V_{OL}	Output voltage LOW level	–		0.6		IOL = 10mA
SID.GIO#2	Rpu	Pull-up resistor when enabled	3.5	5.6	8.5	kΩ	–
SID.GIO#3	Rpd	Pull-down resistor when enabled	3.5	5.6	8.5		
SID.GIO#4	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	TA = 25°C, VDDD = 3V
SID.GIO#5	C_{PIN_A}	Max pin capacitance			22	pF	Capacitance on DP, DM pins
SID.GIO#6	C_{PIN}	Max pin capacitance		3	7		–40°C < TA < +105°C, All VDDD, all other I/Os
SID.GIO#13	V_{HYSTTL}	Input hysteresis, LVTTL, VDDD > 2.7V	100	–	–	mV	VDDD > 2.7 V
SID.GIO#14	$V_{HYSCMOS}$	Input hysteresis CMOS	0.1 × VDDD				–
GPIO AC specifications							
SID.GIO#16	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	Cload = 25 pF
SID.GIO#17	T_{FALLF}	Fall time in Fast Strong mode	2		12		
SID.GIO#18	T_{RISES}	Rise time in Slow Strong mode	10		60		
SID.GIO#19	T_{FALLS}	Fall time in Slow Strong mode	10		60		
SID.GIO#20	F_{GPIO_OUT1}	GPIO FOUT; 3.0V ≤ VDDD ≤ 5.5V. Fast Strong mode.	–		16	MHz	
SID.GIO#21	F_{GPIO_OUT2}	GPIO FOUT; 3.0V ≤ VDDD ≤ 5.5V. Slow Strong mode.			7		
SID.GIO#22	F_{GPIO_IN}	GPIO input operating frequency; 3.0 V ≤ VDDD ≤ 5.5 V.			48		-40°C ≤ TA ≤ +105°C
GPIO OVT DC specifications							
SID.GPIO_20VT_GIO#4	GPIO_20VT_I_LU	GPIO_20VT latch up current limits	–140	–	140	mA	Max/min current in to any input or output, pin-to-pin, pin-to-supply

Table 6 GPIO specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.GPIO_20VT_GIO#5	GPIO_20VT_RPU	GPIO_20VT pull-up resistor value	3.5		8.5	kΩ	–40°C ≤ TA ≤ +105°C, All VDDD
SID.GPIO_20VT_GIO#6	GPIO_20VT_RPD	GPIO_20VT pull-down resistor value	3.5		8.5		–40°C ≤ TA ≤ +105°C, All VDDD
SID.GPIO_20VT_GIO#16	GPIO_20VT_IIL	GPIO_20VT input leakage current (absolute value)	–		2	nA	+25°C TA, 3V VDDD
SID.GPIO_20VT_GIO#17	GPIO_20VT_CPIN	GPIO_20VT pin capacitance			10	pF	–40°C ≤ TA ≤ +105°C, All VDDD
SID.GPIO_20VT_GIO#33	GPIO_20VT_Voh	GPIO_20VT output voltage high level	VDDD - 0.6	–	–	V	IOH = –4mA
SID.GPIO_20VT_GIO#36	GPIO_20VT_Vol	GPIO_20VT output voltage low level	–		0.6		IOL = 8mA
SID.GPIO_20VT_GIO#41	GPIO_20VT_Vih_LV TTL	GPIO_20VT LVTTL input	2		–		–40°C ≤ TA ≤ +105°C, All VDDD
SID.GPIO_20VT_GIO#42	GPIO_20VT_Vil_LV TTL	GPIO_20VT LVTTL input	–		0.8		–40°C ≤ TA ≤ +105°C, All VDDD
SID.GPIO_20VT_GIO#43	GPIO_20VT_Vhysttl	GPIO_20VT input hysteresis LVTTL	100		–	mV	–40°C ≤ TA ≤ +105°C, All VDDD
SID.GPIO_20VT_GIO#45	GPIO_20VT_ITOT_G PIO	GPIO_20VT maximum total sink pin current to ground	–		95	mA	V (GPIO_20VT Pin) > VDDDs
GPIO OVT AC specifications							
SID.GPIO_20VT_70	GPIO_20VT_TriseF	GPIO_20VT Rise time in Fast Strong Mode	1	–	15	ns	All VDDD, Cload = 25 pF
SID.GPIO_20VT_71	GPIO_20VT_TfallF	GPIO_20VT Fall time in Fast Strong Mode	1		15		
SID.GPIO_20VT_GIO#46	GPIO_20VT_TriseS	GPIO_20VT Rise time in Slow Strong Mode	10		70		
SID.GPIO_20VT_GIO#47	GPIO_20VT_TfallS	GPIO_20VT Fall time in Slow Strong Mode	10		70		
SID.GPIO_20VT_GIO#48	GPIO_20VT_FGPIO_OUT1	GPIO_20VT GPIO Fout; 3V ≤ VDDD ≤ 5.5V. Fast Strong mode.	–		33	MHz	
SID.GPIO_20VT_GIO #50	GPIO_20VT_FGPIO_OUT3	GPIO_20VT GPIO Fout; 3V ≤ VDDD ≤ 5.5V. Slow Strong mode.			7		
SID.GPIO_20VT_GIO #52	GPIO_20VT_FGPIO_IN	GPIO_20VT GPIO input operating frequency; 3V ≤ VDDD ≤ 5.5V			8		All VDDD

3.3.3 XRES and POR

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 7 XRES specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
XRES DC specifications							
SID.XRES#1	V_{IH_XRES}	Input voltage HIGH threshold on XRES pin	0.7 × VDDD	–	–	V	CMOS input
SID.XRES#2	V_{IL_XRES}	Input voltage LOW threshold on XRES pin	–		0.3 × VDDD		
SID.XRES#3	C_{IN_XRES}	Input capacitance on XRES pin	–		7	pF	–
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis on XRES pin		0.05 × VDDD	–	mV	
Imprecise POR (IPOR) specifications							
SID185	$V_{RISEIPOR}$	POR rising trip voltage	0.80	–	1.50	V	–40°C < TA < +105°C, all VDDD
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70		1.4		
Precise POR (POR) specifications							
SID190	$V_{FALLPPOR}$	Brown-out detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–40°C < TA < +105°C, all VDDD
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1		1.5		

3.4 Digital peripherals

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

The following specifications apply to the Timer/counter/PWM peripherals in the Timer mode.

3.4.1 Inverter pulse-width modulation (PWM) for GPIO pins

Table 8 PWM AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.TCPWM.1	PWM_OUT	Operating frequency	85	127.7	600	kHz	PWM_OUT pin
SID.TCPWM.3	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of overflow, underflow, and CC (counter equals compare value) outputs. Fc = System clock.

3.4.2 I²C, UART, SWD interface

Table 9 Communication interface specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Fixed I²C AC specifications							
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–
Fixed UART AC specifications							
SID16	F_{UART}	Bit rate	–	–	1	Mbps	–
SWD interface specifications							
SID.SWD#1	F_SWDCLK1	3.0V ≤ VDDIO ≤ 5.5V	–	–	14	MHz	–
SID.SWD#2	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID.SWD#3	T_SWDI_HOLD		0.25 × T		–		
SID.SWD#4	T_SWDO_VALID		–		0.50 × T		
SID.SWD#5	T_SWDO_HOLD		1		–		

3.4.3 Memory

Table 10 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.MEM#2	FLASH_WRITE	Row (block) write time (erase and program)	–	–	20	ms	–
SID.MEM#1	FLASH_ERASE	Row erase time			15.5		
SID.MEM#5	FLASH_ROW_ PGM	Row program time after erase			7		
SID178	$T_{BULKERASE}$	Bulk erase time (32KB)			35		
SID180	$T_{DEVPROG}$	Total device program time			7.5	s	
SID.MEM#6	$FLASH_{ENPB}$	Flash write endurance	100k		–	cycles	25°C < T_A < 55°C
SID182	F_{RET1}	Flash retention, T_A < 55°C, 100K P/E cycles	20			years	–
SID182A	F_{RET2}	Flash retention, T_A < 85°C, 10K P/E cycles	10				

3.5 System resources

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

3.5.1 Internal main oscillator clock

Table 11 IMO AC, clock specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
IMO AC specifications							
SID.CLK#13	F_{IMOTOL}	Frequency variation at 48 MHz (trimmed)	–2	–	+2	%	3.0V < VDDD < 5.5V
SID226	$T_{STARTIMO}$	IMO start-up time	–		7	µs	–
SID.CLK#1	F_{IMO}	IMO frequency	24		48	MHz	
External clock specifications							
SID.305	EXTCLKFREQ	External clock input frequency	–	48	–	MHz	-40°C < T_A < 105°C; 3.0 V < VDDD < 5.5 V. Tolerance ±50 ppm. External clock frequency is 49.935 MHz for MPP mode.

3.5.2 PD

Table 12 PD DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/condi-tions
SID.DC.cc_shvt.1	vSwing	Transmitter output high voltage	1.05	–	1.2	V	–
SID.DC.cc_shvt.2	vSwing_low	Transmitter output low voltage	–		0.075		
SID.DC.cc_shvt.3	zDriver	Transmitter output impedance	33		75	Ω	
SID.DC.cc_shvt.4	zBmcRx	Receiver input impedance	10		–	MΩ	
SID.DC.cc_shvt.8	Rd	Pull down termination resistance when acting as UFP	4.59		5.61	kΩ	
SID.DC.cc_shvt.10	zOPEN	CC impedance to ground when disabled	108		–		
SID.DC.cc_shvt.15	UFP_default_0 p66	CC voltages on UFP side-standard USB	0.61		0.7	V	
SID.DC.cc_shvt.16	UFP_1.5A_1p23	CC voltages on UFP side-1.5 A	1.16		1.31		
SID.DC.cc_shvt.17	Vattach_ds	Deep Sleep attach threshold	0.3		0.6	%	
SID.DC.cc_shvt.18	Rattach_ds	Deep Sleep pull-up resistor	10		50	kΩ	
SID.DC.cc_shvt.19	VTX_step	TX drive voltage step size	80		120	mV	

3.5.3 ADC

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 13 ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	-1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.3	DNL	Differential non-linearity	-2.5		2.5		Reference voltage generated from VDDD
SID.ADC.4	Gain Error	Gain error	-1.5		1.5		Reference voltage generated from bandgap
SID.ADC.5	VREF_ADC1	Reference voltage of ADC	VDDDmin		VDDDmax	V	Reference voltage generated from VDDD
SID.ADC.6	VREF_ADC2	Reference voltage of ADC	1.96	2.0	2.04		Reference voltage generated from deep sleep reference

3.5.4 Current sense amplifier (CSA) / ASK amplifier (ASK_P and ASK_N)

Table 14 CSA/ASK amplifier specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
HS CSA DC specifications							
SID.HSCSA.7	Csa_SCP_Acc1	CSA short circuit protection (SCP) at 6A with 5/10/20 mΩ sense resistor	-10	–	10	%	Active mode
SID.HSCSA.8	Csa_SCP_Acc2	CSA SCP at 10 A with 5/10/20 mΩ sense resistor	-10		10		
SID.HSCSA.9	Csa_OCP_1A	CSA OCP at 1 A with 5/10/20 mΩ sense resistor	104	130	156		
SID.HSCSA.10	Csa_OCP_5A	CSA OCP for 5A with 5/10/20 mΩ sense resistor	117	130	143		
SID.HSCSA.13	Csa_CBL_MON_Acc2	Vsense > 10 mV	–	±3.5	–		CSA sense accuracy. Active mode. 3.0 V < VDDD < 5.5 V. T_A = 25°C.
CSA AC specifications							
SID.HSCSA.AC.1	T_{SCP_GATE}	Delay from SCP threshold trip to external NFET power gate turn off	–	3.5	–	µs	1 nF NFET gate
SID.HSCSA.AC.2	$T_{SCP\_GATE\_1}$	Delay from SCP threshold trip to external NFET power gate turn off		8			3 nF NFET gate

3.5.5 VIN UV/OV

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 15 VIN UV/OV specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.UVOV.1	VTHOV1	Overvoltage threshold accuracy, 4 V-11 V	–3	–	3	%	Active mode
SID.UVOV.2	VTHOV2	Overvoltage threshold accuracy, 11 V-21.5 V	–3.2		3.2		
SID.UVOV.3	VTHUV1	Undervoltage threshold accuracy, 3 V-3.3 V	–4		4		
SID.UVOV.4	VTHUV2	Undervoltage threshold accuracy, 3.3 V-4.0 V	–3.5		3.5		
SID.UVOV.5	VTHUV3	Undervoltage threshold accuracy, 4.0 V-21.5 V	–3		3		

3.5.6 Voltage regulation - VBRG

Table 16 VBRG specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
VBRG discharge specifications							
SID.VBUS.DISC.1	R_DIS1	20V NMOS ON resistance for DS = 1	500	–	2000	Ω	Measured at 0.5 V
SID. VBUS.DISC.2	R_DIS 2	20V NMOS ON resistance for DS = 2	250		1000		
SID. VBUS.DISC.3	R_DIS 4	20V NMOS ON resistance for DS = 4	125		500		
SID. VBUS.DISC.4	R_DIS 8	20V NMOS ON resistance for DS = 8	62.5		250		
SID. VBUS DISC.5	R_DIS 16	20V NMOS ON resistance for DS = 16	31.25		125		
SID. VBUS.DISC.6	VBRG_stop_error	Error percentage of final VBRG value from setting	–		10	%	When VBRG is discharged to 5 V
Voltage regulation DC specifications							
SID.DC.VR.1	VBB	VBB output voltage range	3.0	–	22	V	–
SID.DC.VR.2	VR	VBB voltage regulation accuracy	–5	±3	+5	%	
SID.DC.VR.3	VIN_UVLO	VIN supply below which chip will get reset	1.7	–	3.0	V	
SID.VREG.1	TSTART	Total startup time for the regulator supply outputs	–		200	µs	Specification for VDDD LDO

3.5.7 NFET gate driver specifications

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 17 NFET gate driver specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
NFET gate driver DC specifications							
SID.GD.1	GD_VGS	Gate to source overdrive during ON condition	4.5	5	10	V	NFET driver is ON
SID.GD.2	GD_RPD	Resistance when pull-down enabled	–	–	2	kΩ	Applicable on NFET_CTRL to turn off external NFET.
NFET gate driver AC specifications							
SID.GD.3	T_{ON}	NFET_CTRL Low to High (1V to VBUS + 1V) with 3nF external capacitance.	2	5	10	ms	VBUS = 5V
SID.GD.4	T_{OFF}	NFET_CTRL High to Low (90% to 10%) with 3nF external capacitance.	–	7	–	µs	VBUS = 21.5V

3.5.8 Buck-boost PWM controller

Table 18 PWM controller specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
PWM controller specifications							
PWM.1	FSW	Buck-boost switching frequency	150	–	600	kHz	–
GD1	Fsw Gd Ovr	Inverter switching frequency	85		600		Pins PWM_IN1 and PWM_IN2 are connected to pin PWM_OUT.
PWM.2	FSS	Spread spectrum frequency dithering span	–	10	–	%	–
Buck-boost gate driver specifications							
DR.1	R_HS_PU	Top-side gate driver on-resistance - gate pull-up	–	2	–	Ω	–
DR.2	R_HS_PD	Top-side gate driver on-resistance - gate pull-down		1.5			
DR.3	R_LS_PU	Bottom-side gate driver on-resistance - gate pull-up		2			
DR.4	R_LS_PD	Bottom-side gate driver on-resistance - gate pull-down		1.5			
DR.5	Dead_HS	Dead time before high-side rising edge		30		ns	
DR.6	Dead_LS	Dead time before low-side rising edge		30			
DR.7	Tr_HS	Top-side gate driver rise time		25			
DR.8	Tf_HS	Top-side gate driver fall time		20			
NFET gate driver specifications							
DR.9	Tr_LS	Bottom-side gate driver rise time	–	25	–	ns	–
DR.10	Tf_LS	Bottom-side gate driver fall time		20			

3.5.9 Thermal

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 19 Thermal specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.OTP.1	OTP	Thermal shutdown	120	125	130	°C	–

4 Functional overview

4.1 Wireless power transmitter

WLC1125 supports wireless power transfer between power transmitter (TX) and power receiver (RX), based on inductive power transfer technology (IPT). The Tx runs an alternating electrical current through the Tx coil(s) to generate an alternating magnetic field in accordance with Faraday's law. This magnetic field is mutually coupled to the Rx coil inside the power receiver and is transformed back into an alternating electrical current that is rectified and stored on a Vrect capacitor bank to power the Rx load.

Before the power transfer begins, the Rx and Tx communicate with each other to establish that a valid Rx device has been placed and they negotiate the level of power to be transferred during the charging cycle. The digital communication used by Tx and Rx is in-band communication. The communication from Tx to Rx is frequency shift key (FSK) modulation and from Rx to Tx is amplitude shift key (ASK) modulation. The WLC1125 enables solutions for Qi2.x standard up to 25 W. The WLC1125 operates in MPP, EPP, or BPP depending on the capabilities of the Rx that gets placed by the user.

WLC1125 offers a highly integrated wireless power transmitter solution with a USB Type-C PD controller following the Qi2.x standard[8]. The functional overview below covers MPP, EPP, and BPP as per Qi2.x.

4.2 MPP WPC system control

The receiver in MPP works in either Restricted mode or Full mode.

- Restricted mode operates with one-way communication (PRx-PTx), limited to 5W power using the Qi baseline protocol at an operating frequency of 360 kHz, with no negotiation
- MPP Full mode enables bi-directional communication, allowing negotiation of power contracts up to 25 W. It supports complex operations like identification exchange, capability sharing, power negotiation, and authentication, allowing for higher power levels

MPP receiver in Restricted mode can switch to Full mode to start communication and request higher power.

The WPC system control flowchart for MPP is shown in the following **Figure 4**.

Notes

8. Factory default controllers include boot-loader only. For code examples, contact your local Infineon sales representative.

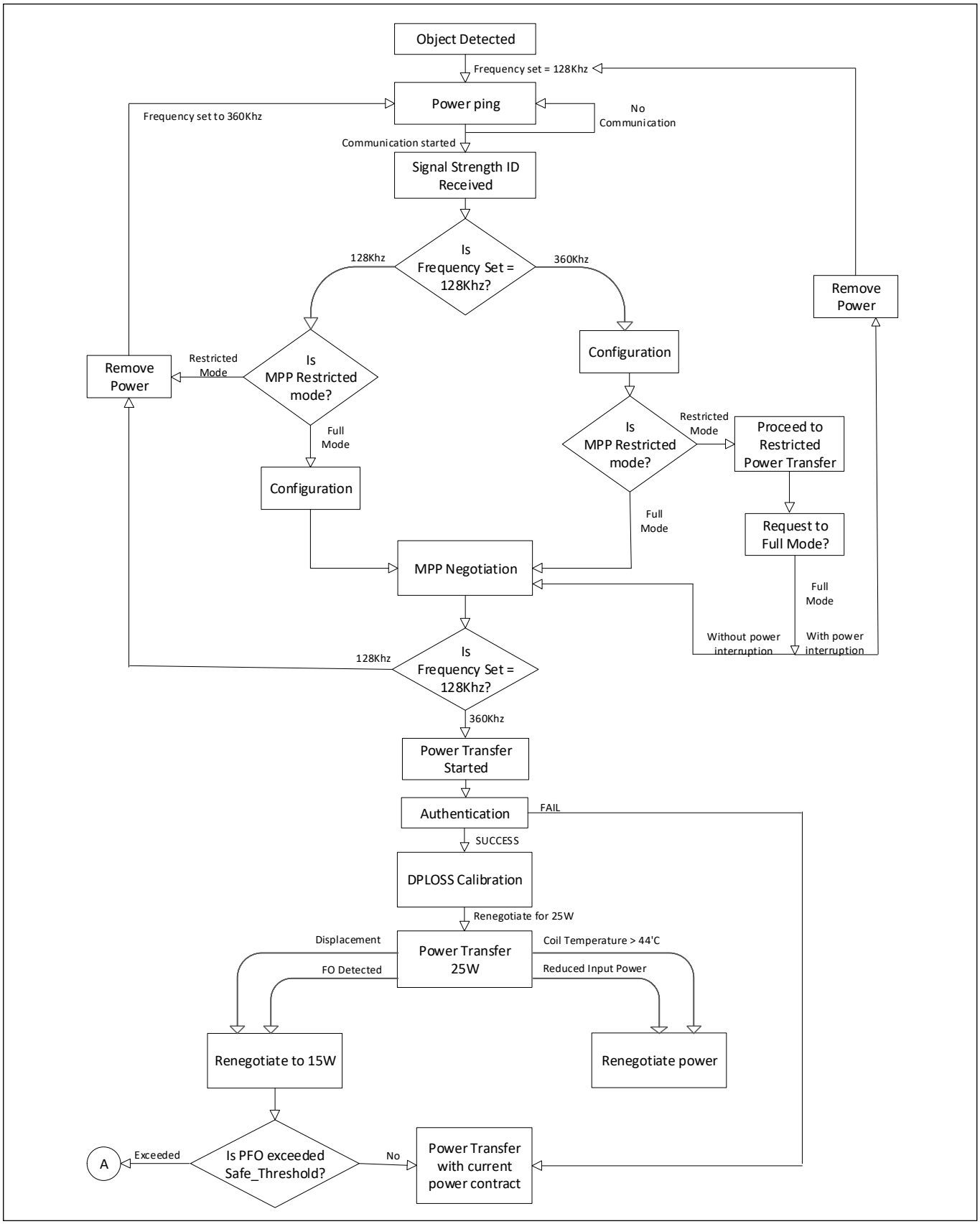


Figure 4 WPC system control flow chart for MPP

4.2.1 Power throttling

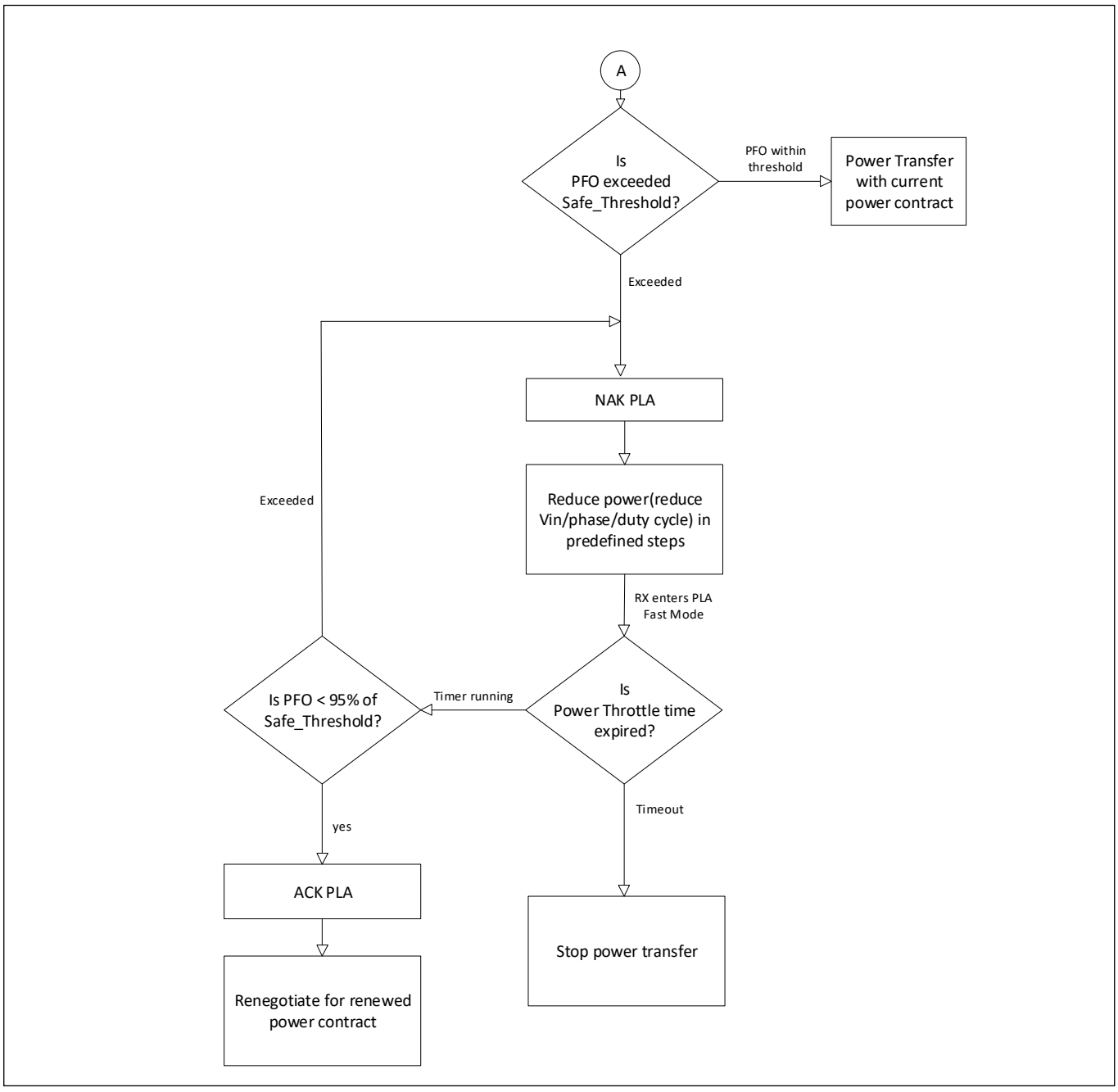


Figure 5 Power throttling

Power throttling is initiated when the transmitter detects that the calculated power loss (PFO) exceeds the safe threshold of 380 mW. The system reduces power in several steps and power reduction is time aligned with a PLA packet. Power Throttling continues until the PFO drops below 95% of the safe threshold, at which point an ACK is sent to exit the power throttle state and a new contract will be created based on the new power equilibrium. Power throttling exceeding the Throttle timeout results in power termination.

4.2.2 Cloaking

Cloaking lets a wireless charging system to pause active power transfer while still maintaining a PTx-PRx link such that power transfer can be resumed any time without going through the entire start up flow and power negotiation stages.

Power pause/cloak may be used in scenarios such as NFC scan by the power receiver, Thermal management or Environmental reasons such as power savings at end of charge.

4.2.3 Additional features supported by WLC1125

- Open air Q FOD
- MatedQ FOD
- K-Estimation
- MPLA2 FOD
- FOD Delta PLOSS calibration
- Power modes
- Gain linearization

See MPP Qi2.x specification for more information.

4.3 EPP WPC system control

WLC1125 controls the wireless power system in compliance with Qi standard version 2.x. The system control covers power transfer, system monitoring, and various phases of operation under BPP or EPP receivers depending on the Rx type placed onto the Tx pad.

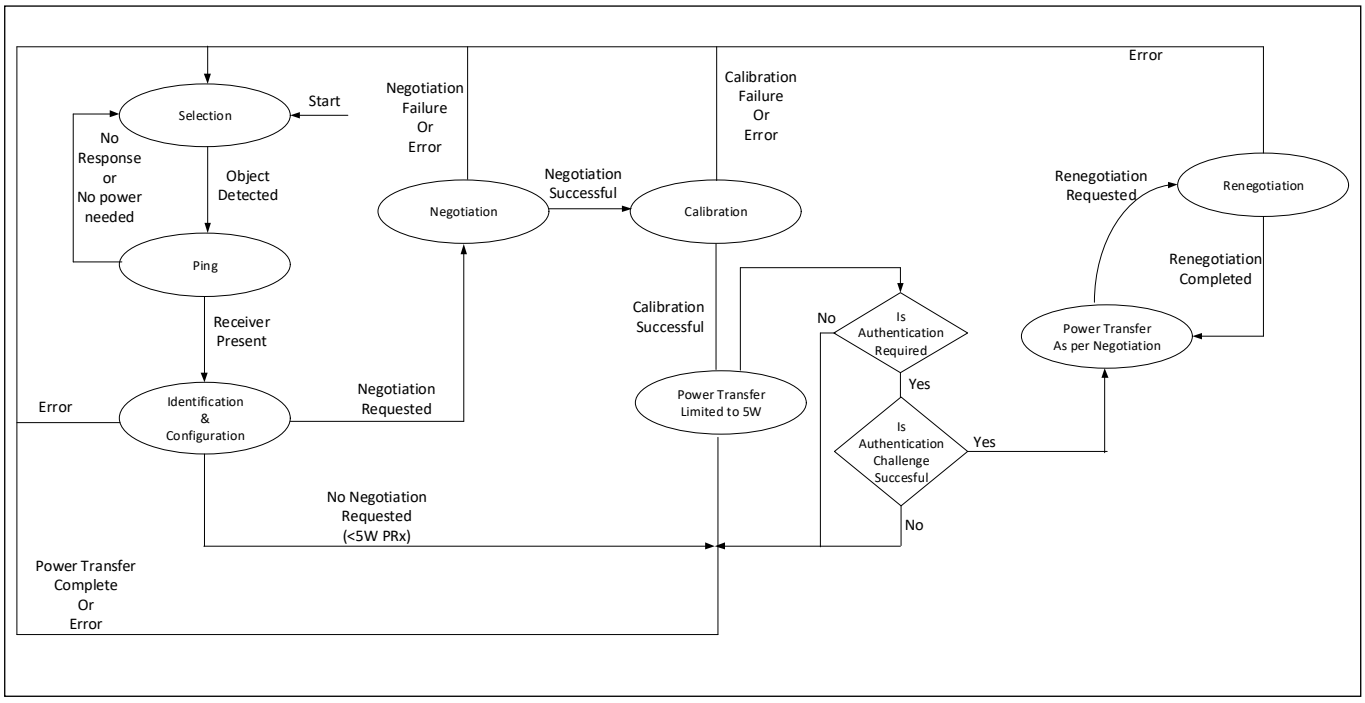


Figure 6 WPC system control flow chart (negotiation, calibration and authentication are for EPP only)[9]

Notes

9. The **Functional overview** section only describes the Qi specification. However, IC can support wireless charging proprietary power delivery extensions (PPDE)/Samsung FC.

4.3.1 EPP selection phase

The Tx monitors the interface surface using low energy signals (analog ping or Q-factor) to detect objects' placement and removal. The Analog Ping energy is limited such that impedance changes above the Tx coil may be detected without powering or waking up the receiver. The WLC1125 sets the Bridge (VBRG) voltage powering the inverter to a low voltage to generate sufficient energy to measure for any interface impedance changes without transferring any power during the selection phase.

4.3.2 EPP digital ping phase

In this phase, the Tx sends a power signal that is sufficient to power the receiver and prompt a response. This signal is called Digital Ping and the magnitude and length of time are predefined by the WPC Tx specifications. The Digital Ping phase ends when no response is detected or the Rx responds with a signal strength packet (SSP). When the Tx receives a valid SSP, the Digital Ping is extended and the system proceeds to the Identification and Configuration phase.

4.3.3 EPP identification and configuration phase

In this phase, the Tx identifies whether the Rx belongs to BPP or EPP profile. Additionally, in this phase, the Tx obtains configuration information such as the maximum amount of power that the Rx may require at its output. The power transmitter uses this information to create a Power Transfer Contract.

If the receiver is a BPP type then the power transmitter enters into the power transfer phase at the completion of the ID and Config phase as shown in **Figure 10** or with EPP receivers it proceeds to the negotiation phase if requested by the Rx.

4.3.4 EPP negotiation

In this phase, the EPP power receiver negotiates with the power transmitter to fine-tune the power transfer contract. For this purpose, the power receiver sends negotiation requests to the power transmitter, which the power transmitter can grant or deny.

In compliance with Q-factor FOD, the Tx will compare the Q-factor reported by the Rx with its own measurement to determine if the Q-factor of the coil is appropriate for the Rx that has been placed (EPP only). If the Tx Q-factor reading is too low it will flag a QFOD alarm and return to the selection phase.

4.3.5 EPP calibration

When this phase is requested, the Tx will ACK the request and commence with the EPP Rx to enable and enter the calibration phase to calibrate for transmitter power losses at two fixed receiver loads. This system’s power loss information will be used by the Tx to detect the presence of foreign objects on the interface surface during the power delivery phase.

4.3.6 EPP authentication

Post successful calibration, Tx enters into power transfer mode limited to 5W. In this mode, Rx can request and challenge Tx for authentication. In case of successful authentication, Tx proceeds with negotiated power delivery. If authentication challenge is not successful then Tx continues to be in power transfer mode, limited to 5 W. WLC1125 provides an I^2C port for interfacing with Authentication IC to enable authentication.

4.3.7 EPP renegotiation phase

In this phase, the EPP Rx can request to adjust the power transfer contract. This phase may be aborted prematurely without changing the power transfer contract.

4.3.8 EPP power transfer phase

In this phase, the Tx transfers power to the Rx and the power level is determined by the control error packets (CEP) and limited by the guaranteed power contract. Power loss FOD is also enabled and utilized to prevent excessive power loss which could result in FO heating.

1. CEP: These packets are used by the Tx to adjust the amount of power being sent. The CEP may be positive, negative, or 0. The Tx adjusts its operating point based on the value of the CEP. The CEP packet must be received every 1.8 s (configurable) or power will be withdrawn along with other constraints that specify when a CEP may be sent by the Rx as defined in the WPC specifications.
2. Received power packet (RPP): The packet (8 bits for BPP and 24 bits for EPP) contains power received by receiver. The RPP is used by the Tx to determine if the power loss is safe or excessive based on the FOD thresholds contained in the FW.
3. End power transmit (EPT): The Rx may send an EPT packet anytime to inform Tx to withdraw/terminate the power delivery. The Tx will end the power transfer immediately if an EPT packet is received.

The Rx and Tx communicate with each other by modulating the carrier wave used to transfer power. The following sections describe the communication layer used and defined by the WPC.

4.3.9 Bidirectional in-band communication interface

The Qi standard requires bi-directional in-band communication between Tx and Rx. The communication from Tx to Rx is FSK and is implemented by the Tx alternating the carrier wave frequency. The communication from Rx to Tx is ASK and is created by modulating the load on the Rx side causing a reflection to appear on the Tx which is filtered and decoded.

4.4 Communication from Tx to Rx – FSK

The power transmitter communicates to the power receiver using frequency shift keying, in which the power transmitter modulates the operating frequency of the power signal.

In FSK, the Tx changes its operating frequency between the current operating frequency (f_{OP}) to an alternate frequency (f_{MOD}) in the modulated state. The difference between these two frequencies is characterized by two parameters that are determined during the initial ID and config stage of the wireless power connection:

- Polarity: This parameter determines whether the difference between f_{MOD} and f_{OP} is positive or negative
- Depth: This parameter determines the magnitude of the difference between f_{OP} and f_{MOD} in Hertz (Hz)

The Tx uses a differential bi-phase encoding scheme to modulate data bits to the carrier wave. For this purpose, the Tx aligns each data bit to segments of 64/128/256/512 cycles of the carrier wave frequency.

4.4.1 FSK bit encoding scheme

The power transmitter aligns each data bit to the number of cycles (NCYCLE) contained in the power transfer contract (default 512 cycles).

EPP receiver could request the transmitter to align the data bit with any of the following NCYCLE count. The MPP receiver will stick to 128 cycle count for bit alignment. The MPP receiver doesn't follow the variable bit alignment scheme.

WLC1125 can support EPP and MPP receiver requirements.

Table 20 FSK bit alignment

FSK bit alignment scheme	Bit alignment cycles (NCYCLES)	Half-bit alignment cycle (NCYCLE/2)
FSK_512 (Default)	512	256
FSK_256	256	128
FSK_128 (MPP)	128	64
FSK_64	64	32

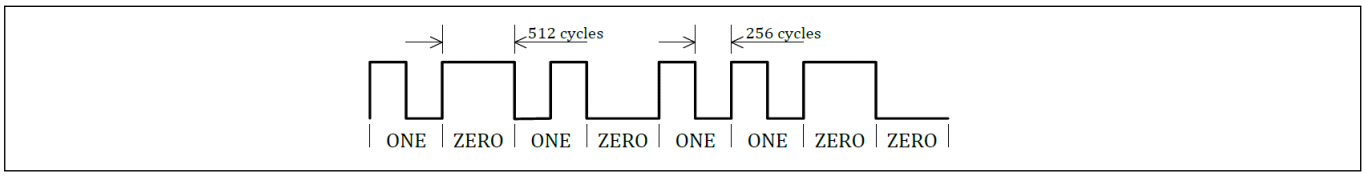


Figure 7 Example of differential bi-phase encoding - FSK

4.5 Communication from Rx to Tx - ASK

In the ASK communication scheme, the Rx modulates the amount of power that it draws from the Tx power signal. The Tx detects this through as a modulation of the Tx current and/or voltage and uses a demodulation scheme to convert the modulated signal into a binary signal.

The Rx uses a differential bi-phase encoding scheme to modulate data bits onto the power signal. For this purpose, the power receiver shall align each data bit to a full period t_{CLK} of an internal clock signal, such that the start of a data bit coincides with the rising edge of the clock signal. This internal clock (INTCLK) signal shall have a frequency fCLK = 2 kHz ±4%. tCLK is time period of the INTCLK clock.

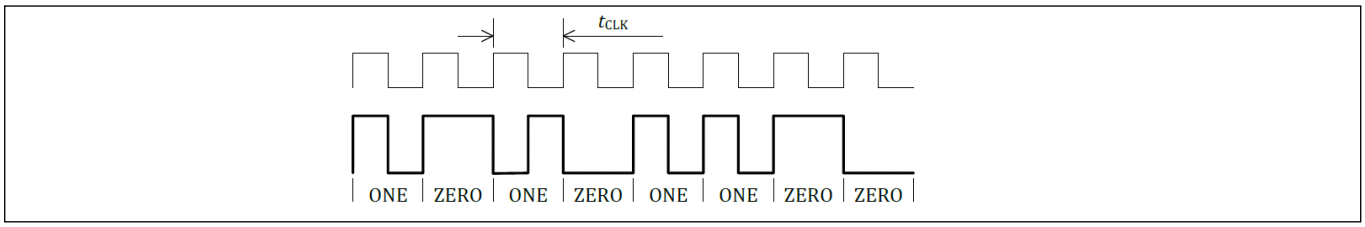


Figure 8 Example of differential bi-phase encoding - ASK

When the Tx receives a modulated signal from the Rx the information is decoded and the Tx will react to the packet according to the type and the WPC specification.

4.6 Demodulation

The WLC1125 ASK demodulating and decoding scheme works by detecting voltage and current variations in the Tx coil caused by the Rx modulation signal. The voltage path for ASK uses an external band pass filter to filter the demod signal out of the carrier wave. The current sense uses the bridge current sense resistor and an integrated differential amplifier to sense the ASK variations. Both ASK sensing paths can be multiplexed to the external Opamp filter and comparator to improve communication in low signal-to-noise environments or conditions.

Figure 9 shows the demodulation path used for current and voltage sensing of the modulation signal for packet decoding.

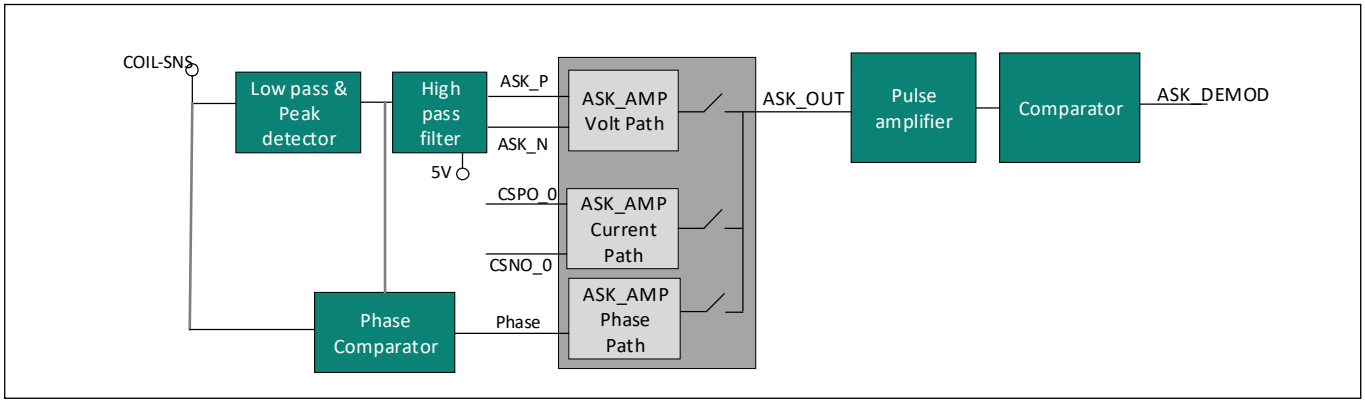


Figure 9 WLC1125 voltage and current demodulation path for ASK

4.7 Inverter configuration for EPP

The WLC1125 uses the integrated buck controller to generate the bridge voltage used to power the full-bridge inverter that powers the Tx resonance tank to deliver power to the Rx. The inverter supports a wide input operating voltage range (3 V to 22 V) for power transfer. The integrated gate drivers of the WLC1125 are designed to control a full bridge or half-bridge Inverter depending on the WPC specification type and operating scenario. The inverter is capable of operating at switching frequencies between 85 kHz and 600 kHz but are typically limited to 110 kHz to 148 kHz. During the power transfer phase, the inverter responds to Rx CEP packets by adjusting the operating frequency or adjusting the bridge voltage. The power control method (variable voltage or variable frequency) is determined by the WPC specification but may be altered in order to promote better interoperability and user experience.

4.8 Rx detection

During the selection phase, the Tx will periodically poll the interface to detect impedance changes in order to quickly send a digital ping within 0.5 s of a user placing an Rx. During this phase, the WLC1125 is able to distinguish between large ferrous objects (such as keys or coins) and regular Rx devices using Q factor, input current, or shifts in resonance frequency to attempt FOD before power transfer. In case of marginally high input current or resonance shifts, the Tx will commence to digital ping in order to guarantee a connection with a valid Rx is made in a timely manner. The typical sequence of operations used to scan the interface for Rx placement (or removal if an EPT is received during power transfer) is shown in **Figure 10**.

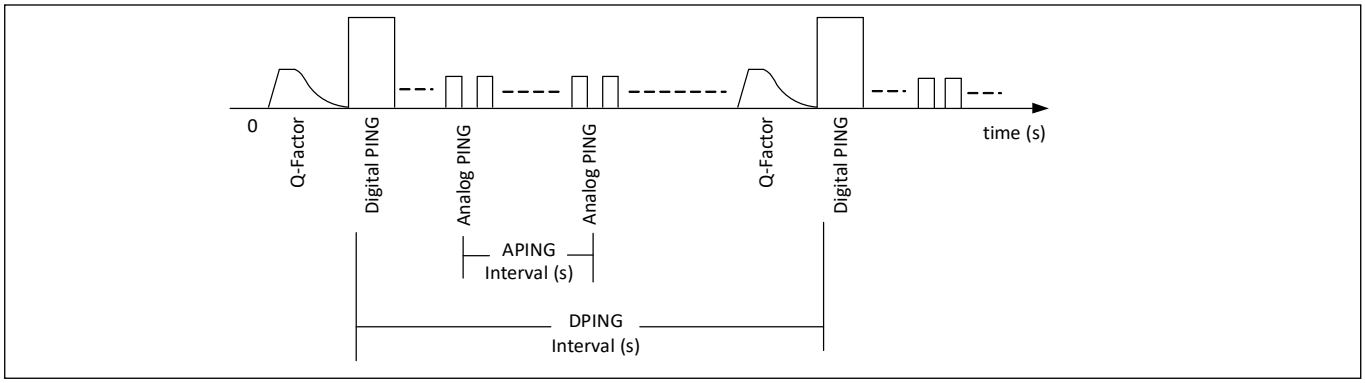


Figure 10 Typical selection phase Rx detection timing diagram

Figure 11 describes the process used during the selection phase for quick Rx detection and connection.

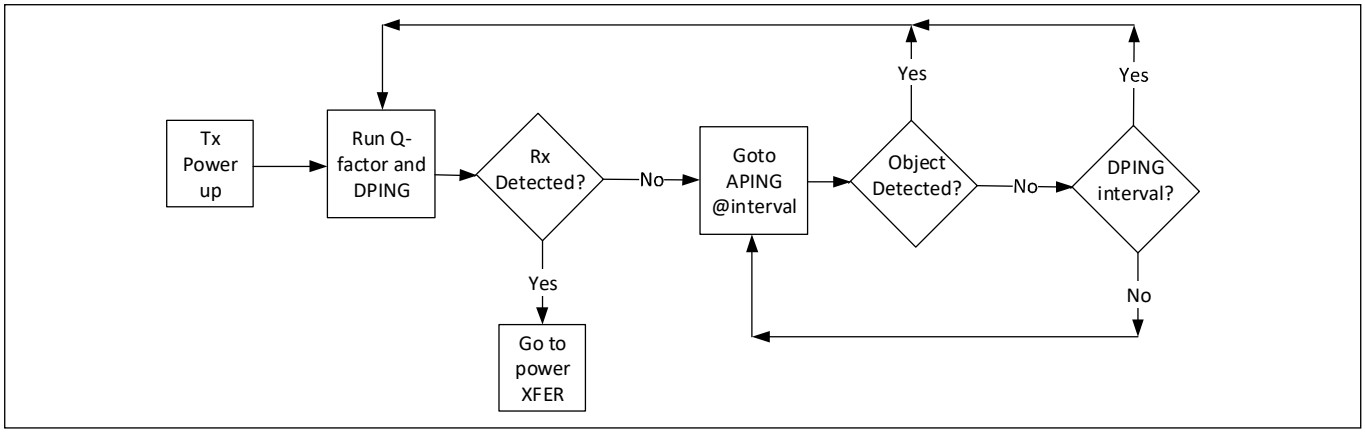


Figure 11 Typical selection phase flow chart for Rx detection and connection

The Rx detection in **Figure 11** also covers foreign object detection. The foreign object is identified by using Q factor. In case of foreign object detection, the process flow proceeds to analog ping (APNG). Further details about foreign object detection is covered in **Foreign object detection (FOD)**.

4.8.1 Foreign object detection (FOD)

WLC1125 supports enhanced FOD as per Qi2.x. This includes FOD based on Q factor, resonance frequency, power loss, and overtemperature (if a thermistor is used).

4.8.2 Q factor FOD and resonance frequency FOD

WLC1125 offers integrated Q factor and resonance frequency measurements for QFOD pre-power delivery. The measurements are made using the internal comparators QCOMP1 and QCOMP2 and the simple external components to charge the resonance capacitor and then discharge by shorting the LC tank and observing the resulting oscillation and voltage decay. The measurement of the Q factor is performed directly before every digital ping. The number of cycle count 'N' between two coil voltages V1 and V2 and period between corresponding rising edge pulses are used for Q factor and resonance frequency measurement as shown in **Figure 12**.

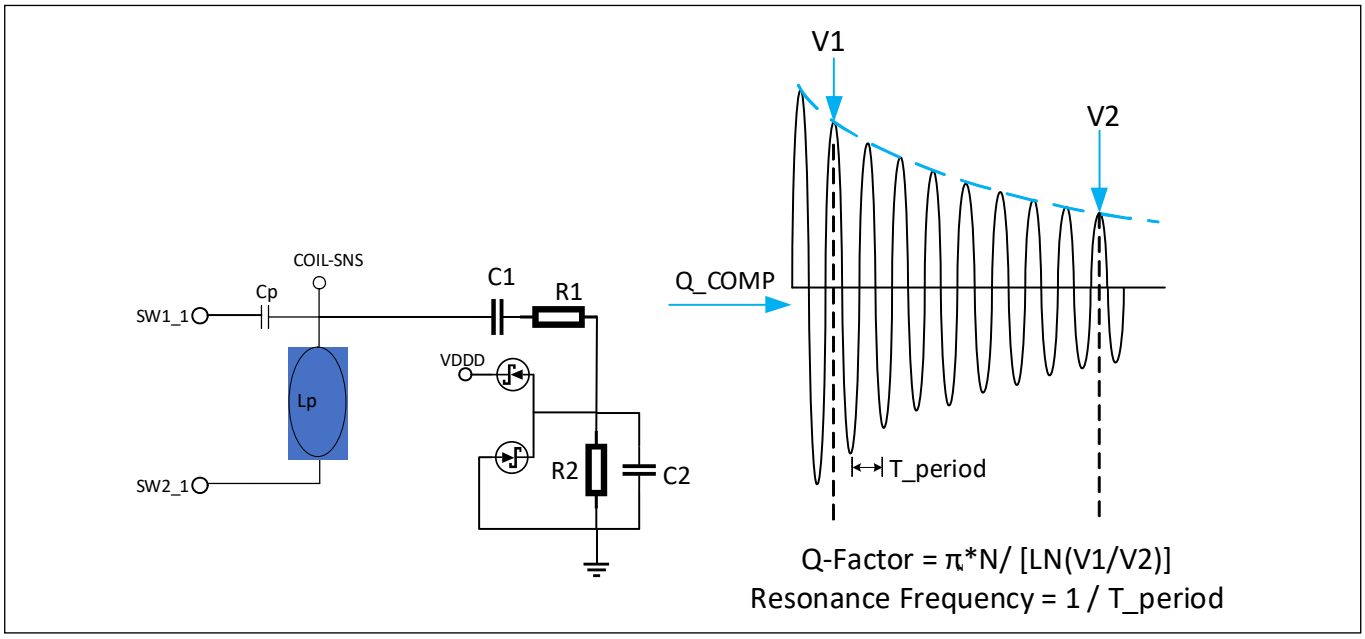


Figure 12 WLC1125 Q factor measurement schematic and signal

4.8.3 Power loss FOD

WLC1125 supports power loss FOD during power transfer. The power loss FOD uses the Tx power measured at the buck output and is the product of the bridge voltage and the bridge current (current is sensed at inputs CSPO_0 and CSNO_0). This result for Tx power is further adjusted by tuning FOD coefficients to account for inverter losses and friendly metal losses. After computing the calibrated Tx power the result is compared against the latest RPP value sent by the Rx. If the difference between Tx_Power_Calibrated and RPP exceeds the Ploss threshold then an FOD event is logged. To prevent erroneous disconnects and improve user experience the WLC1125 will only disconnect the power for Ploss FOD in the event that three consecutive Ploss threshold breaches occur. The FOD coefficients and the Ploss thresholds are configurable to adapt to the system design.

4.8.4 Overtemperature FOD

The WLC1125 is able to monitor interface temperature if an external NTC thermistor is connected and placed in contact with the Tx coil. This can be enabled to disconnect the Tx from the Rx in the event that the Tx coil temperature exceeds a configurable threshold.

4.8.5 Buck-boost regulator

The buck-boost regulator powers the inverter at the input node VBRG to enable power transfer per Qi. The buck-boost regulator of WLC1125 requires input and output bypass capacitors as well as two FETs and an inductor. The necessary external components and connections are shown in **Figure 13**. The buck-boost also offers current protection using a cycle-by-cycle current sense amplifier connected across resistance CSR1, integrated high and low-side gate drivers, and automatic PWM generation for output voltage control. The effective capacitance and inductor have been deliberately selected to optimize buck-boost performance and any substitutions should be made using equivalent components as those found in the reference schematic and using hardware design guidelines.

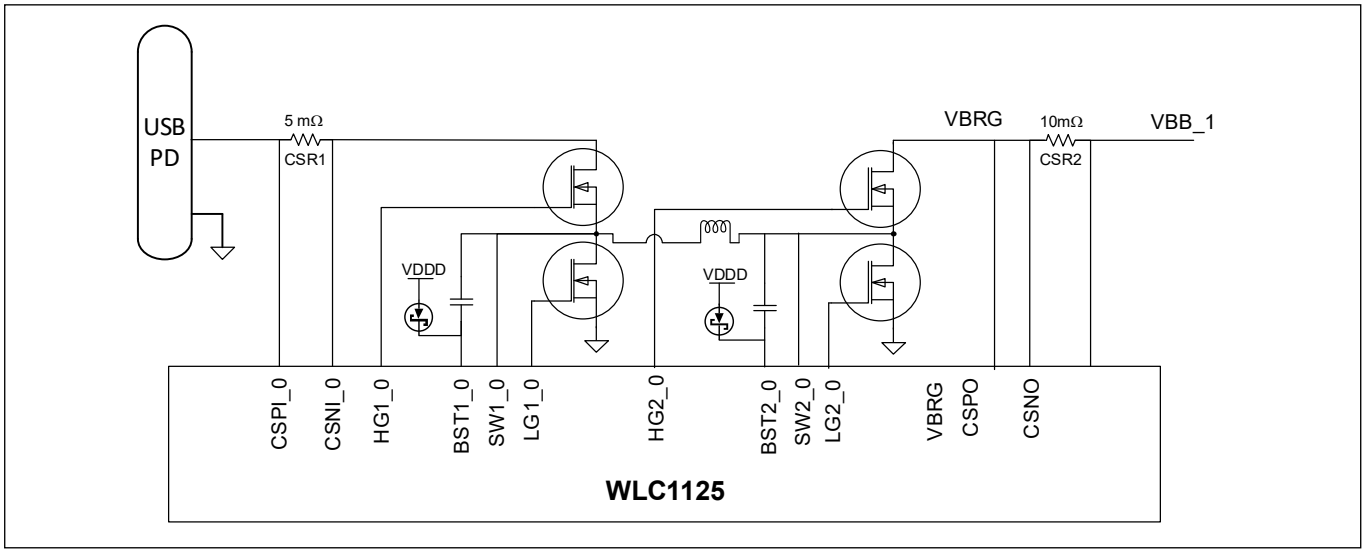


Figure 13 WLC1125 typical buck-boost regulator schematic for VBRG generation

The WLC1125's buck-boost controller provides two N-channel MOSFET gate drivers: complete with a floating high-side gate drivers via HG1_0 and HG2_0, and a ground-referenced low-side driver via LG1_0 and LG2_0 pins. The gate drivers are powered by VDDD and are a nominal voltage of 5 V. The buck-boost regulator switching frequency is programmable and can be set between 150 kHz and 600 kHz. In order to prevent EMI related issue's gate drivers, have programmable drive strength, dead-time, and can be run in a dithering mode to spread the radiated spectrum energy levels. An external capacitor and Schottky diode from the BST1_0 and BST2_0 pins are used for the high-side gate drive power supply. Furthermore, the high and low-side gate driver blocks include zero-crossing detector (ZCD) to implement discontinuous-conduction mode (DCM) mode with diode emulation.

The WLC1125's buck-boost controller uses an integrated error amplifier for output voltage regulation. The error amplifier is a trans-conductance type amplifier with a single compensation pin (COMP_0) which requires the RC filter shown in the reference schematic to be connected from this pin to GND.

The WLC1125 supports high-voltage (22V) VBRG discharge circuitry and upon detection of device disconnection, faults, or hard resets, the chip may discharge the VBRG node to vSafe5V and/or vSafe0V within the time limits specified in the USB PD specification.

4.9 Buck-boost operating modes

4.9.1 Pulse-width modulator (PWM)

The WLC1125 has a PWM generator to control the external FETs using the integrated gate drivers in peak current mode control. This is the primary operating mode when the buck-boost is loaded by the inverter and power transfer is in progress.

4.9.2 Pulse skipping mode (PSM)

The WLC1125 buck-boost has two firmware-selectable operating modes to optimize efficiency and reduce losses under light load conditions: Pulse-skipping mode (PSM) and forced-continuous-conduction mode (FCCM). In PSM, the controller reduces the total number of switching pulses without reducing the active switching frequency by working in “bursts” of normal nominal-frequency switching interspersed with intervals without switching. The output voltage thus increases during a switching burst and decreases during a quiet interval. This mode results in minimal losses with a tradeoff of having higher output voltage ripple. When in this mode, WLC1125 devices monitor the voltage across the buck-boost sync FET to detect when the inductor current reaches zero; when this occurs, the WLC1125 devices switch off the buck-boost sync FET to prevent reverse current flow from the output capacitors (i.e., diode emulation mode).

4.9.3 Forced-continuous-conduction mode (FCCM)

In forced-continuous-conduction mode (FCCM), the nominal switching frequency is maintained at all times, with the inductor current going below zero (i.e., “backwards” or from the output to the input) for a portion of the switching cycle as necessary to maintain the output voltage and current. This keeps the output voltage ripple to a minimum at the cost of light-load efficiency.

4.9.4 Overvoltage protection (OVP)

The WLC1125 offers two types of overvoltage protections. The device monitors and limits VIN and VBRG. In case of a USB VIN overvoltage event detected, WLC1125 can be configured to shutdown the Type-C port completely. In case of VBRG over voltage events, the buck-boost regulator is immediately shut down. The IC can be re-enabled after a physical disconnect and reconnect. The over-voltage fault thresholds are configurable.

4.9.5 Overcurrent protection (OCP)

The WLC1125 protects the inverter from over-current and short-circuit faults by monitoring the bridge current and continuously inspecting for over-current events using the internal CSAs that check the voltage on the current sense resistor. Similar to OVP, the OCP and SCP fault thresholds and response times are configurable as well. The IC can be re-enabled after a physical disconnect and reconnect.

4.9.6 USB-PD controller

The WLC1125 interfaces directly to Type-C USB power supplies and travel adaptors (TA). The WLC1125 manages the incoming power supply throughout operation using the D+, D-, and CC lines. The WLC1125 manages the USB-PD physical communication layer, the VCONN switches, as well as monitoring to prevent under-voltage events caused by drawing too much power from the supply. The WLC1125 offers all the necessary electrical controls to be fully compliant with revisions 3.0 and 2.0 of the USB-PD specification and includes SCP.

The USB-PD physical layer consists of the power transmitter and power receiver that communicates BMC encoded data over the CC channel per the PD 3.0 standard. All communication is half-duplex. The physical layer or PHY includes collision avoidance to minimize communication errors on the channel. The WLC1125 uses the RP and RD resistors to implement connection detection and plug orientation detection. The RD resistor establishes the role of the transmitter system as a USB sink. The device supports PPS operation at all valid voltages from 3V to 22V when connected to a power adaptor.

Further, the WLC1125 device supports USB-PD extended messages containing data of up to 260 bytes by implementing a chunking mechanism; messages are limited to revision 2.0 sizes unless both source and sink confirm and negotiate compatibility with longer message lengths.

4.9.7 MCU

The Cortex®-M0 in WLC1125 device is a 32-bit MCU, which is optimized for low-power operation with extensive clock gating. The device utilizes an interrupt controller (the NVIC block) with 32 interrupt inputs and a wakeup interrupt controller (WIC), which can wake the processor up from Deep Sleep mode. Additionally, the WLC1125 device has 128-KB Flash and 32-KB ROM for nonvolatile storage. ROM stores libraries for device drivers such as I^2C, SPI, and so on. The main wireless power firmware is stored in Flash memory to provide the flexibility to store code for all wireless power features, enable the use of configuration tables, and allow firmware upgrades to meet the latest USBPD specifications and application requirements. The device may be reset anytime by toggling the XRES pin to force a full hardware and software reset.

The WLC1125 devices support external clock (EXTCLK) or INTCLK for the MCU and all internal sub-systems that require clocks. To use the internal clock, float the CLK_IN pin. To use the optional external clock, provide a single ended clock to the CLK_IN pin oscillating at 48 MHz.

The TCPWM block of the WLC1125 device has four timers, counters, or PWM (TCPWM) generators. These timers are used by FW to run the wireless power Tx system as required by WPC and USB compliance directives. The WLC1125 device also has a watchdog timer (WDT) that can be used by FW for various timeout events.

4.9.8 ADC

The WLC1125 device has 8-bit SAR ADCs available for general purpose analog-to-digital conversion applications within the chip and system. The ADCs are accessed from the GPIOs or directly on power supply pins through an on-chip analog mux. See the **Electrical specifications** for detailed specifications of the ADCs.

4.9.9 Serial communications block (SCB)

The WLC1125 devices have four SCB blocks that can be configured for I^2C, SPI, or UART. These blocks implement full multi-master and slave I^2C interfaces capable of multi-master arbitration. I^2C is compatible with the standard Philips I2C specification V3.0. These blocks operate at speeds of up to 1Mbps and have flexible buffering options to reduce interrupt overhead and latency for the CPU. The SCB blocks support 8-byte deep FIFOs for Receive and Transmit to decrease the time needed to interface by the MCU also reducing the need for clock stretching caused by the CPU not having read data on time.

4.9.10 I/O subsystem

The WLC1125 devices have 13 GPIOs but many of them have dedicated functions for 25 W MPP/EPP applications such as I2C comm, mux selector (MUX_SEL), and temperature sensing in the wireless power application and cannot be repurposed. The GPIOs output states have integrated controls modes that can be enabled by FW which include: weak pull-up with strong pull-down, strong pull-up with weak pull-down, open drain with strong pull-down, open drain with strong pull-up, strong pull-up with strong pull-down, disabled, or weak pull-up with weak pull-down and offer selectable slew rates for dV/dt output control. When GPIOs are used as inputs they can be configured to support different input thresholds (CMOS or LVTTL).

During POR, the GPIO blocks are forced to the disable state preventing any excess currents from flowing.

4.9.11 LDOs (VDDD and VCCD)

The WLC1125 has two integrated LDO regulators. The VDDD LDO is powered by VIN and provides 5V for the GPIOs, gate drivers, and other internal blocks. The total load on VDDD LDO must be less than 150 mA including internal consumption. VDDD LDO will be externally loaded as shown in the reference schematic. For connecting any additional external load on it, contact Infineon technical support. The VDDD 5V supply is externally routed to various pins and they should all be externally shorted together. The VCCD LDO is a 1.8 V LDO regulator and is powered by VDDD. Do not externally load VCCD. Both LDOs must have ceramic bypass capacitors placed from each pin to ground close to the WLC1125 device.

5 Programming the WLC1125 device

There are two ways to program application firmware into a WLC1125 device:

- Programming the device flash over SWD Interface
- Application firmware update over specific interfaces (CC, I^2C)

Generally, the WLC1125 devices are programmed over the SWD interface only during development or during the manufacturing process of the end-product. Once the end-product is manufactured, the WLC1125 device application firmware can be updated via the appropriate bootloader interface. Infineon strongly recommends customers to use the configuration utility to turn off the Application FW Update over CC or I^2C interface in the firmware that is updated into WLC1125's flash before mass production. This prevents unauthorized firmware from being updated over the CC interface in the field. If you desire to retain the application firmware update over CC/I^2C interfaces features post-production for on-field firmware updates, contact your local Infineon sales representative for further guidelines.

5.1 Programming the device Flash over SWD interface

The WLC1125 family of devices can be programmed using the SWD interface. Infineon provides the MiniProg4 programming kit (**CY8CKIT-005 MiniProg4 Kit**) which can be used to program the flash and debug firmware. The Flash is programmed by downloading the information from a hex file.

As shown in **Figure 14**, the SWD_DAT and SWD_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the device can be powered by the host programmer by connecting its VTARG (power supply to the target device) to the VDDD pins of the WLC1125 device. If the WLC1125 device is powered using an onboard power supply, it can be programmed using the "Reset Programming" option. For more details, see the WLCXXXX programming specification.

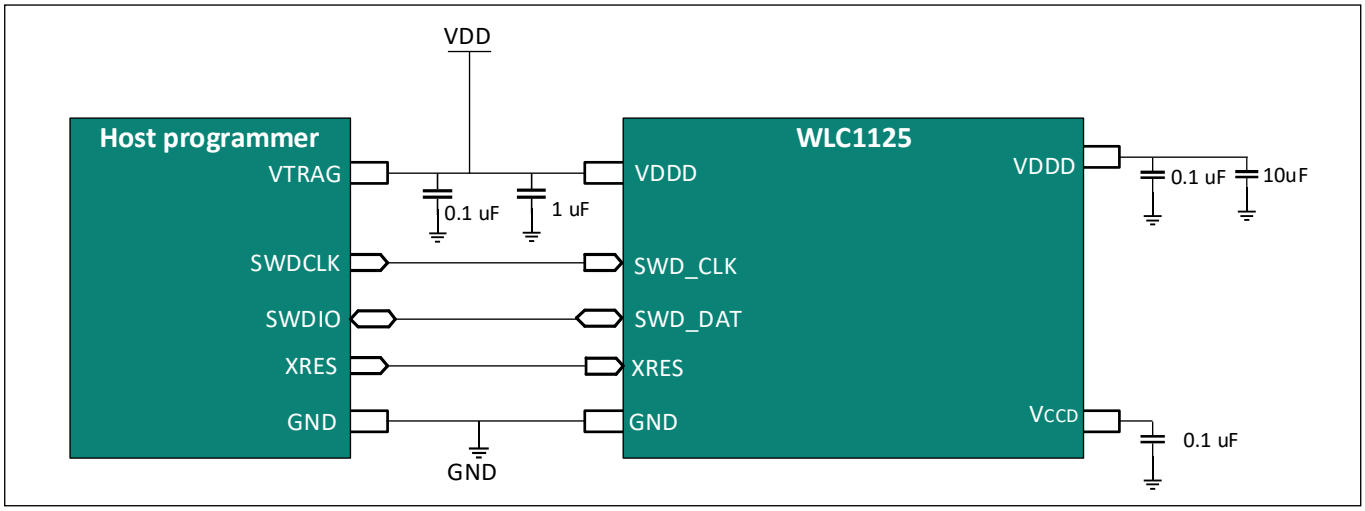


Figure 14 Connecting the programmer to WLC1125

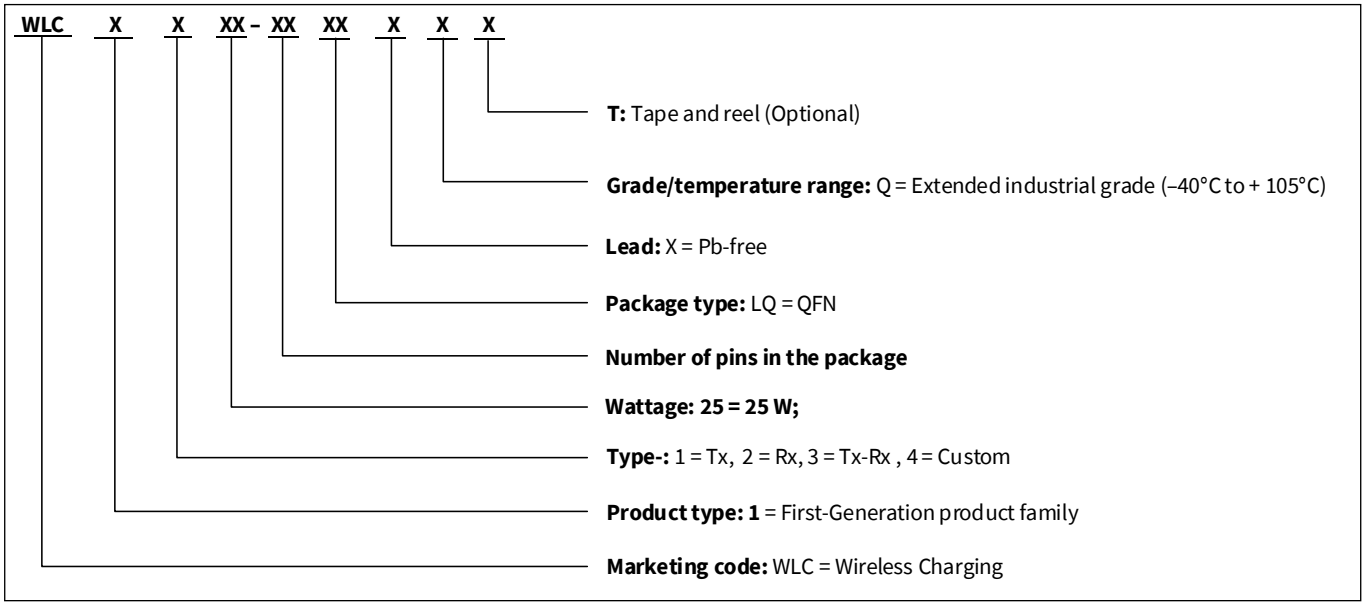
6 Ordering information

Table 21 lists the WLC1125 ordering part numbers and applications.

Table 21 WLC1125 ordering information

Product	Power	Application
WLC1125-68LQXQ	25 W	Qi2.x MPP/EPP Tx
WLC1125-68LQXQT		Qi2.x MPP/EPP Tx - Tape and reel option

6.1 Ordering code definitions



7 Packaging

Table 22 Package characteristics

Parameter	Description	Test conditions	Min	Typ	Max	Unit
T_J	Operating junction temperature	–	–40	25	125	°C
T_{JA}	Package θ_{JA}		–	–	14.8	°C/W
T_{JB}	Package θ_{JB}				4.3	
T_{JC}	Package θ_{JC}				12.9	

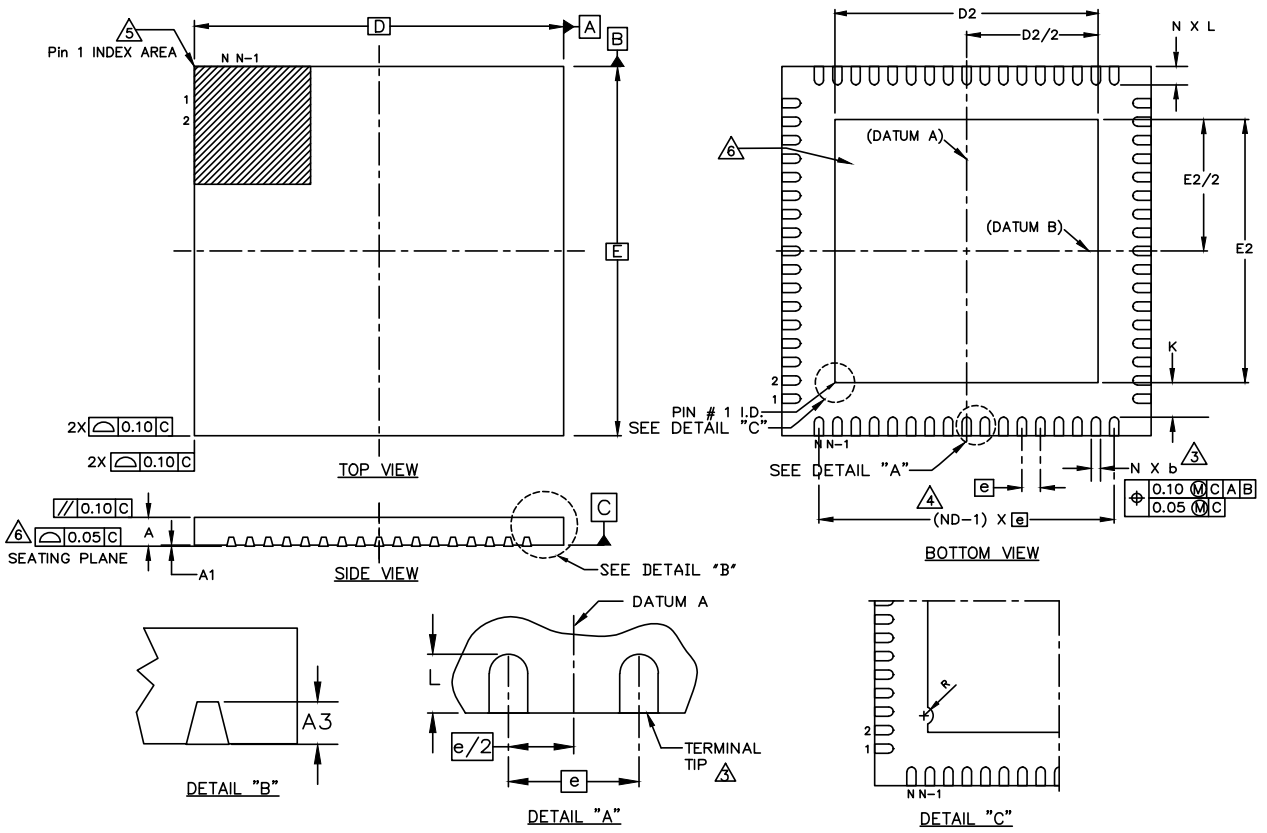
Table 23 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
68-pin QFN	260°C	30 s

Table 24 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
68-pin QFN	MSL 3

8 Package diagram



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.40 BSC	
N		68	
ND		17	
L	0.30	0.40	0.50
b	0.15	0.20	0.25
D2	5.60	5.70	5.80
E2	5.60	5.70	5.80
D		8.00 BSC	
E		8.00 BSC	
A	-	-	0.65
A1	0.00	-	0.05
A3		0.203 REF	
R		0.20 TYP	
K		0.75 MIN	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-31802 *D

Figure 15 68-pin QFN (8.0 × 8.0 × 0.65 mm) LD68B (5.7 × 5.7 MM EPAD) (Sawn) package outline (PG-VQFN-68)

9 Acronyms

Table 25 Acronyms used in this document

Acronym	Description
ACK	acknowledge
ADC	analog-to-digital converter
Arm®	Advanced RISC machine, a CPU architecture
ASK	amplitude shift key
BPP	basic power profile
BMC	BiPhase mark code
CEP	control error packet
CC	configuration channel
CSA	current sense amplifier
DCM	discontinuous-conduction mode
EA	error amplifier
EPP	Extended power profile
EPT	end power transfer
ESD	electrostatic discharge
FET	field effect transistor
FCCM	forced-continuous-conduction mode
FOD	foreign object detection
FO	foreign object
FSK	frequency shift key
FW	firmware
GPIO	general-purpose i/o
HBM	human body model
HS	High-Speed
I^2C	inter-integrated circuit
IC	integrated circuit
IMO	internal main oscillator
IPT	inductive power transfer technology
LDO	linear drop out
MCU	microcontroller unit
NTC	negative temperature coefficient
NVIC	nested vectored interrupt controller
OCP	overcurrent protection
Opamp	operational amplifier
OTP	overtemperature protection
OV	overvoltage
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
POR	power-on reset
PPDE	Proprietary Power Delivery Extensions
PPS	programmable power supply

Table 25 Acronyms used in this document *(continued)*

Acronym	Description
PSM	pulse-skipping mode
PWM	pulse-width modulator
QFOD	Q factor FOD
RPP	received power packet
RCP	reverse current protection
Rx	power receiver
SAR	successive approximation register
SCP	short-circuit protection
SPI	serial peripheral interface
SSP	signal strength packet
SWD	serial wire debug, a test protocol
TCPWM	timer/counter pulse-width modulation
Tx	power transmitter

10 Document conventions

10.1 Units of measure

Table 26 Units of measure

Symbol	Unit of measure
°C	degree celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kiloohm
LSB	least significant bit
MHz	megahertz
MΩ	megaohm
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
%	percent
pF	picofarad
s	second
V	volt
W	watt

Revision history

Document revision	Date	Description of changes
**	2025-10-14	Initial release.

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