OPTIREG™ Powerstage

TLF12505A

Features

- Integrated driver, control MOSFET Q1 and synchronous MOSFET Q2
- On-chip MOSFET Current sensing and reporting at 5uA/A.
- Input voltage (VIN) range of 4.25 V to 20 V
- VCC and VDRV supply of 4.9 V to 5.5 V
- Output voltage ranges from 0.225 V up to 5.5 V at VIN = 12 V
- Output current capability of 60 A
- Operation up to 2 MHz
- VDRV under voltage lockout (UVLO)
- Bootstrap under-voltage protection and flag
- 8mV / °C temperature analog output
- Over temperature protection flag and thermal shutdown
- Cycle-by-cycle over current protection (OCP)
- Nominal OCP threshold is 100 A, and IMON fault reporting is disabled
- Cycle-by-cycle negative over current protection (NOCP)
- Control MOSFET short (HSS) detection and flag
- Auto-replenishment on bootstrap capacitor
- Compatible with 3.3V and 5 V tri-state PWM Input
- DEEP SLEEP mode for power saving via EN= low (32 µA typ.)
- Small 5 mm x 6 mm x 0.9 mm PQFN package
- Lead free RoHS compliant package
- Compliant to automotive AEC-Q100 Rev H Grade 1 requirements

Potential applications

- Automotive Computing (ADAS/AD, Cockpit etc.)
- DDR memory

Description

- Qualified for automotive applications requiring AEC-Q100 Rev H Grade 1 Compliance
- High frequency, low profile DC-DC converters

The TLF12505A integrated power-stage contains a low quiescent current synchronous buck gate-driver IC which is co-packed with control and synchronous MOSFETs. The package is optimized for PCB layout, heat transfer, driver/MOSFET control timing, and minimal switch node ringing when layout guidelines are followed. The paired

gate driver and MOSFET combination enables higher efficiency at lower output voltages required by cutting edge CPU, GPU, and DDR memory designs.

The internal MOSFET sensing achieves superior current sense accuracy vs. best-in-class controller-based Inductor DCR sense methods.

Protection includes IC temperature reporting and over temperature protection feature (OTP with thermal shutdown), cycle-by-cycle over current protection (OCP), negative over current protection, control MOSFET short detection (HSS - High side short detection), VDRV and bootstrap under-voltage protection. The TLF12505A also features "refreshing" of bootstrap capacitor to prevent the bootstrap capacitor from over-discharging.

Operation of up to 2 MHz switching frequency enables high performance transient response, allowing miniaturization of output inductors, as well as input and output capacitors while maintaining industry leading efficiency.

Table of Contents

1 Pinout

Table 1 Product Identification

Part Number	Ambient Temp Range	Package	Marking	Orderable Part Number
TLF12505A	-40 to 125°C	PQFN 5 mm x 6 mm	12505A	TLF12505AAUMA1

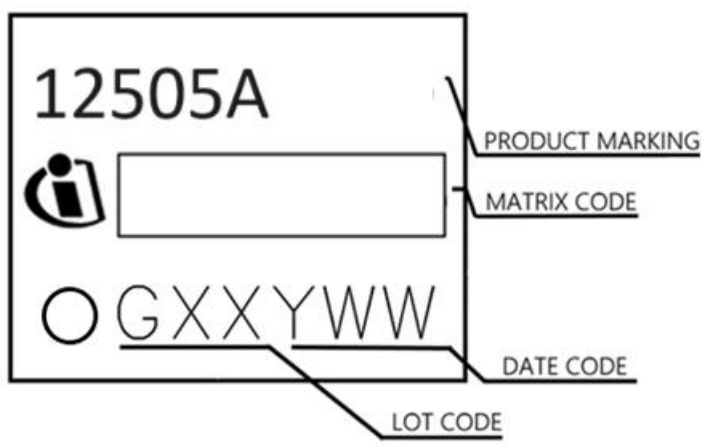

Figure 1 Part Marking

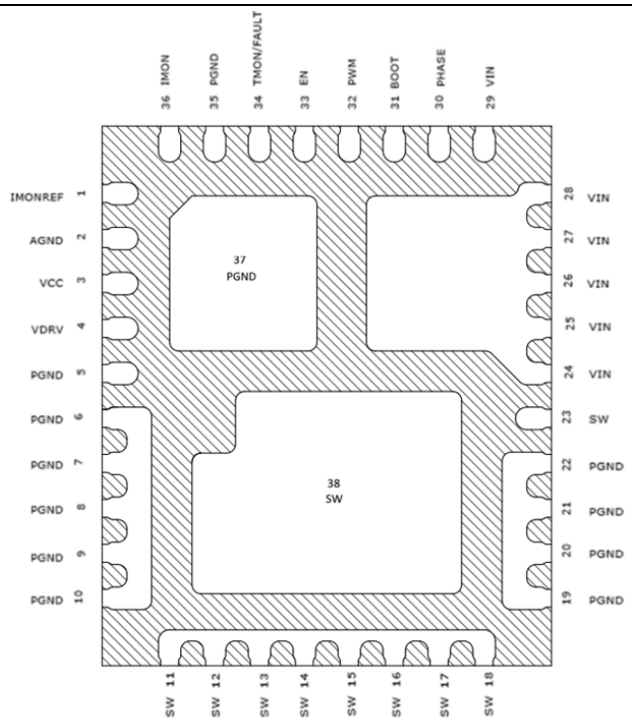

Figure 2 Pinout, Numbering and Name of Pins (transparent top view)

1.1 Pinout, Numbering and Name of Pins (transparent top view)

Table 2 I/O Signals

Pin No.	Name	Pin Type	Buffer Type	Function
1	IMONREF	I/O	Analog	This pin provides a system reference for the IMON information. This pin can be tied to a fixed voltage between 1.1 V and 1.9 V such as bias rails of a PWM controller.
11-18, 23, 38	SW	O	Analog	Switching node of synchronous buck converter.
30	PHASE	I	Analog	Switching node. For Bootstrap capacitor connection only.
31	BOOT	I	Analog	Bootstrap capacitor connection. Connect an X7R ceramic capacitor with value between 0.22 µF to 0.56 µF from BOOT to PHASE pin. Recommended value is 0.47µF. The bootstrap capacitor provides the charge to turn on the control MOSFET. For VIN between 13.2V and 19V, a 2-Ω bootstrap resistor in series with the capacitor is required to help reduce SW ringing and EMI. For VIN > 19V, a 3.3-Ω bootstrap resistor is required.
32	PWM	I/O	+5 V logic	5 V logic level PWM input. PWM input: “High” turns control MOSFET on; “Tri-state” turns both MOSFETs off; “Low” turns the synchronous MOSFET on.
33	EN	I	+3.3 V logic	Pulling EN high enables the driver; pulling EN low disables the driver and enters ultra-low quiescent current mode. Floating this pin is not recommended, however a pull-down is embedded to keep the driver off if the pin is floating. Pin is VCC tolerant.
34	TMON / FAULT	O	Analog	The voltage at this pin is defined by the equation. 8mV * (Celsius Temperature) + 0.6 V. This pin will be pulled up to 3.3 V under severe over-temperature, over-current, HSS or bootstrap under-voltage condition. Maximum recommended external capacitance on this pin is 1 nF.
36	IMON	O	Analog	Sensed current output signal referenced to the IMONREF pin through external resistor. V (IMON – IMONREF) voltage across that resistor represents current information.

Table 3 Power Supply

Pin No.	Name	Pin Type	Buffer Type	Function
3	VCC	POWER	–	Bias voltage for control logic. Connect a 1 µF cap between VCC and AGND. VCC should be connected to +5 V power supply.
4	VDRV	POWER	–	The supply of gate driver. Connect a 1 µF cap between VDRV and PGND. VDRV should be connected to +5 V power supply.

24-29	VIN	POWER	–	4.25 V to 20 V high current input voltage connection.

Table 4 Ground Pins

Pin No.	Name	Pin Type	Buffer Type	Function
2	AGND	GND	–	Signal ground. All interface signals are referenced to this pin.
5-10, 37	PGND	GND	–	Power ground. It is also the power ground of the synchronous MOSFET.
19-22	PGND	GND	–	Power ground. It is also the power ground of the synchronous MOSFET.
35	PGND	GND	–	Power ground. It is also the power ground of the synchronous MOSFET.

2 Block Diagram

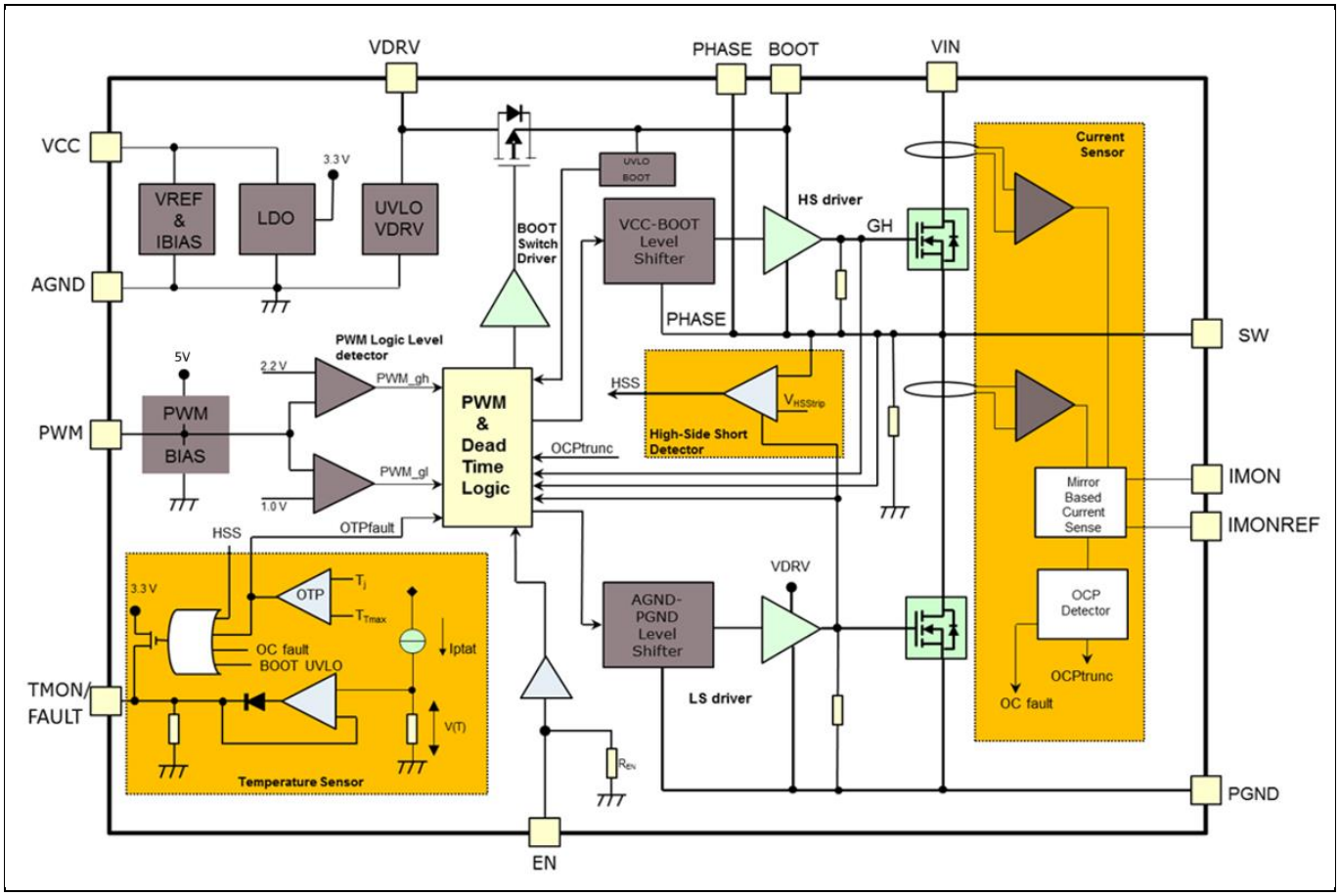

Figure 3 Simplified Block Diagram

3 Electrical Specification

3.1 Absolute Maximum Ratings

Note: TA = 25 °C

Stresses above those listed in Table 5 “Absolute Maximum Ratings” may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied or recommended at these or any other conditions more than those given in the operational sections of this specification. Exposure over values of the recommended ratings for extended periods may adversely affect the operation and reliability of the device.

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency of the PWM input	f_{SW}	0.1	–	2	MHz	
Maximum average load current	I_{OUT}	–	–	60	A	
Input Voltage	V_{IN}	-0.30	–	30	V	Pin VIN
Logic supply voltage	V_{CC}	-0.3	–	6.5	V	Pin VCC
High and low-side driver voltage	V_{DRV}	-0.3	–	6.5	V	Pin VDRV
Switch node voltage	V_{SW} (DC)	-1	–	30	V	Pin SW
	V_{SW} (AC)	-8 for 10 ns	–	32 for 2 ns		
PHASE voltage	V_{PHASE} (DC)	-1	–	30	V	Pin PHASE
	V_{PHASE} (AC)	-8 for 10 ns	–	32 for 2 ns		
VIN-PHASE voltage	$V_{VIN-PHASE}$(DC)	-1	-	30	V	
	$V_{VIN-PHASE}$(AC)	-8 for 10 ns	-	32 for 2 ns	V	
BOOT voltage	V_{BOOT} (DC)	-0.3	–	29	V	Pin BOOT
	V_{BOOT} (AC)	Below -0.3 for 5 ns		34 for 1 ns		
BOOT-PHASE voltage	$V_{BOOT-PHASE}$ (DC)	-0.3	–	6.5	V	
	$V_{BOOT-PHASE}$ (AC)	Below -0.3 for 5 ns		7.5 for 3 ns	V	
EN voltage	V_{EN}	-0.3	–	6.5	V	Pin EN
PWM voltage	V_{PWM}	-0.3	–	6.5	V	Pin PWM
TMON voltage	V_{TMON}	-0.3	–	3.6	V	Pin TMON / FAULT
IMON voltage	V_{IMON}	-0.3	–	3.6	V	Pin IMON
IMONREF voltage	$V_{IMONREF}$	-0.3	–	3.6	V	Pin IMONREF
Junction temperature	T_{Jmax}	-40	–	150	°C	
Storage temperature	T_{STG}	-55	–	150	°C	

Note: All rated voltages are relative to voltages on the AGND and PGND pins unless otherwise specified.

Table 6 ESD Resistivity

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Electrostatic Discharge Voltage at all pins	VESD	-1.5		1.5	kV	Human Body Model (100pF via 1.5kΩ) Note 2
Electrostatic Discharge Voltage at all pins	VESD		500		V	CDM

3.2 Thermal Characteristics

Table 7 Thermal Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance-Junction to PCB (pin 24)	θ_{JC_PCB}	–	1.5	–	K/W	
Thermal resistance-Junction to top of package	θ_{JC_Top}	–	17.8	–		
Thermal resistance-Junction to ambient	θ_{JA} Note	–	28.4	–		

Note: Thermal Resistance (θ_{JA}) is measured with the component mounted on a high effective thermal conductivity test board in free air.

3.3 Recommended Operating Conditions

Table 8 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage	V_{IN}	4.25	–	20	V	Note 3
MOSFET driver voltage	V_{DRV}	4.9	–	5.5		–
Logic supply voltage	V_{CC}	4.9	–	5.5		–
Frequency of the PWM	f_{SW}	300	–	2000	kHz	–
EN voltage	V_{EN}	–	–	5.5	V	Pin EN
PWM voltage	V_{PWM}	–	–	5.5	V	Pin PWM
Current Sense reference voltage	V_{IMON_CM}	1.1	–	1.9	V	Pins IMON, IMONREF
Junction temperature	T_{jOP}	-40	–	+125	°C	

3.4 Electrical Characteristics

Note: $V_{DRV} = V_{CC} = 5$ V, $T_J = 25$ °C, $V_{IMONREF} = 1.2$V

Table 9 Voltage Supply, Biasing Current

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
UVLO VDRV rising	V_{UVLO_R}	3.9	4.05	4.2	V	
UVLO VDRV falling	V_{UVLO_F}	3.7	3.85	4.0		
Bootstrap Under voltage rising threshold	V_{UVBOOT_R}	3.7	3.85	4.0		
Bootstrap Under voltage falling threshold	V_{UVBOOT_F}	3.45	3.61	3.78		
Driver current	I_{VDRV}	–	20	–	mA	EN = H, fSW = 600 kHz, D=15%
		–	220	–	µA	EN = H, PWM floating
		–	2.5	–	µA	EN = L
Supply Current	I_{Vcc}	–	6	–	mA	EN = H, fSW = 600 kHz, D=15%
		–	1.5	–	mA	EN = H, PWM floating
		–	30	–	µA	EN = L
VIN Current	I_{VIN}	–	-	860	µA	No switching

Table 10 Current Sense

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
IMON	IMON Voltage range	V_{IMON}	0.8	–	2.35	V	DC + AC components
	IMON/IMONREF reference voltage range	V_{IMON_CM}	1.1	–	1.9	V	Reference Voltage connected externally for the current sense signal
	Current sense gain	A_{cs}	–	5	–	µA/A	
	IMON Gain resistor range	R_{IMON}	–	1	–	kΩ	Resistor to be connected between IMON and IMONREF. For 5mV/A, recommended 1kΩ R_{IMON}
	Leakage Current	I_{Leak}	-2	0	2	µA	I_{OUT} = 0A, V_{IMON}=1.2V PWM in tri-state
	Zero current offset	I_{offset}	-3	0	3	µA	Corresponds to 3 mV at 5 mV/A. (R_{IMON} = 1 kΩ), device in regulation
	Accuracy at T_J = -5 to 125°C $V_{CC} = V_{DRV} = 5$ V ± 10 %		-3.0	–	3.0	%	for 25A < I_{OUT} < I_{OCP_TH} Note 1, Note 3
			-0.5	–	0.5	A	for -25A < I_{OUT} < 25A Note 1

Table 11 Temperature Sense and Fault Communication

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TMON / FAULT	Temperature Sense Slope	$A_{TMPGAIN}$	7.84	8.0	8.16	mV/°C	25°C ≤ T_J ≤ 125°C, Note 1
	Temperature Sense Offset Voltage	$V_{TMPOFFSET}$	784	800	816	mV	T_J = 25°C, 0.6 V + 8 mV/°C * T_J
	TMON / FAULT Source Current	$I_{TMONSRC}$	2.5	3	3.5	mA	TMON / FAULT pulled low
	TMON / FAULT Sink Current	$I_{TMONSNK}$	26	32	40	µA	TMON / FAULT pulled high
	Fault mode Active High	$V_{TFLTHIGH}$	2.6	3.3	3.6	V	$I_{TMON/FAULT}$ = 5 mA and under Over-Temperature, Over-Current, bootstrap undervoltage or HSS Fault
	TMON / FAULT Low Note 1	$V_{TFLTLOW}$	–	–	0.35	V	No Fault, V_{DRV} < V_{UVLO1_R}
	TMON / FAULT pull down resistance	R_{PULLDN_TMON}	–	150	–	kΩ	No Fault, V_{DRV} < V_{UVLO1_R}

Table 12 Other Logic Functions, Inputs/Outputs and Thresholds

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
EN	Enable Power-on Delay	$t_{EN\_ondelay}$	–	17	35	µs	PWM=0. Measured from EN rising edge to V_{SW}> 1 V.
	Enable Power-off Delay	$t_{EN\_offdelay}$	–	-	1	ns	PWM=0. Measured from EN falling edge to V_{SW} < 0.9* VIN.
	Internal Pull-down Resistance	R_{PULLDN_EN}	–	280	–	kΩ	When EN is floating
	Input High Voltage	V_{EN_H}	2.0	–	–	V	
	Input Low Voltage	V_{EN_L}	–	–	0.8	V	

PWM	PWM Input High Threshold	V_{IH}	2.4	–	–	V	PWM Low or Tri-state to High
	PWM Input Low Threshold	V_{IL}	–	–	0.8	V	PWM High or Tri-state to Low
	PWM Hysteresis	I_{PWM_HYS}	–	40	–	mV	Active to Tri-state or Tri-state to Active
	PWM Input Tri-State Floating Voltage	V_{PWM_TRI}		1.6		V	PWM Input Floating
	Tri-state Window	V_{PWM_S}	1.2	–	2.0	V	
	PWM Input Equivalent Pull-up Resistance	R_{PWM_PU}	–	20	–	kΩ	V_{PWM} = 0 V
	PWM Input Equivalent Pull-down Resistance	R_{PWM_PD}	–	50	–	kΩ	V_{PWM} = 3.3 V
Bootstrap Diode	Forward Voltage	V_{FWD}	-	620	-	mV	I(BOOT) = 5 mA
SW	SW Floating Voltage	V_{SW_FLOAT}	-	-	200	mV	V_{PWM} = 1.6 V or Tri-state, VCC = VDRV = 5V
	SW Pull Down Resistance	$R_{SW\_PULL\_DOWN}$	0.85	1.125	1.5	kΩ	

Table 13 Protection

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
OTP	Over Temp Rising Threshold	T_{RISE}	–	155	–	°C	TMON/FAULT pulled up high Note 1
	Over Temp Falling Threshold	T_{FALL}	–	143	–	°C	TMON/FAULT released Note 1
HSS FAULT	High-side MOSFET Short Threshold	V_{HSS_TH}	–	560	–	mV	$V_{SW} - V_{PGND}$
	TMON/FAULT Delay	T_{HSS_DEL}	–	150	–	ns	After V_{HSS_TH} is detected, and TMON/FAULT is pulled high

OCP	Over-Current Threshold	I_{OCP_TH}	87	100	113	A	-
OCPn	Negative OCP Threshold	T_{OCPN_TH}	-55	-50	-45	A	-

Table 14 Timing Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PWM High Propagation Delay	$t_{PWM\_HI\_DELAY}$	–	48	–	ns	Measured from PWM rising edge to V_{SW} starts to rise
PWM Low Propagation Delay	$t_{PWM\_LO\_DELAY}$	–	45	–	ns	Measured from PWM falling edge to V_{SW} starts to fall
Tri-State to High Propagation Delay	$t_{TRI\_HI\_DELAY}$	–	53	–	ns	PWM Tri-state to High transition to V_{SW} > 1 V
Tri-State Hold Off Time	$t_{TriHold}$	–	56	–	ns	PWM Low to Tri-state transition to SW starts to fall Note 1
			75			PWM High to Tri-state transition to SW starts to fall Note 1
Minimum Recognized PWM Pulse Width Note 1	t_{MinPWM}	–	17	–	ns	PWM pulses shorter than t_{MinPWM} will be ignored by driver. Note 1
Minimum output pulse width	$t_{OnSWmin}$	–	18	–	ns	Positive load current. PWM pulses shorter than $t_{OnSWmin}$ will be extended to $t_{OnSWmin}$. Note 1

Note:

1. *Guaranteed by design but not tested in production.*
2. *ESD Susceptibility HBM according to EIA / JESD 22-A 114*
3. *Device is functional down to VIN =3V. IMON signal accuracy guaranteed down to minimum VIN = 6V.*

4 Typical Operating Characteristics

Single Phase Circuit of Figure 16, V_{IN} = 12 V, V_{OUT} = 0.8 V, f_{SW} = 500 kHz, L = 150 nH, VCC = VDRV = 5 V, $T_{AMBIENT}$ = 25 °C, no heat sink, no air flow, 8-layer PCB board of 3.7” (L) x 2.6” (W), no PWM controller loss, no inductor loss, unless specified otherwise.

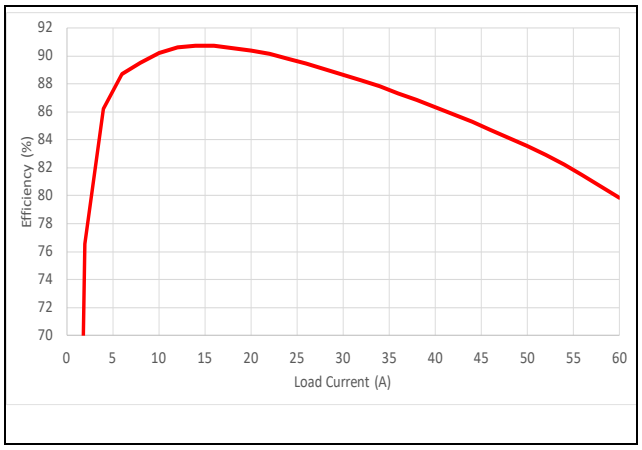

Figure 4 Power Stage Efficiency

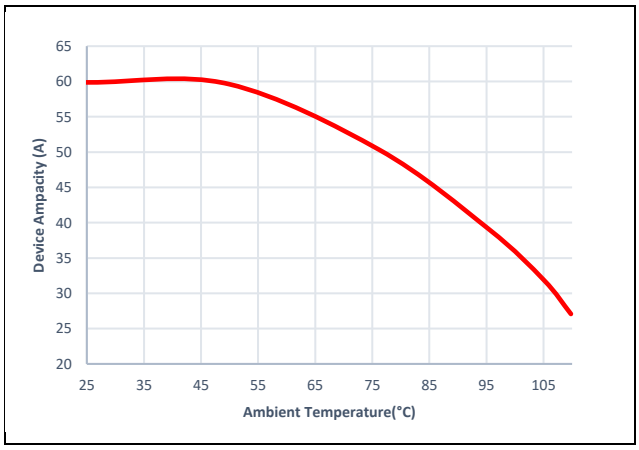

Figure 7 Thermal Derating, Tcase<=125°C

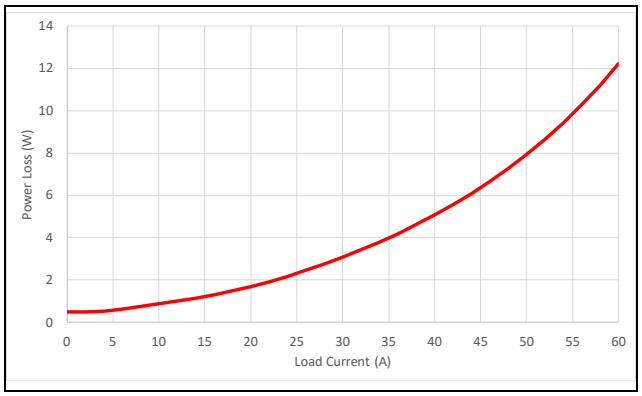

Figure 5 Power Stage Loss

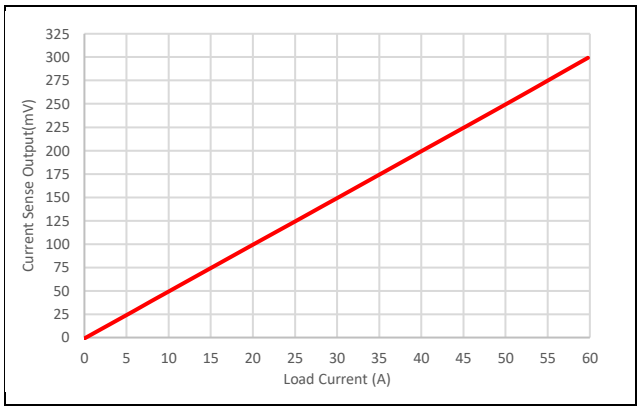

Figure 8 Current Sense Output

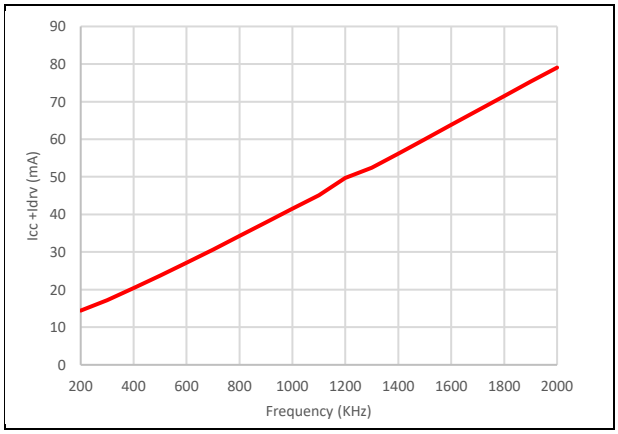

Figure 6 Vcc + Vdrv Current vs Frequency

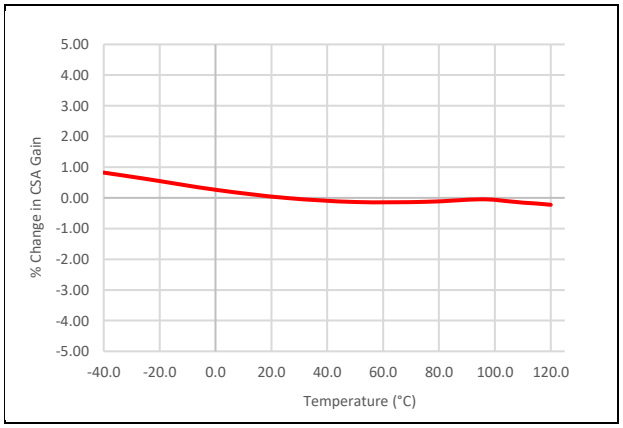

Figure 9 Current Sense Gain vs Temperature

Single Phase Circuit of Figure 16, V_{IN} = 12 V, V_{OUT} = 0.8 V, f_{SW} = 500 kHz, L = 150 nH, VCC = VDRV = 5 V, $T_{AMBIENT}$ = 25 °C, no heat sink, no air flow, 8-layer PCB board of 3.7” (L) x 2.6” (W), no PWM controller loss, no inductor loss, unless specified otherwise.

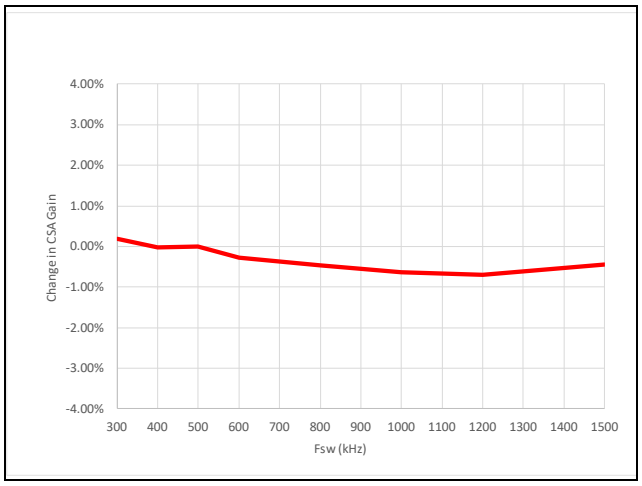

Figure 10 Current sense gain variation vs Frequency

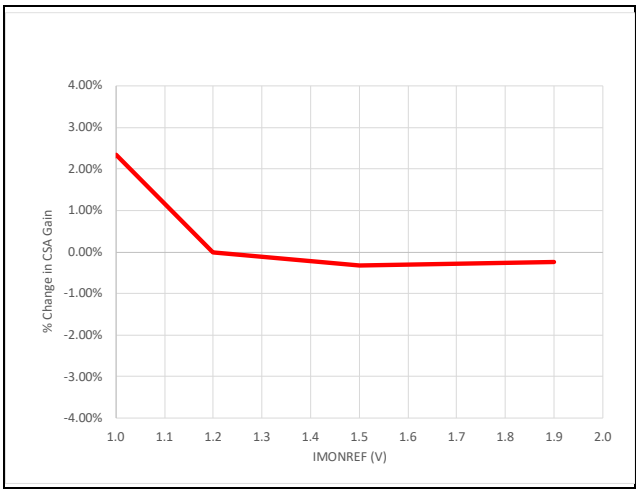

Figure 13 Current Sense gain variation vs IMONREF

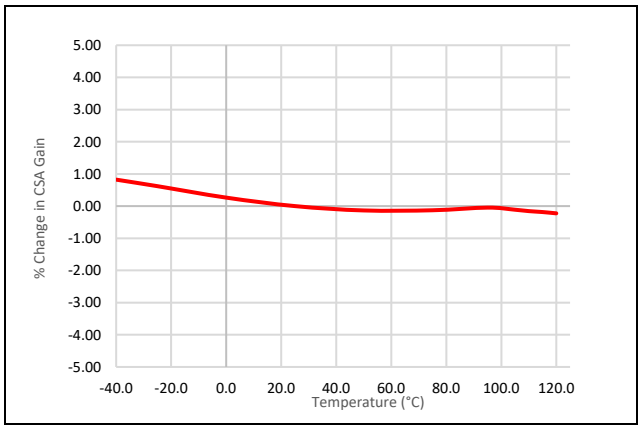

Figure 11 Current sense gain variation vs Temperature

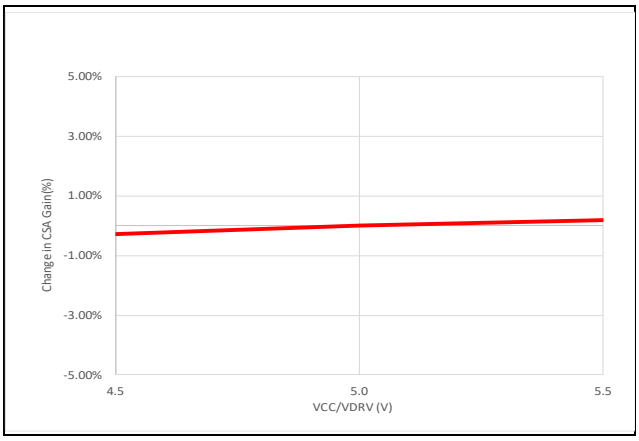

Figure 14 Current sense gain variation vs VCC/VDRV

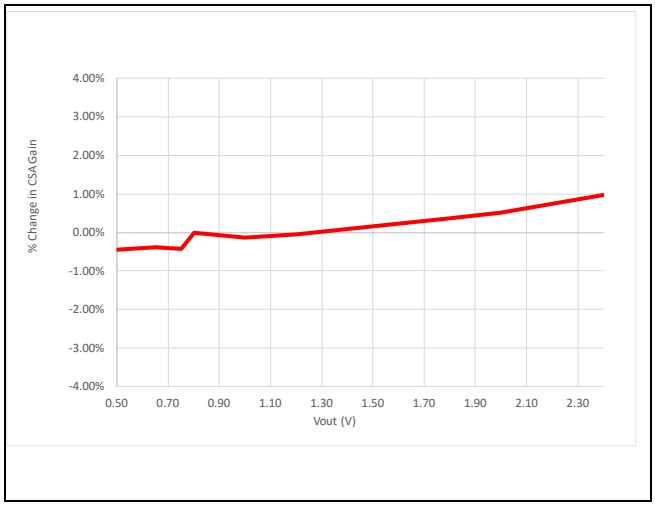

Figure 12 Current sense gain variation vs Vout

5 Theory of Operation

5.1 Description

The TLF12505A contains an improved high speed MOSFET driver optimized to drive a pair of co-packaged high-side and low-side OptiMOS MOSFETs at frequency up to 2 MHz's. DC-DC controllers using traditional current sense methods like DCR sensing and Rdson sensing typically have limitations. DCR current sensing is sensitive to temperature changes of the inductor and needs temperature compensation either implemented externally using a thermo-couple or inside the power stage. Rdson current sensing, on the other hand, is not dependent on the inductor but there is a temperature co-efficient associated with the MOSFET Rdson. Besides, it is difficult to implement Rdson current sensing for high-side MOSFET which is therefore replaced by emulated current while the low-side current is sensed across the MOSFET. With the advanced current mirror sensing in TLF12505A, all these limitations are eliminated while achieving superior accuracy. Current on both high-side as well as low-side MOSFET is mirrored on a sense MOSFET which is a part of the main MOSFET device and hence comes with an inherent temperature compensation without the need for an additional circuitry. Real current-sensing on both MOSFET ensures that the system is always monitoring the real output current and can immediately react to any critical events like load step or over-current fault.

The TLF12505A reports accurate temperature with the gain of 8 mV / °C, which helps the system to actively monitor the temperature in real time. Temperature outputs from multiple power stages can be connected to report the highest temperature to Infineon's digital PWM controller.

The TLF12505A PWM input is compatible with industry standard 3.3V PWM input with tri-state and is tolerant for signals up to 5V inputs.

The TLF12505A can enable Body-Braking mode by responding to PWM tri-state signals sent from the controller, quickly disabling both MOSFETs in the power stage to enhance transient performance or provide a high impedance output.

The TLF12505A supports diode emulation mode through the PWM tri-state signal. Controlled by Infineon's digital PWM controller, the PWM tri-state signal will force the low-side FET to be off when the inductor current is about to go negative. The light-load efficiency then can be increased by preventing conduction loss caused by negative inductor current.

The TLF12505A also supports deep-sleep power saving mode. When in deep-sleep mode, the driver will disable most of the function circuitry to greatly reduce power consumption.

The TLF12505A features a full-range of protection, including VCC/VDRV Under-Voltage-Lockout (UVLO), thermal shutdown against an internal over-temperature condition, phase fault detection of a shorted high-side MOSFET, and cycle-by-cycle over-current protection due to an overload condition or saturated output inductor.

The TLF12505A also features internal protection circuitry to automatically replenish the voltage across the bootstrap capacitor. It avoids the gradual depletion of capacitor energy when the power stage sits in tri-state for a long period of time.

5.2 Sleep Modes

When EN is pulled low, the power stage enters deep-sleep mode. The gate driver circuitry will be turned off immediately and most of the logic circuitry will be shut down to reduce the bias current to less than 32 µA. The IMON output will be shorted to IMONREF in deep sleep mode.

When EN toggles from low to high, the power stage will be active and able to accept PWM signals after a delay of 17 µs.

5.3 Current Sensing and Reporting

The TLF12505A features a very accurate current mirror architecture on both high-side as well as low-side MOSFET, thus reporting the real time current information. The current information is reported using the IMON pin. The reported current is in the form of current output with the gain of 5µA /A from the IMON pin. To convert this into voltage, a 1kΩ, 0.1% resistor is recommended at the IMON pin and placed close to the PWM controller. A differential voltage signal from this resistor is connected to the controller as the reported current information. Note that for accurate current reporting, it is important that the other end of the resistor cannot be left floating. The converted voltage signal at the controller side has an effective gain of 5mV/A i.e., for every 1 A load, the controller will read 5mV from the power stage. The current-output differential signal from the power stage provides excellent noise immunity to the reported current information.

5.4 VDRV Under-voltage Lock-out (UVLO)

TLF12505A features a VDRV under-voltage lock-out fault circuitry that monitors the VDRV voltage actively. This is a non-catastrophic fault, and the TMON/FAULT pin is pulled low with a weak pull down if the VDRV voltage is below the UVLO threshold. If the power stage has not started up, the power stage PWM pin is also pulled down to 0V with a weak pull down. This can be monitored by the PWM controller as a signal from the power stage indicating that it is not ready yet for power up. As soon as VDRV voltage is above the UVLO threshold, the PWM pin is at tri-state instead of 0V, this indicating the controller that it is OK to send the PWM signals.

Once the power stage is in normal operation, if then it encounters a VDRV UVLO condition, the power stage stops switching, and both TMON pins and IMON-IMONREF signal are pulled down to 0V. If there are multiple phases connected in the same loop, the TMON pin voltage, being connected to other power stage TMON pins, will continue reporting the highest power stage temperature.

5.5 Temperature Reporting and Over-temperature protection

An internal temperature-sense circuit monitors the temperature of the TLF12505A. The sensed temperature is reported at the TMON/FAULT pin with a linear voltage slope of 8mV/°C and a 0.6V offset at 0°C, as shown in equation (1).

$$V_{TMON/FAULT}(V) = 0.6V + 0.008V/°C \ \ x\ T_j(°C) \quad \text{.....} \quad (1)$$

The TMON/FAULT pin also serves as a FAULT pin that is pulled to 3.3V in case of any catastrophic faults and is pulled down to 0V in case of any non-catastrophic faults. When there is no fault, it continues reporting temperature as long as the VCC supply is connected to a voltage in the recommended operating range. For a junction temperature below -25°C, the TMON voltage is clamped to 0.4V to avoid false triggering of VDRV under-voltage.

Once the temperature rises above the OTP rising threshold (155 °C), the TMON/FAULT output will be pulled high immediately, the driver will stop switching and stop responding to the PWM signal input from the controller. Both high-side and low-side MOSFET are turned off. The TMON/FAULT will remain high until temperature falls below the falling threshold (143 °C).

5.6 Over-current Protection

This feature protects the power stage from self-destruction from repetitive high current events such as saturated inductors due to poor component selection or by incorrectly optimized control loops. These high current events

could eventually lead to a shorted high-side MOSFET failure. With cycle-by-cycle self-preservation, the current is monitored every cycle.

If the over-current threshold (nominal 100 A) has been exceeded, the PWM high pulse will be truncated so that the inductor current is allowed to relax. There is no fault reporting via the IMON pin, it has been disabled.

5.7 Bootstrap Capacitor Under-Voltage

TLF12505A features a bootstrap capacitor under-voltage circuitry that detects a missing bootstrap capacitor before powering up or a damaged bootstrap capacitor during normal operation. Once bootstrap capacitor under-voltage is determined, the TMON/FAULT pin will be pulled high to report a catastrophic fault to the PWM controller.

5.8 Negative over current protection

TLF12505A features a negative over-current protection in the device to protect from very high negative current. As soon as the power stage detects the IMON reported (negative) current exceeding the negative over-current threshold (OCPn), the high-side FET is enabled for 200ns before the power stage continues following the PWM input signal. TMON continues reporting the power stage temperature during negative over-current fault event.

6 Design Procedure

6.1 Input Capacitors C_{VIN}

A 0402 or 0603, X7R, 1-µF ceramic capacitor and three 10-µF X7R ceramic capacitor are recommended at the VIN pins. Use of capacitors with lower ESR will improve efficiency, especially in single-phase operation. Layout guidelines and examples are available.

6.2 Bootstrap Capacitor Cboot and Resistor Rboot

A high temperature 0.22-µF or greater value 0402 X7R capacitor is recommended. It should be mounted on the same side of the PCB as the TLF12505A and as close as possible to the BOOT Pin. Low inductance routing of the PHASE pin connection to the negative terminal of the bootstrap capacitor is strongly recommended.

Bootstrap capacitor connection. Connect an X7R ceramic capacitor with value between 0.22 µF to 0.56 µF from BOOT to PHASE pin. Recommended value is 0.22µF. The bootstrap capacitor provides the charge to turn on the control MOSFET. For VIN > 13.2 V, a 2-Ω bootstrap resistor in series with the capacitor is required to help reduce SW ringing and EMI.

6.3 Vcc and Vdrv Decoupling Capacitors

A 1-µF X7R decoupling capacitor is required between VCC and LGND pins, and a 1-Ω VCC resistor is recommended. A 1-µF X7R decoupling capacitor is required between VDRV and PGND pins and can be directly connected to the 5-V supply. Both capacitors should be mounted on the same side of the PCB as the power stage and as close as possible to the VCC-LGND and VDRV-PGND pins. Low inductance routing between the capacitor and the PMC41520 is strongly recommended. Layout guidelines and examples are available.

6.4 Mounting of Heat Sinks

Care should be taken in the mounting of heat sinks so that even pressure is applied on the power stage surface. A thermal interface material should be used between the power stage and the heat sink to solve planarity issues and ensure even thermal conduction.

The VCC, VDRV, VIN and bootstrap capacitors are typically located on the same side of the PCB as the power stage. The height of these capacitors must be considered when using heat sinks.

7 Application Diagram

7.1 Typical Application

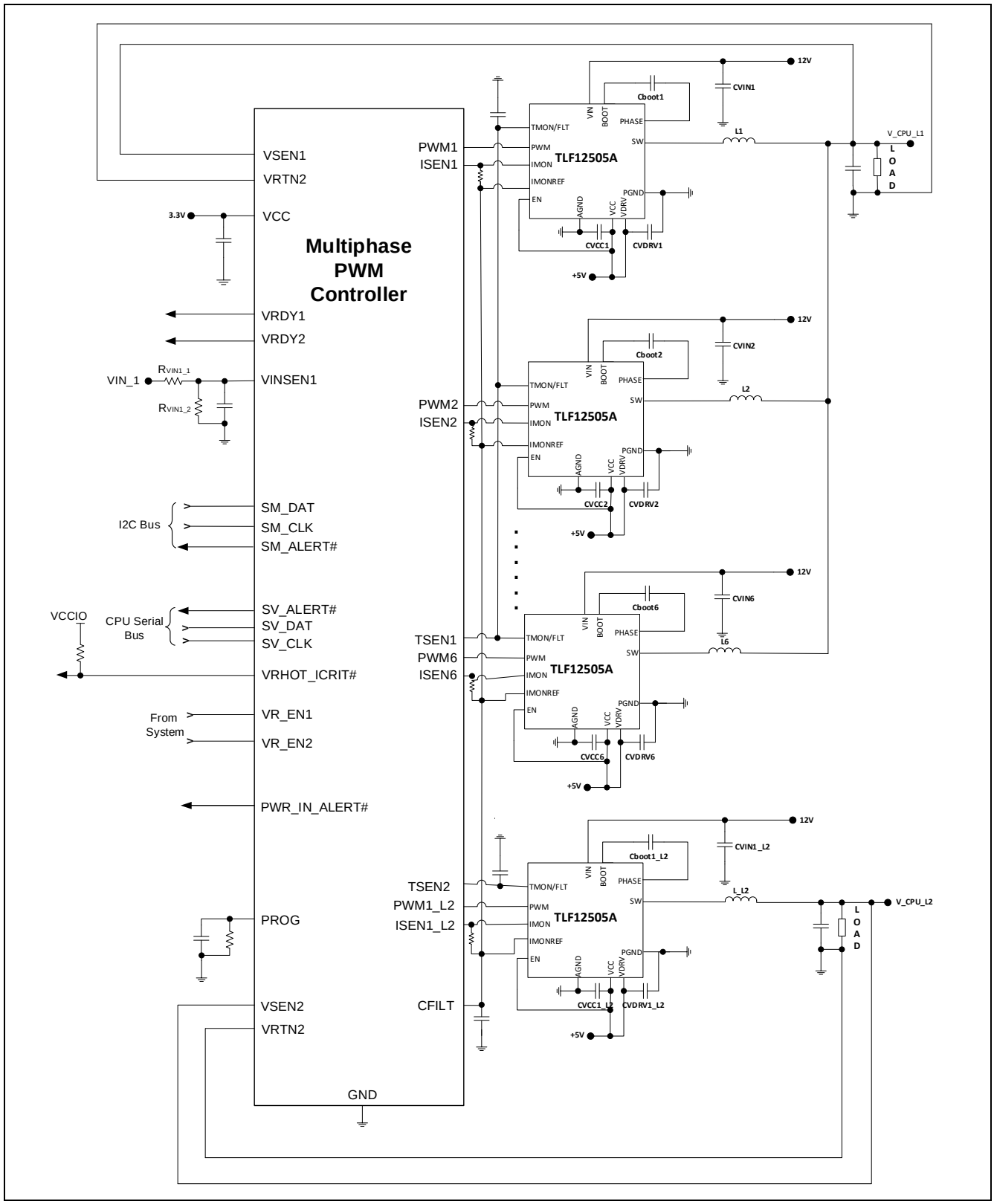

Figure 15 6+1 - Phase Voltage Regulator - Typical Application (simplified schematic)

7.2 Typical Single-phase Application Diagram

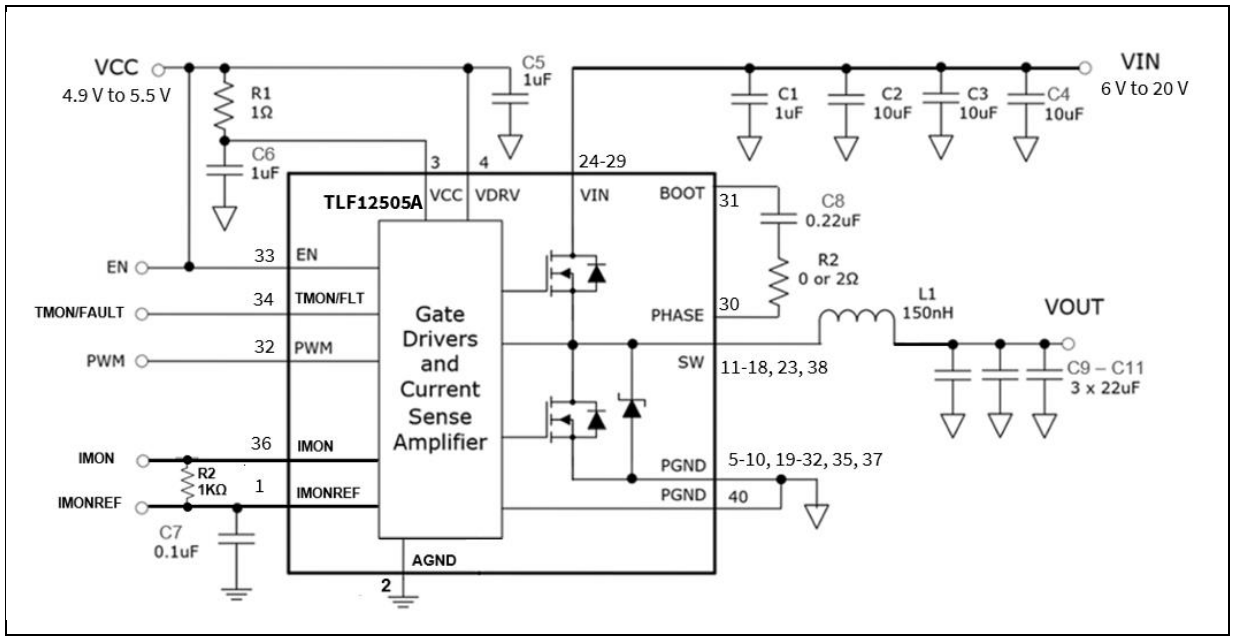

Figure 16 Typical Application Diagram for Single-Phase Voltage Regulator

8 Mechanical Drawing

8.1 Mechanical Dimensions (Top View and Side View)

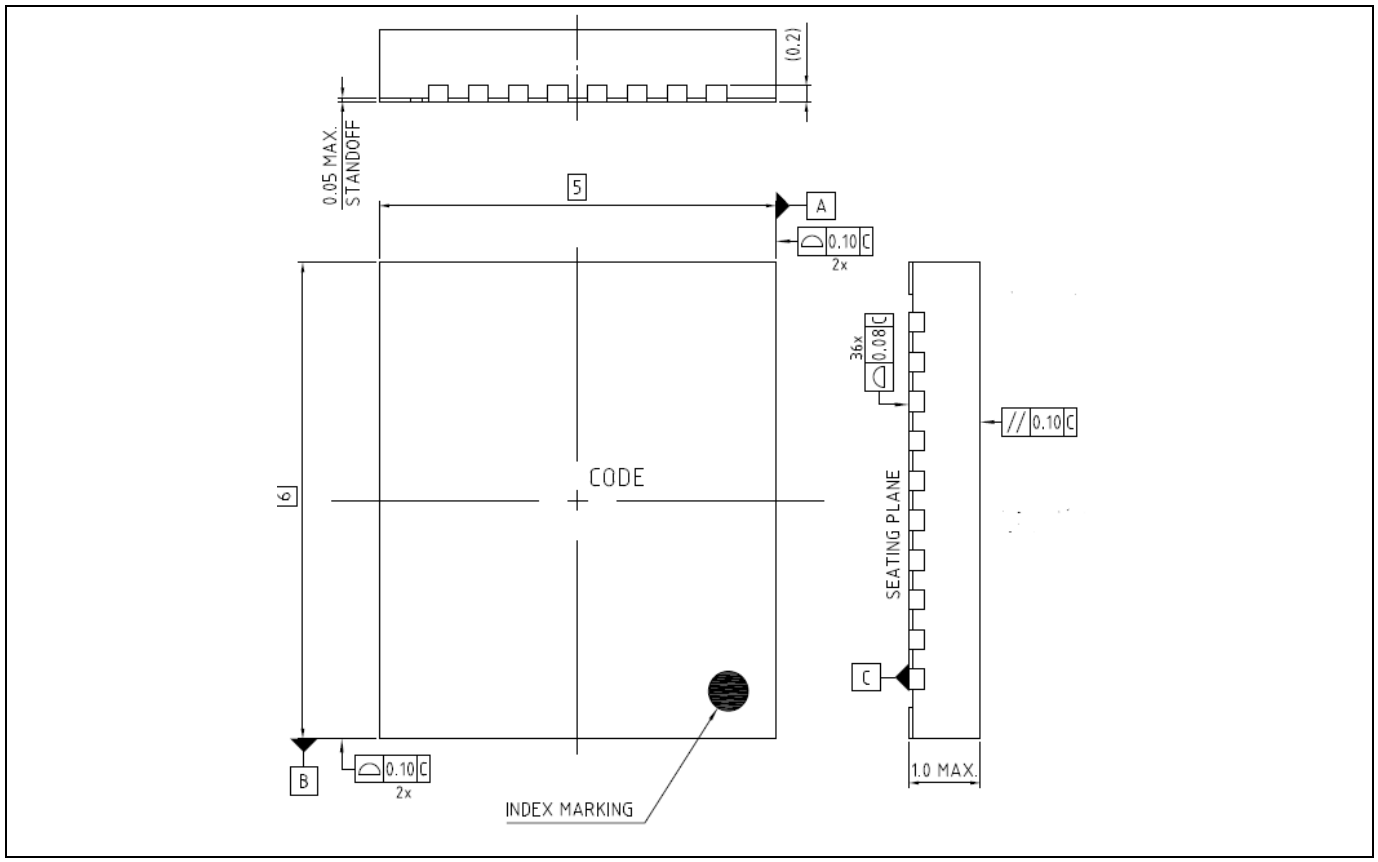

Figure 17 Mechanical Dimensions of Package (Top View and Side View) in mm

8.2 Mechanical Dimensions of Package in mm

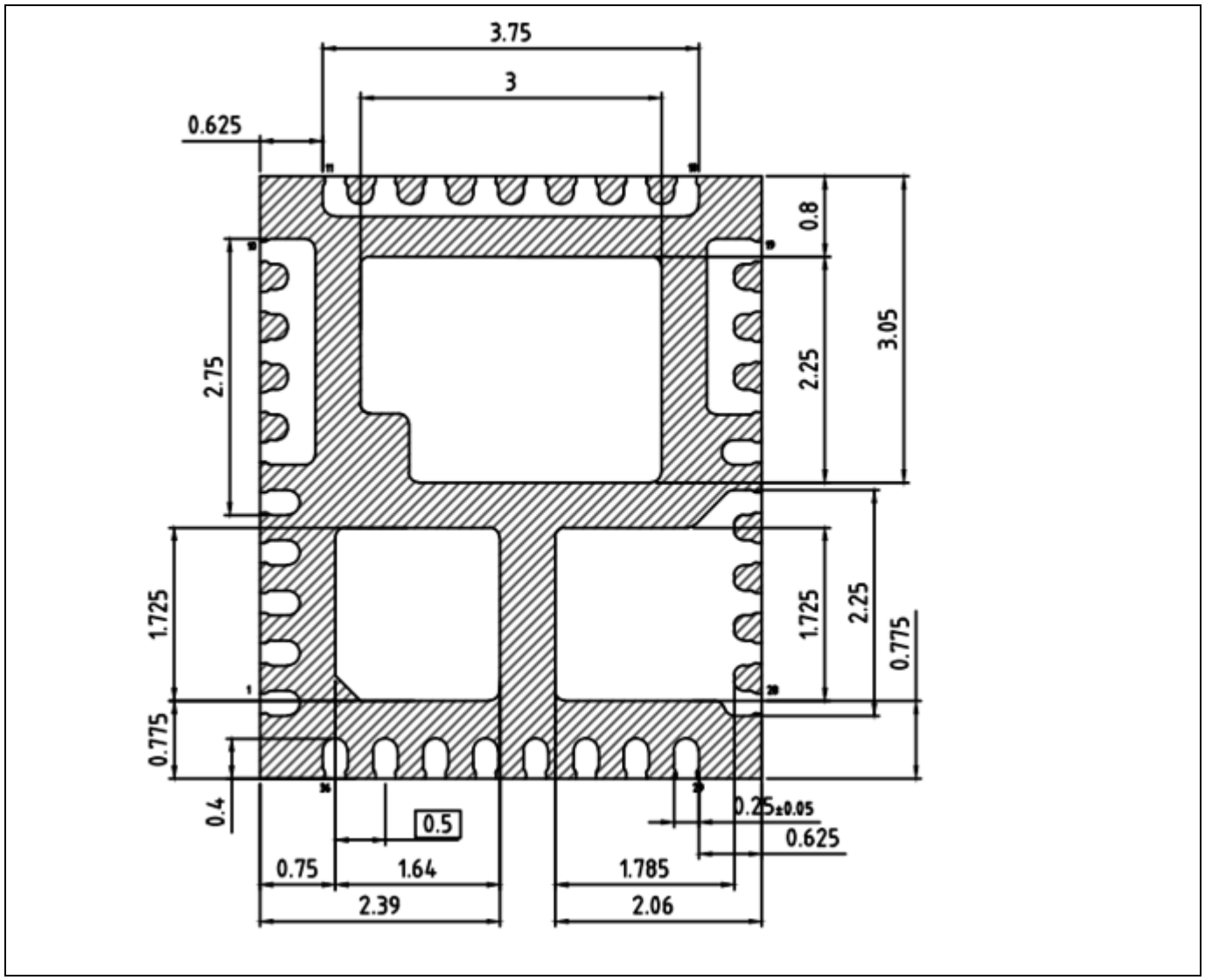

Figure 18 Mechanical Dimensions of Package (Bottom View) in mm

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-06-24

Published by

Infineon Technologies AG

81726 München, Germany

Do you have a question about this document?

Email: **erratum@infineon.com**

Document reference

Z8F80756562

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”) .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies’ products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

Revision history

TLF12505A

Revision 2025-07-30, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-07-30	Release of final version

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

We Listen to Your Comments Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: **erratum@infineon.com**

Published by
Infineon Technologies AG
81726 München, Germany

Important notice
The products which may also include samples and may be comprised of hardware or software or both ("Product") are sold or provided and delivered by Infineon Technologies AG and its affiliates ("Infineon") subject to the terms and conditions of the frame supply contract or other written agreement(s) executed by a customer and Infineon or, in the absence of the foregoing, the applicable Sales Conditions of Infineon. General terms and conditions of a customer or deviations from applicable Sales Conditions of Infineon shall only be binding for Infineon if and to the extent Infineon has given its express written consent.

For the avoidance of doubt, Infineon disclaims all warranties of non-infringement of third-party rights and implied warranties such as warranties of fitness for a specific use/purpose or merchantability.

Infineon shall not be responsible for any information with respect to samples, the application or customer's specific use of any Product or for any examples or typical values given in this document.

The data contained in this document is exclusively intended for technically qualified and skilled customer representatives. It is the responsibility of the customer to evaluate the suitability of the Product for the intended application and the customer's specific use and to verify all relevant technical data contained in this document in the intended application and the customer's specific use. The customer is responsible for properly designing, programming, and testing the functionality and safety of the intended application, as well as complying with any legal requirements related to its use.

Unless otherwise explicitly approved by Infineon, Products may not be used in any application where a failure of the Product or any consequences of the use thereof can reasonably be expected to result in personal injury. However, the foregoing shall not prevent the customer from using any Product in such fields of use that Infineon has explicitly designed and sold it for, provided that the overall responsibility for the application lies with the customer.

If the Product includes security features:
Because no computing device can be absolutely secure, and despite security measures implemented in the Product, Infineon does not guarantee that the Product will be free from intrusion, data theft or loss, or other breaches ("Security Breaches"), and Infineon shall have no liability arising out of any Security Breaches.

If this document includes or references software:
The software is owned by Infineon under the intellectual property laws and treaties of the United States, Germany, and other countries worldwide. All rights reserved. Therefore, you may use the software only as provided in the software license agreement accompanying the software. If no software license agreement applies, Infineon hereby grants you a personal, non-exclusive, non-transferable license (without the right to sublicense) under its intellectual property rights in the software (a) for software provided in source code form, to modify and reproduce the software solely for use with Infineon hardware products, only internally within your organization, and (b) to distribute the software in binary code form externally to end users, solely for use on Infineon hardware products. Any other use, reproduction, modification, translation, or compilation of the software is prohibited.

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).