Never stop thinking

TLE4966-2K

High Precision Hall Switch with two Outputs

Datasheet

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Sense & Control

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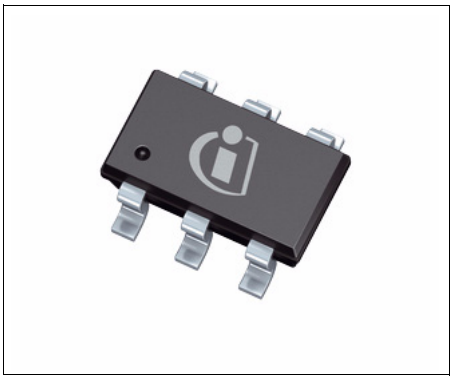
1 Overview



1.1 Features

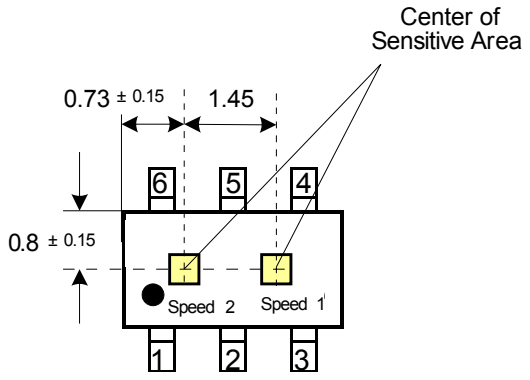
- 2.7V to 24V supply voltage operation
- Operation from unregulated power supply
- High sensitivity and high stability of the magnetic switching points
- High resistance to mechanical stress by Active Error Compensation
- Reverse battery protection (-18V)
- Superior temperature stability
- Peak temperatures up to 195°C
- Low jitter (typ. 1µs)
- Digital output signals
- Excellent matching of the 2 Hall probes
- Hall plate distance 1.45mm
- Two independent speed outputs
- SMD package PG-TSOP6-6-5

1.2 Functional Description

The TLE4966-2K is an integrated circuit dual Hall-effect sensor designed specifically for highly accurate applications. Precise magnetic switching points and high temperature stability are achieved by active compensation circuits and chopper techniques on chip. The sensor provides two independent speed outputs at Q1 and Q2 with the status (high or low) corresponding to the magnetic field value at the respective Hall element H1 and H2. Both Hall elements have the identical thresholds for B_{OP} and B_{RP} (B_{OP1} = B_{OP2} and B_{RP1} = B_{RP2}). For positive magnetic fields (south pole) exceeding the threshold B_{OP1} and/or B_{OP2} the corresponding output Q1 and/or Q2 is low, whereas for negative magnetic fields (north pole) lower than B_{RP} the output switches to high. Due to the spatial distance of the two Hall elements on the chip (d = 1.45mm) the two output signals will show a phase difference in case the sensor is used with a rotating magnetized pole wheel.

Product Name	Product Type	Ordering Code	Package
TLE4966-2K	Double Hall Switch	SP000788888	PG-TSOP6-6-5

1.3 Pin Configuration (top view)



PG-TSOP6-6-5

Figure 1 Pin Definition and Center of Sensitive Area

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Function
1	Q2	Speed 2
2	GND	Recommended connection to GND
3	Q1	Speed 1
4	V_{DD}	Supply voltage
5	GND	Recommended connection to GND
6	GND	Ground

2 General

2.1 Block Diagram

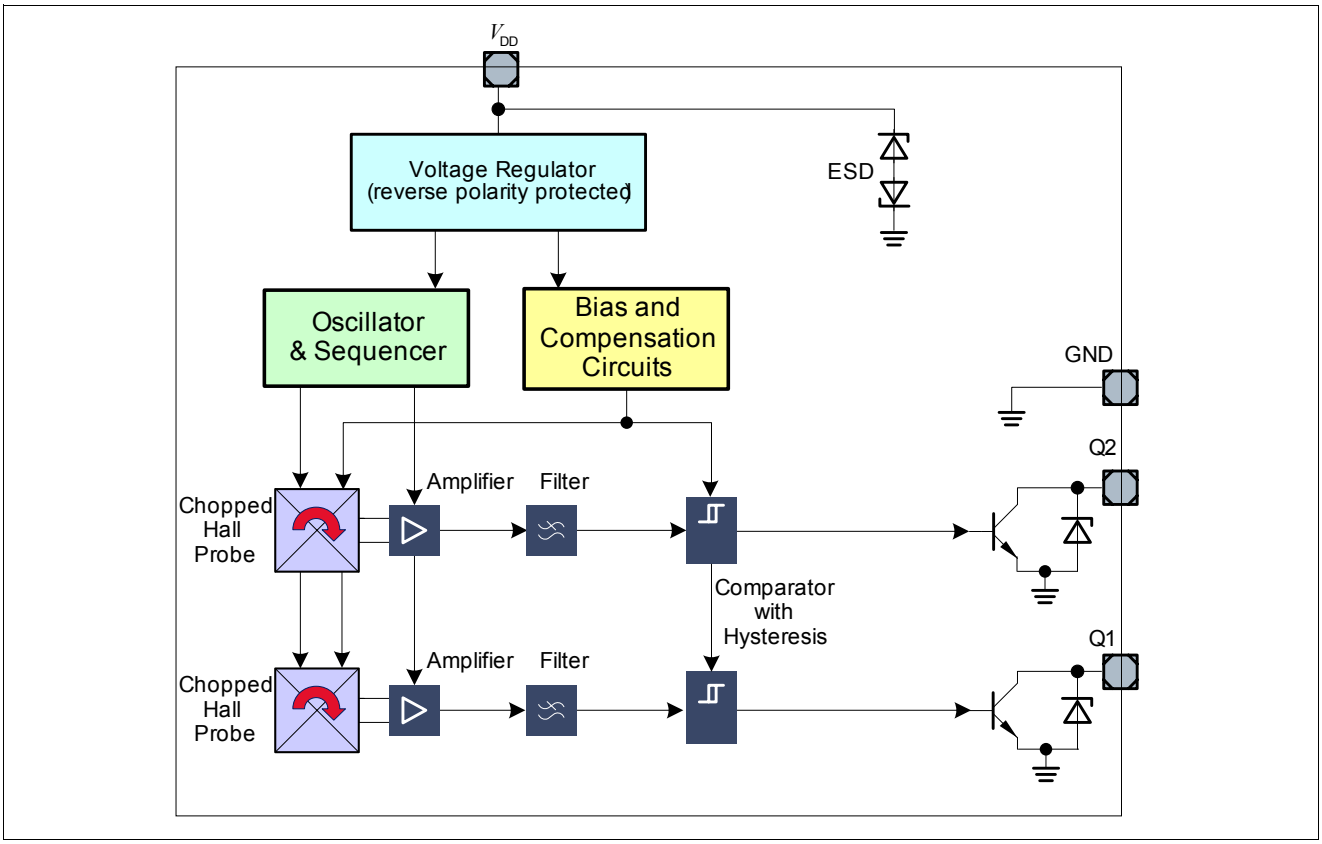


Figure 2 Block Diagram

2.2 Circuit Description

The chopped Dual Hall Switch comprises two Hall probes, bias generator, compensation circuits, oscillator, and output transistors.

The bias generator provides currents for the Hall probes and the active circuits. Compensation circuits stabilize the temperature behavior and reduce influence of technology variations.

The Active Error Compensation rejects offsets in signal stages and the influence of mechanical stress to the Hall probes caused by molding and soldering processes and other thermal stresses in the package. This chopper technique together with the threshold generator and the comparator ensures high accurate magnetic switching thresholds.

2.3 Application Circuit

It is recommended to use a series resistor R_S with 200Ω and a capacitor of C_S = 4.7nF for protection against overvoltage and transients on the supply line. Pull-up resistors R_L are required for the output pins Q_1 and Q_2.

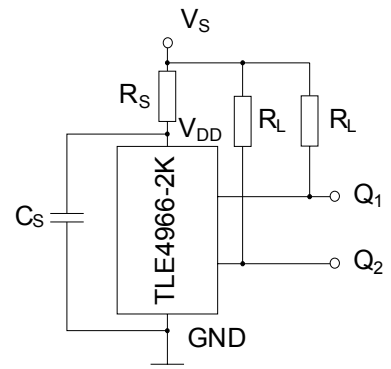


Figure 3 Application Circuit

3 Maximum Ratings

Table 2 Absolute Maximum Ratings
T_j = -40°C to 150°C

Parameter	Symbol	Limit Values		Unit	Conditions
		min.	max.		
Supply voltage	V_{DD} V_s V_s	-18 -18 -18	18 24 26	V	 for 1 h, $R_S \geq 200\ \Omega$ for 5 min, $R_S \geq 200\ \Omega$
Supply current through protection device	I_{DD}	-50	50	mA	
Output voltage	V_Q	-0.7 -0.7	18 26	V	 for 5 min @ 1.2 kΩ pull up
Continuous output current	I_Q	-50	50	mA	
Junction temperature	T_j	– – – –	155 165 175 195	°C	for 2000 h (not additive) for 1000 h (not additive) for 168 h (not additive) for 3 x 1 h (additive)
Storage temperature	T_S	-40	150	°C	
Magnetic flux density	B	–	unlimited	mT	

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 3 ESD Protection [1)]

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
ESD voltage	V_{ESD}	–	±4	kV	HBM, R = 1.5 kΩ, C = 100 pF T_A = 25°C

1) Human Body Model (HBM) tests according to: EOS/ESD Association Standard S5.1-1993 and Mil. Std. 883D method 3015.7

4 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE4966-2K. All parameters specified in the following sections refer to theses operating conditions unless otherwise mentioned.

Table 4 Operating Range

Parameter	Symbol	Limit Values			Unit	Conditions
		min.	typ.	max.		
Supply voltage	V_{DD} V_S V_S	2.7 – –	– – –	18 24 26	V	 1 h with $R_S \geq 200\ \Omega$ for 5 min $R_S \geq 200\ \Omega$
Output voltage	V_Q	-0.7	–	18	V	
Junction temperature	T_j	-40 –	– –	150 175	°C	 for 168 h
Output current	I_Q	0	–	10	mA	

5 Electrical and Magnetic Parameters

Product characteristics involve the spread of values guaranteed within the specified voltage and temperature range. Typical characteristics are the median of the production.

Table 5 Electrical Characteristics [1)]

Parameter	Symbol	Limit Values			Unit	Conditions
		min.	typ.	max.		
Supply current	I_{DD}	4	5.2	7	mA	V_{DD} = 2.7 V ... 18 V
Reverse current	I_{SR}	0	0.2	1	mA	V_{DD} = -18 V
Output saturation voltage	V_{QSAT}	–	0.3	0.6	V	I_Q = 10 mA
Output leakage current	I_{QLEAK}	–	0.05	10	µA	for V_Q = 18 V
Output fall time	t_f	–	0.2	1	µs	R_L = 1.2 kΩ; C_L < 50 pF see: Figure 4 on Page 11
Output rise time	t_r	–	0.2	1	µs	
Chopper frequency	f_{OSC}	–	320	–	kHz	
Switching frequency	f_{SW}	0	–	15 [2)]	kHz	
Delay time [3)]	t_d	–	13	–	µs	
Count Signal Delay	t_{dc}	50	200	1000	ns	
Output jitter [4)]	t_{QJ}	–	1	–	$µs_{RMS}$	Typ. value for square wave signal 1 kHz
Repeatability of magnetic thresholds [5)]	B_{REP}	–	40	–	$µT_{RMS}$	Typ. value for $\Delta B/\Delta t$ > 12 mT/ms
Power-on time [6)]	t_{PON}	–	13	–	µs	$V_{DD} \geq$ 2.7 V
Distance of hall plates	d_{HALL}	–	1.45	–	mm	
Thermal resistance [7)]	R_{thJA}	–	100	–	K/W	PG-TSOP6-6-5

1) over operating range, unless otherwise specified. Typical values correspond to V_{DD} = 12 V and T_A = 25°C
2) To operate the sensor at the max. switching frequency, the magnetic signal amplitude must be 1.4 times higher than for static fields. This is due to the -3 dB corner frequency of the low pass filter in the signal path.
3) Systematic delay between magnetic threshold reached and output switching
4) Jitter is the unpredictable deviation of the output switching delay
5) B_{REP} is equivalent to the noise constant
6) Time from applying $V_{DD} \geq$ 2.7 V to the sensor until the output state is valid
7) Thermal resistance from junction to ambient

Calculation of the ambient temperature (PG-TSOP6-6-5 example)

e.g. for V_{DD} = 12.0 V, I_{DDtyp} = 5.5 mA, $V_{QSATtyp}$ = 0.3 V and 2 x I_Q = 10 mA :
Power Dissipation: P_{DIS} = 72.0 mW.
In $T_A = T_j - (R_{thJA} \times P_{DIS})$ = 175°C – (100 K / W × 0.072 W)
Resulting max. ambient temperature: T_A = 167.8°C

Table 6 Magnetic Characteristics [1].

Parameter	Symbol	T_j [°C]	Limit Values			Unit	Conditions
			min.	typ.	max.		
Operate point	B_{OP1}, B_{OP2}	-40 25 150	5.2 5.0 4.7	7.7 7.5 7.1	10.3 10.0 9.5	mT	B_{OP1} for Hall element 1 B_{OP2} for Hall element 2
Release point	B_{RP1}, B_{RP2}	-40 25 150	-10.3 -10.0 -9.5	-7.7 -7.5 -7.1	-5.2 -5.0 -4.7	mT	B_{RP1} for Hall element 1 B_{RP2} for Hall element 2
Hysteresis	B_{HYS1}, B_{HYS2}	-40 25 150	– 10.0 –	– 15.0 –	– 20.0 –	mT	$B_{HYS1} = B_{OP1} - B_{RP1}$ $B_{HYS2} = B_{OP2} - B_{RP2}$
Magnetic matching	B_{MATCH}	-40 25 150	– -2.0 –	– 0 –	– 2.0 –	mT	Valid for $B_{OP1} - B_{OP2}$ and $B_{RP1} - B_{RP2}$
Magnetic offset	B_{OFF1}, B_{OFF2}	-40 25 150	– -2.0 –	– 0 –	– 2.0 –	mT	$B_{OFF1} = (B_{OP1} + B_{RP1})/2$ $B_{OFF2} = (B_{OP2} + B_{RP2})/2$
Temperature compensation of magnetic thresholds	TC	–	–	-350	–	ppm/°C	

1) over operating range, unless otherwise specified. Typical values correspond to V_{DD} = 12 V

Note: Typical characteristics specify mean values expected over the production spread.

Field Direction Definition

Positive magnetic fields related with south pole of the magnet to the branded side of package.

6 Timing Diagrams for the Speed Outputs

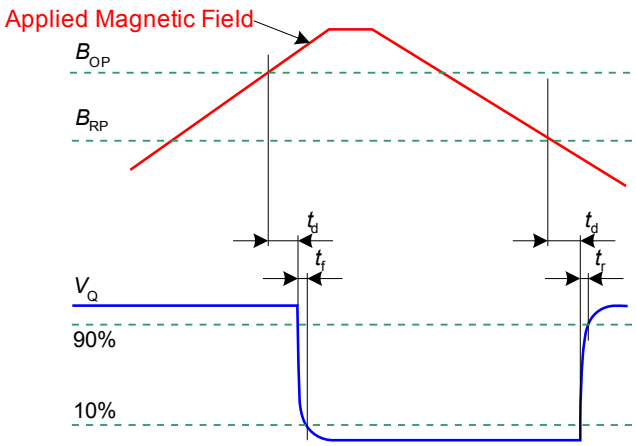


Figure 4 Timing Definition of the Speed Signal

7 Package Information

7.1 Package Marking

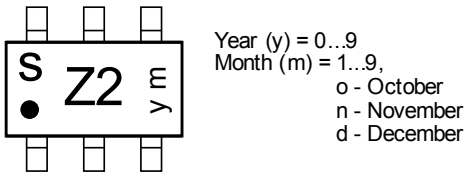


Figure 5 **Marking PG-TSOP6-6-5**

7.2 Distance between Chip and Package Surface

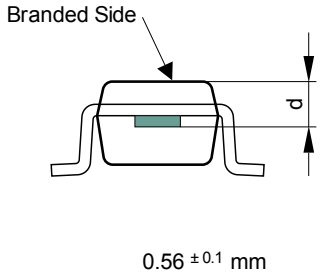


Figure 6 **Distance Chip to Upper Side of IC**

7.3 Package Outlines

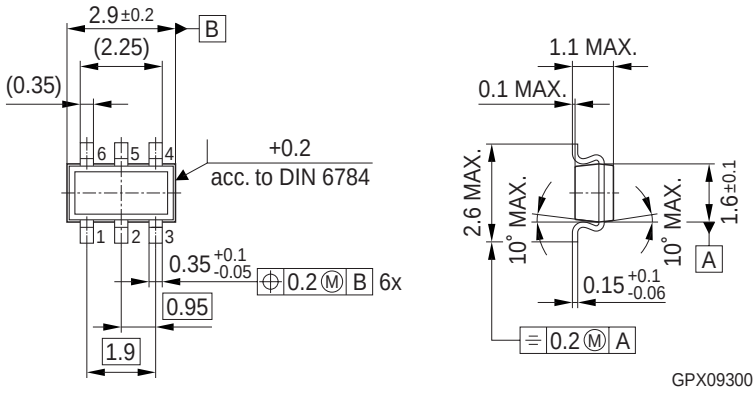


Figure 7 **PG-TSOP6-6-5** (Plastic Thin Small Outline Package)

PCB Footprint for PG-TSOP6-6-5

The following picture shows a recommendation for the PCB layout.

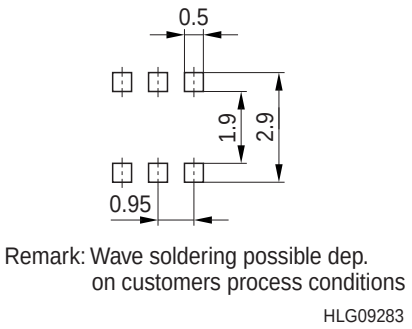


Figure 8 Footprint PG-TSOP6-6-5

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