TDF10A01

100V, 1A Constant Frequency Synchronous Buck Regulator

Features

- Wide input voltage range: 4.2 V to 100 V
- Constant frequency current-mode control with 40 ns minimum on-time
- Frequency settings from 200 kHz to 2.25 MHz
- Selectable forced CCM or high-efficiency PFM operation with diode emulation (I_Q<10 µA)
- On-the-fly frequency and mode setting with automatic voltage loop compensation
- Internal 5 ms soft-start timer
- Low Shutdown Current: <1 µA
- Precision 0.8 V ± 1 % feedback reference
- Optional bypass LDO input for highest efficiency
- Optional Power Good Output
- Programmable input undervoltage lockout
- Over-/Negative current and Overtemperature Protection
- Wide operating temp: -40 °C ≤ T_J ≤ 150 °C
- Synchronizable to an external clock or optional low-EMI spread spectrum (QFN package)
- On-the-fly V_{OUT} adjust (QFN package)
- VSON8 (4x4), DSO8 and QFN13 (3x3) packages

Potential Applications

- Telecom-/AI-/Brick-Power-Modules, bias supplies
- Industrial/Medical equipment
- Battery-powered systems, Motor drives: LEV, e-Bike & - Scooter, Drones
- Distributed point of load power systems

Description

The TDF10A01 is a fully integrated and highly efficient synchronous buck regulator which offers simplicity, performance and ruggedness for a wide variety of applications. Featuring a high-speed current mode control architecture, the TDF10A01 supports direct step-down conversion from high voltage with unparalleled solution size and efficiency, while constant frequency operation makes the TDF10A01 an excellent choice for EMI-sensitive applications.

Dual light-load operating modes and programmable switching frequency allow the TDF10A01 to be tailored to the needs of each application. For the highest efficiency, a bypass bias regulator can be used to bootstrap the internal bias and gate drive from the regulated output voltage.

For the most EMI-sensitive applications, the TDF10A01 offers PLL synchronization to an external clock or low-EMI spread-spectrum operation. For gate-drive bias supplies, a unique on-the-fly V_{OUT} adjustment can be used to reduce light-load power loss. Protection features such as pre-bias start-up, over/negative current and over voltage protection, and thermal shutdown ensure reliable operation.

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

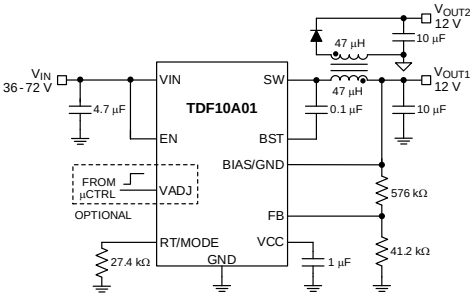

Figure 1 Isolated Buck Bias Supply

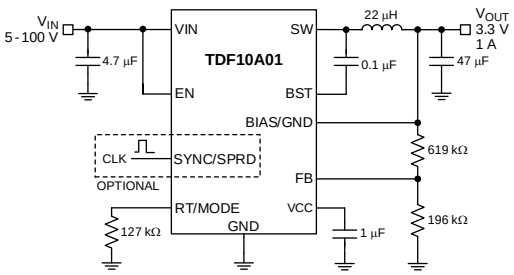

Figure 2 High-Efficiency Buck Regulator

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1 Feature comparison for TDF10A01 family

Table 1. Feature Comparison

Product Name	Package Type	Output Current	Bias Reg	PGOOD	VADJ	SYNC/SPRD
TDF10A01BG	PG-VSON-8-5	1 A	YES	NO	NO	NO
TDF10A01BF	PG-DSO-8-101	1 A	YES	NO	NO	NO
TDF10A01BVQ	PG-VQFN-13-1	1 A	YES	NO	YES	YES
TDF10A01PG	PG-VSON-8-5	1 A	NO	YES	NO	NO
TDF10A01PF	PG-DSO-8-101	1 A	NO	YES	NO	NO
TDF10A01PBQ	PG-VQFN-13-1	1 A	YES	YES	NO	YES

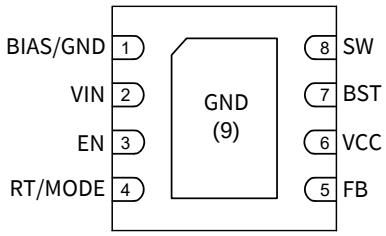
2 Ordering information

Table 2. Ordering Information

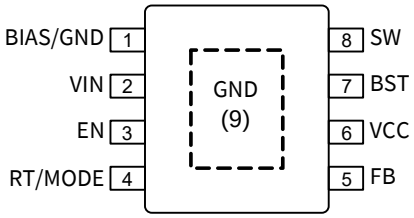
Product Name	Package Type	Standard Pack Form and Qty		Orderable Part Number
TDF10A01BG	PG-VSON-8-5	Tape and Reel	5000	TDF10A01BGxxxxx
TDF10A01BF	PG-DSO-8-101	Tape and Reel	2500	TDF10A01BFxxxxx
TDF10A01BVQ	PG-VQFN-13-1	Tape and Reel	4000	TDF10A01BVQxxxxx
TDF10A01PG	PG-VSON-8-5	Tape and Reel	5000	TDF10A01PGxxxx
TDF10A01PF	PG-DSO-8-101	Tape and Reel	2500	TDF10A01PFxxxx
TDF10A01PBQ	PG-VQFN-13-1	Tape and Reel	4000	TDF10A01PBQxxxx

3 Pin configurations

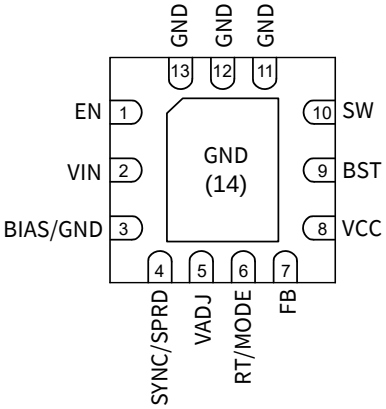
TDF10A01BG
VSON-8 (4 mm x 4 mm)



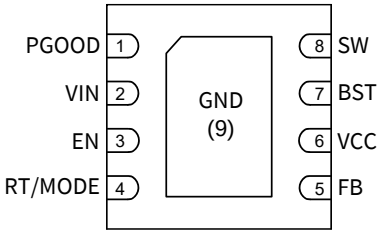
TDF10A01BF
DSO-8 (3.9 mm x 4.9 mm)



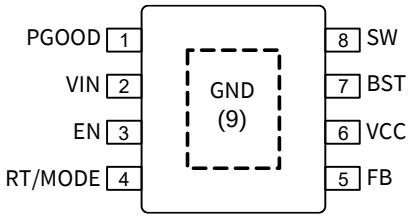
TDF10A01BVQ
VQFN-13 (3 mm x 3 mm)



TDF10A01PG
VSON-8 (4 mm x 4 mm)



TDF10A01PF
DSO-8 (3.9 mm x 4.9 mm)



TDF10A01PBQ
VQFN-13 (3 mm x 3 mm)

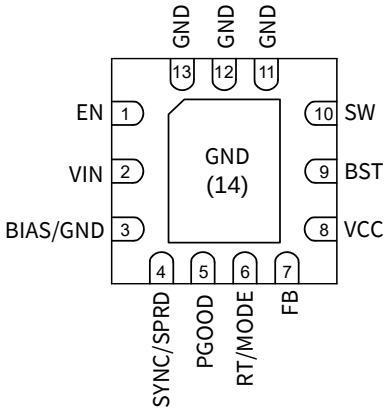


Figure 3 Pin Configuration (Top transparent view)

4 Functional block diagram

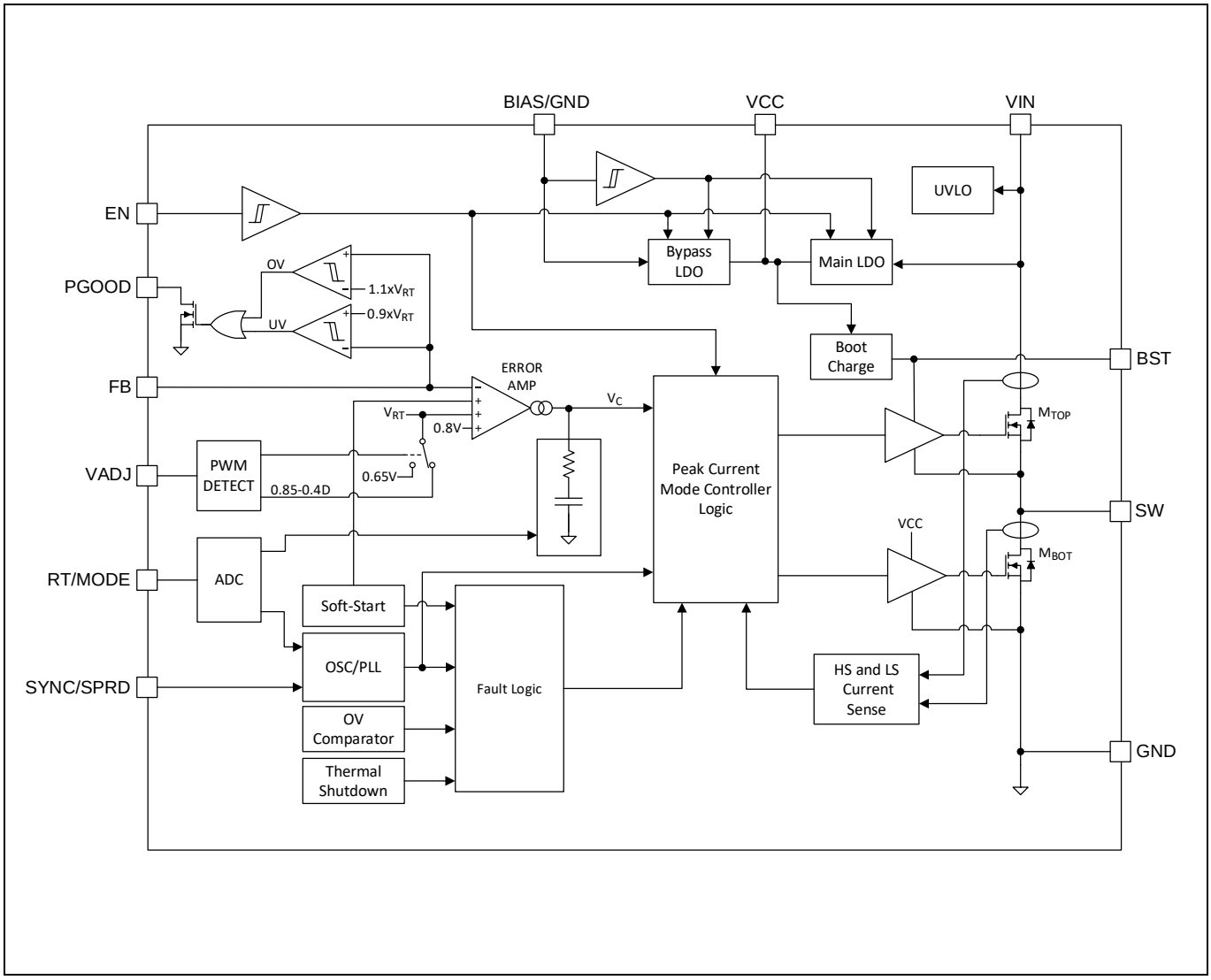


Figure 4 Block diagram

5 Pin descriptions

Note: I = Input, O = Output; [A] = Analog, [D] = Digital, [P] = Power

Pin VSON8/ DSO8	Pin QFN13	Pin Name	Type	Pin Description
1	3	BIAS/GND	I [P]	Optional input voltage to second LDO. This LDO supplies VCC voltage from the BIAS/GND pin, bypassing the VIN-powered LDO to reduce power dissipation. Connect BIAS/GND to a voltage between 3V and 24V or tie to GND if not used.
1	5	PGOOD	O [D]	Open-drain power good indicator. When the FB pin is outside of regulation, this pin is pulled low.
2	2	VIN	I [P]	Main input voltage that supplies power to the internal high-side power MOSFET and LDO that generates VCC. Place decoupling capacitors close to this pin and connect using a wide PCB trace to VIN and multiple vias to the GND plane.
3	1	EN	I [A]	Enable Input. EN can be driven directly by logic to turn the regulator on and off. Place a resistor divider between VIN and GND on the EN pin to implement an input undervoltage lockout. Tie EN directly to VIN to always enable the regulator.
4	6	RT/MODE	I [A]	Frequency and mode selection pin. Connect a resistor from this pin to GND to program the switching frequency and choose the light-load operating mode.
5	7	FB	I [A]	Output voltage feedback pin. Connect this pin to the output of the regulator via a resistor divider to set the output voltage.
6	8	VCC	O [P]	Internal 3V LDO output. The driver and control circuits are powered from this voltage. Decouple with a 1 µF ceramic capacitor as close to the VCC pin as possible.
7	9	BST	I [P]	Bootstrap supply input. Connect a 0.1 µF ceramic capacitor between BST and SW and close to the BST pin to form a floating supply across the high-side MOSFET driver.
8	10	SW	O [P]	Power switch output. Connect SW to the inductor and bootstrap supply capacitor. SW is driven internally between VIN and GND. Use wide PCB traces when connecting to SW.
9	11-14	GND		System Ground. Use multiple vias to one or more ground planes for good electrical and thermal performance.
	4	SYNC/SPRD	I [D]	Oscillator synchronization and spread-spectrum control input. Tie to an external TTL-compatible clock to enable PLL synchronization of the regulator switching frequency, or tie to VCC to enable low-EMI spread-spectrum mode. Tie to GND if not used.
	5	VADJ	I [D]	Output voltage adjustment control input. When VADJ is TTL high, the output of the regulator is reduced to 81% of its normal level. A PWM signal on this pin adjusts the regulator output based on the duty cycle of the incoming PWM signal. There is a 200 kΩ internal pull-down on VADJ to GND.

6 Absolute maximum ratings

Table 3. Absolute maximum ratings

Description	Min	Max	Unit	Conditions
VIN, EN to GND	-0.3	120	V	
BST to GND	-0.3	120	V	
BIAS/GND to GND	-0.3	27	V	
VCC to GND	-0.3	4.0	V	
BST to SW	-0.3	4.0	V	
SYNC/SPRD, FB, VADJ, RT/MODE to GND	-0.3	4.0	V	
PGOOD to GND	-0.3	27	V	
Storage Temperature Range	-55	150	°C	
Junction Temperature Range	-40	150	°C	

Attention: ***Stresses beyond these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.***

7 Thermal characteristics

7.1 Thermal characteristics

Description	Symbol	VDSON-8	DSO-8	VQFN-13	Units	Test Conditions
Junction to Case Bottom Thermal Resistance	θ_{JC-B}	4.3	7.7 (TBD)	4.7	°C/W	Bottom
Junction to Case Top Thermal Resistance	θ_{JC-T}	39	66	50	°C/W	Top
Junction to Ambient Thermal Resistance	θ_{JA-JD}	42	44 (TBD)	53	°C/W	On JEDEC Board, Note **1**
Junction to Ambient Thermal Resistance	θ_{JA-DB}	32 (TBD)	28 (TBD)	40 (TBD)	°C/W	On Demo Board, Note **2**

Note:

1. *Device on 76.2 mm x 114.3 mm x 1.5 mm PCB (JEDEC 2s2p) with 6 cm^2 copper area for GND connection, vertical in still air.*
2. *Thermal resistance is measured with components mounted on a standard EVAL_TBD demo board, vertical in still air.*

8 Electrical specifications

8.1 Recommended operating conditions

Description	Min	Max	Unit	Note
VIN Voltage Range	4.2	100	V	
BIAS/GND Voltage Range	0	24	V	
SYNC/SPRD, VADJ Voltage Range	0	3.3	V	
PGOOD Voltage Range	0	24	V	
Output Voltage Range	0.8	100	V	Note **3**
Continuous Output Current		1	A	
Switching Frequency	200	2250	kHz	
Operating Junction Temperature	-40	150	°C	

Note:

3. *In typical application circuit. The minimum and maximum output voltages are also limited by the minimum on-time and the minimum off-time.*

8.2 Electrical characteristics

Note: Unless otherwise specified, V_{IN} = 12 V, EN = 2V, R_T = 48.7 kΩ. Typical values are specified at T_J = 25 °C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Current and UVLO						
VIN Shutdown Supply Current	$I_{IN(SD)}$	EN = 0 V, T_J = 25 °C		0.5	2	µA
	$I_{IN(SD)}$	EN = 0 V, -40°C ≤ T_J ≤ 150°C		0.5	80	µA
VIN Static Supply Current	$I_{IN(Static)}$	EN = 2 V, FCCM Mode, No switching		740	900	µA
VIN Sleep Supply Current	$I_{IN(Sleep)}$	EN = 2 V, PFM Mode, No switching, T_J = 25 °C		10	13	µA
VIN UVLO Rising Threshold	$V_{TH(UV\_R)}$		4.15	4.30	4.50	V
VIN UVLO Falling Threshold	$V_{TH(UV\_F)}$		3.9	4.0	4.1	V
EN Rising Threshold	$V_{TH(EN\_R)}$		1.14	1.20	1.26	V
EN Falling Threshold	$V_{TH(EN\_F)}$		1.04	1.10	1.16	V
EN Shutdown Threshold	$V_{TH(SD\_R)}$	EN voltage falling		0.5		V
Internal Regulators						
VCC LDO Output Voltage	$V_{CC(REG)}$	Internally loaded only	2.85	3.0	3.15	V
VCC UVLO Rising Threshold	$V_{CC(UV\_R)}$		2.6	2.7	2.8	V
VCC UVLO Falling Threshold	$V_{CC(UV\_F)}$		2.5	2.6	2.7	V
BIAS Rising Switchover Voltage	$V_{BIAS(SO\_R)}$		2.9	3.0	3.1	V
BIAS Falling Switchover Voltage	$V_{BIAS(SO\_F)}$		2.8	2.9	3.0	V
Feedback and Soft Start						
FB Regulation Voltage	$V_{FB(REG)}$	In test circuit, No switching, line and load variation included.	0.792	0.800	0.808	V
FB Input Bias Current	$I_{FB(LEAK)}$		-50		50	nA
FB Regulation, VADJ Active	$V_{FB,ADJ}$	VADJ = 2 V, In test circuit	0.630	0.650	0.670	V
	$V_{FB,\ ADJ25\%}$	VADJ = PWM, DC = 25 %, F = 100 kHz	0.726	0.750	0.774	V
	$V_{FB,\ ADJ75\%}$	VADJ = PWM, DC = 75 %, F = 100 kHz	0.533	0.550	0.567	V
VADJ Threshold Voltage	$V_{IH(ADJ)}$		2			V
	$V_{IL(ADJ)}$				0.8	V
VADJ PWM Frequency Range			100		1000	kHz
Internal Soft-Start Time	t_{SS}		3.5	5	6.5	ms
Switching Frequency						
Switching Frequency Presets	$F_{SW(PS1)}$	R_{RT} = 226 kΩ for PFM Mode R_{RT} = 59 kΩ for FCCM Mode	170	200	230	kHz

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
	$F_{SW(PS2)}$	R_{RT} = 187 kΩ for PFM Mode R_{RT} = 48.7 kΩ for FCCM Mode	255	300	345	kHz
	$F_{SW(PS3)}$	R_{RT} = 154 kΩ for PFM Mode R_{RT} = 40.2 kΩ for FCCM Mode	340	400	460	kHz
	$F_{SW(PS4)}$	R_{RT} = GND for PFM Mode R_{RT} = VCC for FCCM Mode	468	550	633	kHz
	$F_{SW(PS5)}$	R_{RT} = 127 kΩ for PFM Mode R_{RT} = 33.2 kΩ for FCCM Mode	638	750	863	kHz
	$F_{SW(PS6)}$	R_{RT} = 105 kΩ for PFM Mode R_{RT} = 27.4 kΩ for FCCM Mode	850	1000	1150	kHz
	$F_{SW(PS7)}$	R_{RT} = 86.6 kΩ for PFM Mode R_{RT} = 22.6 kΩ for FCCM Mode	1275	1500	1725	kHz
	$F_{SW(PS8)}$	R_{RT} = 71.5 kΩ for PFM Mode R_{RT} = 18.7 kΩ for FCCM Mode	1912	2250	2588	kHz
Synchronization and Spread Spectrum						
Sync Input Frequency Range	F_{SYNC}	SYNC/SPRD = Ext Clock	200		2250	kHz
Sync Input Duty Cycle Range	D_{SYNC}	SYNC/SPRD = Ext Clock	10		90	%
Sync Input Threshold Voltage	$V_{IH(SYNC)}$		2			V
	$V_{IL(SYNC)}$				0.8	V
Spread Spectrum Frequency (Relative to F_{SW} Preset)	$F_{SSM(MIN)}$	SYNC/SPRD = VCC, Minimum Freq		0		%
	$F_{SSM(MAX)}$	SYNC/SPRD = VCC, Maximum Freq		20		%
Power Stage Operation						
Top MOSFET On-Resistance	$R_{ON(TOP)}$	$V_{BST} - V_{SW}$ = 3 V, I_{SW} = 0.5 A		830		mΩ
Bottom MOSFET On-Resistance	$R_{ON(BOT)}$	I_{SW} = 0.5 A		440		mΩ
Minimum SW voltage On Time	$T_{ON(MIN)}$	FCCM Mode, SW > VIN/2		40	60	ns
Minimum SW voltage Off Time	$T_{OFF(MIN)}$	FCCM Mode, SW > VIN/2		80		ns
BST UVLO Rising Threshold	V_{BST_R}	BST-SW voltage rising	2.1	2.3	2.5	V
BST UVLO Falling Threshold	V_{BST_F}	BST-SW voltage falling	2.0	2.2	2.4	V
Protection Features						
High-Side Peak Current Limit	$I_{LIM(PK)}$		1.35	1.50	1.65	A
Low-Side Valley Current Limit	$I_{LIM(VA)}$		1.44	1.60	1.76	A
Low-Side Reverse Current Limit	I_{REV}			-600		mA
FB OVP Fault Rising Threshold	V_{OVP_R}	V_{FB} Rising	109	110	111	%
FB OVP Fault Falling Threshold	V_{OVP_F}	V_{FB} Falling	106.5	107.5	108.5	%
FB OVP Fault Delay	t_{OVP}			1		µs
Thermal Shutdown	T_{OTP}	**Note 4**		175		°C
Thermal Hysteresis	$T_{OTP(HYS)}$	**Note 4**		20		°C

Power Good						
PGOOD Voltage Low		I_{PGOOD} = 2 mA		0.2	0.4	V
PGOOD Leakage Current		V_{PGOOD} = 3.3 V			1	µA
PGOOD Overvoltage Threshold (Relative to Regulated FB)		V_{FB} Rising, VADJ = 0 V	109	110	110	%
		V_{FB} Rising, VADJ active	108	110	112	%
		Hysteresis		2.5		%
PGOOD Undervoltage Threshold (Relative to Regulated FB)		V_{FB} Falling, VADJ = 0 V	89	90	91	%
		V_{FB} Falling, VADJ active	88	90	92	%
		Hysteresis		2.5		%
PGOOD Delay		Rising or Falling		50		µs

Note:

4. Guaranteed by construction and not tested in production.

9 Functional Description

9.1 Constant Frequency Current Mode Control (VIN, SW and FB Pins)

The TDF10A01 is a high-efficiency, synchronous step-down DC/DC converter with integrated top (high-side) and bottom (synchronous) MOSFET switches. These high-voltage MOSFETs are switched using a constant frequency peak current mode control scheme, which comprises an outer voltage loop and an inner current loop. The voltage loop regulates V_{OUT} using an internal transconductance error amplifier, which senses V_{OUT} using a resistor divider on the FB pin. This amplifier produces an internal error or control voltage (V_C) which is used by the current loop to set the peak inductor current on a cycle-by-cycle basis. Overall voltage loop regulation is then achieved as the error amplifier demands a peak current that exactly corresponds to the load demand on V_{OUT}.

The current loop operates via the accurate and high-speed sensing and control of the current in the top MOSFET (M_{TOP}). At the beginning of each clock cycle, M_{TOP} turns on, causing the inductor current to ramp up. When the current in the M_{TOP} exceeds the peak level that is demanded by the error amplifier (V_C), the M_{TOP} turns off and the bottom MOSFET (M_{BOT}) turns on, causing the inductor current to ramp back down. The stability of this current loop is ensured using a proprietary internal ramp compensation, and the value of the peak inductor current is limited internally between -0.3 A and 1.5 A.

The TDF10A01 automatically adjusts internal voltage loop compensation settings based on the switching frequency as selected by the RT/MODE pin. This provides for a superb transient response that is optimized for the selected switching frequency.

Unlike many products that make use of a voltage-mode constant-on-time (COT) architecture, no external compensation or stabilizing components of any kind are required. Moreover, loop stability is inherently maintained even with large values of output capacitance.

9.2 Enable and Soft-Start Sequence (EN Pin)

The EN pin provides on/off control of the device. When the EN pin voltage is less than 0.45V, the TDF10A01 will be in a low-power shutdown state where the V_{IN} supply current is reduced to under 1 µA. When EN is greater than 0.45V, a precision internal undervoltage lockout (UVLO) circuit is activated which monitors the voltage on the EN and VIN pins and the internal LDO begins to generate bias voltage on the VCC pin. Once the EN pin voltage exceeds 1.2 V and the VIN pin voltage exceeds 4.3 V, the device begins its start-up sequence to produce the desired voltage at the output of the DC/DC converter.

An internal 5 ms soft-start ramp limits the rise time of V_{OUT} to prevent excessive input current during start-up. During soft-start, the operating mode is forced into pulse-skipping or diode emulation mode (DEM) to avoid discharging a pre-biased output voltage. Once the output voltage is in regulation, the TDF10A01 will resume the operating mode set by state of the RTMODE pin. The internal soft-start ramp is quickly reset in the event of a shutdown, under-voltage or fault condition.

9.3 Internal Bias Regulators (VIN, BIAS/GND, VCC and BST Pins)

In addition to providing power to the high-side power switch (M_{TOP}), the VIN pin also serves as an input to an internal high-voltage LDO that produces 3 V on the VCC pin. This voltage is used for internal chip bias as well as gate drive for low-side power switch M_{BOT}. A precision UVLO circuit monitors the VCC pin voltage to ensure that it is adequate before switching is allowed.

The TDF10A01 also offers an optional bypass LDO that receives input voltage from the BIAS/GND pin. In most applications, this pin can simply be tied directly to the output of the DC/DC converter to achieve high-efficiency bootstrapping of the bias and gate drive power. Whenever the voltage on BIAS/GND is adequate, the TDF10A01 will automatically switch over to using the bypass LDO and disable the main LDO, and it will switch back to the main LDO if the BIAS/GND voltage falls below the required level. While this bypass LDO is important for the highest possible efficiency when operating at high input voltages, it is not required for proper operation, and the BIAS/GND pin can be tied to GND if not needed.

Gate drive voltage for M_{TOP} is supplied by the floating supply (C_{BST}) that is between the BST and SW pins. An internal bootstrap charging circuit charges the C_{BST} capacitor from the VCC pin whenever M_{BOT} is on. Internal logic together with a floating UVLO ensure that this voltage is always adequate for safe operation. Special circuitry monitors the bootstrap charging current to ensure safe startup into a pre-biased output voltage, even when operating in near drop-out conditions.

9.4 Switching Frequency and Light Load Operating Mode (RT/MODE Pin)

The switching frequency and light load operating mode are both set using the RT/MODE pin as described in **Error! Reference source not found.** of Application Information section. The switching frequency can be set to any one of eight pre-selected frequencies between 200 kHz and 2.25 MHz. The TDF10A01 also features two light load operating modes: Forced Continuous-Conduction (FCCM) mode and high-efficiency Pulse-Frequency Modulation (PFM) Mode. PFM mode is selected when using R_T values greater than 70 kΩ, and FCCM mode is selected when using R_T values less than 70 kΩ.

In FCCM mode, the bottom MOSFET (M_{BOT}) will generally be on whenever the top MOSFET (M_{TOP}) is off, even if the inductor current reverses and goes negative. If the reverse current in the bottom switch exceeds -0.6 A, then a reverse over-current trip will turn off M_{BOT} and turn on M_{TOP} to prevent a large reverse current in M_{BOT}.

In PFM mode, the bottom MOSFET emulates an ideal diode by turning off the MOSFET to avoid reverse current conduction. In addition, PFM mode forces a minimum peak inductor current, regardless of the demand on V_{OUT}. As a result, when the load current decreases below approximately 100mA, the TDF10A01 will begin cycling between sleep and wake states to reduce the effective switching frequency. When the sleep state is active, both power switches are off, and the VIN pin current is reduced to less than 10 μA.

Note that the RT/MODE pin is continuously monitored, so that a change in the state of the pin will result in a corresponding change in switching frequency and/or operating mode. This allows for on-the-fly changes if required for a particular application. In addition, the switching frequency that is selected by the RT/MODE pin is used to internally adjust the voltage loop compensation to ensure optimum voltage loop performance and stability.

When synchronized by an external clock on the SYNC/SPRD pin, or when the VADJ feature is active, the TDF10A01 will automatically operate in FCCM mode, even if PFM mode is selected by the RT/MODE pin.

9.5 External Synchronization and Spread-Spectrum Modulation (SYNC/SPRD Pin)

The SYNC/SPRD pin is dual-use and allows either synchronization of the internal clock to an external clock or the ability to operate with a low-EMI spread spectrum modulation of the internal clock. When the SYNC/SPRD pin is grounded, the TDF10A01 simply operates at the free-running switching frequency as set by the RT/MODE pin. If an external clock is detected on the SYNC/SPRD pin, the internal phase-locked loop (PLL) is activated, and the internal switching frequency and phase will gradually shift until the rising edge of the SW pin voltage aligns with the rising edge of the external clock. After synchronization, if the external clock is removed (SYNC/SPRD = GND)

for more than approximately 16 µs, the internal switching frequency will gradually return to the free-running switching frequency. This smooth engaging and disengaging of the PLL ensures that there is minimal perturbation on VOUT. When synchronized, the TDF10A01 will operate in FCCM mode so that the frequency content will be well-defined even during light load operation.

Note that the free-running switching frequency selected by the RT/MODE pin is used to set the voltage loop compensation. To ensure adequate voltage loop compensation, the frequency of the external clock on the SYNC/SPRD pin should be no more than 30% higher than the free-running frequency set by the RT/MODE pin.

When the SYNC/SPRD pin is tied to VCC, spread spectrum modulation is activated. The TDF10A01 uses a proprietary method to evenly vary the switching frequency over a range that varies between the nominal free-running frequency (F_{NOM}) and 1.2 x F_{NOM}. This method achieves a uniform spread of EMI energy that enables a well-designed application circuit to readily pass difficult EMI specifications, such as CISPR 25.

9.6 On-the-Fly Output Voltage Adjust (VADJ Pin)

The VADJ pin allows for on-the-fly adjustments of the regulated output voltage by modifying the reference voltage into the Error Amplifier (EA). Changes to the target regulation level are made gradually, with a time constant of approximately 160 µs. In addition, the internal over-voltage and PGOOD detection levels are adjusted along with the EA reference voltage to avoid unwanted over-voltage or PGOOD trips. When VADJ is tied to VCC, the EA reference is decreased to 81 % of its nominal value, or 0.65 V. A PWM signal can also be applied to VADJ, in which case the EA reference (V_{REF}) is reduced by an amount that is proportional to the duty cycle (D) of the signal on VADJ. For 0 < D < 1, V_{REF} will vary with D as follows:

$$V_{FB(ADJ)} = 0.79 + \frac{\tanh 5D}{17} - 0.4D$$

$$\cong MIN(0.8, 0.85 - 0.4D)$$

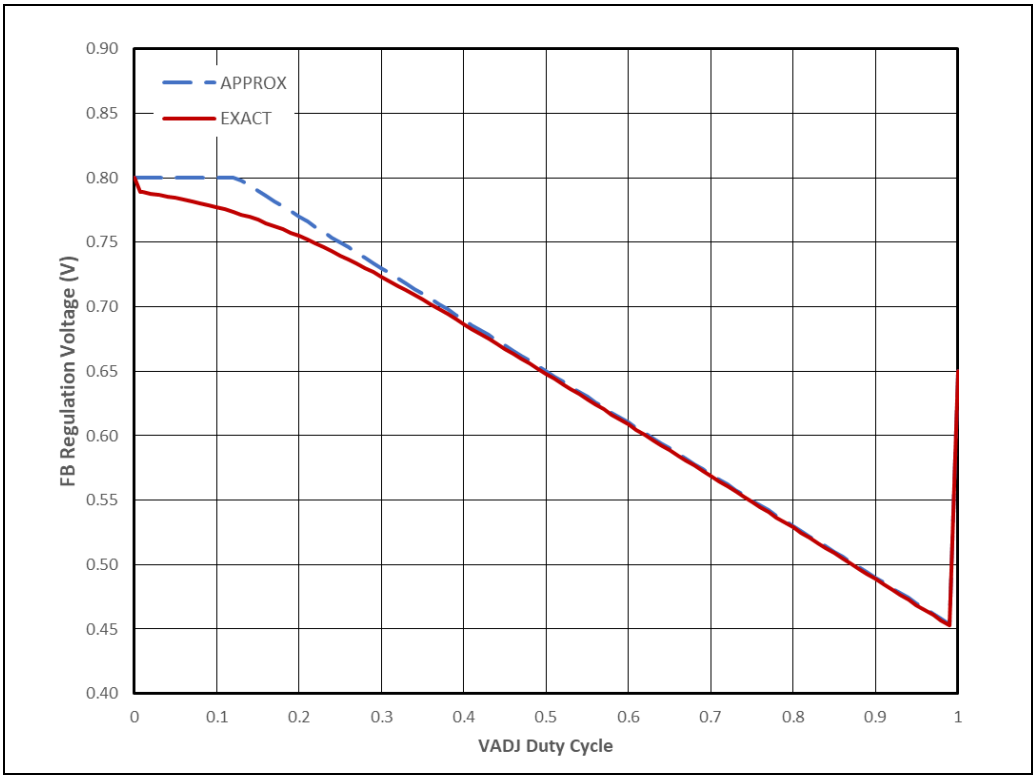


Figure 5 Error Amplifier Reference Voltage vs VADJ Duty Cycle

As shown in **Figure 5**, the FB pin regulation voltage decreases smoothly down to a minimum value of 0.45 V with increasing duty cycle of the VADJ signal. Note that the approximate equation (shown with a dashed line in **Figure 5**) is accurate to within 3.5 %. At D = 0 %, the regulation level will revert to the default value of 0.8 V. At D = 100 %, the regulation level will change to 81 %, just as it is for the case where the VADJ pin is tied to VCC.

When the VADJ feature is activated, the TDF10A01 will operate in FCCM mode, regardless of the mode selected by the RT/MODE pin. This is necessary so that the output voltage will follow a reduction in the target regulation level, even when operating with no load.

9.7 Power Good Indicator

The PGOOD pin is an open-drain indicator that is pulled low whenever the FB pin is 10 % or more outside of the intended regulation level. The PGOOD pin is also pulled low both in shutdown and during soft-start. There is a 50µs delay before any change in the PGOOD reporting. When the FB pin is within 7.5 % of the intended regulation level, the PGOOD pull-down is turned off and the pin can be pulled up by an external resistor to a voltage up to 24 V. Note that if the VADJ feature is active, the PGOOD threshold will track along with the target regulation level, such that there will not be unwanted trips on the PGOOD output when the regulation level is being intentionally adjusted.

9.8 Fault Protection and Monitoring

9.8.1 Output Current Limit and Short-Circuit Protection

The top MOSFET (M_{TOP}) forward current is internally limited to 1.5 A using a high-speed cycle-by-cycle current comparator. The value is determined by an internal clamp on the control voltage (V_C), which sets the peak current. Unlike most products that use peak current control, the value of the peak current limit on the TDF10A01 is not affected by the internal slope compensation and is therefore independent of operating duty cycle. This means that the full rated output current can be achieved at high operating duty cycle.

During a short-circuit, the bottom MOSFET (M_{BOT}) current comparator may activate if the valley current exceeds 1.6 A and prevent a subsequent turn on of M_{TOP}. This cycle-skipping behavior ensures that the inductor current is always limited to a level that is safe for the integrated MOSFET switches.

In addition to limiting the forward inductor current, the TDF10A01 also limits the reverse inductor current in the FCCM operating mode. If the current flowing into the SW pin and through M_{BOT} exceeds 0.6 A, the bottom MOSFET is quickly turned off, and the top MOSFET is turned on until a subsequent trip of the peak current comparator occurs.

For a buck converter application, the above current-limit architecture ensures safe operation throughout any overload or short-circuit condition without the use of foldback or hiccup-restart. This constant-current behavior eases the design for starting into large or unknown capacitive loads while ensuring a high availability of the DC output voltage.

In the special case of an isolated buck topology, a short-circuit on the secondary represents a unique challenge for any synchronous buck switching regulator. When the bottom MOSFET turns on and the secondary is shorted, any voltage present on the main output capacitor essentially appears directly on the SW pin. Since FCCM is required for an isolated buck topology, this will cause a rapid increase of current into the drain of the bottom MOSFET, the rate of which is set by transformed leakage inductance. This trips the low-side reverse current limit at -0.6 A, thereby turning off M_{BOT} and then turning on M_{TOP}. Since there is a short-circuit condition, the top MOSFET will generally turn off quickly due to the reflected load current from the secondary. The TDF10A01 automatically detects this condition and turns off both switches until the next switching cycle. If

this condition persists for 15 consecutive switching cycles, a hiccup-restart is initiated to avoid transformer saturation. After a wait time of approximately 135 ms, the main output should be fully discharged, and a restart of the 5 ms soft-start ramp will be initiated.

9.8.2 Output Overvoltage Protection

The TDF10A01 has a number of design features to prevent an overvoltage condition on the main output voltage V_{OUT} of the DC/DC converter.

When operating in FCCM with a high step-down ratio and high switching frequency, it is possible to reach the minimum on-time limit of the current loop. If this happens, the TDF10A01 will automatically skip a top MOSFET turn-on and keep the bottom MOSFET on for a switching cycle as needed to maintain regulation of V_{OUT}. Since this occurs only as needed on a cycle-by-cycle basis, this eliminates the possibility of an output overvoltage while maintaining the highest possible switching frequency for a given operating condition.

If V_{OUT} is overdriven by an external source in FCCM operation, the current loop will quickly work to bring the output back into regulation. This situation will cause the low-side reverse current limit to establish a controlled negative inductor current that pulls current from the load and sends it back to the input source.

The TDF10A01 also monitors the FB pin to detect an overvoltage condition. In PFM operation, an overvoltage condition will prevent the turn-on of the top MOSFET as well as the Sleep state. In both PFM and FCCM operation, an overvoltage condition will trigger a rapid discharge of the control voltage V_C to eliminate any voltage loop delay.

9.8.3 Thermal Shutdown (Overtemperature Protection)

An internal thermal shutdown circuit detects when the junction temperature has exceeded the normal range and prevents any switching or LDO operation until it returns to the normal operating range. This feature provides an added layer of system robustness for conditions that are outside of normal design parameters.

10 Package

This section includes marking, mechanical and packaging information for the TDF10A01.

10.1 Marking Information

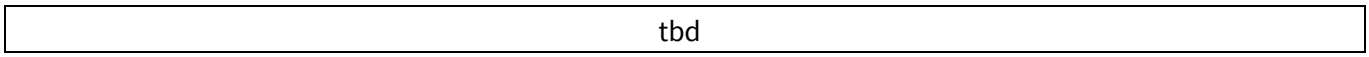


Figure 6 Package Marking

10.2 Dimensions

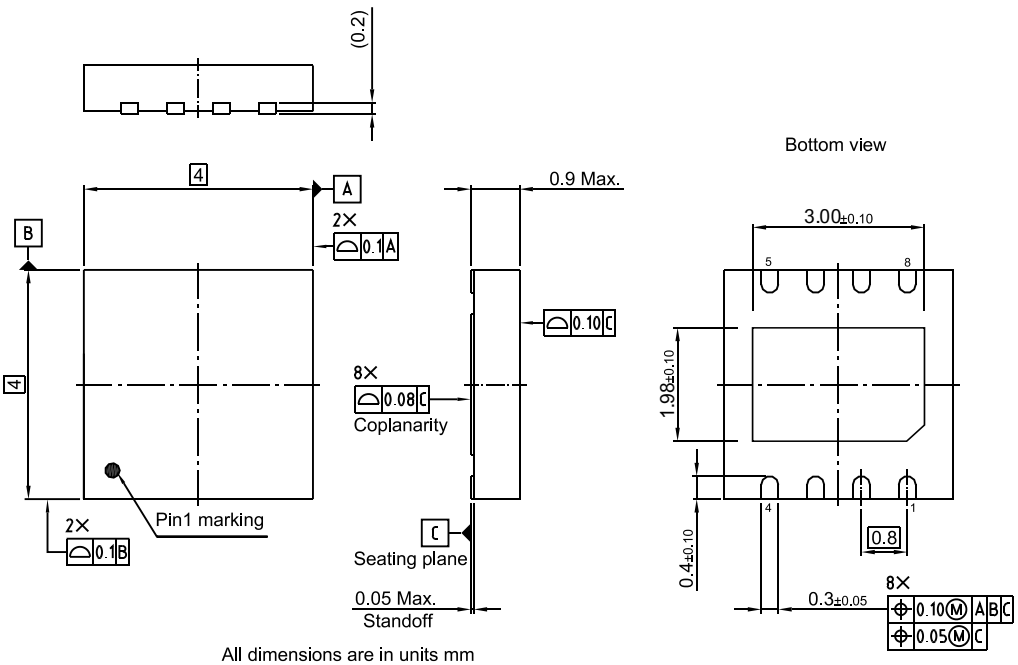


Figure 7 PG-VSON-8 Package dimensions (PREMININARY)

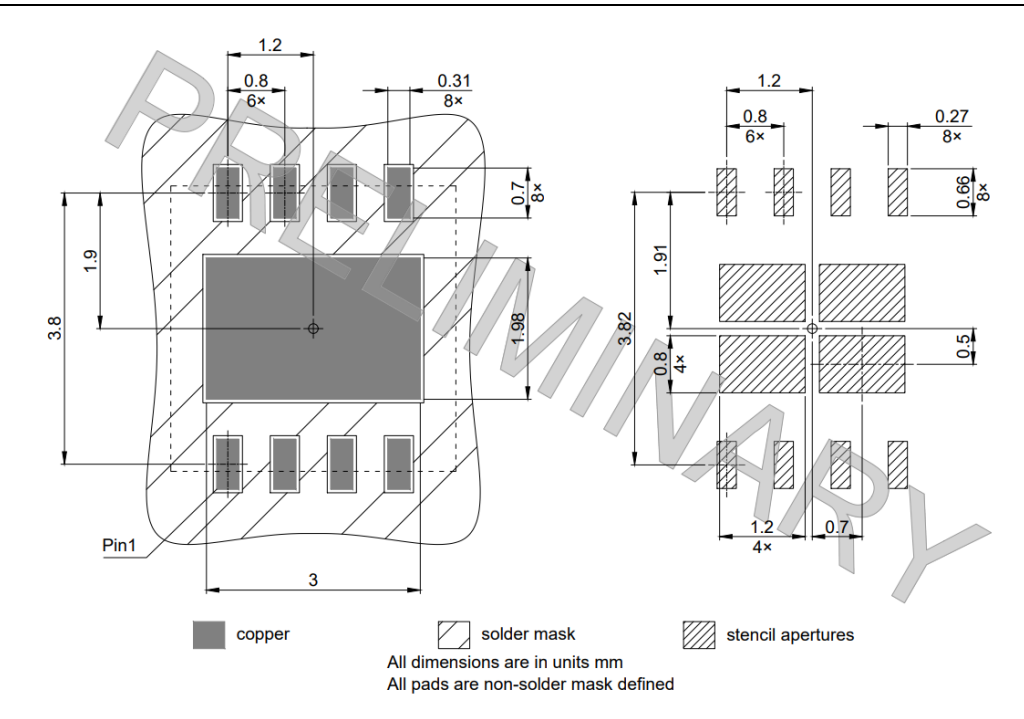


Figure 8 PG-VSON-8 Footprint dimensions

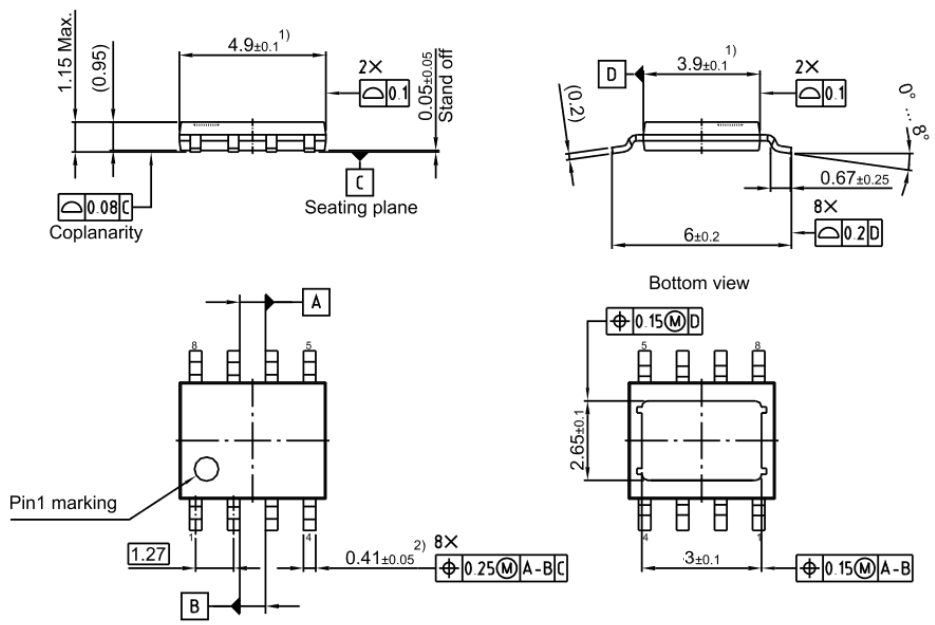


Figure 9 PG-DSO-8-101 Package dimensions (PREMININARY)

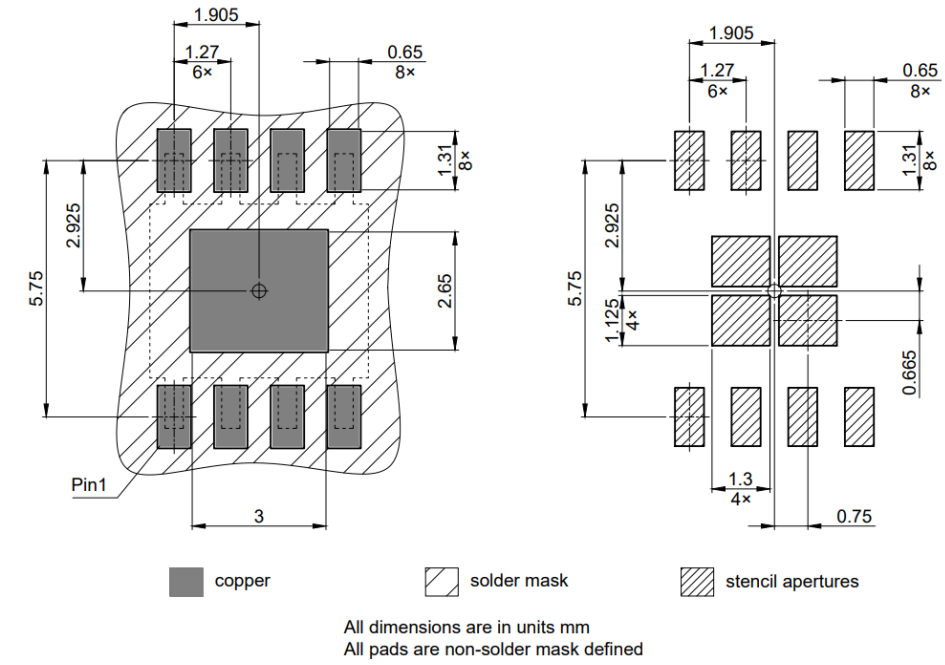


Figure 10 PG-DSO-8-101 Footprint dimensions (PREMININARY)

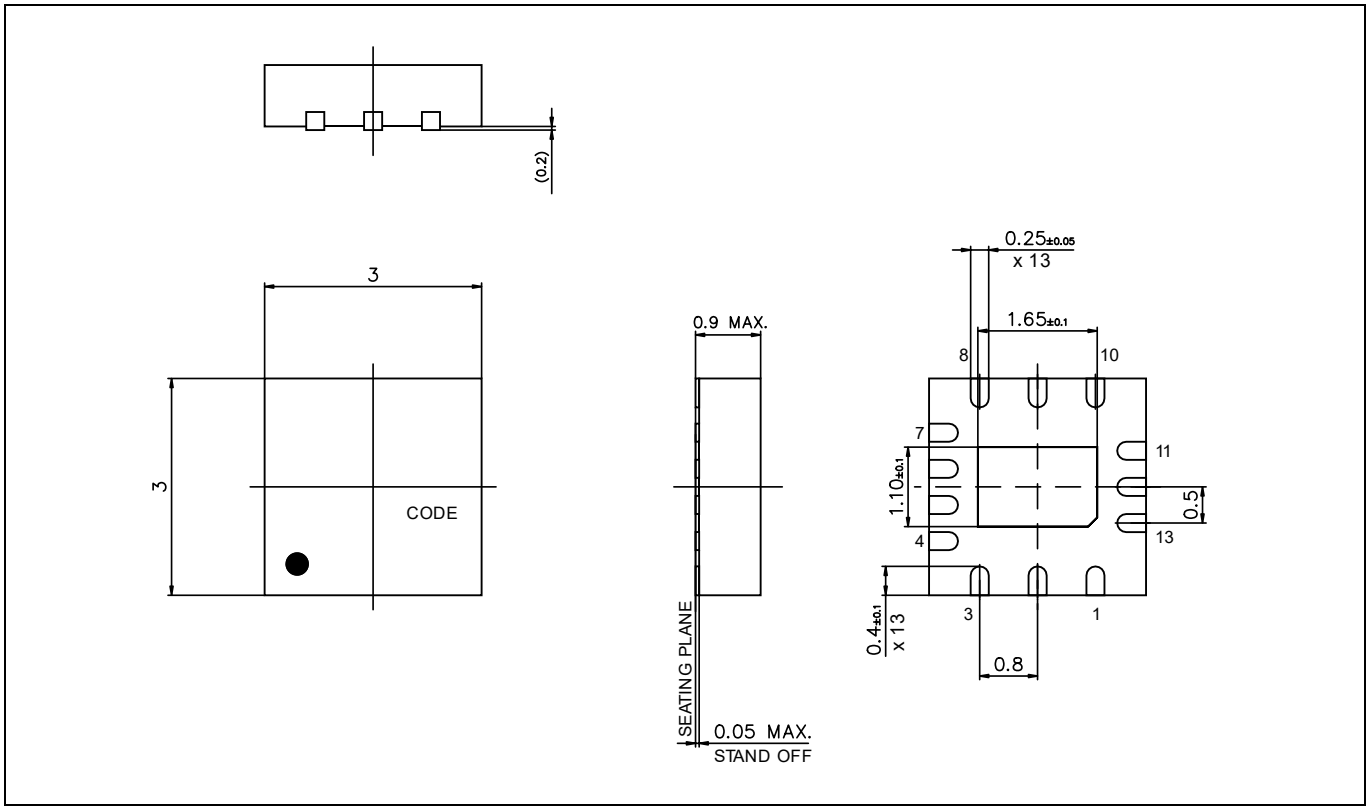


Figure 11 PG-VQFN-13-1 Package dimensions (PREMININARY)

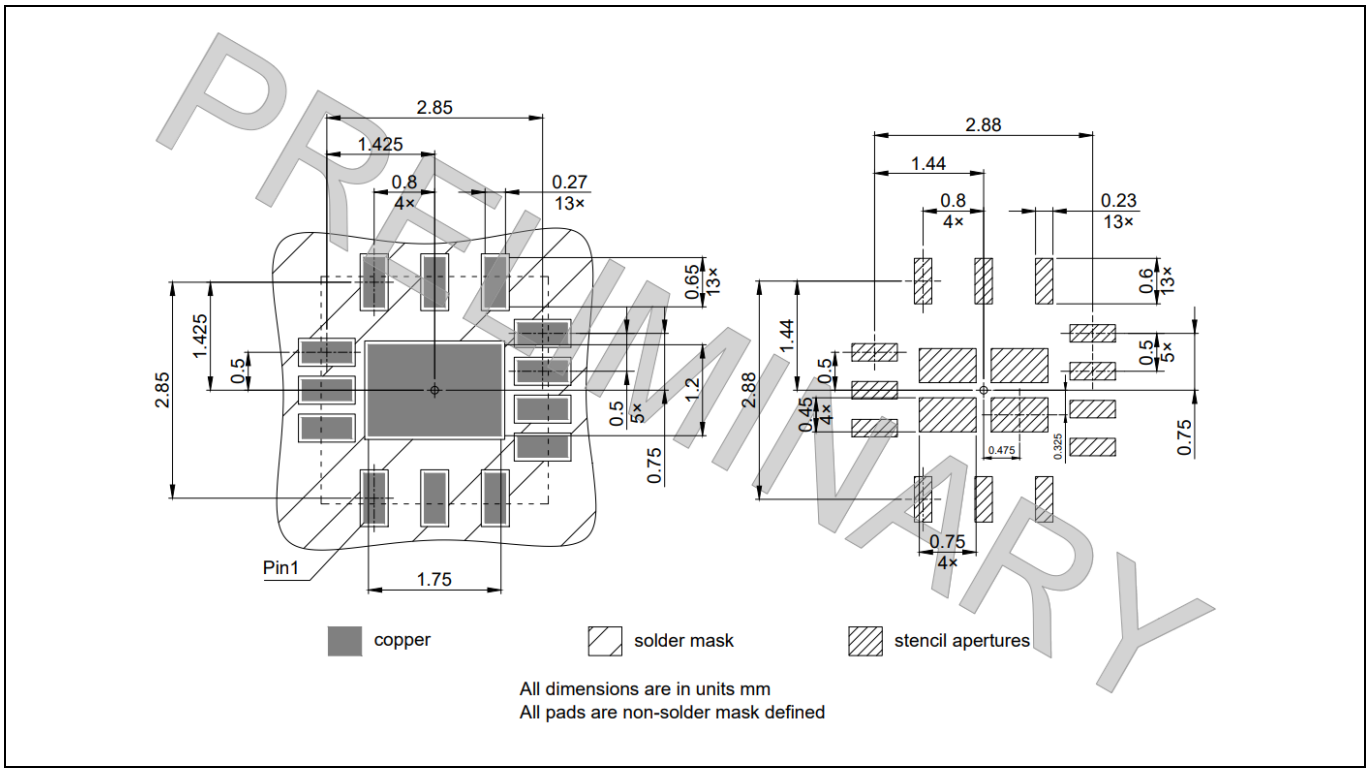


Figure 12 PG-VQFN-13-1 Footprint dimensions

10.3 Tape and Reel Information

tbd

Figure 13 Tape and reel drawing

Revision History

Document version	Date of release	Description of changes
V1.0	4/30/2026	Initial version of the preliminary Datasheet

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