TDA38540 OptiMOS™ IPOL

40 A single-voltage stackable synchronous Buck regulator

Features

- Single 4.5 V to 17 V application or wide input voltage range from 3.0 V to 17 V with an external VCC supply
- Output voltage range: 0.6 V to 6 V
- Precision reference voltage (0.6 V +/- 0.5%)
- Integrated OptiMOS™ 5 FETs
- Current-mode control with selectable ramp compensation
- Programmable switching frequency from 400 kHz to 2 MHz
- Optional synchronization to an external clock signal
- Standalone or stackable 2-phase, 3-phase or 4-phase operation with up to 40 A/phase
- Monotonic start-up with two selectable soft-start times, and enhanced pre-bias start-up
- Remote Vout sense
- Thermally-compensated internal overcurrent protection with four selectable settings
- Enable input with voltage monitoring capability and power good output
- Thermal shut down
- Operating temperature range: -40 °C $\leq T_j \leq$ 150 °C
- Small size: 5 mm x 6 mm PQFN package
- Halogen-free and RoHS2-compliant with exemption 7a

Potential applications

- Telecom and Datacom Applications
- Server Applications
- Storage Applications
- Distributed Point of Load Power Architectures

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

The TDA38540 is an easy-to-use, fully integrated dc-dc Buck regulator. The onboard PWM controller and OptiMOS™ 5 FETs with integrated bootstrap diode result in a small footprint solution and provide high-efficiency power delivery. The TDA38540 is a versatile regulator, offering synchronization to an external clock signal, and stackable operation. Stackable configurations include a Primary regulator with one, two or three Secondary regulators. Current-mode control with a fixed switching frequency makes it attractive for telecom applications.

The TDA38540 also features important protection functions, such as pre-bias start-up, thermally-compensated current limit, overvoltage and undervoltage protection, and thermal shutdown to give required system-level security in the event of fault conditions.

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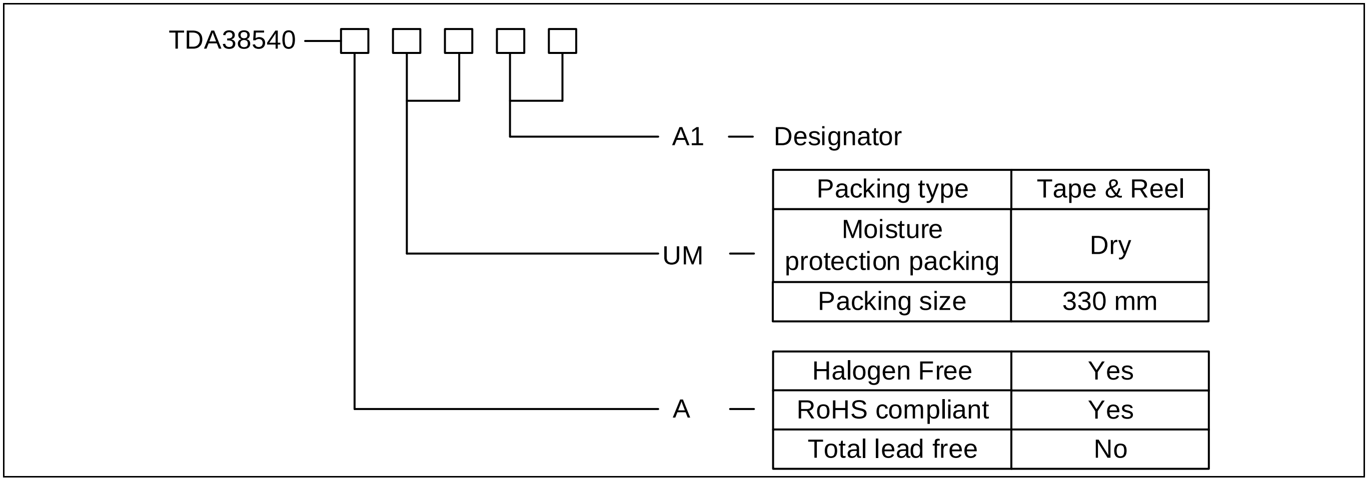
1 Ordering information

Table 1. Ordering Information

Sales Product Name	Package Type	Standard Pack Form and Qty		Orderable Part Number
TDA38540	QFN 5 mm x 6 mm	Tape and Reel	5000	TDA38540AUMA1



Packing type	Tape & Reel
Moisture protection packing	Dry
Packing size	330 mm

Halogen Free	Yes
RoHS compliant	Yes
Total lead free	No

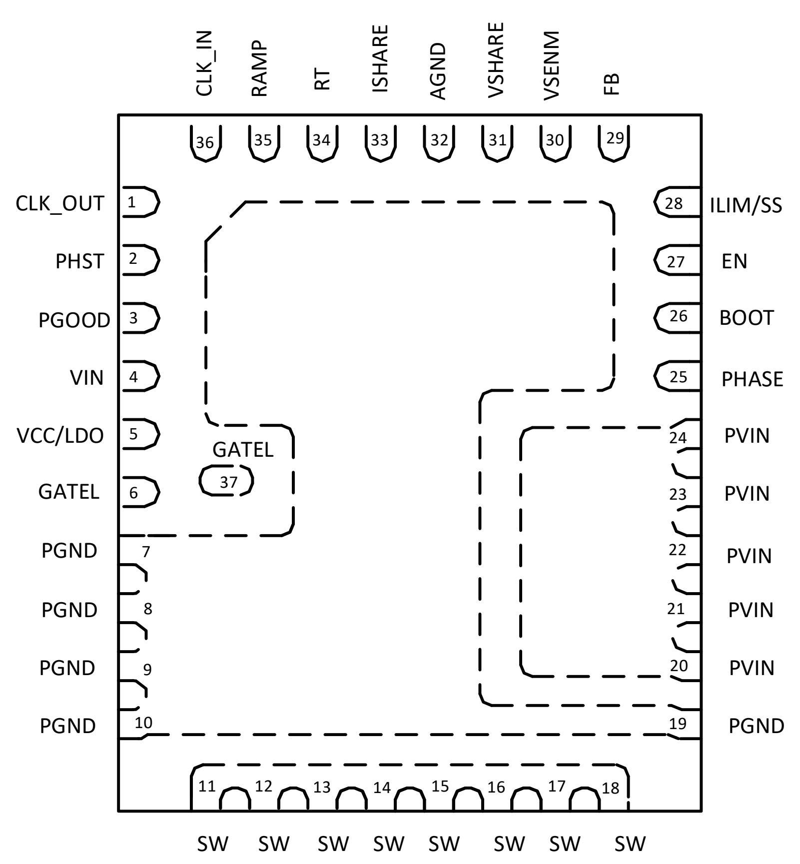


Figure 1 Package Top View

2 Functional block diagram

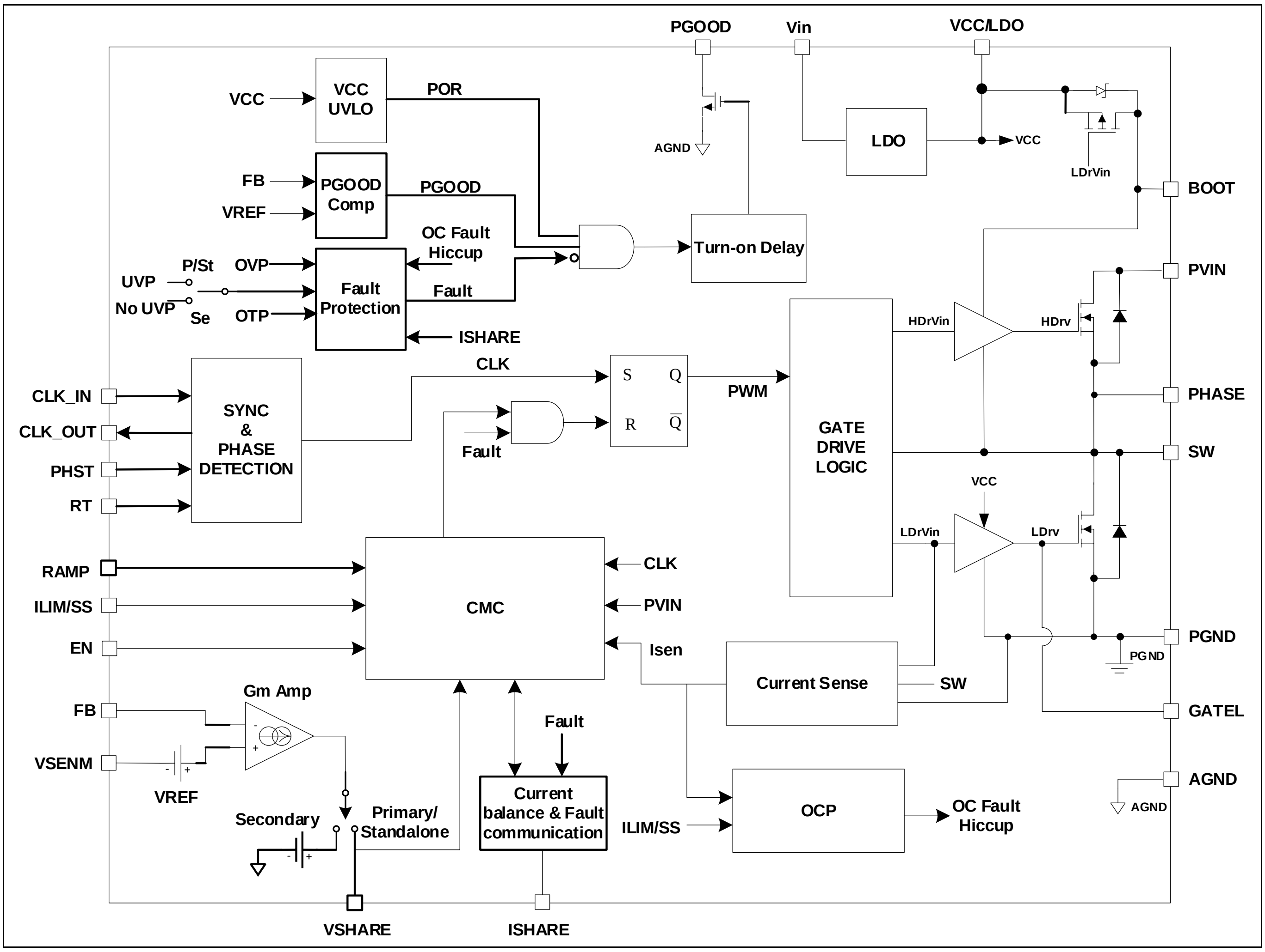


Figure 2 Block diagram

3 Typical application diagram

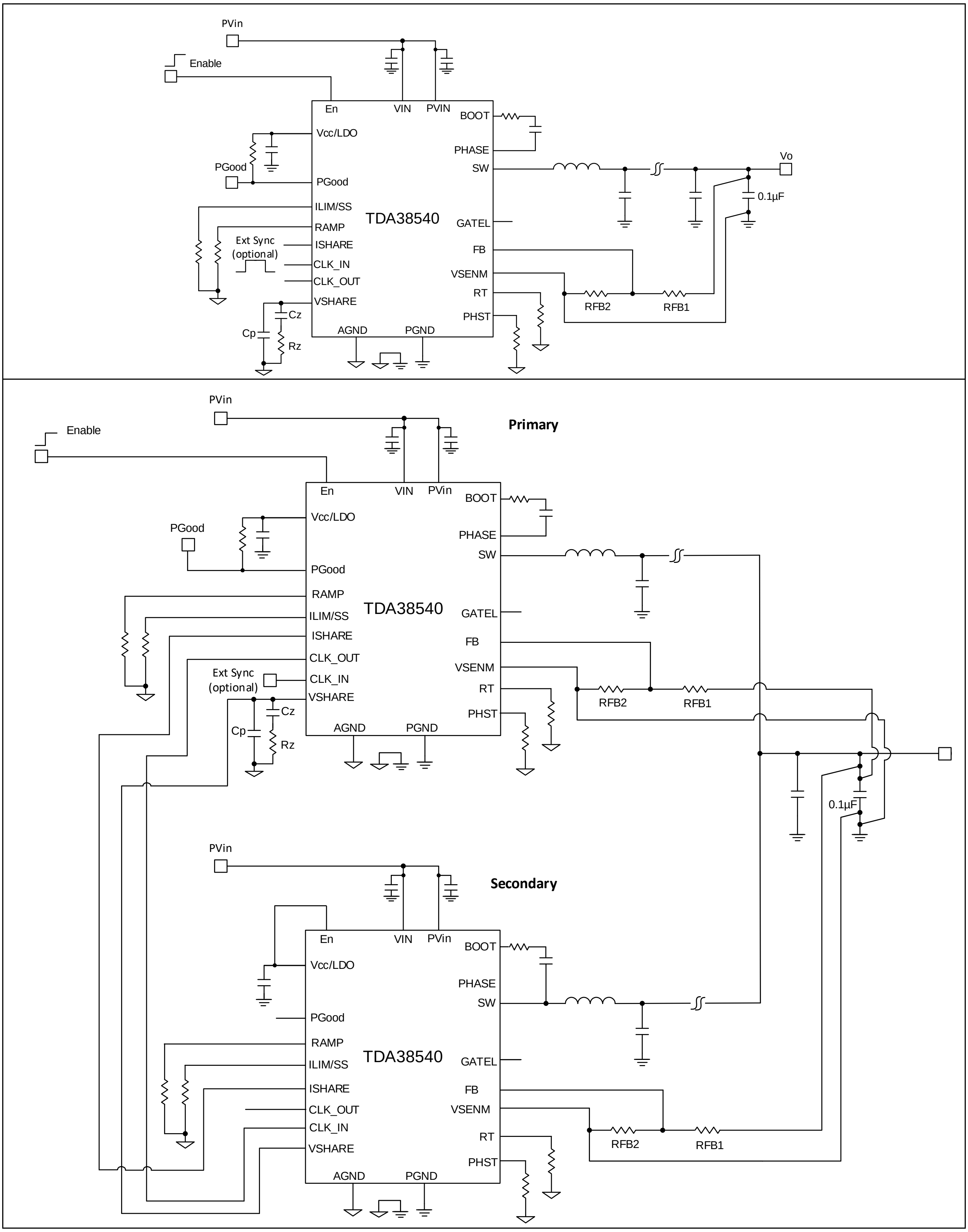


Figure 3 **Top: standalone configuration. Bottom: stackable 2-phase configuration.**

4 Pin descriptions

Note: I = Input, O = Output

Pin#	Pin Name	I/O	Type	Pin Description
1	CLK_OUT	O	Digital	The CLK_OUT function is only enabled on the Primary. When an external sync clock is present at CLK_IN, CLK_OUT duplicates the CLK_IN signal. Otherwise, CLK_OUT provides the internal switching clock signal. It is recommended to connect CLK_OUT of the Primary to CLK_IN of each Secondary. In standalone mode or on the Secondary, CLK_OUT must be left floating.
2	PHST	I	Analog	The PHST pin is used to configure the operating mode. Options include standalone mode or stackable mode with phase shift selection for up to four phases. PHST must be connected to AGND through a resistor as described in **Table 3**.
3	PGOOD	O	Analog	PGOOD is the Power Good status open-drain output. Connect a pull-up resistor from this pin to VCC/LDO, or to an external bias voltage. A 10 kΩ pull-up resistor to a PGOOD bias voltage of 3.3 V is commonly used.
4	VIN	I	Power	VIN is the input voltage for the Internal LDO. A 4.7 µF capacitor should be connected between this pin and PGND. If an external supply is connected to VCC/LDO, this pin should be shorted to the VCC/LDO pin and a 10 µF ceramic capacitor can be shared by the VIN and VCC/LDO pins.
5	VCC/LDO	I/O	Power	VCC/LDO is the output of the internal LDO or input for an external VCC supply. A ceramic capacitor (2.2 µF - 10 µF) should be connected between VCC/LDO and the power ground (PGND).
6, 37	GATEL	I	Analog	GATEL is the gate of the low-side FET. No external components should be connected to it.
7, 8, 9, 10, 19	PGND	-	Ground	Power Ground. All PGND IC pins and the bottom PGND paddle must be connected to the system's power ground plane. PGND and AGND are internally connected via the lead frame.
11, 12, 13, 14, 15, 16, 17, 18	SW	O	Power	Switch Node. Connect these pins to an output inductor.
20, 21, 22, 23, 24	PVIN	I	Power	Input supply for the power stage.
25	PHASE	O	Analog	PHASE connects to the source of the high-side FET. Connect a bootstrap capacitor between this pin and the BOOT pin. A high-temperature (X7R) ceramic capacitor of 0.1 µF is recommended.
26	BOOT	I	Analog	Supply voltage for the high-side driver. Connect this pin to the PHASE pin through a bootstrap capacitor. A resistor (e.g., 1 Ω to 2 Ω) can be placed in series with the bootstrap capacitor to control the slew rate of the SW node rising edge. See **Note 5**.
27	EN	I	Analog	EN is the enable pin to turn the device on and off. It can also be used to implement input voltage UVLO by connecting this pin to PVIN pin through a resistor divider.

Pin#	Pin Name	I/O	Type	Pin Description
28	ILIM/SS	I	Analog	Multi-function pin. Connect a resistor to AGND to set the overcurrent protection (OCP) limit and soft-start (SS) time. There are four selectable current limits and two SS options available. See **Table 7**.
29	FB	I	Analog	FB is the output voltage feedback pin. Connect this pin to the output of the regulator via a resistor divider to set the output voltage.
30	VSENM	-	Analog	VSENM provides the return connection for remote output voltage sensing. The feedback resistor divider should be connected to this pin.
31	VSHARE	I/O	Analog	VSHARE is the connection for voltage control loop compensation. VSHARE is connected to the output of an internal transconductance amplifier. A type II compensator must be connected from this pin to AGND to configure the voltage control loop for standalone operation, or for the Primary in stacked operation. In stacked operation, VSHARE of each Secondary must be connected to that of the Primary.
32	AGND	-	Ground	AGND is the signal ground for the internal circuitry.
33	ISHARE	I/O	Analog	The ISHARE pin is used for current balance and fault communication. ISHARE of each phase must be connected together in Stackable mode. The ISHARE pin should be left floating when operating in standalone mode.
34	RT	I	Analog	RT sets the switching frequency to one of eight settings by connecting a resistor to ground per configuration **Table 5**.
35	RAMP	I	Analog	Connect the RAMP pin to AGND with a resistor to select one of eight internal ramp options per configuration **Table 9**. Different internal ramp options provide different inner current loop response.
36	CLK_IN	I	Digital	Input for an external synchronization clock signal. It is recommended to apply the external clock 100 µs before EN is pulled high. The CLK_IN pin must be left floating if an external clock is not used.

5 Absolute maximum ratings

Table 2. Absolute maximum ratings

Description	Min	Max	Unit	Conditions
PVIN, VIN, EN to PGND	-0.3	25	V	Note **1**
PVIN to SW and PHASE	-0.3 V(dc), below -5 V for 5 ns	25 V(dc), above 32 V for 2 ns	V	
SW and PHASE to PGND	-0.3 (dc), below -5 V for 5 ns	25 V(dc), above 32 V for 2 ns	V	Note **1**
BOOT to PGND	-0.3 V(dc), below -0.3 V for 5 ns	29	V	Note **1**
BOOT to PHASE	-0.3	6 V(dc), 7 V for 5 ns	V	
VCC/LDO to PGND	-0.3	6	V	Note **1**
PGOOD, CLK_IN, and GATEL to AGND	-0.3	6	V	Note **1**
FB, VSHARE, ISHARE, RT, CLK_OUT, RAMP, ILIM/SS, and PHST to AGND	-0.3	3.6	V	Note **1**
PGND to AGND	-0.3	0.3	V	
VSENM to AGND	-0.3	0.3	V	
Storage Temperature Range	-55	150	°C	
Junction Temperature Range	-40	150	°C	

Note:

1. *PGND, VSENM, and AGND pins are connected together*

Attention: ***Stresses beyond these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.***

6 Thermal Characteristics

6.1 Thermal Characteristics

Description	Symbol	Values	Test Conditions
Junction to Ambient Thermal Resistance	θ_{JA}	14 °C/W	Note **2**
Junction to PCB Thermal Resistance	$\theta_{JC\text{-}PCB}$	5.3 °C/W	Note **3**
Junction to Case Top Thermal Resistance	θ_{JC}	24 °C/W	

Note:

2. *Thermal resistance is measured with components mounted on a standard single-phase EVAL_38540_1Vout_1P demo board in free air.*
3. *Thermal resistance is based on the board temperature within 10 mm from pin 8.*

7 Electrical specifications

7.1 Recommended operating conditions

Description	Min	Max	Unit	Note
PVIN Voltage Range with External VCC	3	17	V	Note **4**, Note **5**
PVIN Voltage Range with Internal LDO	4.5	17	V	Note **5**, Note **6**
VCC Supply Voltage Range	4.3	5.5	V	Note **4**
Output Voltage Range	0.6	6	V	Note **7**, Note **8**
Continuous Output Current Range/phase		40	A	Note **8**
Switching Frequency	400	2000	kHz	
VSENM - AGND	-0.1(dc) +/-0.3 (AC)	0.3	V	
Operating Junction Temperature	-40	150	°C	

Note:

4. *VIN is shorted to VCC and an external bias voltage is used.*
5. *A common practice is to have 20% margin on the maximum SW node voltage in the design. For applications requiring PVIN equal to or above 14 V, a small resistor in series with the Boot pin should be used to ensure the maximum SW node spike voltage does not exceed 20 V. Alternatively, an RC snubber can be used at the SW node to reduce the SW node spike.*
6. *Vin is connected to PVIN and the internal LDO is used. For single-rail applications with the internal LDO and PVIN = VIN = 4.5 V to 5.4 V, the internal LDO may enter dropout mode. OCP limits can be reduced due to the lower VCC voltage.*
7. *The minimum and maximum output voltages are also limited by the minimum on-time and the minimum off-time. Please refer to **Section 12.16** for details. Also note that the OCP limit may decrease when off-time is close to the minimum off-time.*
8. *Refer to **Figure 4** for maximum output current capability at different ambient temperatures.*

7.2 Electrical characteristics

Note: *Unless otherwise specified, specifications apply over 4.5 V ≤ VIN = PVIN ≤ 17 V, -40 °C ≤ T_J ≤ 150 °C. Typical values are specified at Ta = 25 °C.*

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Stage						
Top Switch	$R_{DS(on)\_Top}$	V_{Boot} - V_{Phase}= 5.0 V, I_O = 40 A, T_j =25 °C		3.0		mΩ
Bottom Switch	$R_{DS(on)\_Bot}$	VCC = 5.0 V, Io = 40 A, T_j =25 °C		0.93		
Bootstrap Forward Voltage		I(BOOT) = 25 mA		150	250	mV
SW float voltage	V_{SW}	EN = 0 V			300	mV
		EN = high, No Switching			300	
Dead Band Time	T_{db}	SW node falling edge, Io = 40 A, Internal LDO, T_j = 25 °C, **Note 9**		10		ns
		SW node rising edge, Io = 40 A, Internal LDO, T_j = 25 °C, **Note 9**		5		ns
Supply Current						
VIN Supply Current (standby)	$I_{in(Standby)}$	EN = Low, No Switching		6	8.3	mA
VIN Supply Current (static)	$I_{in(Static)}$	EN = 2 V, No Switching		6	8.3	mA
Soft Start						
Soft Start Ramp Rate	RR_{ss}	ILIM/SS resistor = 0 Ω; 10 kΩ; 18 kΩ; or 33 kΩ	0.43	0.6	0.77	mV/ µs
		ILIM/SS resistor = 56 kΩ; 82 kΩ; 120 kΩ; or floating	0.11	0.15	0.19	
Feedback Voltage						
Feedback Voltage	V_{FB}			0.6		V
Accuracy		0°C ≤ Tj ≤ 85°C	-0.5		0.5	%
		-40°C ≤ Tj ≤ 150°C	-1		1	%
Feedback input Bias Current	IV_{FB}	V_{FB}=0.6 V, -40°C ≤ Tj ≤ 85°C			100	nA
		V_{FB}=0.6 V, -40°C ≤ Tj ≤ 150°C			1.0	µA
Transconductance Gm Error Amplifier						
Output Sink/Source Current Capability	Isink	**Note 9**		-130		µA
	Isource	**Note 9**		130		µA
Transconductance Gm	Gm	**Note 9**		1.5		mA/V
Switching Frequency						
Switching Frequency	F_{sw}	RT = 0 Ω	360	400	440	kHz
		RT = 10 kΩ	540	600	660	
		RT = 18 kΩ	720	800	880	
		RT = 33 kΩ	900	1000	1100	
		RT = 56 kΩ	1080	1200	1320	

Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
		RT = 82 kΩ	1260	1400	1540	
		RT = 120 kΩ	1440	1600	1760	
		RT = floating	1800	2000	2200	
Minimum On-Time	$T_{on\ (Min)}$	**Note 9**		23	32	ns
Minimum Off-Time	$T_{off\ (Min)}$			270	360	ns
Synchronization						
CLK_IN frequency range	$Error_{sync}$	Difference between Sync freq and typical RT freq, **Note 9**	-20		20	$\%F_{sw}$
CLK_IN duty-cycle range	D_{CLK_IN}	**Note 9**	40	50	60	%
CLK_OUT duty-cycle range	D_{CLK_OUT}	Use internal clock, **Note 9**	45	50	55	%
CLK_IN threshold	CLK_IN_High	High- level input voltage	2			V
	CLK_IN_Low	Low- level input voltage			0.6	
CLK_OUT threshold	CLK_OUT_High	High- level output voltage, Cload = 100 pF, Io = 2 mA, **Note 9**	2.6			V
	CLK_OUT_Low	Low- level output voltage, Cload = 100 pF, Io = 2 mA, **Note 9**			0.4	
VCC LDO Output						
Output Voltage	VCC	5.5 V ≤ Vin ≤ 17 V, Icc = 25 mA	4.7	5.0	5.3	V
VCC Dropout	VCC_drop	Vin = 4.5 V, Icc = 50 mA, CVcc = 2.2 µF			356	mV
Short Circuit Current	I_{short}	5.5 V ≤ Vin ≤ 17 V		100		mA
LDO Undervoltage Lockout						
VCC-Start Threshold	VCC_UVLO_Start	VCC Rising Trip Level	3.75	3.9	4.02	V
VCC-Stop Threshold	VCC_UVLO_Stop	VCC Falling Trip Level	3.6	3.7	3.85	V
Hysteresis				200		mV
Enable						
Enable-Start-Threshold	En_UVLO_Start	ramping up	1.14	1.2	1.36	V
Enable-Stop-Threshold	En_UVLO_Stop	ramping down	0.9	1	1.06	
Input Impedance	R_{EN}		500	1000	1500	kΩ
Overcurrent Limit						
Positive Current Limit (Valley current)	ILIM_p	Tj = 25 °C, int LDO, ILIM/SS = 33 kΩ, or Floating	46	52	56	A
		Tj = 25 °C, int LDO, ILIM/SS = 18 kΩ, or 120 kΩ	36	42	46	
		Tj = 25 °C, int LDO, ILIM/SS = 10 kΩ, or 82 kΩ	27	32	36	
		Tj = 25 °C, int LDO, ILIM/SS = 0 kΩ, or 56 kΩ	17.7	22	26	
Hiccup Blanking Time	Tblk_Hiccup			20		ms

Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
(Positive OCP)						
Negative Current Limit	ILIM_n	Tj = 25 °C, int LDO	-25	-20	-15	A
Negative current time out	Timeout_NOCP	**Note 9**		200		ns
Overvoltage Protection						
OVP Trip Threshold	OVP_Vth	FB Rising	115	120	125	% Vref
		FB Falling, OVP hysteresis	110	115	120	
OVP Protection Delay	OVP_Tdly				1	µs
Hiccup Blanking Time	Tblk_Hiccup			20		ms
Undervoltage Protection						
UVP Enable Threshold	UVP_EN	FB Rising, **Note 9**		200		mV
UVP Trip Threshold	UVP_Vth	FB Falling	75	80	85	% Vref
UVP Protection Delay	UVP_Tdly			8		µs
Hiccup Blanking Time	Tblk_Hiccup			20		ms
Power Good						
PGOOD Turn on Threshold	$V_{PG(upper)}$	FB Rising	85	90	95	% Vref
PGOOD Turn off Threshold	$V_{PG(lower)}$	FB Falling	80	85	90	% Vref
PGOOD Voltage Low with VCC	$V_{PG(low)\_VCC}$	I_{PG_sink} = 5 mA, VCC ≥3.8 V			0.5	V
PGOOD Voltage Low at no VCC	$V_{PG(low)\_0V}$	Vin = VCC =0 V, Rpull-up = 10 kΩ to 3.3 V		0.75	0.9	V
PGOOD Turn on Delay	$V_{PG(on)\_Dly}$	FB rising during soft-start, see $V_{PG(upper)}$. Standalone mode, or the Primary in stackable mode, **Note 9**		1.0		ms
		PGOOD re-assertion delay after soft -start. **Note 9**, **Figure 18**		100		µs
PGOOD Comparator Delay	$V_{PG(comp)\_Dly}$	VFB < $V_{PG(lower)}$ or VFB > $V_{PG(upper)}$	1	2.5	3.5	µs
PGOOD Open Drain Leakage Current	I_{PG_leak}	PG = 3.3 V			10	µA
Ramp						
Ramp	K_{ramp}	RT = 0 Ω		20		m
		RT = 10 kΩ		40		
		RT = 18 kΩ		60		
		RT = 33 kΩ		80		
		RT = 56 kΩ		100		
		RT = 82 kΩ		130		
		RT = 120 kΩ		160		
		RT = floating		200		
Thermal Shutdown						
Thermal Shutdown	OTP_th	**Note 9**	160	170		°C
Hysteresis	OTP_hys	**Note 9**		20		

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hiccup Blanking Time	Tblk_Hiccup			20		ms
Current Sharing Accuracy						
Ratio of current difference between phases to the total current	Ishare_acc	Tj = 25 °C, Io ≥ 20 A/Phase, **Note 9**		±15		%
		Tj = 25 °C, Io ≤ 20 A/Phase, **Note 9**		±3		A

Note:

9. *Guaranteed by construction and not tested in production*
10. *VIN supply current does not include the current from PVIN.*

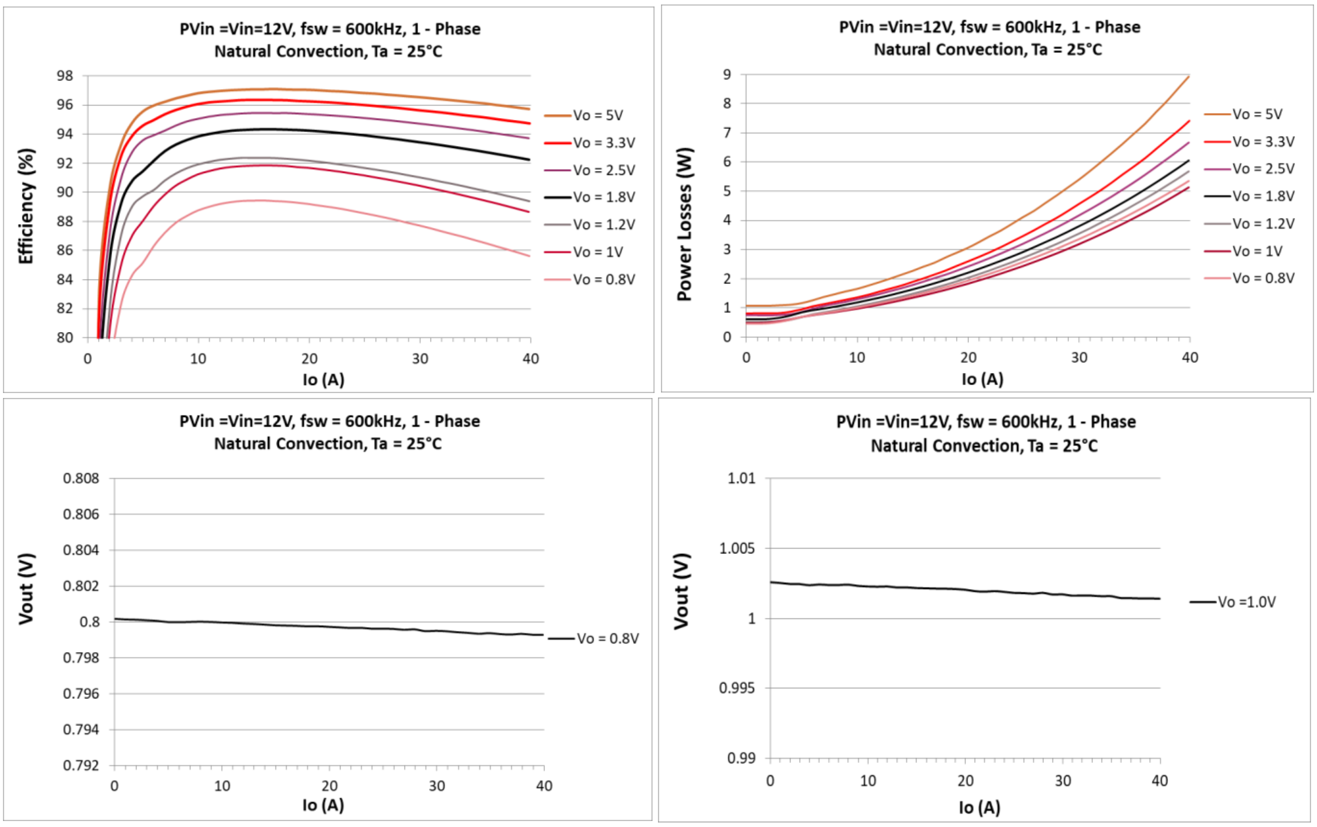
8 Typical efficiency and power loss curves

8.1 PVin = Vin = 12 V, VCC = Internal LDO, fsw = 600 kHz

Note that the efficiency and power loss curves include the losses of TDA38540, the inductor losses, the losses of the input and output capacitors, and PCB trace losses.

Table 1 Inductors for PVin = Vin = 12 V, fsw = 600 kHz

Vout (V)	Lout (nH)	P/N	DCR (mΩ)	Size (mm)
0.8	120	HCBS9610F-121 (Delta)	0.145	6.4x9.6x10
1.0	150	HCB138380F-151 (Delta)	0.145	12.4 x8.3x8
1.2	150	HCB138380F-151 (Delta)	0.145	12.4 x8.3x8
1.8	250	HCUVE117512-251 (Delta)	0.15	7.5x10.7x12
2.5	250	HCUVE117512-251 (Delta)	0.15	7.5x10.7x12
3.3	350	HCBD101195-351(Delta)	0.35	10.1 x 11.4 x 9.5
5	350	HCBD101195-351(Delta)	0.35	10.1 x 11.4 x 9.5

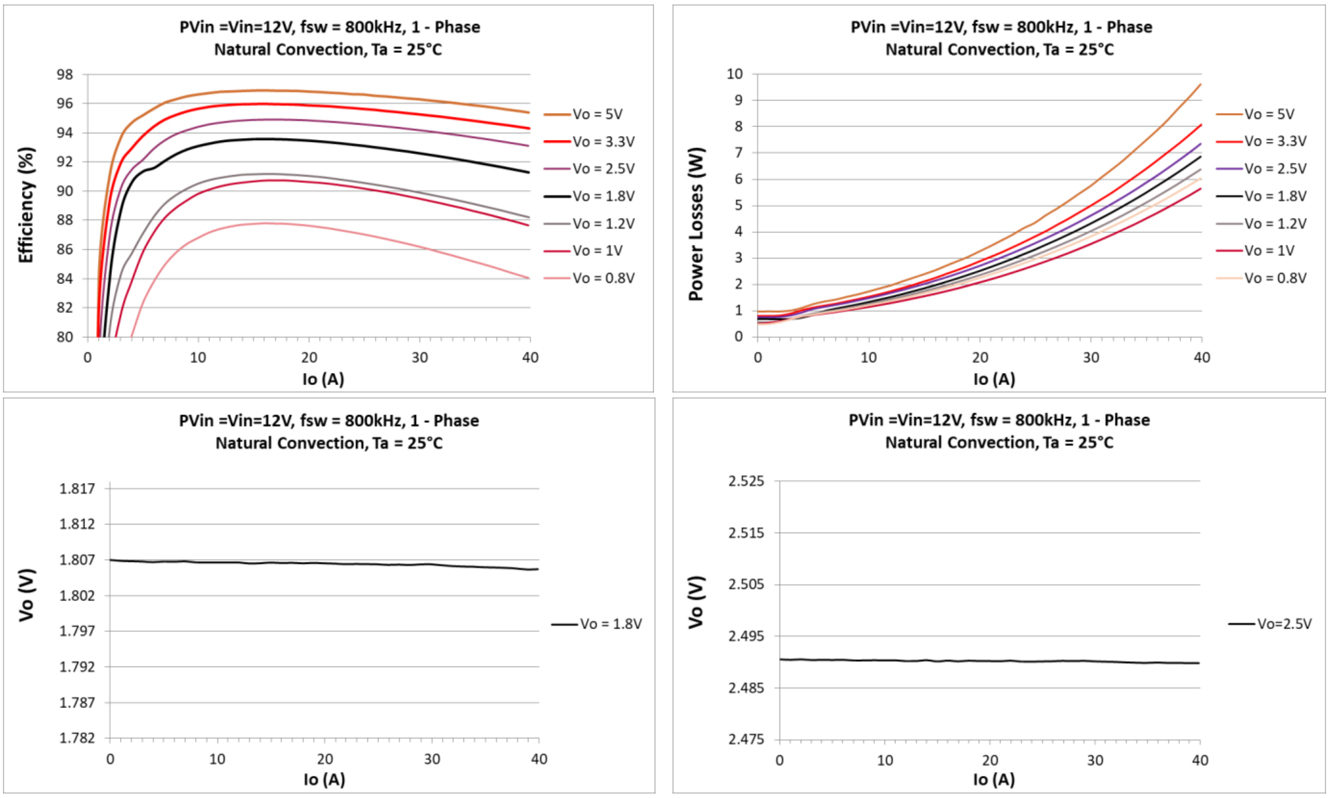


8.2 PVin = Vin = 12 V, VCC = Internal LDO, fsw = 800 kHz

Note that the efficiency and power loss curves include the losses of TDA38540, the inductor losses, the losses of the input and output capacitors, and PCB trace losses.

Table 2 Inductors for PVin = Vin =12 V, fsw = 800 kHz

Vout (V)	Lout (nH)	P/N	DCR (mΩ)	Size (mm)
0.8	120	HCBS9610F-121 (Delta)	0.145	6.4 x 9.6 x 10
1.0	120	HCBS9610F-121 (Delta)	0.145	6.4 x 9.6 x 10
1.2	150	HCB138380F-151 (Delta)	0.15	12.4 x 8.3 x 8
1.8	150	HCB138380F-151 (Delta)	0.15	12.4 x 8.3 x 8
2.5	250	HCUVE117512-251 (Delta)	0.15	7.5x10.7x12
3.3	250	HCUVE117512-251 (Delta)	0.15	7.5x10.7x12
5	350	HCBD101195-351(Delta)	0.35	10.1 x 11.4 x 9.5

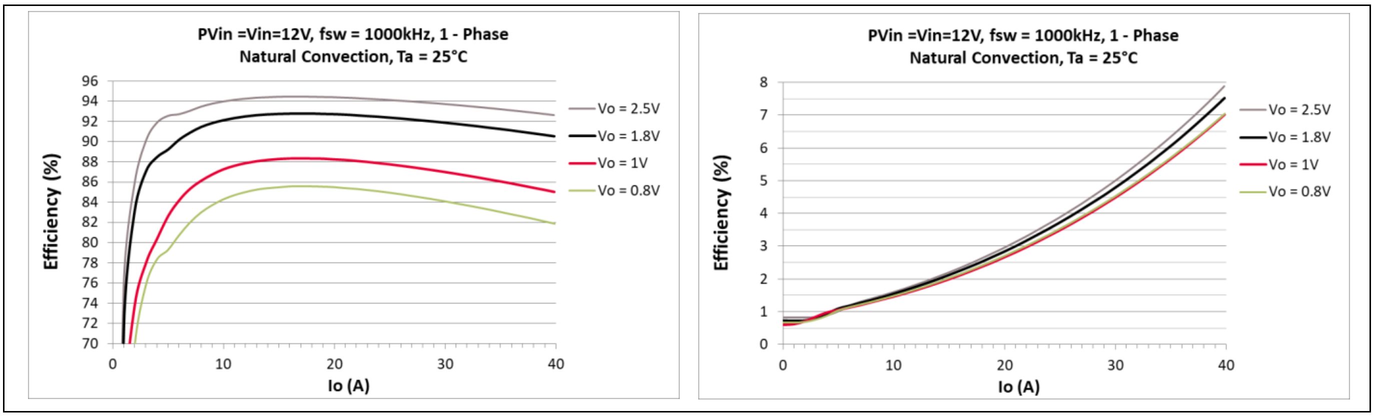


8.3 PVin = Vin = 12 V, VCC = Internal LDO, fsw = 1000 kHz

Note that the efficiency and power loss curves include the losses of TDA38540, the inductor losses, the losses of the input and output capacitors, and PCB trace losses.

Table 3 **Inductors for PVin = Vin = 12 V, fsw = 1000 kHz**

Vout (V)	Lout (nH)	P/N	DCR (mΩ)	Size (mm)
0.8	70	AH3740A-70K (ITG)	0.145	6.4 x 9.5 x 10
1.0	120	HCBS9610F-121 (Delta)	0.145	6.4 x 9.6 x 10
1.8	150	HCB138380F-151 (Delta)	0.15	12.4 x 8.3 x 8
2.5	150	HCB138380F-151 (Delta)	0.15	12.4 x 8.3 x 8

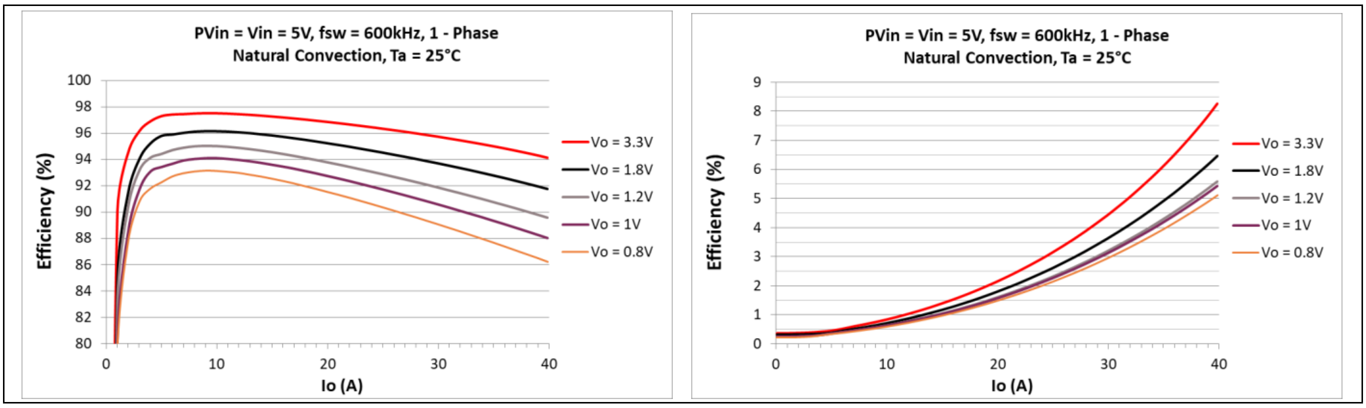


8.4 PVin = Vin = 5 V, VCC = Internal LDO, fsw = 600 kHz

Note that the efficiency and power loss curves include the losses of TDA38540, the inductor losses, the losses of the input and output capacitors, and PCB trace losses.

Table 4 **Inductors for PVin = Vin = 12 V, fsw = 600 kHz**

Vout (V)	Lout (nH)	P/N	DCR (mΩ)	Size (mm)
0.8	70	AH3740A-70K (ITG)	0.145	6.4 x 9.5 x 10
1.0	120	HCBS9610F-121 (Delta)	0.145	6.4 x 9.6 x 10
1.8	150	HCB138380F-151 (Delta)	0.15	12.4 x 8.3 x 8
2.5	150	HCB138380F-151 (Delta)	0.15	12.4 x 8.3 x 8
3.3	150	HCB138380F-151 (Delta)	0.15	12.4 x 8.3 x 8



9 Thermal De-rating curves

Measurement is done on Evaluation board EVAL_38540_1Vout_1P. PCB is an 8-layer board with 2-ounce Copper for all layers, FR4 material, size 3.10”x5.00”.

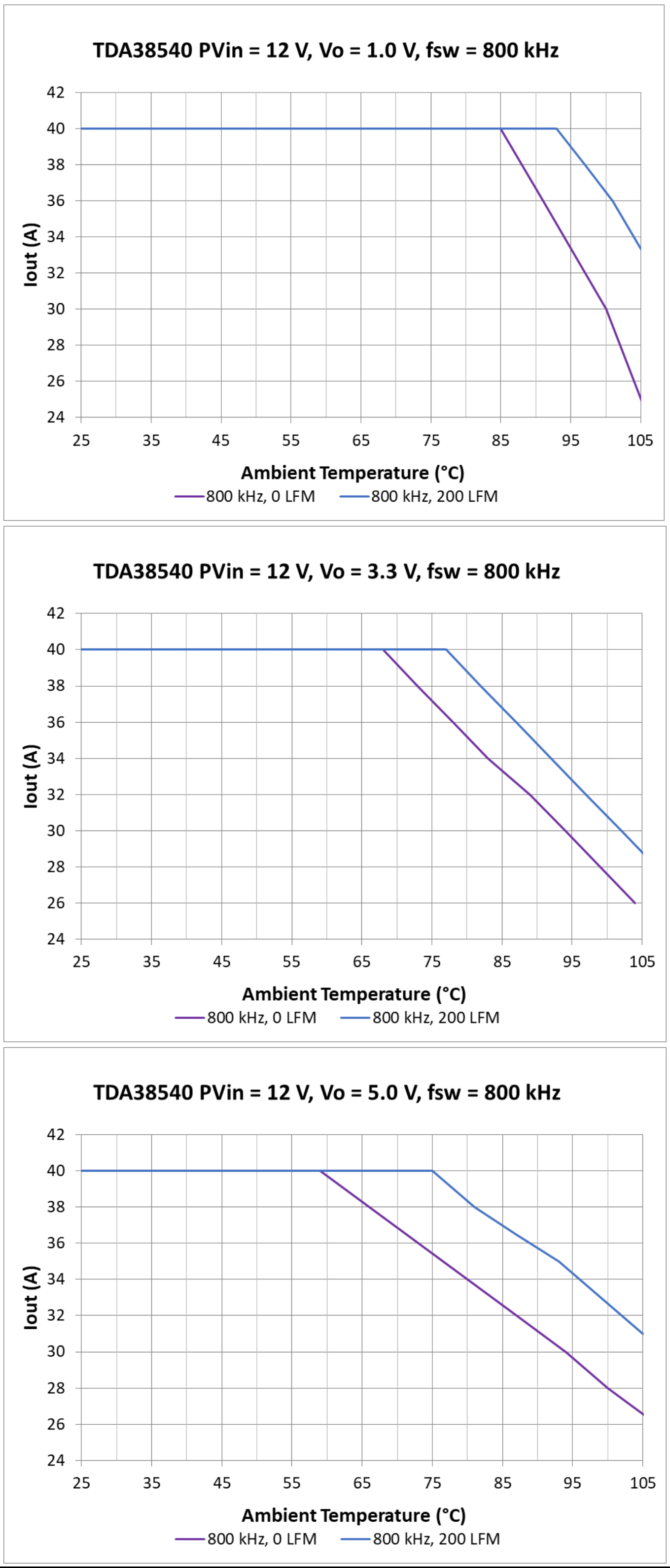


Figure 4 **Thermal de-rating curves, PVin = 12 V, Vout= 1.0 V/3.3 V/5 V, VCC = Internal LDO**

10 $R_{DS(ON)}$ of MOSFET Over Temperature

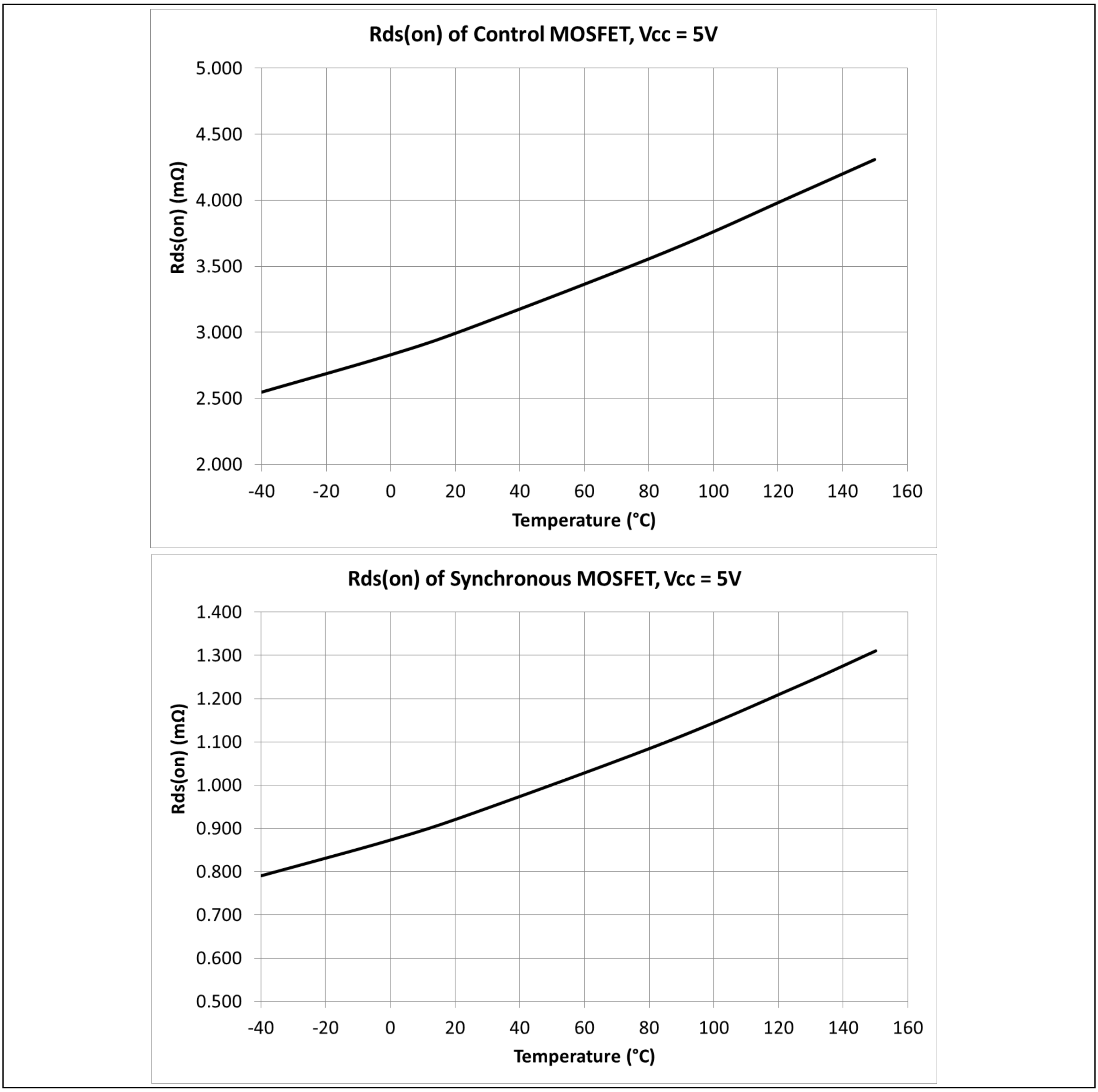


Figure 5 $R_{DS(on)}$ of MOSFETs over junction temperature

11 Typical operating characteristics (-40 °C ≤ Tj ≤ +150 °C)

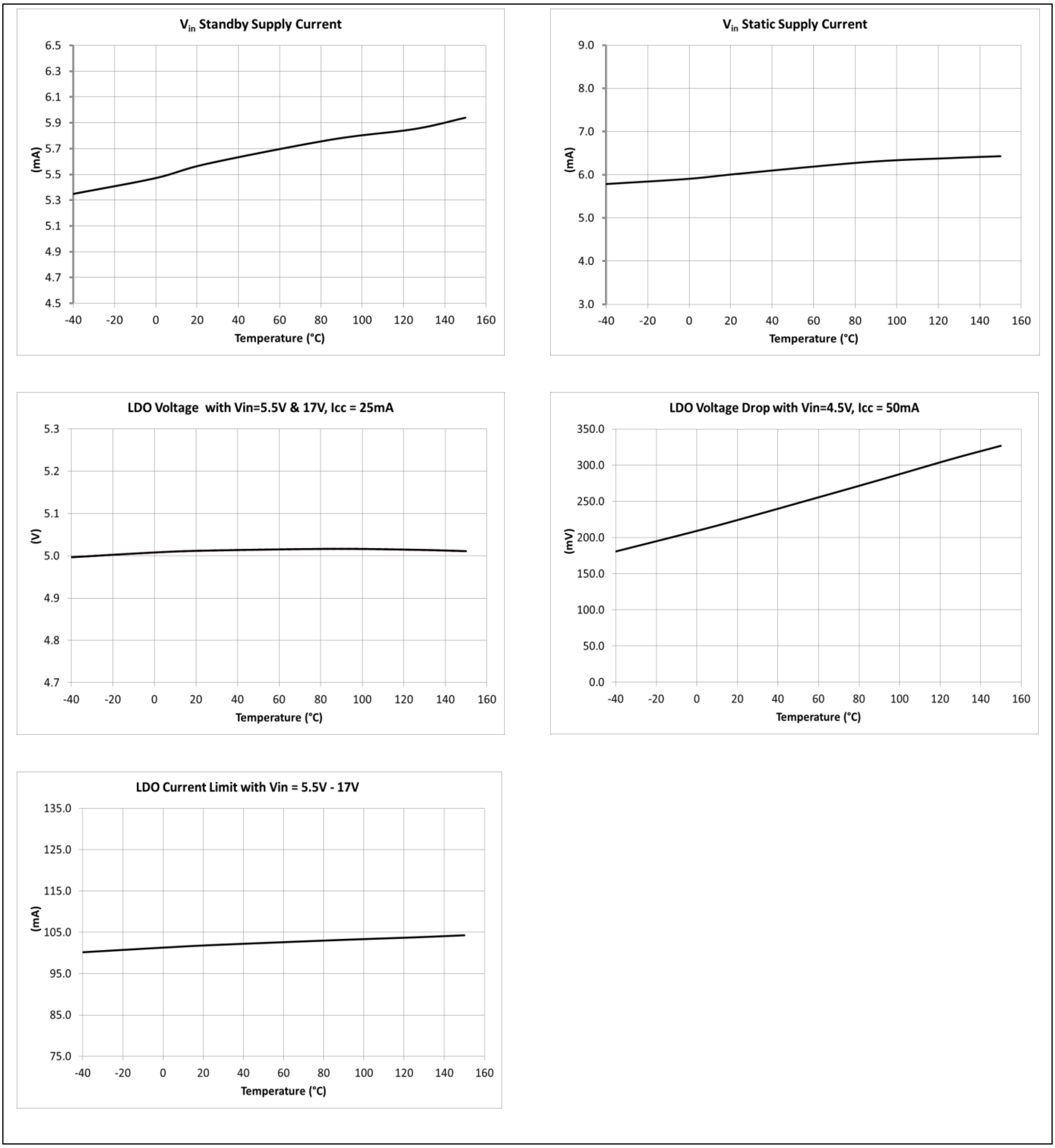


Figure 6 Typical operating characteristics (set 1 of 3)

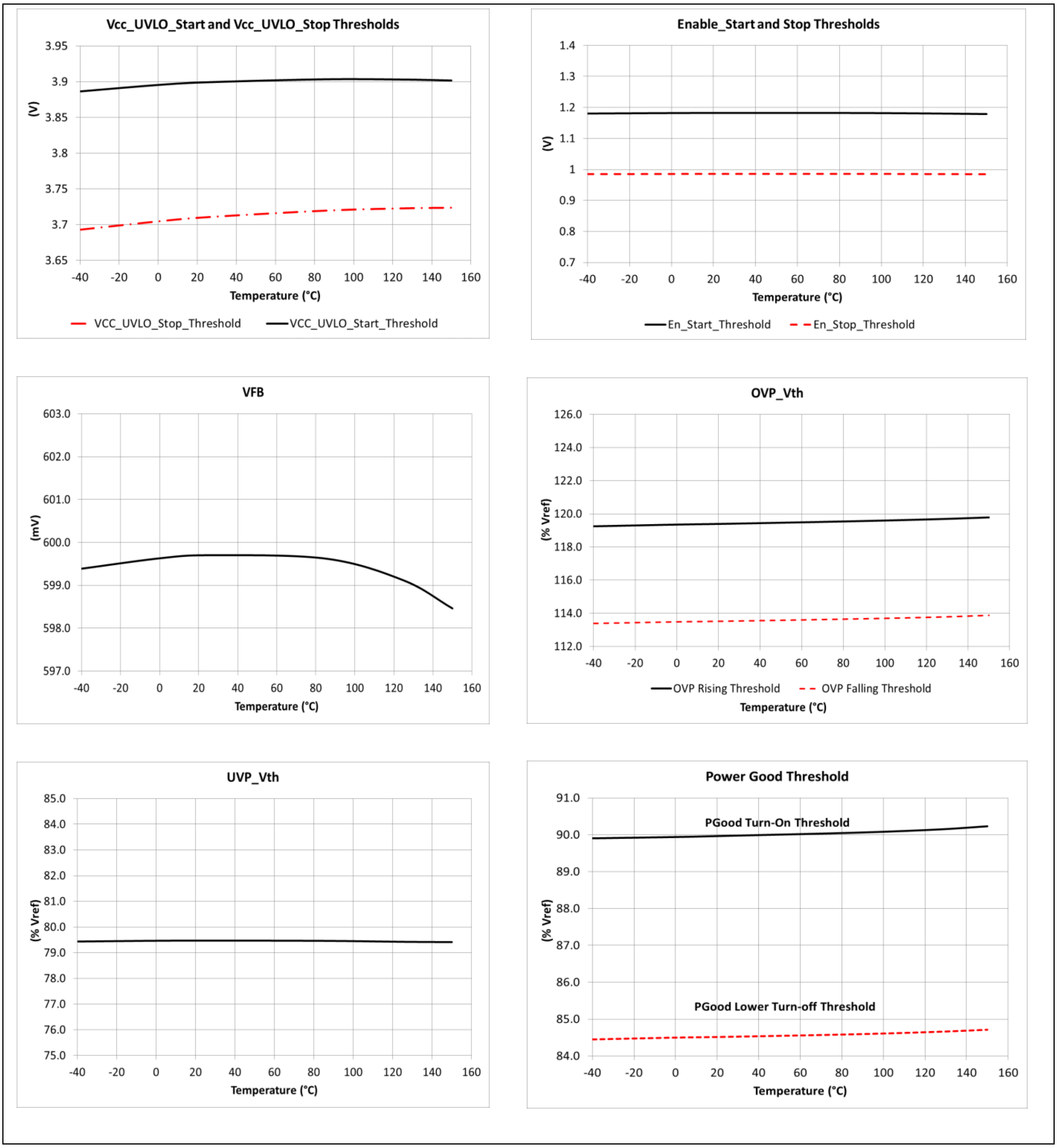


Figure 7 Typical operating characteristics (set 2 of 3)

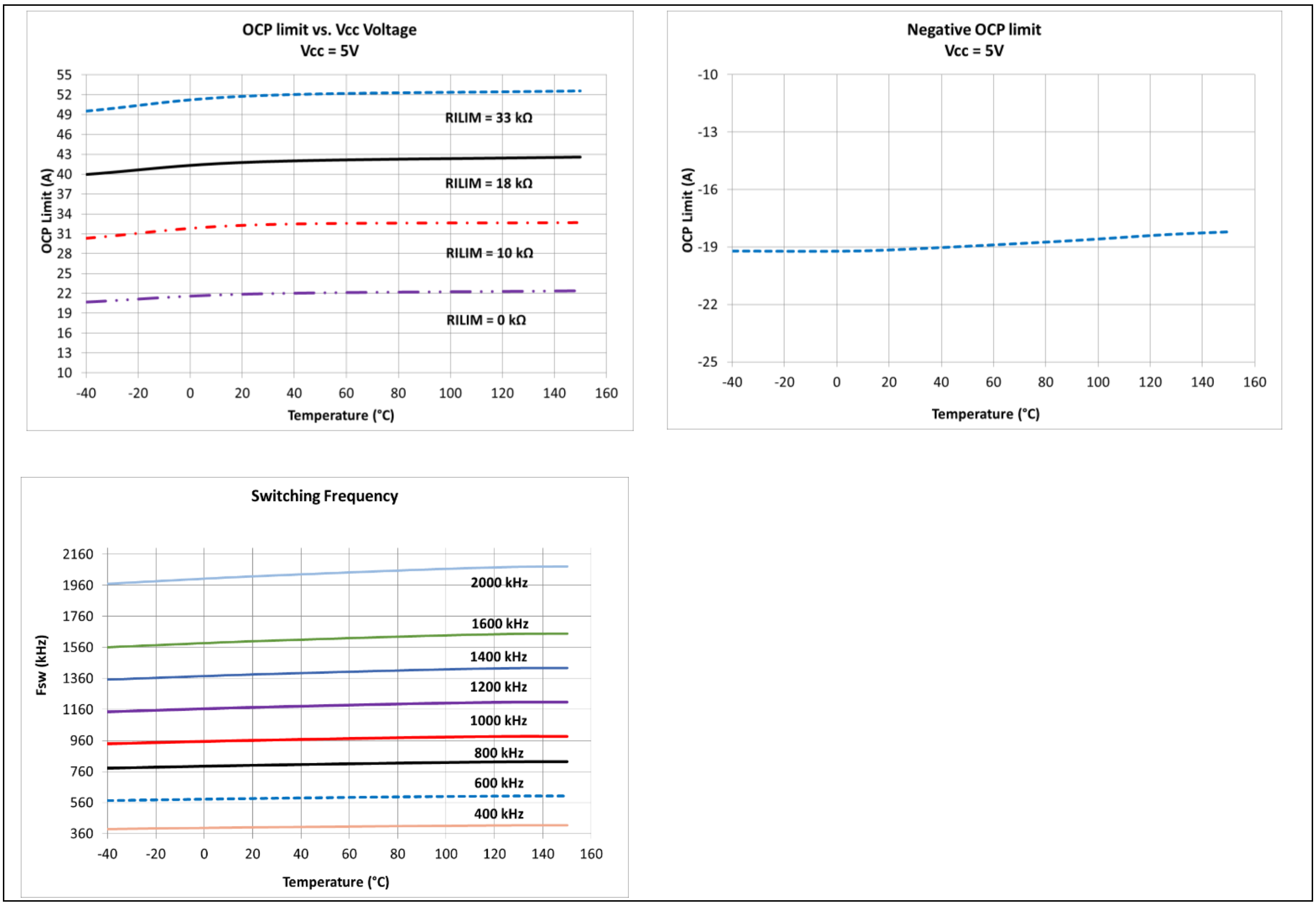


Figure 8 Typical operating characteristics (set 3 of 3)

12 Theory of operation

12.1 Current Mode Control

The TDA38540 features proprietary peak-current-mode control with constant switching frequency. The control scheme includes a voltage loop and two current loops. The output voltage is regulated using a transconductance error amplifier. A type II compensator is used at VSHARE to adjust the voltage loop response. Current loop stability is ensured using the internal ramp compensation. The TDA38540 offers eight selectable internal ramps, providing flexibility to optimize the current loop response for different output filter configurations.

12.2 Configuration of Standalone and Stackable Operation

The TDA38540 offers standalone operation, or stackable interleaved operation with up to four phases. The configuration is selected by connecting a resistor, as listed in **Table 3**, between the PHST pin and AGND. A summary of the configuration differences is given in **Table 4**.

Table 3. Configuration resistors for PHST pin

PHST Resistor (kΩ) ± 10%	Standalone/ Primary/ Secondary Config	Phase Shift (Degree)
0	Standalone mode	0
120	Primary phase in stackable mode	0
Floating		0
10	Secondary phases in stackable mode	90
18		120
33		180
56		240
82		270

Table 4. Summary of differences in pin configurations between Standalone and Stackable Mode

Pin	Standalone Mode	Stackable Mode	
		Primary	Secondary
FB and VSENM pins	• Remote Vout sense lines for Vout regulation, PGOOD, UVP and OVP • Connect to Vout and GND through a FB resistor divider	• Same as Standalone mode	• Remote Vout sense for OVP **Note 11** • Connected to Vout and GND through a FB resistor divider
CLK_OUT	• Disabled • Must be left floating	• Enabled • Connect it to CLK_IN of each Secondary	• Disabled • Must be left floating
ISHARE	• Not used • Must be left floating	• For current balance and fault communication • ISHARE of Primary and each Secondary must be connected together	

Pin	**Standalone Mode**	**Stackable Mode**	
		Primary	Secondary
VSHARE	• Output of an internal transconductance amplifier • A type II compensator must be connected at this pin with reference to AGND	• Same as Standalone mode • Must be also connected to each Secondary	• Internal transconductance amplifier is disabled • Must be connected to VSHARE of the Primary
EN	• During power on, pull EN high when or after VCC passes the VCC UVLO.		• Recommend to connect EN to VCC of the phase
PGOOD	• Open drain connection	• Same as standalone mode • Suggest use PGOOD of Primary only in stackable mode	

Note:

11. UVP is disabled on the Secondary. Refer to ***Section 12.11*** *for details.*

12.3 Selection of switching frequency

The TDA38540 offers eight programmable switching frequencies, f_{sw}, from 400 kHz to 2 MHz, selected by connecting a resistor from the RT pin to AGND, as shown in **Table 5**, **Figure 9** and **Figure 10**. The selection of switching frequency cannot be changed on the fly. To change the switching frequency, VCC needs to be cycled.

In stackable operation, the CLK_IN pin of the Secondary must be connected to CLK_OUT pin of the Primary. It must be noted that although the switching frequency of the Secondary follows that of the Primary, the same RT resistor used on the Primary must also be installed on the Secondary for two purposes: (1) to ensure the proper operation of the control loop; (2) to allow the Secondary to operate at the internal free-running clock in case the external clock is lost.

Table 5. Configuration Resistors for RT pin

RT Resistor (kΩ) ± 10%	**Switching Frequency (kHz)**
0	400
10	600
18	800
33	1000
56	1200
82	1400
120	1600
Floating	2000

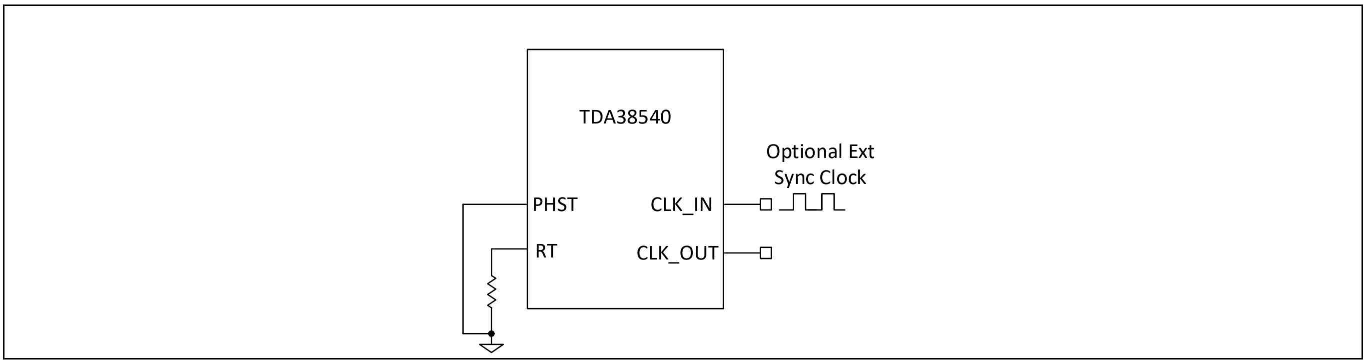


Figure 9 **Configurations of switching frequency in standalone mode.**

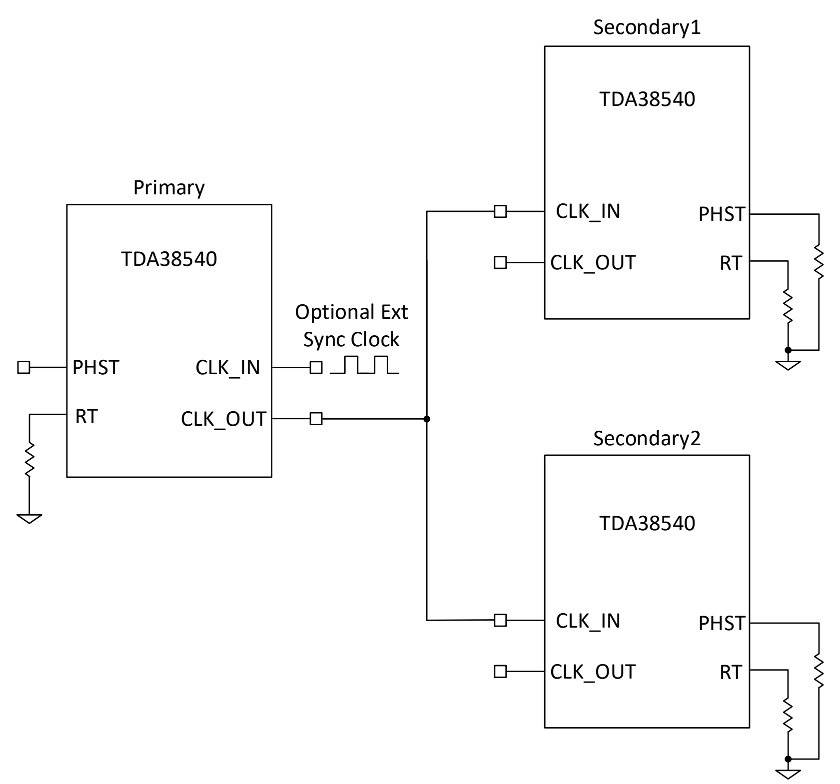


Figure 10 **Configurations of switching frequency in a 3-phase stackable mode.**

12.4 External synchronization

The TDA38540 can be synchronized to an external clock in both standalone and stackable operation, as shown in **Figure 9** and **Figure 10**. During start-up, TDA38540 checks if there is a valid external clock available on the CLK_IN pin. If no valid clock signal is detected, the TDA38540 switches to the internal free-running clock determined by the RT resistor, and the Primary sends the internal clock to CLK_OUT. It is recommended to apply the external clock at least 100 µs before the EN signal is applied to avoid output disturbance during the transition between the internal and external clocks.

During operation, the TDA38540 continues monitoring the CLK_IN pin. It can switch to the external clock when a valid external clock signal is detected later on. If the external clock is lost, TDA38540 will switch back to the internal clock.

The external clock frequency must be within ±20% tolerance of the internal free-running clock set by the RT resistor, with a duty-ratio ranging from 40% to 60%. **Figure 11** illustrates the start-up timing diagram with and without an external synchronization clock.

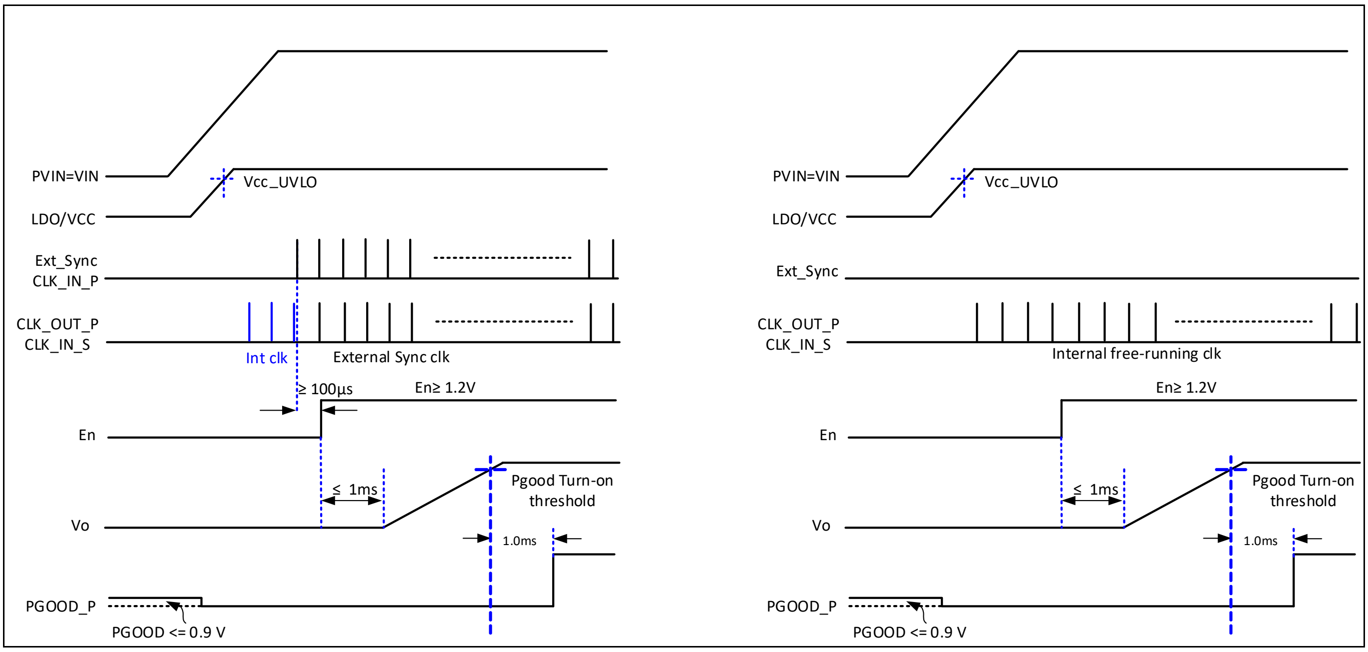


Figure 11 **Start-up timing diagram of two-phase operation. Left: synchronized to an external clock signal. Right: operation with the free-running internal clock.**

Please note that when the TDA38540 transitions from the external clock to the internal clock, the firing of the next PWM pulse could be delayed for a short period of time, as shown in **Figure 12**. The extended off-time can cause some disturbance on V_o, therefore extra output capacitance might be needed in this scenario. The approximated time delay is given in **Table 6** for reference.

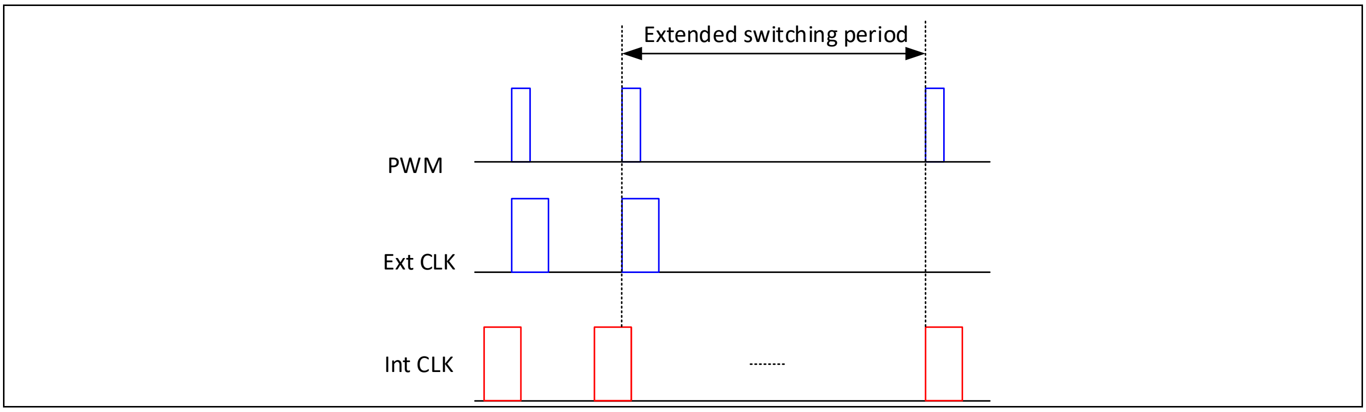


Figure 12 **The delayed PWM pulse when transitioning from the external clock to the internal clock.**

Table 6. **Approximated time duration of the delayed PWM pulse**

Set Frequency (kHz)	Approximated time delay (µs)
400	7.0
600	4.7
800	3.7

Set Frequency (kHz)	Approximated time delay (µs)
1000	3.0
1200	2.6
1400	2.3
1600	2.1
2000	1.8

12.5 Soft-start

The TDA38540 has an internal digital soft-start to control the output voltage rise and to limit the input current surge at start-up. To ensure a correct start-up, the soft-start sequence initiates when the EN and VCC voltages rise above their respective thresholds. The internal soft-start signal rises linearly from 0 V to 0.6 V in a defined time duration. The soft-start time does not change with the output voltage. The TDA38540 has two soft-start time options, 1 ms and 4 ms, selected by placing a resistor from ILIM/SS to AGND. **Table 7** lists the resistor values and their corresponding soft-start time. Please note that the ILIM/SS pin is a multi-function pin, which is also used to select different Overcurrent Protection (OCP) limits. The selection of ILIM/SS cannot be changed on the fly. To change the selection, VCC must be cycled.

Table 7. Configuration Resistors for ILIM/SS pin

ILIM/SS Resistor (kΩ) ± 10%	ILIM (A)	SS (ms)
33	52	1
18	42	
10	32	
0	22	
Floating	52	4
120	42	
82	32	
56	22	

12.6 Enabling the TDA38540

The EN pin controls the on/off state of the TDA38540. An internal Undervoltage Lock-Out (UVLO) circuit monitors the EN voltage. When the EN voltage is above an internal threshold, the TDA38540 starts to switch after a turn-on delay, which is usually within 1 ms.

Figure 13 shows three ways to configure EN. Configuration 1 and 2 are mainly for standalone mode or for the Primary phase in stackable mode. It is recommended to use configuration 3 for the Secondary devices, because the on/off of state the Secondary units are controlled by the Primary through the ISHARE bus.

To ensure a proper power on, the EN signal should be pulled up after VCC has passed the UVLO threshold, as shown in **Figure 11** and **Figure 14**. The time duration from VCC passes the UVLO threshold to when EN can be pulled up is not critical. If an external VCC is used, PVin can be applied either before or after VCC. There is no specific power sequencing requirement for power off.

With configuration 2, the Enable signal is derived from the PVin voltage by a resistive divider, REN1 and REN2. By selecting different divider ratios, users can program a UVLO threshold voltage for the bus voltage. This is a very desirable feature because it prevents the TDA38540 from operating until PVin is higher than a desired voltage level. Below is the recommended design guideline of R_{EN1} and R_{EN2}, where PV_{in_min} is the minimum input voltage, 4.5 V is the minimum recommended PV_{in} using the internal LDO, and EN_UVLO_Start_max is the maximum limit of the EN start threshold.

$$\max(PV_{in\_min}, 4.5\ V) \times \frac{R_{EN2}}{R_{EN1}+R_{EN2}} \geq EN\_ULVO\_Start\_max$$

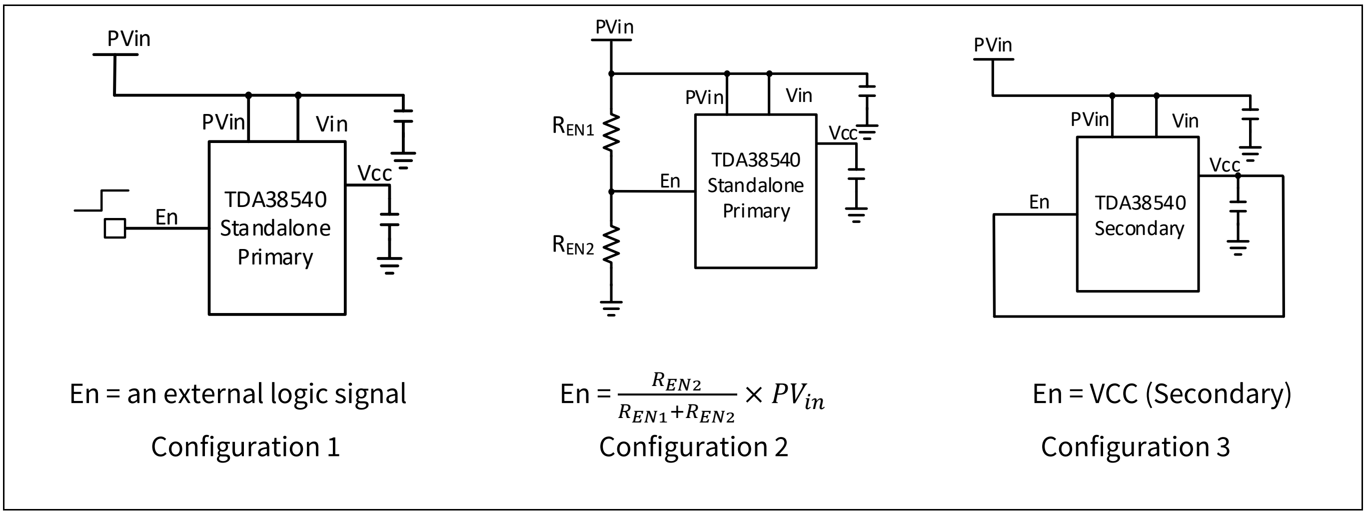


Figure 13 **Enable Configurations: Configuration1 & 2 are for standalone mode or for the Primary phase in stackable mode. Configuration 3 is for Secondary phases.**

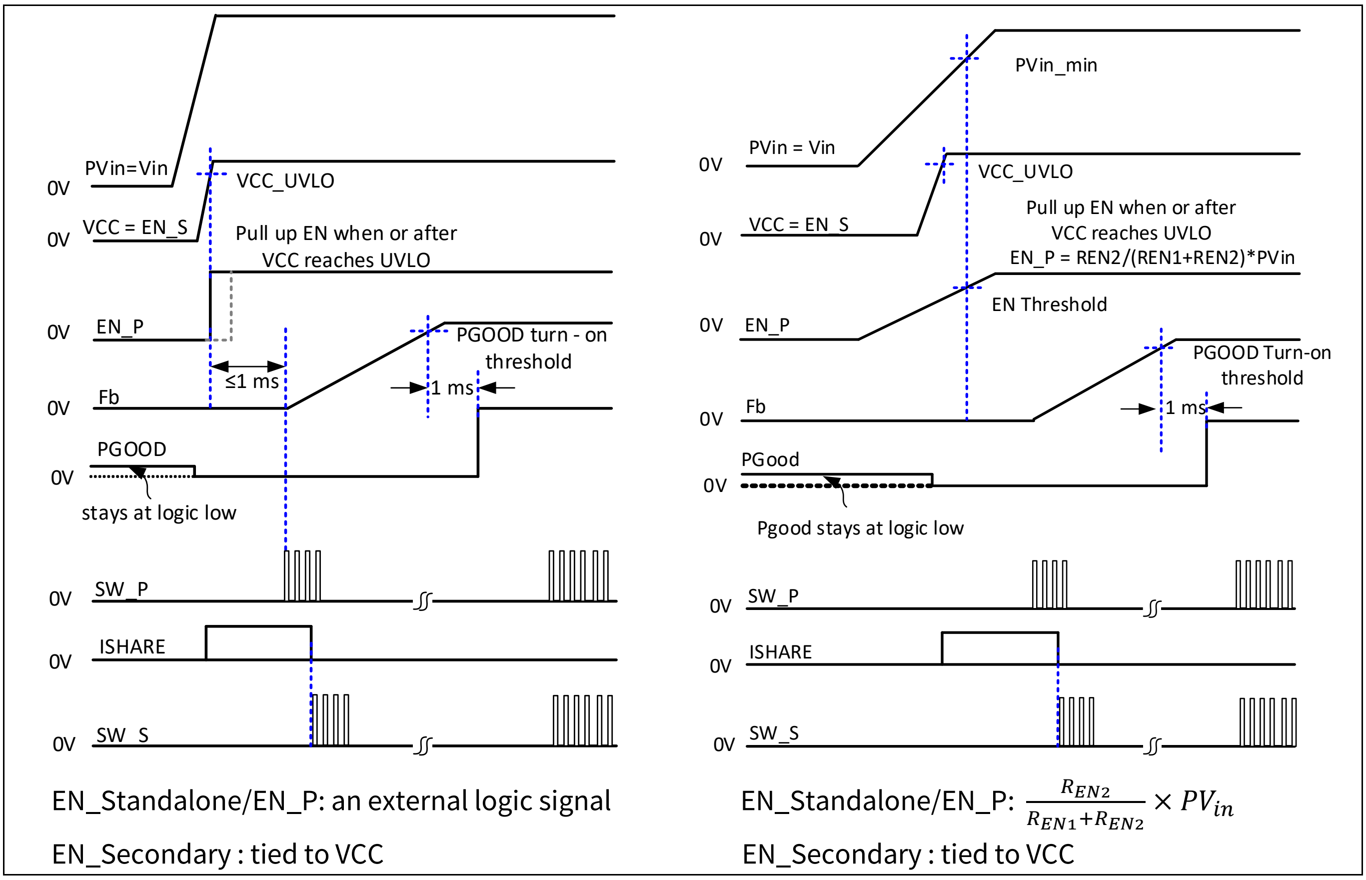


Figure 14 **Start-up sequence**

12.7 Pre-bias Start-up

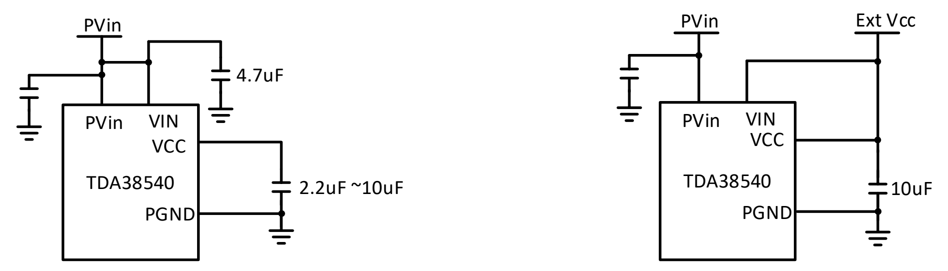
The TDA38540 is able to start up into a pre-charged output without causing oscillations and disturbances of the output voltage. When the TDA38540 starts up with a pre-biased output voltage, both control FET and synch FET are kept off until the internal soft-start signal exceeds the pre-bias voltage on the FB pin.

12.8 Internal Low-Dropout (LDO) Regulator

The TDA38540 has an integrated low-dropout (LDO) regulator providing the bias voltage for the internal circuitry. When using the internal LDO for single-rail operation, VIN should be connected to PVIN. To save the power losses on the LDO, an external bias voltage can be used by connecting VIN to VCC/LDO. **Figure 15** illustrates the configuration of the VCC/LDO and VIN pins.

Section 7.1 specifies the recommended operating voltage range of VIN and VCC under different configurations. The following design guidelines are recommended.

- Place a bypass capacitor to minimize disturbance on the VCC pin. For single-rail operation using the internal LDO, a 4.7 µF low ESR ceramic capacitor must be used between VIN and PGND and a 2.2 µF to 10 µF low ESR ceramic capacitor is required to be placed close to the VCC/LDO pin referenced to PGND. A 10 µF MLCC is recommended for the VCC bypass capacitor when VIN is below 5.5 V. When using an external VCC bias voltage, a 10 µF ceramic capacitor can be shared by VIN and VCC/LDO.



Single rail operation with the internal LDO

Use an external VCC

Figure 15 **Configuration of Using the internal LDO or an external VCC.**

12.9 Positive Low-side Overcurrent Protection (OCP)

The TDA38540 monitors the current of the synchronous MOSFET through its $R_{DS(on)}$. Four current limit options are available. The OCP threshold is set by the resistance at ILIM/SS as shown in **Table 7**. The selected OCP limit value is loaded to the IC's operating memory during power up and cannot be changed on the fly. To change the OCP limit, users must cycle VCC. The OCP is activated after EN is above its threshold.

Figure 16 illustrates OCP operation in stackable mode operation. In standalone mode, the OCP operation is the same as that for the Primary phase. Inductor current is checked near the end of each switching cycle. When a single OCP event is detected, OCP fault is registered and PGOOD is pulled low. In the meantime, the TDA38540 turns off both FETSETs and enters hiccup mode with 20 ms blanking time. After the completion of blanking time, the TDA38540 attempts to recover to the nominal output voltage with a soft-start. It repeats hiccup mode and attempts to recover until the OCP condition is removed.

In stackable mode, there is some difference in the OCP operation between Primary and Secondary phases. Primary enters hiccup mode immediately after an OCP event is detected, and pulls ISHARE high to broadcast the fault to all Secondary phases that enter hiccup mode subsequently.

If a Secondary phase detects an OCP event prior to Primary phase, it skips the next PWM pulse to ramp down the phase current. If the OCP event is no longer detected at the beginning of the following switching cycle, the PWM pulse resumes. Otherwise, the PWM pulse is skipped again. ISHARE and other phases remain in normal operation. In conclusion, OCP of Secondary phases does not trigger hiccup mode. But if the Primary also detects OCP, it will pull down ISHARE to force all Secondary phases to enter hiccup mode, as shown in **Figure 16**.

As discussed above, the TDA38540 senses the valley current for OCP. Therefore, the OCP limits specified in **Section 7** is referred to the valley of the inductor current. The corresponding output dc current can be calculated as follows:

$$I_{out\_OCP} = I_{LIM\_P} + \frac{\Delta i_L}{2}$$

Where: I_{out_OCP} is the output dc current when OCP is tripped. I_{LIM_P} = positive OCP limit specified in the **Section 7**, which is the valley of inductor current. ΔiL is the Peak-peak inductor ripple current.

To avoid inductor saturation during OCP events, the following criterion is recommended for the inductor saturation current rating.

$$I_{sat} \geq I_{LIM\_P\_max} + \Delta i_L$$

Where: I_{sat} is the inductor saturation current and $I_{LIM\_P\_max}$ is the maximum spec of the positive OCP limit.

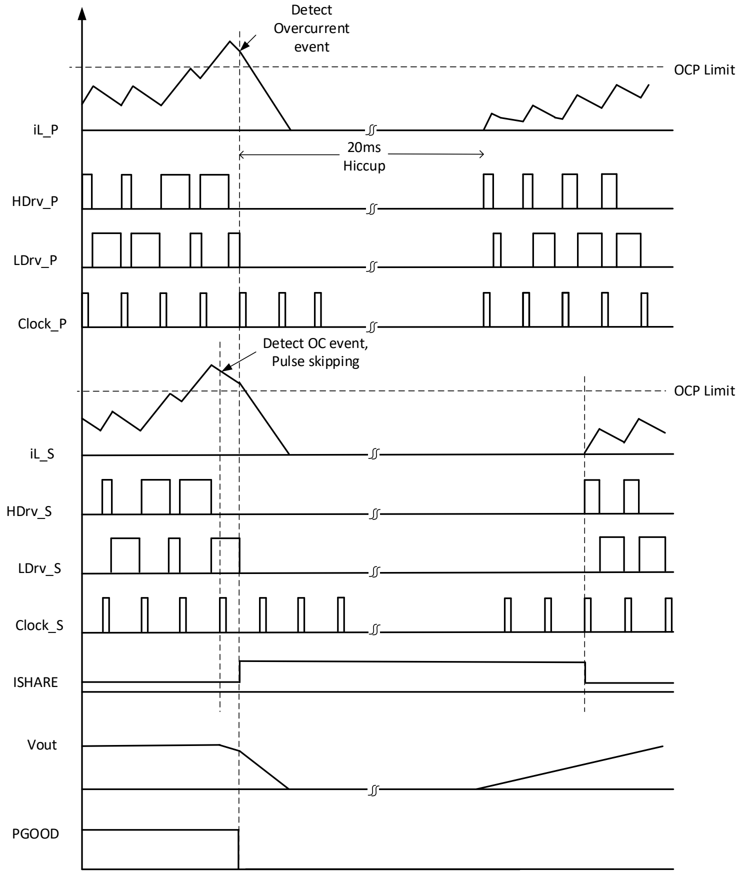


Figure 16 **Operation of positive low-side OCP in stackable mode. In this case, OCP of Secondary is detected earlier than that of Primary, but does not enter hiccup mode until Primary also detects OCP.**

12.10 Negative Low-Side Overcurrent Protection (OCP)

The TDA38540 also features a negative low-side OCP with a fixed OCP limit. Similar to the positive OCP, the negative OCP circuit also monitors the current of the synchronous MOSFET through its $R_{DS(on)}$ during the off time. If the current drops below -20 A, the synchronous MOSFET is turned off for about 200 ns to let the current flow through the body diode of the control MOSFET. This feature is intended to prevent the occurrence of excessive negative current, such as during a large load release or an OVP event.

12.11 Undervoltage Protection (UVP)

Under Voltage Protection (UVP) provides additional protection during OCP fault or other faults. UVP circuitry monitors the FB voltage and is activated during start-up when the FB voltage rises above around 200 mV. When the FB voltage drops below the UVP threshold for a duration longer than the UVP protection delay, an undervoltage trip signal asserts and both the control MOSFET and the synchronous MOSFET are turned off. The TDA38540 then enters hiccup mode with a blanking time of 20 ms, during which the control MOSFET and the synchronous MOSFET remain off. After the completion of blanking time, the TDA38540 attempts to recover to the nominal output voltage with a soft-start, as shown in **Figure 17**. The TDA38540 will repeat hiccup mode and attempt to recover until the UVP condition is removed.

Please note that UVP is available in standalone mode and on the Primary in stackable mode, but not on the Secondary in stackable mode. When Primary detects a UV fault, ISHARE is pulled high and all phases enter hiccup mode.

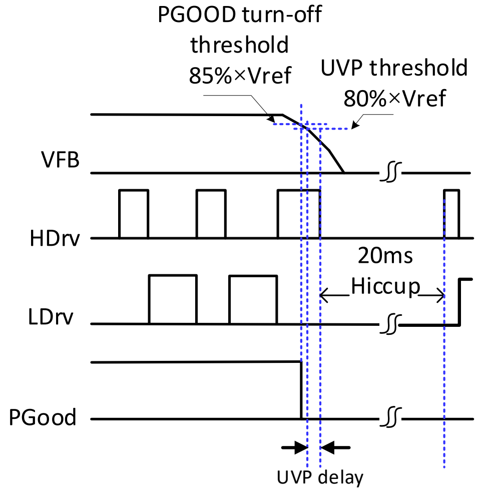


Figure 17 **Illustration of output UVP operation**

12.12 Overvoltage Protection (OVP)

Overvoltage Protection (OVP) is achieved by comparing the FB voltage to a fixed internal OVP threshold voltage equal to 120% of the reference voltage, V_{ref}. When the FB voltage exceeds the OVP threshold for a time duration longer than the OVP delay, an overvoltage trip signal is asserted. The control MOSFET is latched off immediately and PGOOD flags low. The synchronous MOSFET remains on to discharge the output capacitor until the FB voltage drops below 115% of V_{ref}, after which the device enters hiccup mode with a blanking time of 20 ms. After hiccup blanking time expires, the TDA38540 tries to restart with a soft-start. The OVP operation is illustrated in **Figure 18**. OVP becomes active after Power On Ready (POR) is high regardless if EN is high or low.

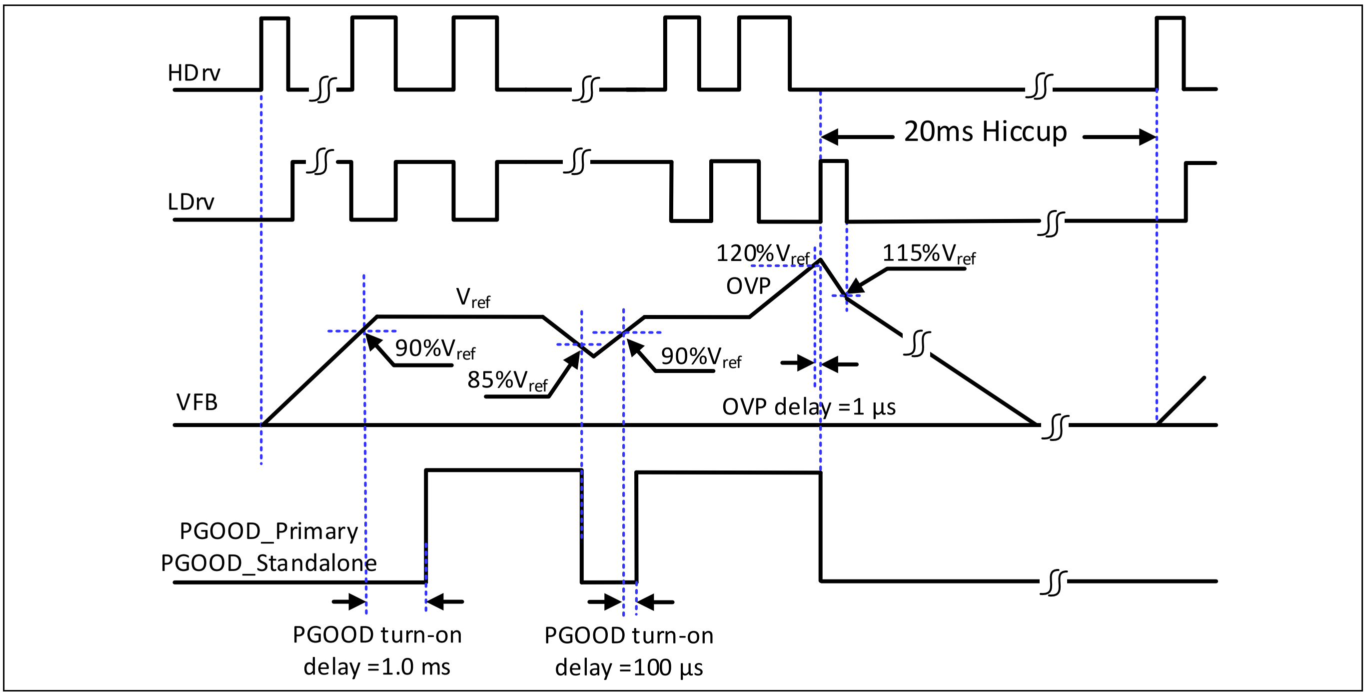


Figure 18 **Illustration of OVP. Please note that PGOOD turn-on delay of 1.0 ms is only applied to standalone mode or the Primary in stackable mode. After soft - start, if Vout drops below the PGOOD threshold without triggering UVP, PGOOD will be pulled high with about 100 µs delay after Vout recovers.**

12.13 Overtemperature Protection (OTP)

Temperature of the controller is monitored internally. When the temperature exceeds the overtemperature threshold (170 °C typical), OTP circuitry turns off both control and synchronous MOSFETs and resets the internal soft start. The device enters hiccup mode with a blanking time of 20 ms. After hiccup blanking time expires, if the sensed temperature drops below 150 °C (typical), the TDA38540 tries to restart with a soft-start. If the sensed temperature is above overtemperature threshold, the TDA38540 initiates another 20 ms of hiccup blanking time. OTP will cycle in this manner till the cause of the overtemperature event is removed.

12.14 Power Good (PGOOD) Output

The PGOOD signal is used to indicate that output voltage is in regulation and the TDA38540(s) is operating properly. The PGOOD pin is the open drain of an internal NFET, and needs to be externally pulled high through a pull-up resistor. In stackable mode, it is recommended to use PGOOD of Primary as system-level PGOOD. **Figure 18** illustrates the PGOOD response. Detailed PGOOD behavior is summarized in **Table 8**.

Note that during start-up with a pre-biased voltage, the PGOOD signal is held low before the first PWM pulse is generated and is then pulled high with the PGOOD turn-on delay after FB voltage rises above the PGOOD threshold.

Please also note that during start-up, PGOOD is asserted 1 ms after FB voltage rises above the PGOOD turn-on threshold. However, in operation, if FB voltage momentarily drops below PGOOD turn-off threshold, causing PGOOD to be pulled low, but it could recover without triggering UVP, PGOOD is re-asserted with just 100 µs delay, to reduce system recovery time.

Table 8. Criteria for PGOOD Assertion for Standalone and for Primary Phase in Stackable Mode

	Standalone	Primary in Stackable mode
Criteria for PGOOD Assertion	1. EN signal and VCC voltage are above their respective thresholds 2. V_{out} is in regulation 3. No faults are triggered including output UV, OV fault, OT fault, and OC fault	1. EN signal and VCC voltage of Primary phase are above their respective thresholds 2. EN signal of Secondary phases are above their respective thresholds **Note 12** 3. V_{out} is in regulation 4. No faults are triggered on Primary including output UV, OV fault, OT fault, and OC fault 5. No output UV, OV fault, and OT fault are triggered on Secondary phases **Note 12**

Note:

12. VCC voltages of Secondary phases need to be present.

12.15 Selection of Internal Ramp

The inner current loop of the TDA38540 employs peak-current-mode control. To ensure loop stability and to provide some flexibility to adjust the current loop response, the TDA38540 implements eight selectable internal ramp compensation gains, Kramp, which can be selected by connecting a resistor from RAMP pin to AGND, as shown in **Table 9**.

Table 9. Configuration for RAMP pin

RAMP Resistor (kΩ) ± 10%	Kramp
0	20×10^{-3}
10	40×10^{-3}
18	60×10^{-3}
33	80×10^{-3}
56	100×10^{-3}
82	130×10^{-3}
120	160×10^{-3}
Floating	200×10^{-3}

To ensure the inner current loop stability, Kramp is recommended to satisfy the following criteria.

$$K_{ramp} \geq \frac{10^{-2} \times (2 - D)}{2 f_{sw} L}$$

Higher Kramp can help improve noise immunity and switching node jitter, but reduces the bandwidth of the inner current loop.

12.16 Minimum and Maximum Duty Ratio

The minimum on-time, $T_{on(min)}$, and the minimum off-time, $T_{off(min)}$, are specified in **Section 7.2**. They set limitations on the achievable minimum duty ratio and the maximum duty ratio for any given switching frequency.

$$D_{min} = (T_{on(\mathrm{min})} + T_{db(rise)}) \times f_{sw} \times 1.1$$

$$D_{max} = 1 - T_{off(\mathrm{min})} \times f_{sw} \times 1.1$$

It should be noted that, the worst case, D_{min}, occurs at no load. Due to the negative inductor current, the effective on-time is increased by the dead time on the PWM rising edge, which should be considered in the calculation. To ensure sufficient design margin, the maximum specification of $T_{on(min)}$ and $T_{off(min)}$ must be used in the above equations. 10% f_{sw} variations have also been considered in the equations. **Figure 19** shows the minimum and maximum achievable Vout at different PVIN and f_{sw}.

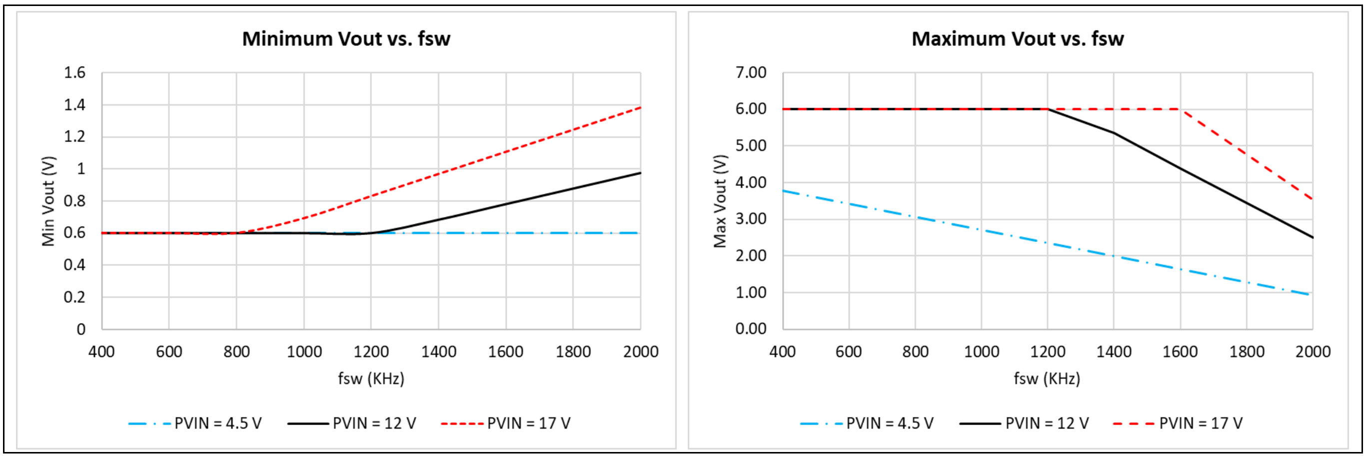


Figure 19 **Minimum and maximum achievable Vout at different PVIN and f_{sw}.**

12.17 Output Voltage Programming

Output voltage can be programmed with an external voltage divider. The FB voltage is compared to an internal reference voltage of 0.6 V. The divider ratio is set to provide 0.6 V at the FB pin when the output is at its desired value.

$$V_{out} = V_{ref} \times (1 + \frac{R_{FB1}}{R_{FB2}})$$

Where, R_{FB1} is the top feedback resistor and R_{FB2} is the bottom feedback resistor.

Small leakage currents flow into FB and VSHARE which have some adverse impact on the output voltage accuracy, it is recommended to select R_{FB1} as follows.

$$R_{FB1} = \frac{n \times V_{out}}{G_m \times V_{ref}}$$

Where, n = total phase count and G_m = 1.5 m, transconductance of the amplifier. For the unoptimized R_{FB1} value different from the calculation above, the resulting V_{out} error can be calculated as below.

$$\Delta V_{out\_LK} = IV_{FB} \times (R_{FB1} - \frac{n \times (R_{FB1} + R_{FB2})}{G_m \times R_{FB2}})$$

Where, IV_{FB} is the leakage current of FB pin. The worst case IV_{FB} current is 1 μA occurring at 150°C.

12.18 Output voltage sensing

The TDA38540 can be configured for either remote sensing or single-ended sensing through VSENM pin, as shown in **Figure 3** and **Figure 20** respectively. Remote V_o sensing is often used when the TDA38540 is placed away from the load. The output voltage at a remote location is sensed to compensate for the voltage drop on the PCB traces. Single-ended sensing can be used when the voltage drop on the PCB traces is of less concern. It offers simpler PCB routing.

It should be noted that the VSENM pin carries some internal bias current. Therefore, it is not recommended to add additional resistor to the VSENM sensing line. Otherwise, the induced voltage drop on the VSENM sensing line can affect V_o regulation.

When connecting V_o sense lines to the output, sense points should be always tapped from a high-frequency bypass capacitor of 0.1 µF or higher. Please refer to **Section 15** for more information of PCB routing.

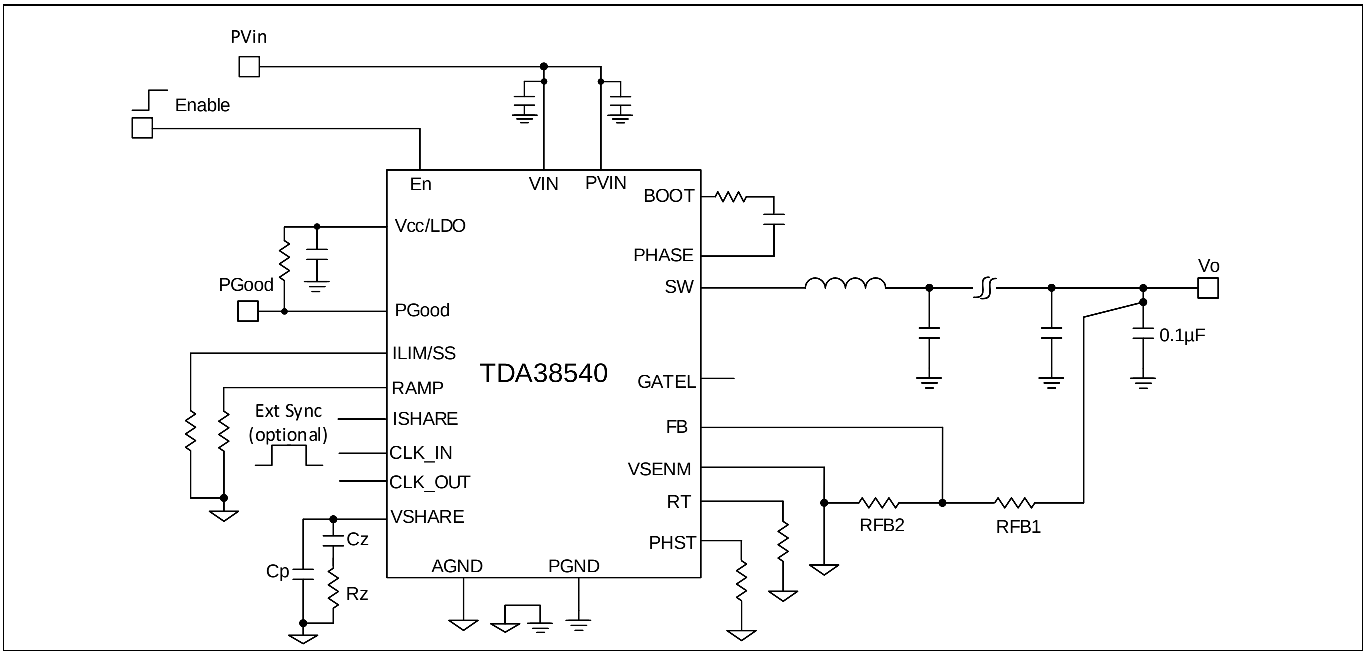


Figure 20 Configuration of single-ended Vout sensing

13 Design Example

In this section, an example is used to explain how to design a 2-phase buck regulator with the TDA38540. The application circuit is shown in **Figure 3** . The design specifications are given below.

- PV_{in} = 12 V (±10%)
- V_{out} = 1.0 V
- I_o = 80 A total, 40 A/Phase
- F_{sw} = 800 kHz
- V_{out} ripple voltage = ±1% of V_o
- Load transient response = ± 4% of V_{out} with a step load current = 40 A and slew rate = 10 A/µs

13.1 Enabling the TDA38540

The TDA38540 has a precise EN threshold voltage, which can be used to implement a UVLO of the input bus voltage by connecting the EN pin to PVin with a resistor divider, as shown in Configuration 2 of **Figure 13**.

Therefore, the EN resistor divider of Primary phase, R_{EN1} and R_{EN2}, can be calculated as follows.

$$\max(PV_{in\_min}, 4.5) \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \geq EN\_ULVO\_Start\_max$$

Where *EN_UVLO_Start_max* = 1.36 V. For PV_{in_max} = 10.8 V, select R_{EN1}= 49.9 kΩ, and R_{EN1}= 7.5 kΩ.

The EN of Secondary phase is tied to the VCC as shown in Configuration 3 of **Figure 13**.

13.2 Configuring operation mode and phase Shift

The TDA38540 can support up to 4-phase operation. As shown in **Table 3**, to configure a 2-phase operation, the PHST pin of the Primary phase can be left floating or be connected to a quiet ground (AGND or PGND) through a 120 kΩ resistor. The PHST of the Secondary phase should be connected to the ground through a 33 kΩ resistor, to achieve 180 ° phase shift.

13.3 Programming the switching frequency

To set the switching frequency at 800 kHz, the RT pin of both Primary phase and Secondary phase should be connected to an 18 kΩ resistor. Please refer to **Table 5**.

13.4 Selecting input capacitors

Without input capacitors, the pulse current of Control MOSFET is directly from the input supply power. Due to the impedance on the cable, the pulse current can cause disturbance on the input voltage and potential EMI issues. The input capacitors filter the pulse current, resulting in almost constant current from the input supply. The input capacitors should be selected to tolerate the input pulse current, and to reduce the input voltage ripple. The RMS value of the input ripple current can be expressed by:

$$I_{RMS} = I_0 \times \sqrt{(D - \frac{m}{n}) \times (\frac{1+m}{n} - D)}$$

$$D = \frac{V_o}{PV_{in}}; m = Integer\ (n \times D)$$

Where, I_{RMS} is the RMS value of the input capacitor current; I_0 is the output current, D is the Duty Cycle; n is the total phase count; and m is the integer part of $(n \times D)$. For I_0 = 80 A and $D_{(max)}$ = 0.09, the resulting RMS current flowing into the input capacitor is about 15 A.

To meet the requirement of the input ripple voltage, the minimum input capacitance can be calculated below.

$$C_{in(\min)} > \frac{I_o \times (\frac{m+1}{n} - D) \times (D - \frac{m}{n})}{f_{sw} \times (\Delta PV_{in} - ESR \times I_o \times \left(\frac{m+1}{n} - D\right))}$$

Where ΔPVin is the maximum allowable peak-to-peak input ripple voltage, and ESR is the equivalent series resistor of the input capacitors. Ceramic capacitors are recommended due to low ESR, ESL and high RMS current capability. For I_o = 80 A, f_{sw} = 800 kHz, and ΔPV_{in} = 240 mV, $C_{in(min)}$ > 15 µF. Due to layout constraints, the coupling of the input capacitors between each phase is usually not as good as in theory, in real applications, which reduces the effectiveness of the input ripple current cancellation, and usually more input capacitance than the calculation is desired. In addition, to account for the de-rating of ceramic capacitors under a bias voltage and to consider the current rating, 10 x 22 µF/0805/25V MLCC are used for the input capacitors for each phase. Additional bulk capacitors are recommended if the input supply is not located close to the voltage regulator.

13.5 Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value results in a large ripple current, lower efficiency and high output noise, but helps with size reduction and transient load response. Generally, the desired peak-to-peak ripple current in the inductor (Δi) is found between 20% and 60% of the output current.

The inductor saturation current must be higher than the maximum spec of the OCP limit plus the peak-to-peak inductor ripple current. For some core material, inductor saturation current may decrease as the increase of temperature. So, it is important to check the inductor saturation current at the maximum operating temperature.

The inductor value for the desired operating ripple current can be determined using the following relation:

$$L = (1 - \frac{V_0}{PV_{in(\max)}}) \times \frac{V_0}{\Delta i_{Lpp} \times F_{sw}}$$

$$I_{sat} \geq OCP_{max} + \Delta i_{Lpp}$$

Where $PV_{in(max)}$ = Maximum input voltage; Δi_{Lpp} = Peak-to-peak inductor ripple current per phase; OCP_{max} = maximum spec of the OCP limit as defined in **Section 7**; and I_{sat} = inductor saturation current. In this case, select inductor L =150 nH to achieve Δi_{Lpp} = 20% of phase current. The I_{sat} should be no less than 67 A.

13.6 Output Capacitor Selection

The output capacitor selection is mainly determined by the output voltage ripple and transient requirements.

To satisfy the V_0 ripple requirement, C_0 should satisfy the following criterion.

$$C_o > \frac{\Delta i_{nLpp}}{8 \times \Delta V_{or} \times n \times f_{sw}}$$

Where, ΔV_{or} = desired output ripple voltage, Δi_{nLpp} = combined output peak to peak ripple current from each phase current. Due to the interleaved operation, the equivalent total output ripple current in multiphase operation is smaller than that in single-phase operation and can be calculated as follows.

$$\Delta i_{nLpp} = \frac{\Delta i_{Lpp} \times n \times \left(D - \frac{m}{n}\right) \times \left(\frac{m+1}{n} - D\right)}{D(1-D)}$$

Where Δi_{Lpp} is the peak-to-peak inductor ripple current of one phase. m is a factor as defined in **Section 13.4**. n is the total phase count and D is the duty-ratio.

For Δi_{Lpp} = 7.6 A, ΔV_{or} = 20 mV, f_{sw} = 800 kHz, C_o must be larger than 27 µF. The ESR and ESL of the output capacitors, as well as the parasitic resistance or inductance due to PCB layout, can also contribute to the output voltage ripple. It is suggested to use Multi-Layer Ceramic Capacitor (MLCC) for their low ESR, ESL and small size.

To meet the overshoot requirements during the load transient, the output capacitors should meet the following criterion.

$$C_o > \frac{L \times \Delta I_o^2}{2 \times n \times \Delta V_{oL} \times V_{out}}$$

Where, ΔV_{oL} is the allowable Vout deviation during the load transient. ΔI_o is the step load current.

To meet the undershoot requirements during the transient load, the output capacitors should also meet the following criterion.

$$C_o > \Delta I_o \times \frac{(1-D)}{\Delta V_{oL} \times f_{sw}} + \frac{\Delta I_o^2 \times L}{2 \times \Delta V_{oL} \times n \times (V_{in} - V_{out})}$$

The resulting $C_o$should meet both criterial. Please note that the impact of ESL, ESR, control loop response, transient load slew rate, and PWM latency is not considered in the calculation shown above. Extra capacitance is usually needed to meet the transient requirements.

In this case, to meet the transient load requirement (i.e. ΔV_{oL}= 40 mV, ΔI_o = 40 A), calculated C_o should be higher than 1500 µF for overshoot requirement, and should be higher than 1282 µF to satisfy undershoot requirement. 2300 µF is selected in the final design. For more accurate estimation of C_o, simulation tool can be used to aid the design.

13.7 Selection of FB Resistors

As discussed in **Section 12.17**, it is recommended to select the FB resistors as follows.

$$R_{FB1} = \frac{n \times V_{out}}{G_m \times V_{ref}}$$

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{out}}{V_{ref}} - 1}$$

With n = 2, G_m= 1.5m, V_{out} = 1 V, V_{ref} = 0.6 V, select R_{FB1} = 2.21 kΩ, R_{FB2} = 3.32 kΩ.

13.8 Designing Voltage Loop Compensation

Thanks to the peak current-mode control, the LC double pole seen with voltage mode control is separated by the inner current loop, referred as the low-frequency pole and the high-frequency pole below.

The voltage loop DC gain is

$$K_{DC} = \frac{F_m n R_{Load} P V_{in}}{n\, R_{Load}(1 + F_m F_V P V_{in}) + F_m R_{sen} P V_{in}} \times \frac{V_{ref}}{V_{out}}$$

The location of the low-frequency pole is

$$\omega_{LFP} = \frac{n \times (1 + F_m F_v P V_{in}) + F_m R_{sen} P V_{in}}{\left(C_{o1} + C_{o2} + \frac{C_{o2} ESR2}{R_{Load}}\right) F_m R_{sen} P V_{in} + \frac{L}{R_{Load}}}$$

The location of the high-frequency pole is

$$\omega_{HFP} = \frac{\left(C_{o1} + C_{o2} + C_{o2} \times \frac{ESR2}{R_{Load}}\right) F_m R_{sen} P V_{in} + \frac{L}{R_{Load}}}{\left(C_{o1} + C_{o2} + C_{o2} \times \frac{ESR2}{R_{Load}}\right) \times L}$$

Where

$$F_m = \frac{D}{K_{ramp} \times V_{out} - \Delta i_{Lpp} \times R_{sen}}$$

$$F_V = \frac{\Delta i_{Lpp} \times R_{sen}}{2 \times (1 - D) \times V_{out}}$$

C_{o1} and C_{o2} are two types of output capacitors, e.g. MLCC and electrolytic capacitors. The corresponding equivalent series resistance of C_{o1} and C_{o2} is ESR1 and ESR2 respectively. R_{Load} is the load resistance. R_{sen} is the equivalent current sensing resistance, equal to ~ 10 mV/A. Since ESR of MLCC is usually small, ESR1 is ignored here to simplify the calculation. For constant current load, the above formulas are still valid by treating R_{Load} as an infinite value.

The ESR zero of C_{o2} is located at

$$\omega_{ESR2} = \frac{1}{C_{o2} \times ESR2}$$

the TDA38540 uses a type -II compensator for its voltage loop compensation, as shown in **Figure 3**. The transfer function can be expressed as below.

$$H_v(s) = \frac{K_v\left(1 + \frac{s}{\omega_z}\right)}{s\left(1 + \frac{s}{\omega_p}\right)}$$

Where

$$\omega_z = \frac{1}{R_z C_z},\ \omega_p = \frac{C_z + C_p}{R_z C_z C_p}, K_v = \frac{G_m}{C_p + C_z}$$

Table 10 provides the compensation design guidelines as the starting point. Further optimization is usually recommended for optimized loop performance. ω_c is the desired cross-over frequency of the voltage loop.

Table 10. Placement of compensator zero and pole

Location of ESR zero	Placement of compensator zero & pole	Compensation design
$\omega_c < \omega_{ESR2}$	$\omega_z = 0.75\omega_{LFP}, \omega_p = \frac{\omega_{sw}}{2}$ $K_v = \frac{\omega_c \omega_z}{K_{DC}\omega_{LFP}}$	$C_p = \frac{\omega_z G_m}{\omega_p K_v}, C_z = \frac{G_m}{K_v} - C_p, R_z = \frac{1}{\omega_z C_z}$

Location of ESR zero	Placement of compensator zero & pole	Compensation design
$\omega_{LFP} < \omega_{ESR2} < \omega_c$	$\omega_z = 0.75\omega_{LFP}, \omega_p = \frac{\omega_{sw}}{2}$ $K_v = \frac{\omega_c \omega_z \omega_{ESR2}}{K_{DC}\omega_{LFP}}$	

It has been calculated in **Section 13.6** that 2300 µF is selected for C_o. This can be achieved with 12 x 47 µF and 4 x 470 µF with ESR = 6 mΩ. If the desired cross-frequency is 100 kHz and 100 m is selected for k_{ramp}, the calculated compensation parameters are shown below.

Table 11. **Summary of compensation calculations**

Parameter	Value	Parameter	Value
C_o	$12 \times 47\ \mu F + 4 \times 470\ \mu F/6\ \text{m}\Omega$	Kramp	100m
R_{sen}	10 mΩ	R_Z	5.49 kΩ
C_z	4.7 nF	C_p	120 pF

13.9 Selecting Internal Ramp Compensation

As discussed in **Section 12.15**, K_{ramp} should meet the following criterion to ensure the inner current loop stability. Smaller K_{ramp} leads to a higher current loop gain and maybe more phase margin, but may also result in higher switching jitter. As a tradeoff, 100m is selected for K_ramp.

$$K_{ramp} \geq \frac{10^{-2} \times (2 - D)}{2 f_{sw} L}$$

I.e. $K_{ramp} \geq 80m$

13.10 Bootstrap Capacitor

For most applications, a 0.1 µF ceramic capacitor is recommended for bootstrap capacitor placed between PHASE and BOOT Pin. To ensure the maximum SW node spike voltage does not exceed 20 V, a 2 Ω resistor is used in series with the BOOT pin on the evaluation board. The resistance should be optimized with different PCB layout design and operation conditions.

13.11 PVin, Vin and VCC/LDO Bypass Capacitors

A ceramic capacitor (2.2 µF - 10 µF) should be connected between VCC/LDO and the power ground (PGND) and and a 4.7 µF MLCC is selected for Vin bypass capacitor. Besides the input capacitance calculated in Section 13.4, a 4.7 µF MLCC in 0603 package in parallel with a 2.2 µF MLCC in 0402 package are suggested placed close to the PVin pin, which proves effective in suppressing the SW node spike.

14 Application Information

14.1 Application Diagram

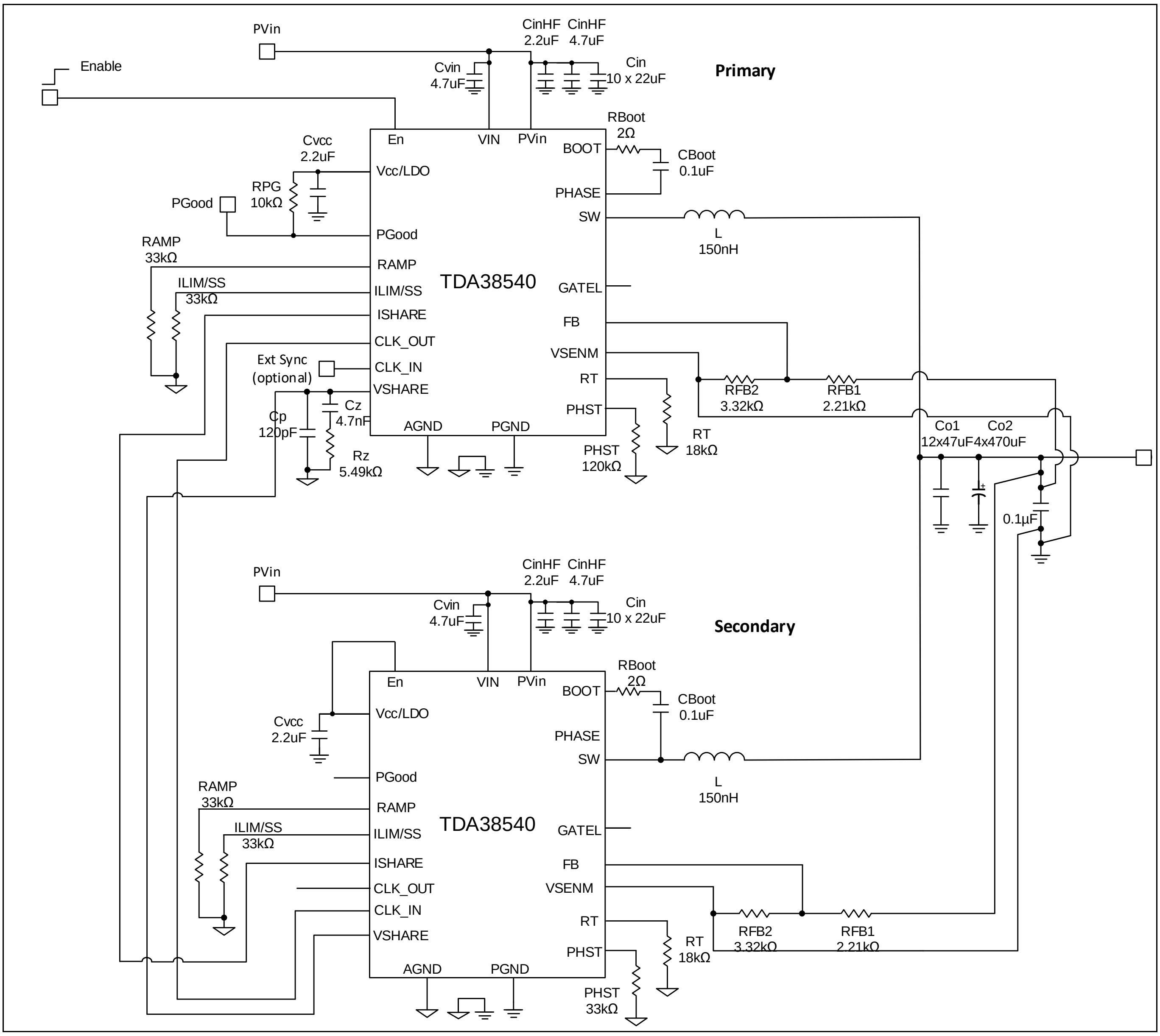
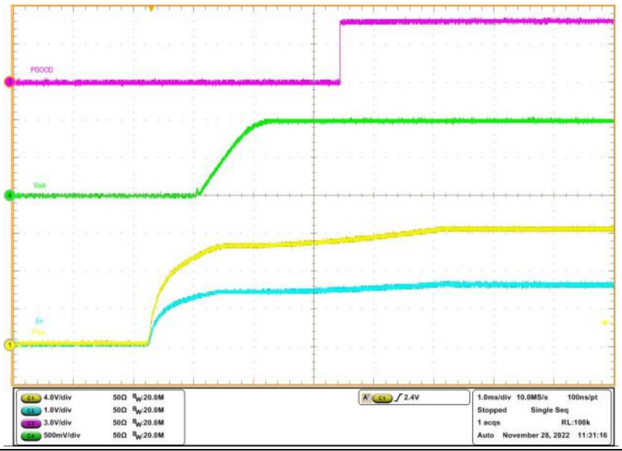


Figure 21 **Application diagram of TDA38540 with 2-phase operation. PVin = 12 V, Vout = 1 V, Io = 80 A, fsw = 800 kHz**

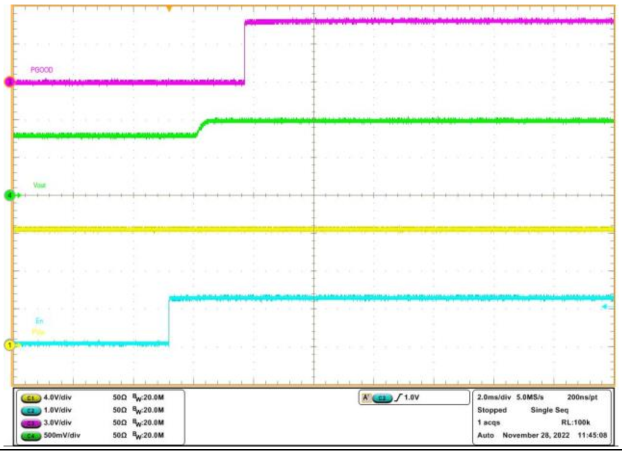
14.2 Typical Operating Waveforms

PVin = Vin = 12.0 V, Vout = 1 V, Io = 0-80 A, fsw = 800 kHz, Room Temperature, no airflow



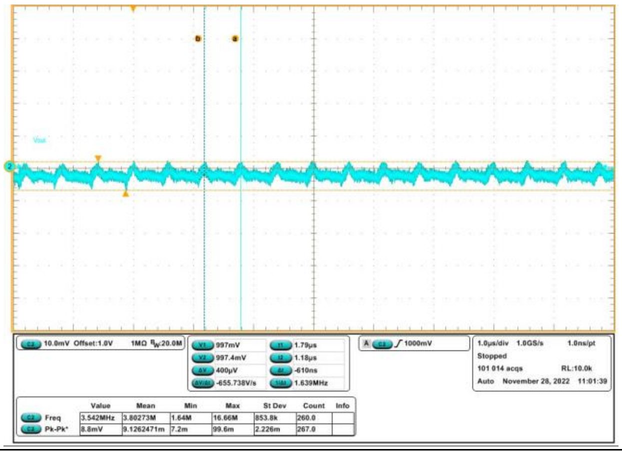
C1 4.0V/div 50Ω BW:20.0M
C2 1.0V/div 50Ω BW:20.0M
C3 3.0V/div 50Ω BW:20.0M
C4 500mV/div 50Ω BW:20.0M
A' C1 ∫ 2.4V
1.0ms/div 10.0MS/s 100ns/pt
Stopped Single Seq
1 acqs RL:100k
Auto November 28, 2022 11:31:16

Figure 22 Start-up at 80 A load (Ch1: PV$_{in}$, Ch2: Enable, Ch3: PGood, Ch4: V_o)



C1 4.0V/div 50Ω BW:20.0M
C2 1.0V/div 50Ω BW:20.0M
C3 3.0V/div 50Ω BW:20.0M
C4 500mV/div 50Ω BW:20.0M
A' C2 ∫ 1.0V
2.0ms/div 5.0MS/s 200ns/pt
Stopped Single Seq
1 acqs RL:100k
Auto November 28, 2022 11:45:08

Figure 23 Pre-bias start-up at 0 A load (Ch1: PV$_{in}$, Ch2: Enable, Ch3: PGOOD, Ch4: V$_{out}$)



C2 10.0mV Offset:1.0V 1MΩ BW:20.0M
V1 997mV
V2 997.4mV
ΔV 400μV
ΔV/Δt -655.738V/s
t1 1.79μs
t2 1.18μs
Δt -610ns
1/Δt 1.639MHz
A C2 ∫ 1000mV
1.0μs/div 1.0GS/s 1.0ns/pt
Stopped
101 014 acqs RL:10.0k
Auto November 28, 2022 11:01:39

	Value	Mean	Min	Max	St Dev	Count	Info
C2 Freq	3.542MHz	3.80273M	1.64M	16.66M	853.8k	260.0	
C2 Pk-Pk*	8.8mV	9.1262471m	7.2m	99.6m	2.226m	267.0	

Figure 24 V$_{out}$ ripple at 80 A load, f$_{sw}$ = 800 kHz (Ch2: V$_{out}$), peak to peak V$_{out}$ ripple = 8.8 mV

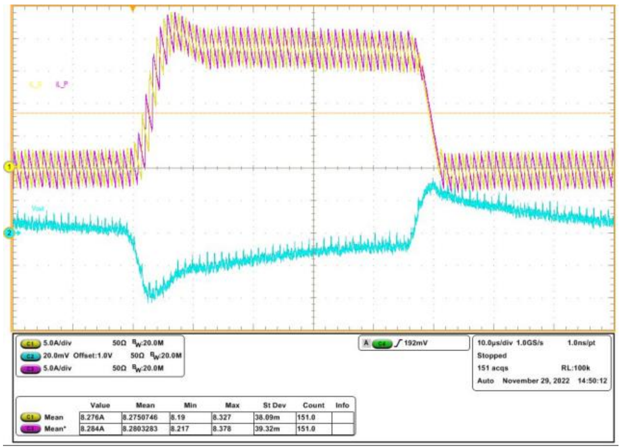
C2 5.0V/div 50Ω B_W:2.5G
C3 5.0V/div 50Ω B_W:2.5G

A C3 ∫ 4.8V

500ns/div 1.0GS/s 1.0ns/pt
FastAcq Sample
2 417 574 acqs RL:5.0k
Auto March 11, 2024 15:57:08

	Value	Mean	Min	Max	St Dev	Count	Info
C2 Freq	825.4kHz	825.33713k	822.9k	825.6k	84.98	651.0	
C3 Freq	827.0kHz	827.00514k	824.1k	827.4k	196.1	651.0	
C2C3 Phas*	-175.2°	-175.22039	-175.5	-175.1	35.32m	651.0	

Figure 25 SW node, 80 A load, f_{sw} = 800 kHz



C1 5.0A/div 50Ω B_W:20.0M
C2 20.0mV Offset:1.0V 50Ω B_W:20.0M
C3 5.0A/div 50Ω B_W:20.0M

A C4 ∫ 192mV

10.0µs/div 1.0GS/s 1.0ns/pt
Stopped
151 acqs RL:100k
Auto November 29, 2022 14:50:12

	Value	Mean	Min	Max	St Dev	Count	Info
C1 Mean	8.276A	8.2750746	8.19	8.327	38.09m	151.0	
C3 Mean*	8.284A	8.2803283	8.217	8.378	39.32m	151.0	

Figure 26 Transient response at 40 A step-load current at 10 A/µs slew rate: I_{out} = 0 A to 40 A (Ch_1: iL_s, Ch_3: iL_p, Ch_2: V_{out}), f_{sw} = 800 kHz. Peak-to-Peak: 80 mV

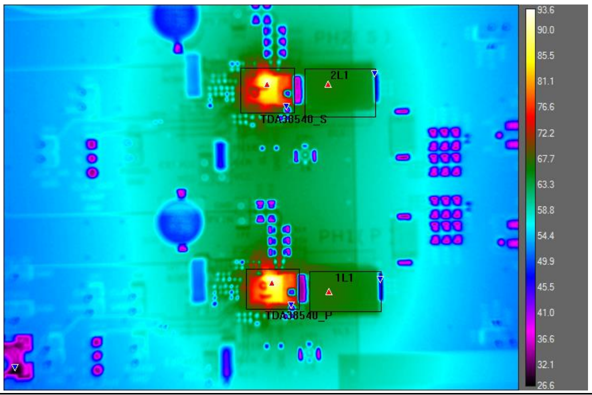


Figure 27 Thermal image of the board at 80 A load. TDA38540 (P)= 94 °C, L (P) = 66 °C, TDA38540 (S)= 91 °C, L (S) = 66 °C, f_{sw} = 800 kHz, T_a = 26 °C , natural convection

15 Layout Recommendations

PCB layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results. Following design guidelines are recommended to achieve the best performance.

- Bypass capacitors, including input/output capacitors, Vin and VCC bypass capacitors, should be placed near the corresponding pins as close as possible.
- Place bypass capacitors from TDA38540 power input (Drain of Control MOSFET) to PGND (Source of Synchronous MOSFET) to reduce noise and ringing in the system. The output capacitors should be terminated to a ground plane that is away from the input PGND to mitigate the switching spikes on the Vout. The VCC bypass capacitor should be terminated to PGND.
- Place a boot strap capacitor near the TDA38540 BOOT and PHASE pin as close as possible to minimize the loop inductance.
- SW node copper should only be routed on the top layer to minimize the impact of switching noises
- Connect AGND pin to the PGND pad through a single point connection. On the TDA38540 demo board, AGND pin is connected to the exposed PGND pad with a copper trace.
- Via holes can be placed on PVin and PGND pads to aid thermal dissipation.
- Wide copper polygons are desired for PVin and PGND connections in favor of power losses reduction and thermal dissipation. Sufficient via holes should be used to connect power traces between different layers.
- Single-ended Vout sensing is often used for local sensing. To implement this configuration, following design guidelines should be followed, as illustrated in **Figure 20**.
    - The output voltage can be sensed from a high-frequency bypass capacitor of 0.1 µF or higher, through a 15 mil PCB trace.
    - Keep the Vout sense line away from any noise sources and shield the sense line with ground planes.
    - The sense trace is connected to a feedback resistor divider with the lower resistor terminated at VSENM pin.
    - Short VSENM pin and AGND pin with a short trace.
- If it is required to sense the output voltage at a remote location, pseudo remoting sensing can be implemented as follows. The configuration is also shown in **Figure 3**.
    - A pair of PCB traces with at least 15 mil trace width, running close to each other and away from any noise sources such as inductor and SW nodes, should be used to implement Kelvin sensing of the voltage across a high bypass capacitor of 0.1 µF or higher.
    - The ground connection of the remote sensing signal must be terminated at VSENM pin.
    - The Vout connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor terminated at VSENM pin.
    - Shield the pair of remote sensing lines with ground planes above and below.
    - Do **NOT** connect VSENM pin and AGND pin in this configuration
- In stackable operation, Keep the signals of VSHARE, ISHARE and CLK away from any noise sources such as SW node and PVin.
- The EN pin and configuration pins including ILIM/SS, RT, and PHST should be terminated to a quiet ground. On the TDA38540 evaluation board, they are terminated to the PGND copper plane away from the power current flow. Alternatively, they can be terminated to a dedicated AGND PCB trace.

15.1 Solder Mask

Evaluation has shown that the best overall performance is achieved using the substrate/PCB layout as shown in the following figures. PQFN devices should be placed to an accuracy of 0.050 mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

Infineon recommends that larger Power or Land Area pads are Solder Mask Defined (SMD). This allows the underlying copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05 mm larger (on each edge) than the openings in the solder mask. This allows for layers to be misaligned by up to 0.1 mm on both axes. Ensure that the solder resist between the smaller signal lead areas is at least 0.15 mm wide, due to the high x/y aspect ratio of the solder mask strip.

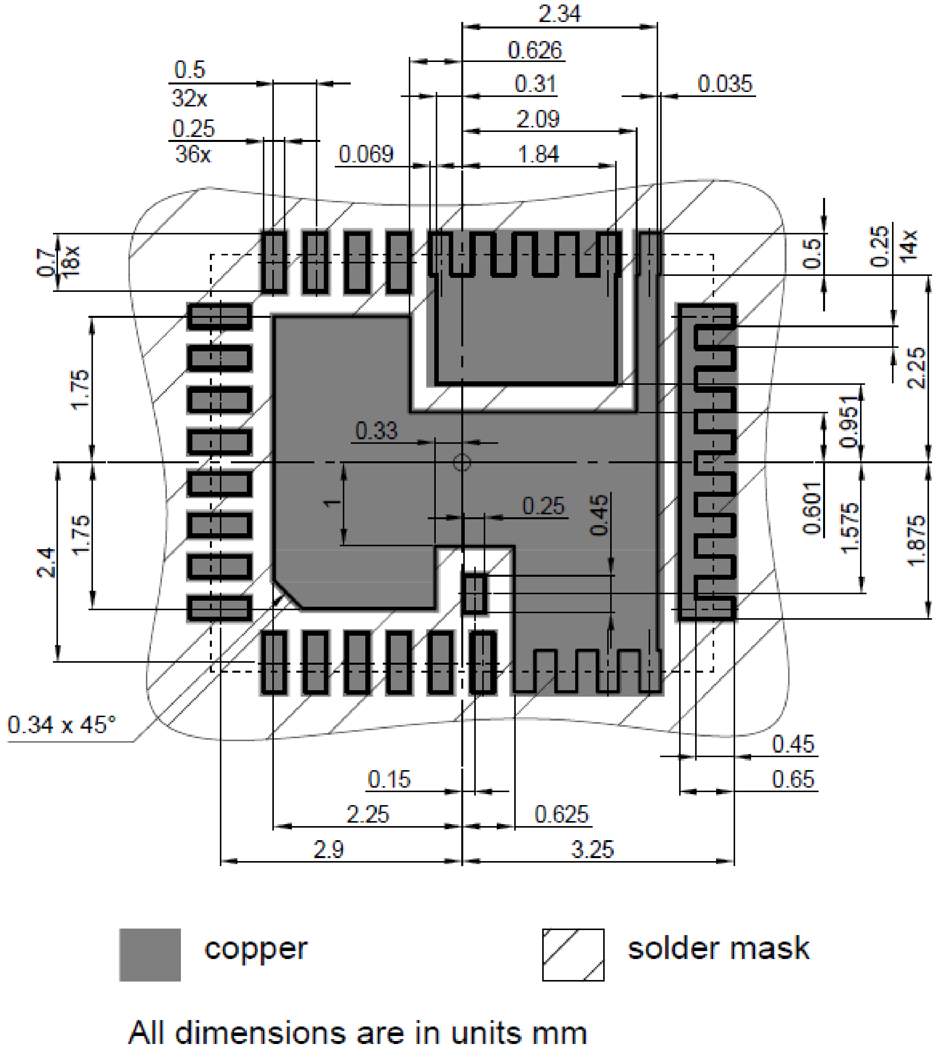


Figure 28 **Solder mask (all dimensions in mm)**

15.2 Stencil Design

In most cases, the thickness of a stencil has to be matched to the needs of all components on the PCB. For typical integrated QFN or SON packages, stencils with a thickness of 100 µm to 120 µm are recommended. Further details and specific stencil design recommendations can be found in the application note "Recommendations for Board Assembly of Infineon Integrated Packages without Leads". A recommended stencil design is shown below. This design is for a stencil thickness of 100 µm.

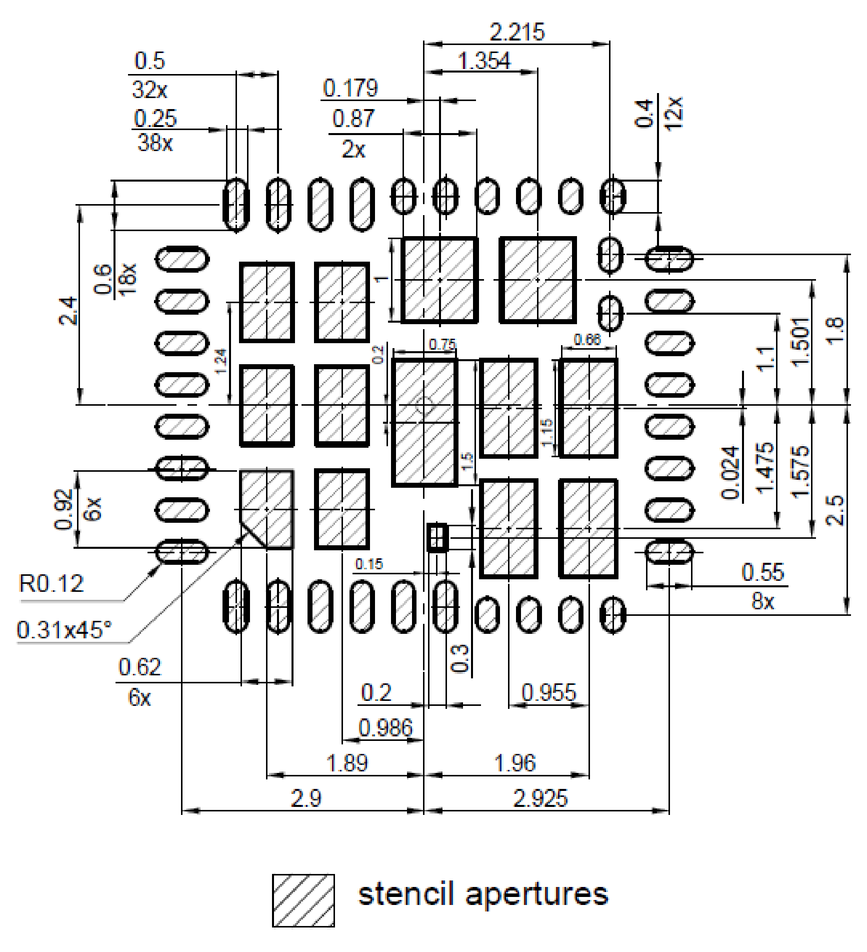


Figure 29 Stencil pad size and spacing (all dimensions in mm)

16 Package

This section includes marking, mechanical and packaging information for the TDA38540.

16.1 Marking Information

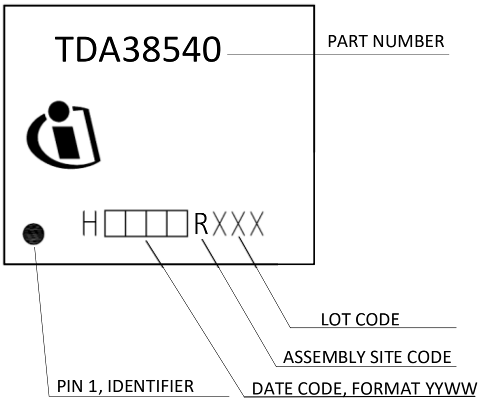
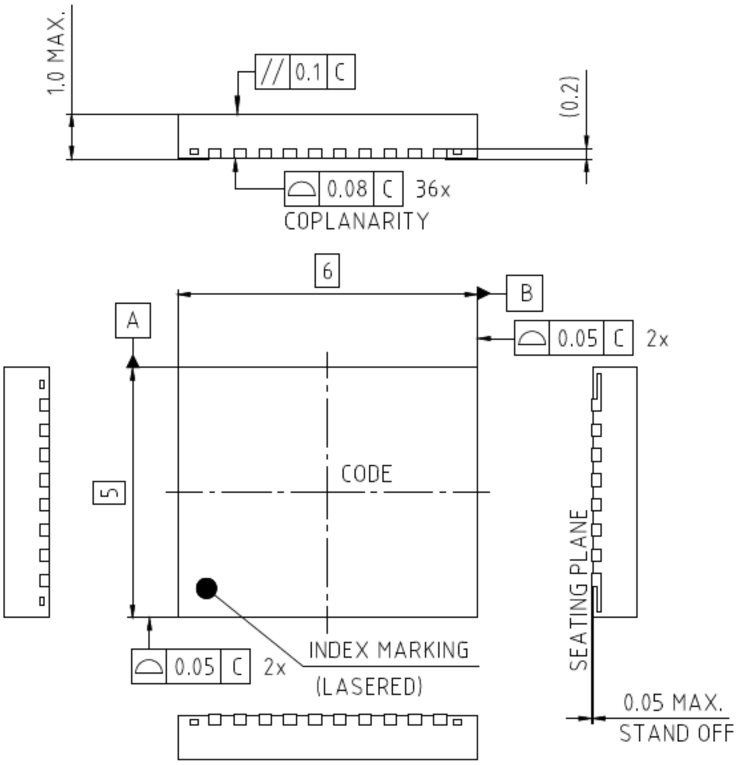
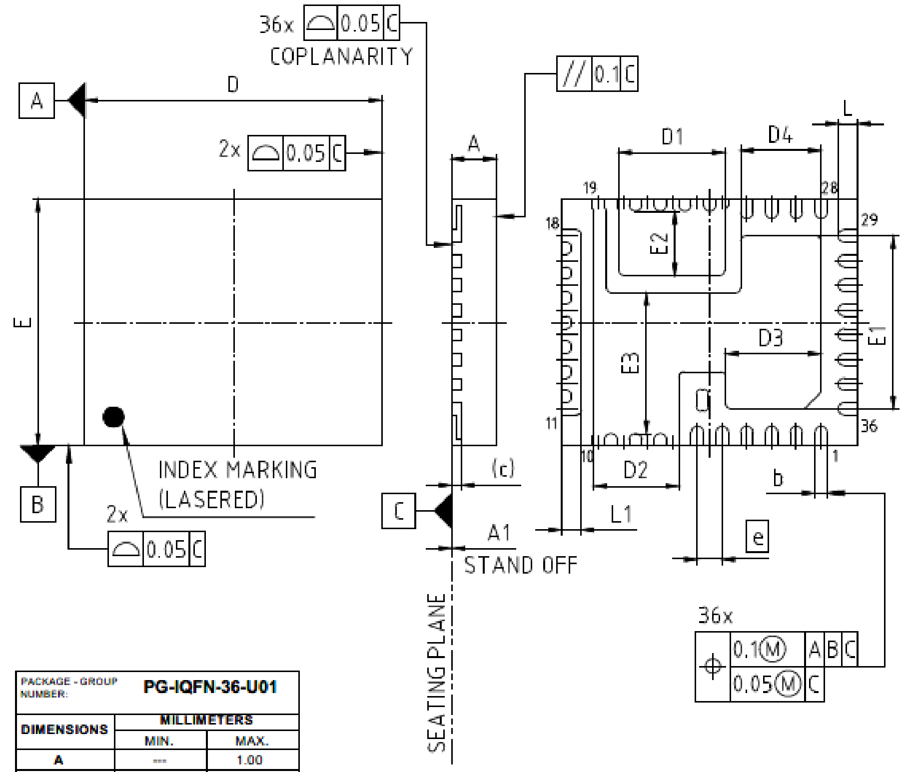


Figure 30 **Package Marking**

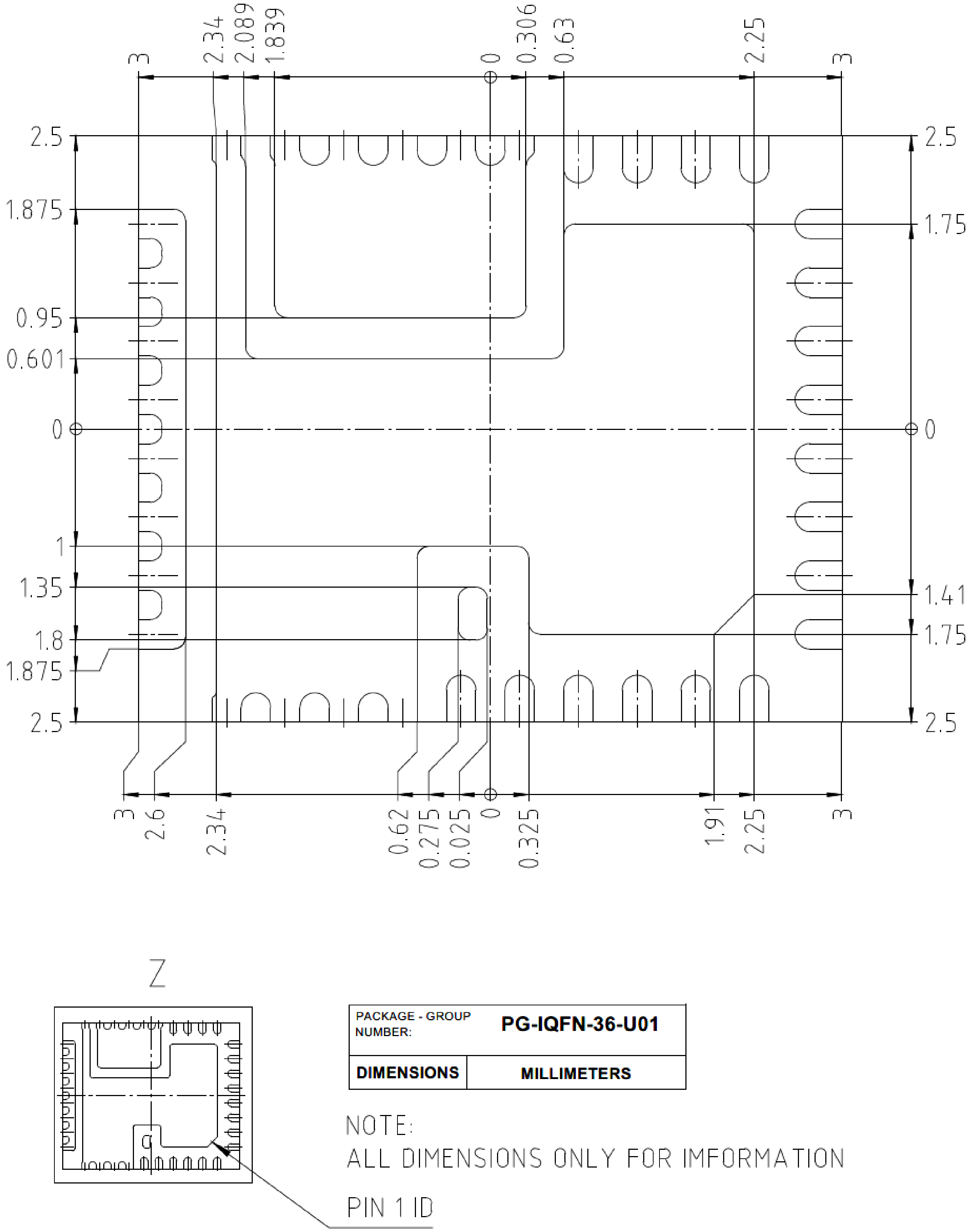
16.2 Dimensions





PACKAGE - GROUP NUMBER:	PG-IQFN-36-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	---	1.00
A1	0.00	0.05
b	0.20	0.30
c	(0.20)	
e	0.50	
D	5.90	6.10
D1	2.045	2.245
D2	1.615	1.815
D3	1.825	2.025
D4	1.524	1.725
E	4.90	5.10
E1	3.40	3.60
E2	1.199	1.399
E3	2.75	2.95
L	0.35	0.45
L1	0.30	0.50

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH,
PROTRUSION OR GATE BURRS



PACKAGE - GROUP NUMBER:	PG-IQFN-36-U01
DIMENSIONS	MILLIMETERS

NOTE:
ALL DIMENSIONS ONLY FOR IMFORMATION

Figure 31 Package dimensions

16.3 Tape and Reel Information

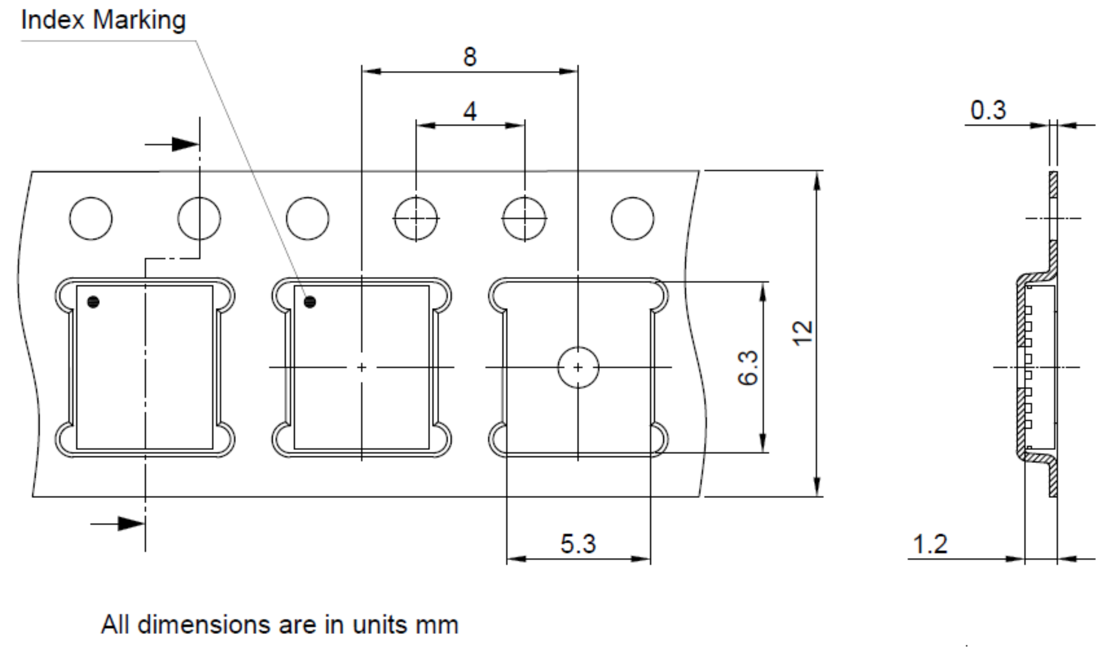


Figure 32 **Tape and reel drawing**

17 Environmental Qualifications

Qualification Level		**Industrial**	
Moisture Sensitivity		QFN Package	JEDEC Level 2 @ 260 °C
ESD	Human Body Model	ANSI/ESDA/JEDEC JS-001, Level 2 (2000 V to < 4000 V)	
	Charged Device Model	ANSI/ESDA/JEDEC JS-002, Level C3 (≥1000 V)	
RoHS2 Compliant		This product complies with EU Directive 2015/863/EU amending Annex II to EU Directive 2011/65/EU (RoHS) and contains Pb according RoHS exemption 7a, Lead in high melting temperature type solders.	

18 Evaluation Boards and Support Documentation

Table 5 TDA38540 Evaluation Boards and User Guides

Evaluation board	Specifications	Website Address
EVAL_38540_1Vout_1P	1-Phase, 12 V±10%, 1 V, 40 A	www.infineon.com/ EVAL_38540_1Vout_1P
EVAL_38540_1Vout_2P	2-Phase, 12 V±10%, 1 V, 80 A	www.infineon.com/ EVAL_38540_1Vout_2P

Table 6 TDA38540 Package Information

Device	Package Type	Website Address
TDA38540	PG-IQFN-36-3	https://www.infineon.com/cms/en/product/packages/PG-IQFN

Revision History

TDA38540

Revision 2024-09-19, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2024-09-19	Release of final

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