OptiMOS^{TM} Small-Signal MOSFET, -100V

Features

- ° P-channel
- ° Logic level
- ° AEC-Q101 Qualified
- ° 100% avalanche tested
- ° Pb-free lead plating; RoHS compliant
- ° Halogen-free according to IEC61249-2-21

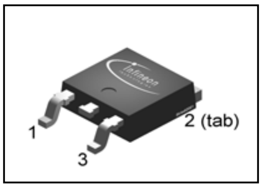
Product validation

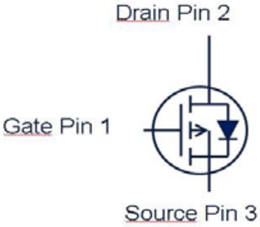
- ° Qualified for automotive applications. Product validation according to AEC-Q101

Product Summary

V_{DS}	-100	V
$R_{DS(on),max}$	0.20	Ω
I_D	-15	A

PG-TO252-3





Type	Package	Marking	Lead free	Packing
SPD15P10PL G	PG-TO252-3	15P10PL	Yes	Non dry

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	-15	A
		T_C=100 °C	11.3	
Pulsed drain current	$I_{D,pulse}$	T_C=25 °C	-60	
Avalanche energy, single pulse	E_{AS}	I_D=-15 A, R_{GS}=25 Ω	230	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	128	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
ESD Class			1C (1kV to 2kV)	
Soldering temperature			260 °C	
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - soldering point	R_{thJC}		-	-	1.17	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint, steady state	-	-	75	
		6 cm^2 cooling area[1], steady state	-	-	45	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{\text{(BR)DSS}}$	V_{GS}=0 V, I_D= -1 mA	-100	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	V_{DS}=V_{GS}, I_D=-1.54 mA	-1	-1.5	-2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=-100 V, V_{GS}=0 V, T_j=25 °C	-	-0.1	-1	µA
		V_{DS}=-100 V, V_{GS}=0 V, T_j=150 °C	-	-10	-100	
Gate-source leakage current	I_{GSS}	V_{GS}=-20 V, V_{DS}=0 V	-	-10	-100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	V_{GS}=-4.5 V, I_D=-9.7 A	-	190	270	mΩ
		V_{GS}=-10 V, I_D=-11.3 A	-	140	200	mΩ
Transconductance	g_{fs}	$\lvert V_{\text{DS}}\rvert>2\lvert I_D\rvert R_{\text{DS(on)max}}$, I_D=-11.3 A	5.5	11.0	-	S

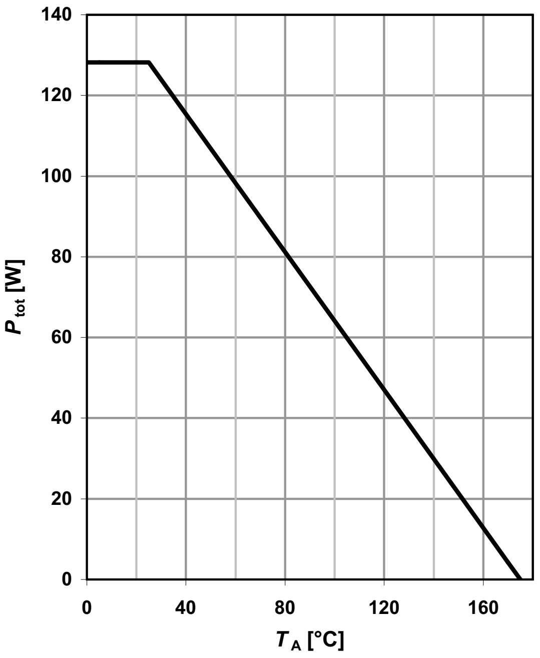
[1] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=-25 V, f=1 MHz	-	1120	1490	pF
Output capacitance	C_{oss}		-	272	362	
Reverse transfer capacitance	C_{rss}		-	120	180	
Turn-on delay time	$t_{d(on)}$	V_{DD}=-50 V, V_{GS}=-10 V, I_D=-15 A, R_G=6 Ω	-	7.6	11	ns
Rise time	t_r		-	21	31	
Turn-off delay time	$t_{d(off)}$		-	50	75	
Fall time	t_f		-	29	44	
Gate Charge Characteristics[2]						
Gate to source charge	Q_{gs}	V_{DD}=-80 V, I_D=-15 A, V_{GS}=0 to -10 V	-	4.3	5.7	nC
Gate to drain charge	Q_{gd}		-	17	26	
Gate charge total	Q_g		-	47	62	
Gate plateau voltage	$V_{plateau}$		-	4.0	-	V
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	-15	A
Diode pulse current	$I_{S,pulse}$		-	-	-60	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=-15 A, T_j=25 °C	-	-0.96	-1.35	V
Reverse recovery time	t_{rr}	V_R=50 V, I_F=|I_S|, di_F/dt=100 A/µs	-	110	165	ns
Reverse recovery charge	Q_{rr}		-	450	675	nC

[2] See figure 16 for gate charge parameter definition

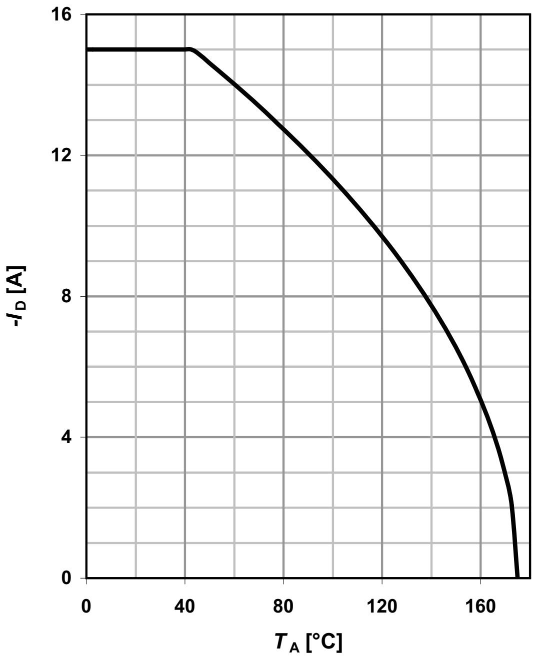
1 Power dissipation

P_{tot}=f(T_C)



2 Drain current

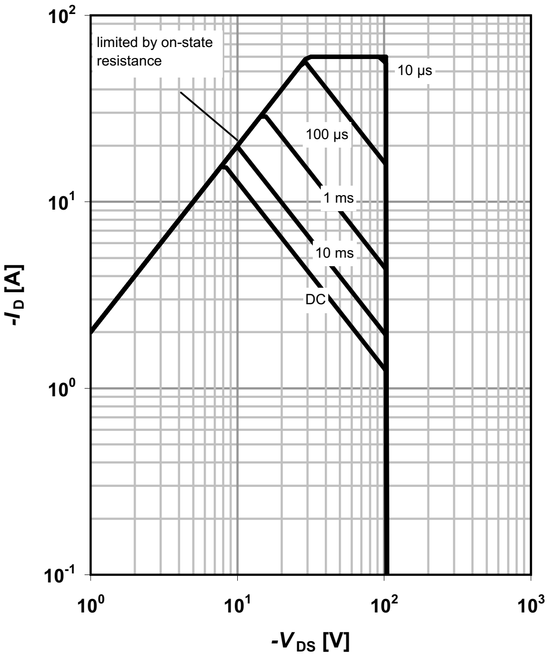
I_D=f(T_C); $|V_{GS}|$≥10 V



3 Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0

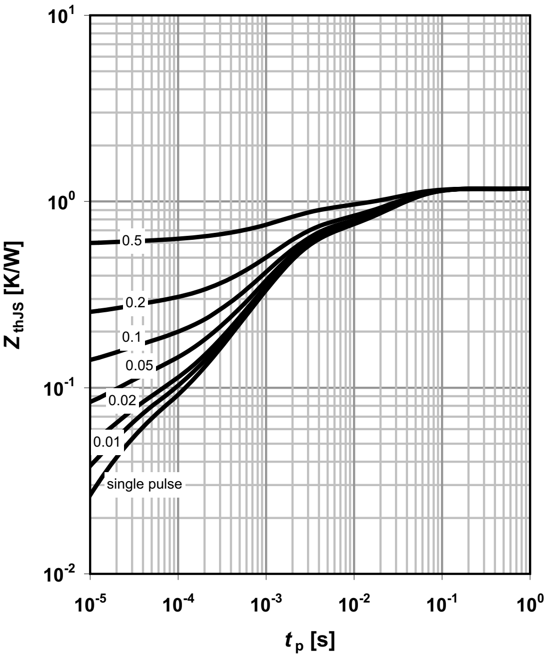
parameter: t_p



4 Max. transient thermal impedance

Z_{thJC}=f(t_p)

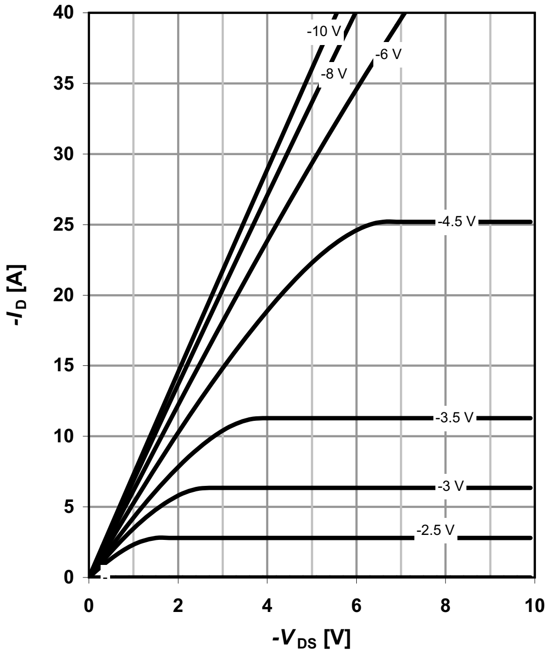
parameter: $D=t_p/T$



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

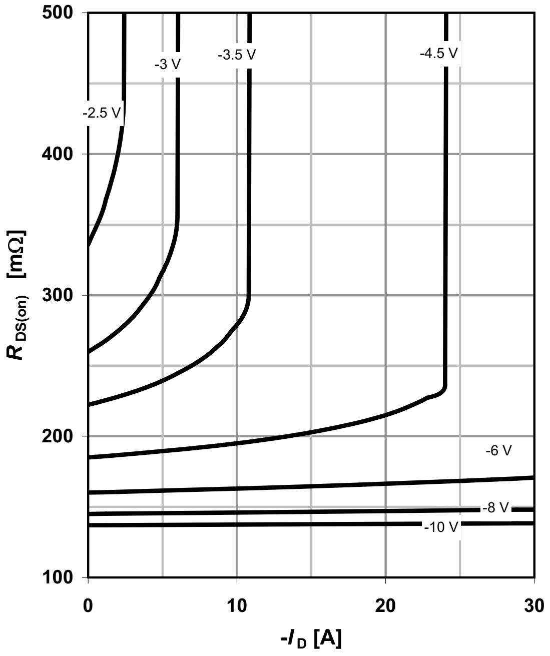
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

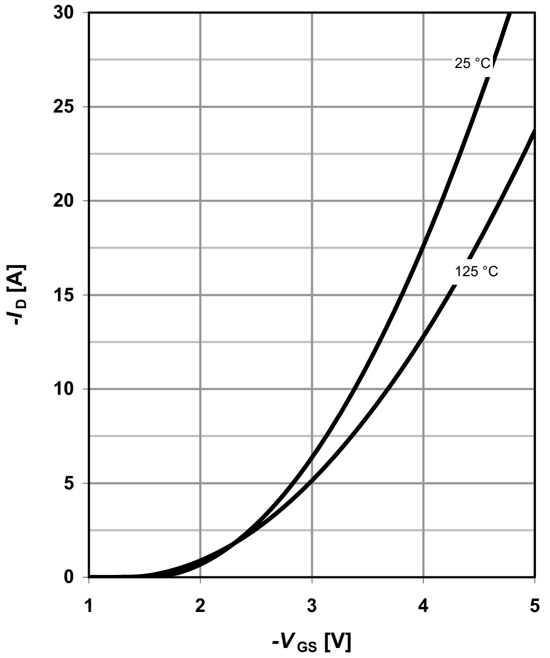
parameter: V_{GS}



7 Typ. transfer characteristics

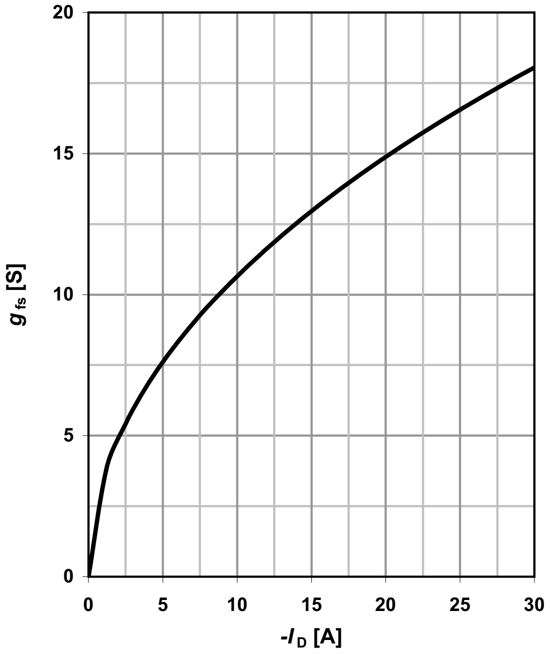
I_D=f(V_{GS}); $|V_{DS}|$>2$|I_D|R_{DS(on)max}$

parameter: T_j



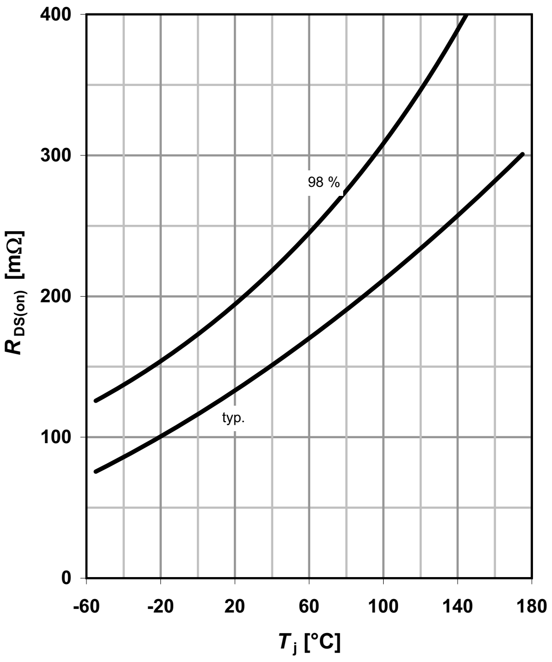
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



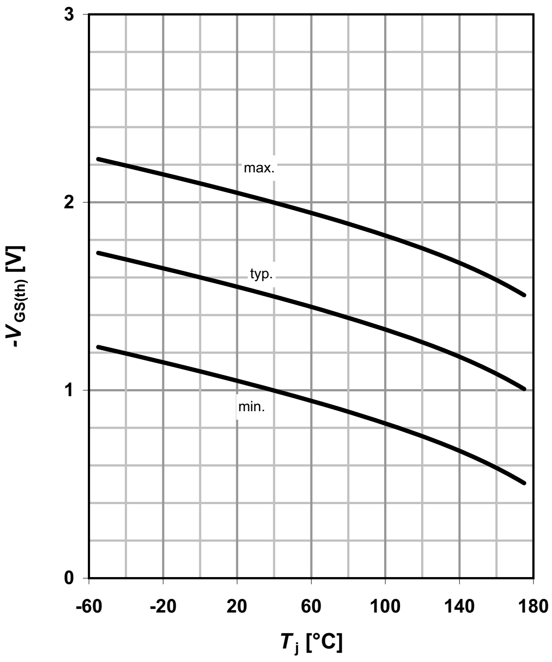
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=-11.3 A; V_{GS}=-10 V



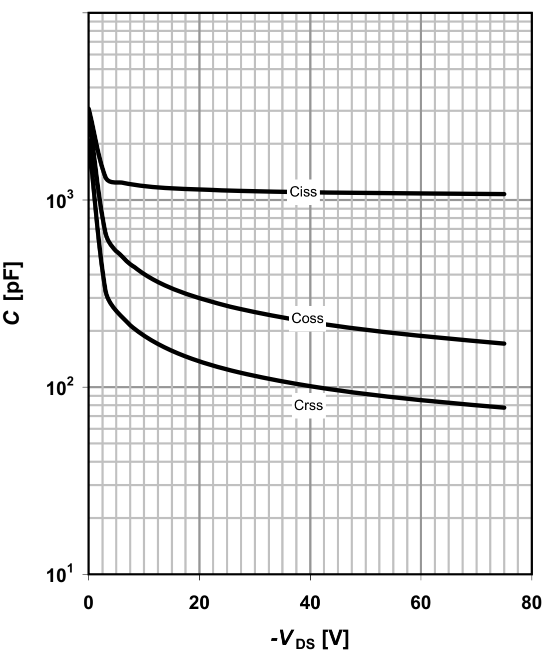
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=-1.54 mA



11 Typ. capacitances

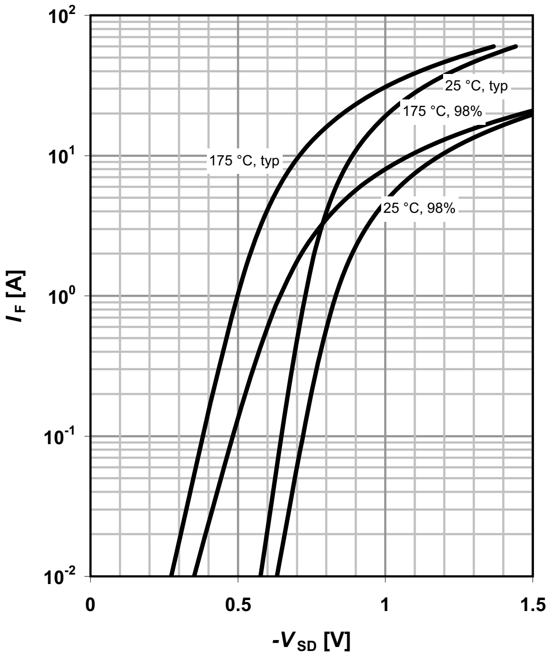
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

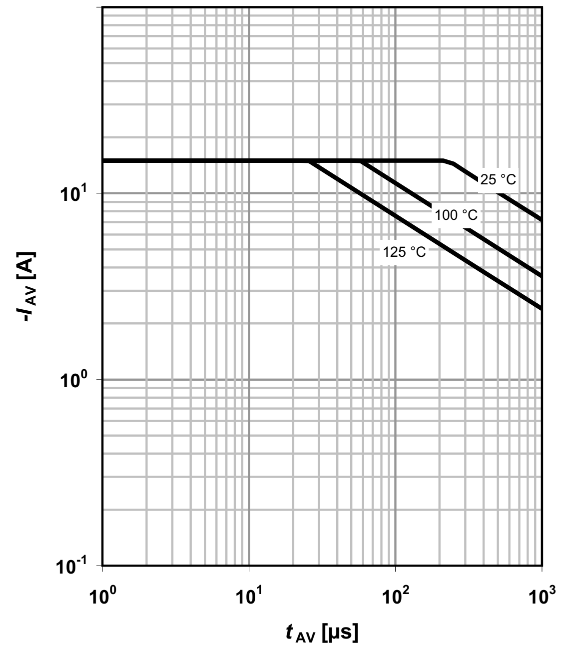
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$

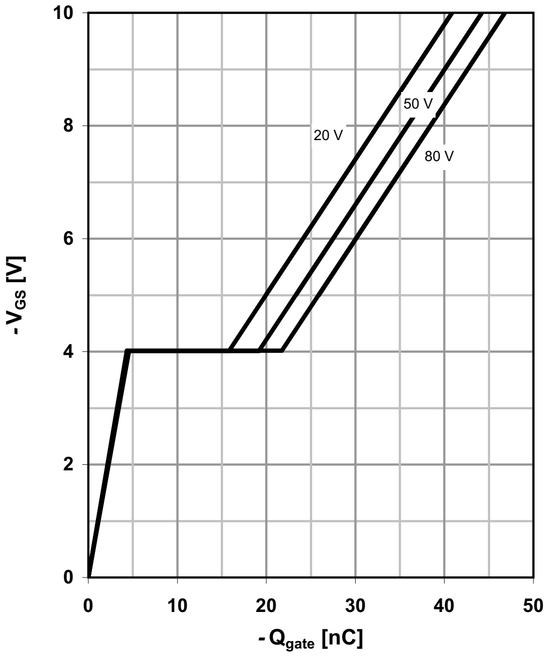
parameter: $T_{j(start)}$



14 Typ. gate charge

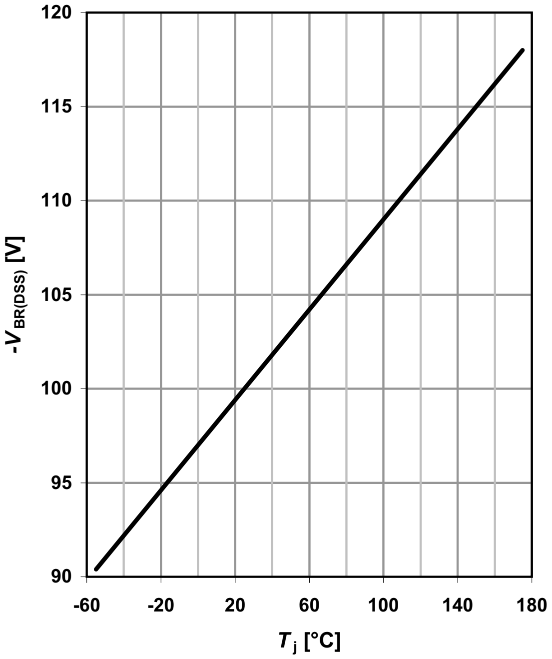
$V_{GS}=f(Q_{gate})$; I_D=-15 A pulsed

parameter: V_{DD}

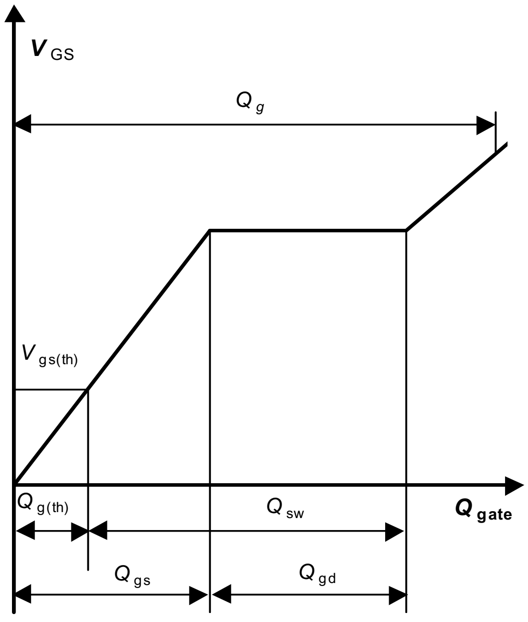


15 Drain-source breakdown voltage

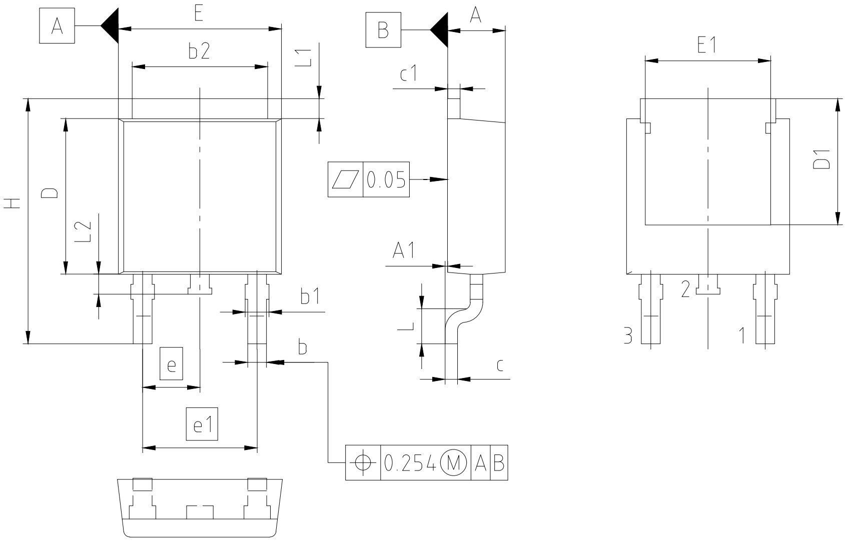
$V_{BR(DSS)}=f(T_j)$; I_D=-1mA



16 Gate charge waveforms



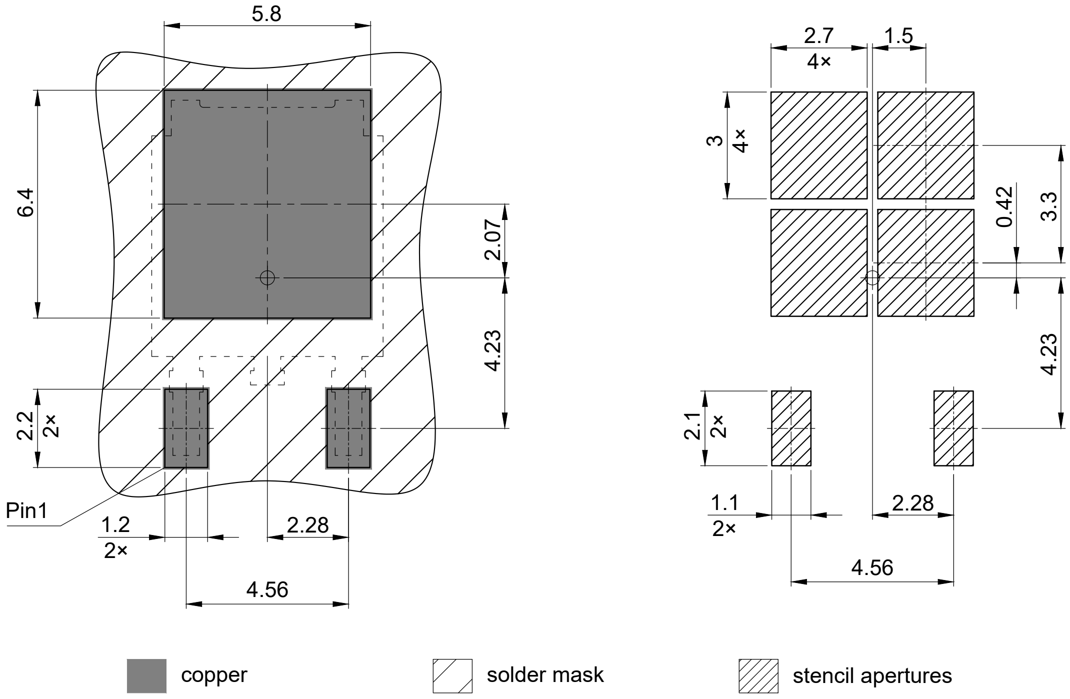
5 Package outlines



PACKAGE - GROUP NUMBER:	PG-TO252-3-U02	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.16	2.41
A1	0.00	0.15
b	0.64	0.89
b1	0.65	1.15
b2	4.95	5.50
c	0.46	0.61
c1	0.40	0.98
D	5.97	6.22
D1	5.02	5.84
E	6.35	6.73
E1	4.32	5.50
e	2.29	
e1	4.57	
N	3	
H	9.40	10.48
L	1.18	1.78
L1	0.89	1.27
L2	0.51	1.02

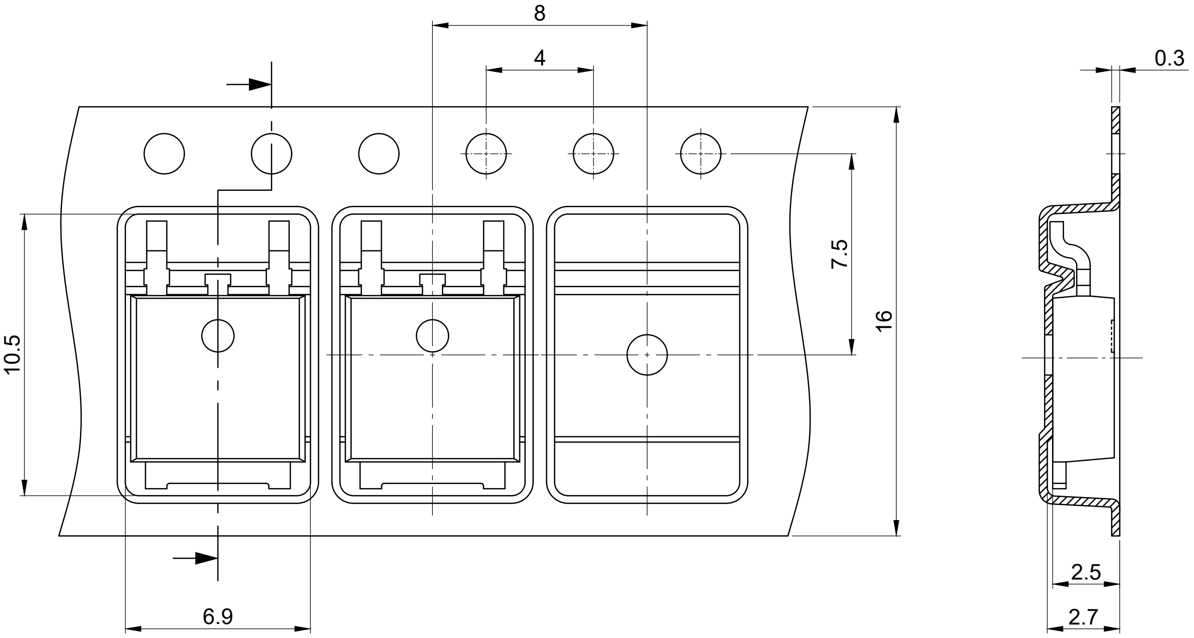
ALL DIMENSIONS REFER TO JEDEC
STANDARD TO-252 AND DO NOT INCLUDE MOLD
FLASH OR PROTRUSIONS.

Figure 1 Outline PG-TO252-3, dimensions in mm



All dimensions are in units mm
All pads are solder mask defined

Figure 2 Footprint drawing PG-TO252-3, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊲⊕]

Figure 3 Packaging variant PG-TO252-3, dimensions in mm

Revision history

SPD15P10PL G

Revision 2026-03-09, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-03-09	Update to halogen free, features, Id for VBR(DSS) and package drawings

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