OptiMOS^{TM} Small-Signal MOSFET, -60V

Features

- ° P-channel
- ° Normal level
- ° AEC-Q101 Qualified
- ° 100% avalanche tested
- ° Pb-free lead plating; RoHS compliant
- ° Halogen-free according to IEC61249-2-21

Product validation

° Qualified for automotive applications. Product validation according to AEC-Q101

RoHS

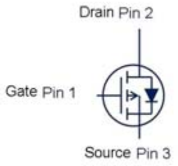
AEC Qualified

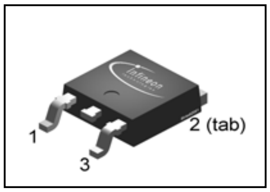
HAL Halogen-Free

Product Summary

V_{DS}	-60	V
$R_{DS(on),max}$	0.3	Ω
I_D	-8.8	A

PG-TO252-3





Type	Package	Tape and reel information	Marking	Lead free	Packing
SPD08P06PG	PG-TO252-3	1000 pcs / reel	08P06P	Yes	Non dry

Parameter	Symbol	Conditions	Value	Unit
			steady state	
Continuous drain current	I_D	T_A=25 °C	-8.83	A
		T_A=100 °C	-6.25	
Pulsed drain current	$I_{D,pulse}$	T_A=25 °C	-35.32	
Avalanche energy, single pulse	E_{AS}	I_D=8.83 A, R_{GS}=25 Ω	70	mJ
Avalanche energy, periodic limited by T_{jmax}	E_{AR}		4.2	
Reverse diode dv/dt	dv/dt	I_D=8.83 A, V_{DS}=48 V, di/dt=-200 A/µs, $T_{j,max}$=175 °C	-6	kV/µs
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_A=25 °C	42	W
Operating and storage temperature	T_j, T_{stg}		"-55 ... +175"	°C
ESD class				
Soldering temperature			260 °C	
IEC climatic category; DIN IEC 68-1			55/175/56	

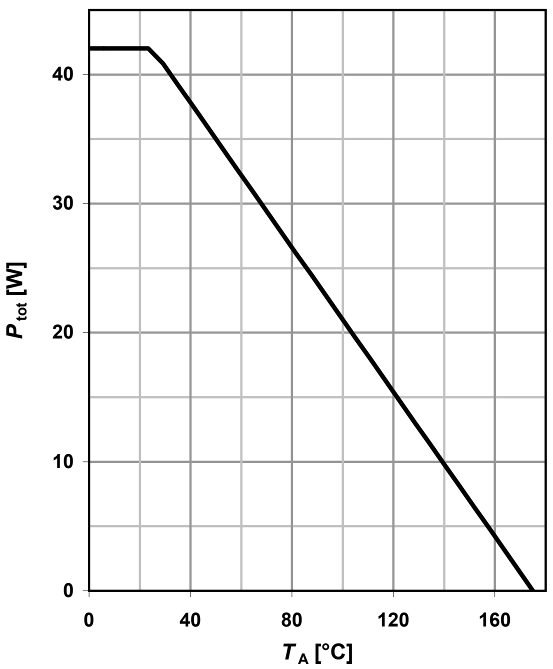
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	3.6	K/W
Thermal resistance, junction - ambient,leaded	R_{thJA}		-	-	-	
SMD version, device on PCB:	R_{thJA}	minimal footprint	-	-	75	K/W
		6 cm^2 cooling area[1]	-	-	50	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=-250 µA	-60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250 µA	-2.1	-3.0	-4	
Zero gate voltage drain current	I_{DSS}	V_{DS}=-60 V, V_{GS}=0 V, T_j=25 °C	-	-0.1	-1	µA
		V_{DS}=-60 V, V_{GS}=0 V, T_j=150 °C	-	-10	-100	
Gate-source leakage current	I_{GSS}	V_{GS}=-20 V, V_{DS}=0 V	-	-10	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=-6.2 V, I_D=-10 A	-	230	300	mΩ
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=-6.2 A	2.5	4.9	-	S

[1] Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6 cm^2 (one layer, 70µ, thick) copper area for drain connection. PCB is vertical without blown air.

Parameter	**Symbol**	**Conditions**	**Values**			**Unit**
			min.	**typ.**	**max.**	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=-25 V, f=1 MHz	-	335	420	pF
Output capacitance	C_{oss}		-	105	135	
Reverse transfer capacitance	C_{rss}		-	65	95	
Turn-on delay time	$t_{d(on)}$	V_{DD}=-30 V, V_{GS}=-10 V, I_D=-6.2 A, R_G=6 Ω	-	16.0	24.0	
Rise time	t_r		-	46.0	69	
Turn-off delay time	$t_{d(off)}$		-	48	72	
Fall time	t_f		-	14	21	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=-48 V, I_D=-8.8 A, V_{GS}=0 to -10 V	-	-1.9	-2.6	nC
Gate to drain charge	Q_{gd}		-	-5	-8	
Gate charge total	Q_g		-	-10	-13	
Gate plateau voltage	$V_{plateau}$		-	-6	-	V
Reverse Diode						
Diode continuous forward current	I_S	T_A=25 °C	-	-	-8.80	A
Diode pulse current	$I_{S,pulse}$		-	-	-35.3	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=-8.83 A, T_j=25 °C	-	-0.98	-1.55	V
Reverse recovery time	t_{rr}	V_R=30 V, I_F=|I_S|, di_F/dt=100 A/µs	-	60	90	ns
Reverse recovery charge	Q_{rr}		-	100	150	nC

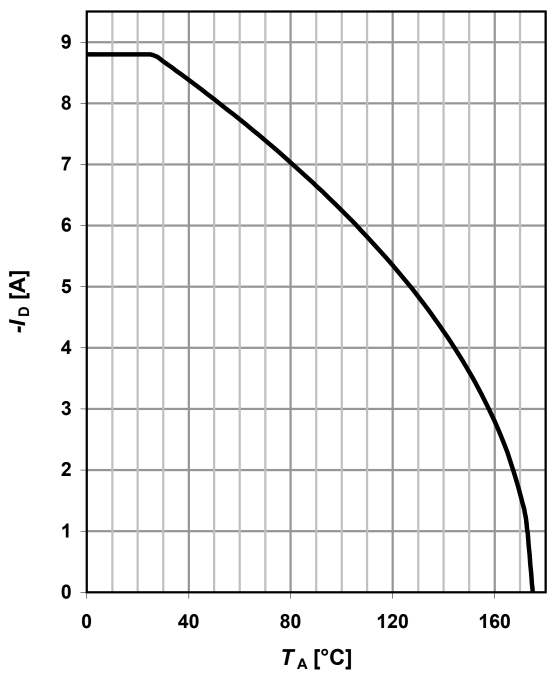
1 Power dissipation

P_{tot}=f(T_A)



2 Drain current

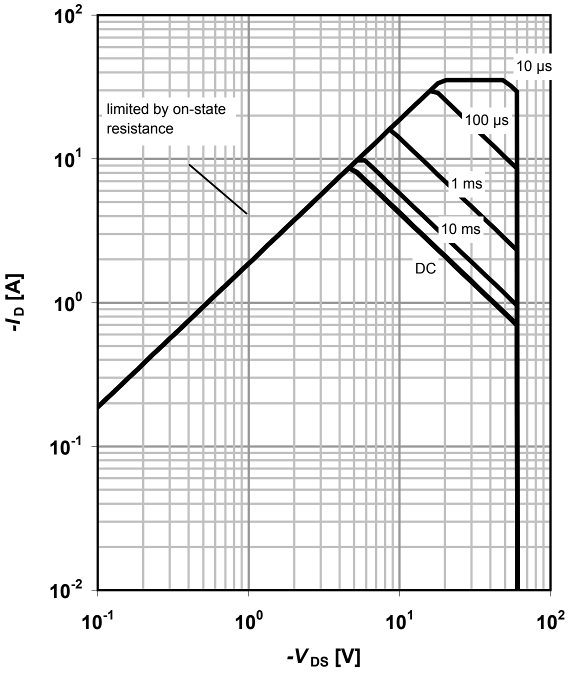
I_D=f(T_A); $|V_{GS}|$≥10 V



3 Safe operating area

I_D=f(V_{DS}); T_A=25 °C; D =0

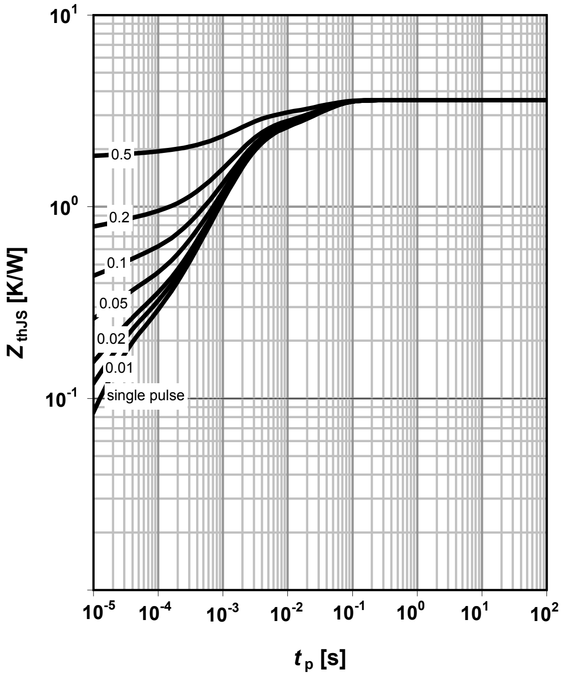
parameter: t_p



4 Max. transient thermal impedance

Z_{thJA}=f(t_p)

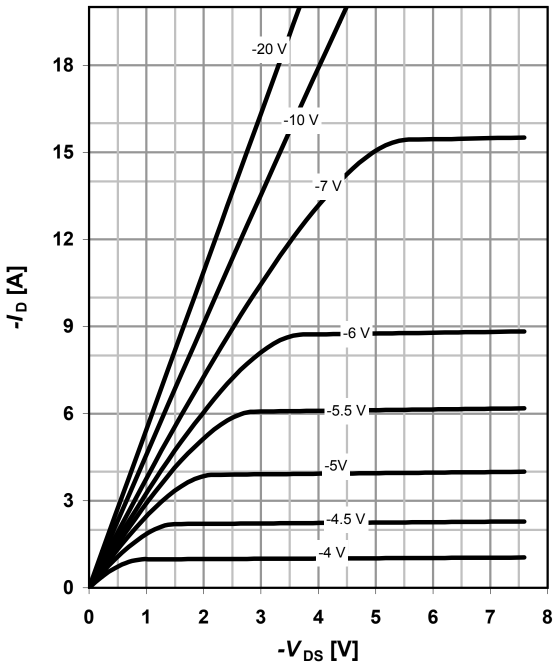
parameter: D =t_p/T



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C

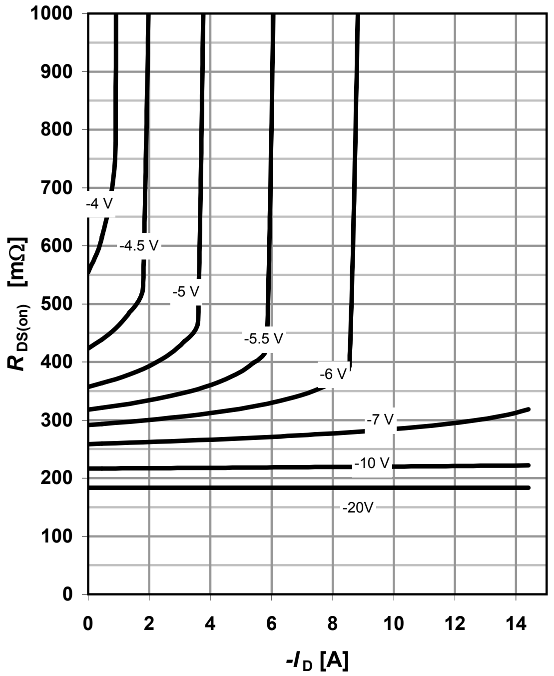
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C

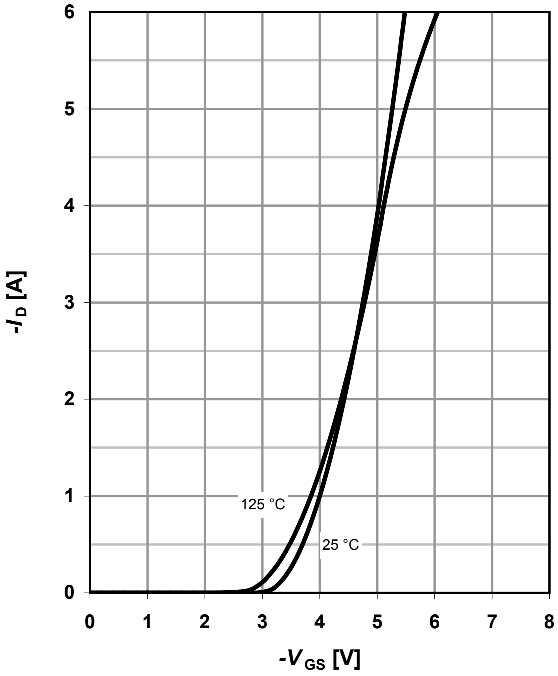
parameter: V_{GS}



7 Typ. transfer characteristics

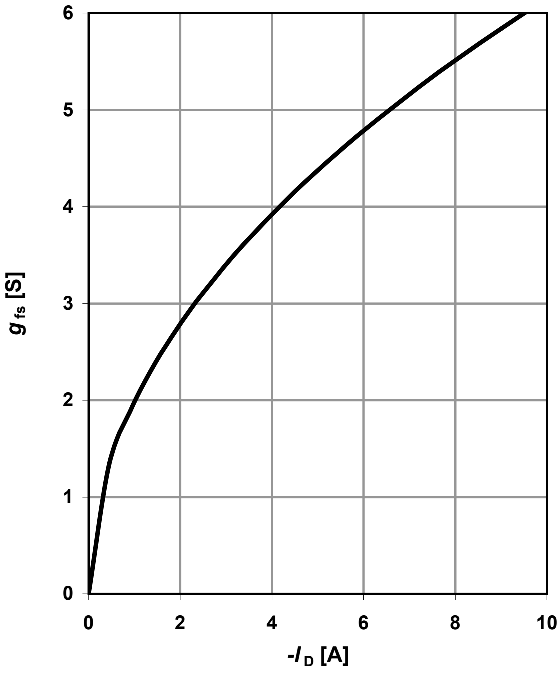
$I_D = f(V_{GS})$; $|V_{DS}| > 2|I_D| R_{DS(on)max}$

parameter: T_j



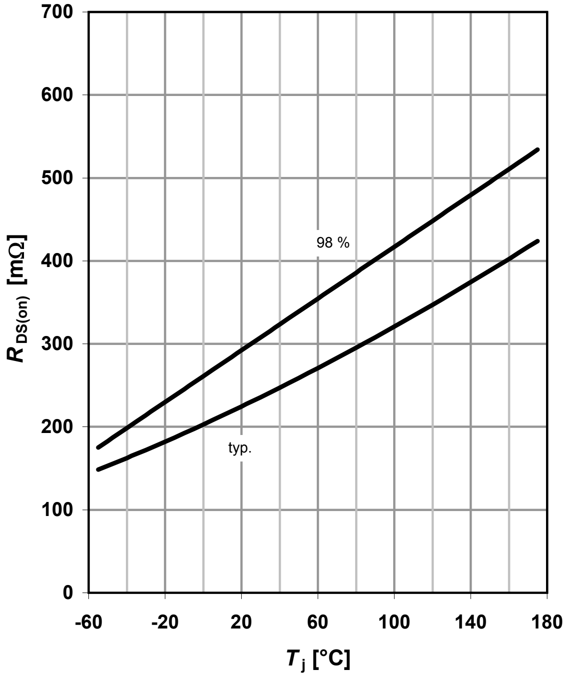
8 Typ. forward transconductance

$g_{fs} = f(I_D)$; $T_j = 25$ °C



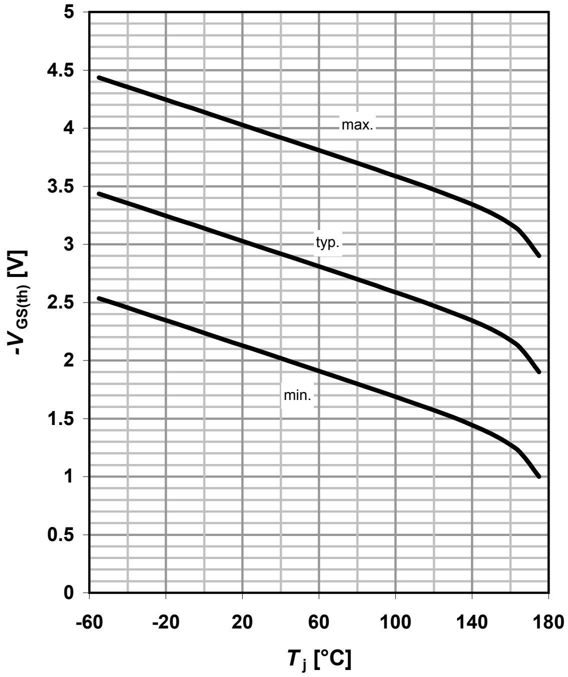
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=-6.2 A; V_{GS}=-10 V



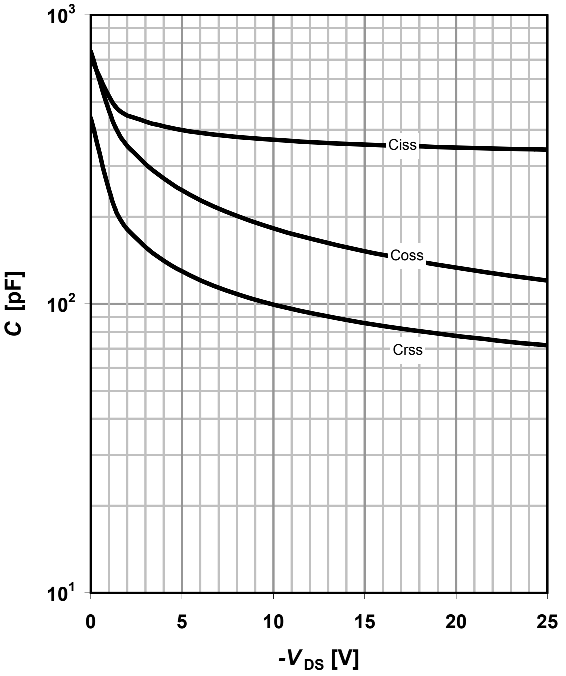
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=-250 µA



11 Typ. capacitances

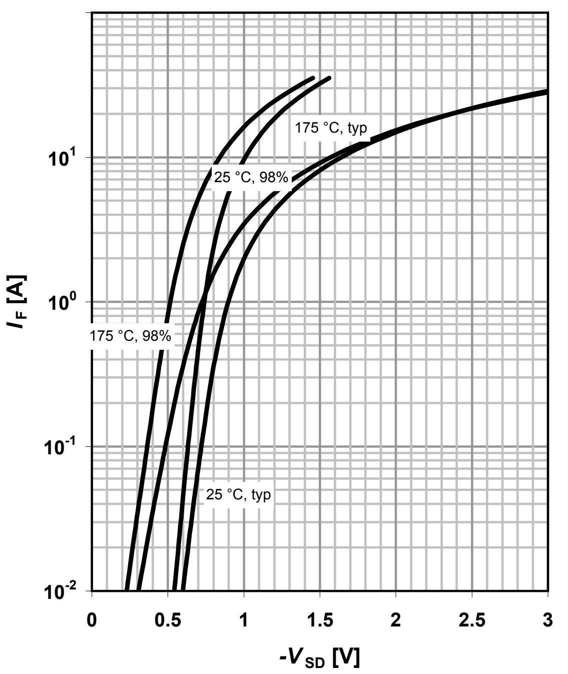
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

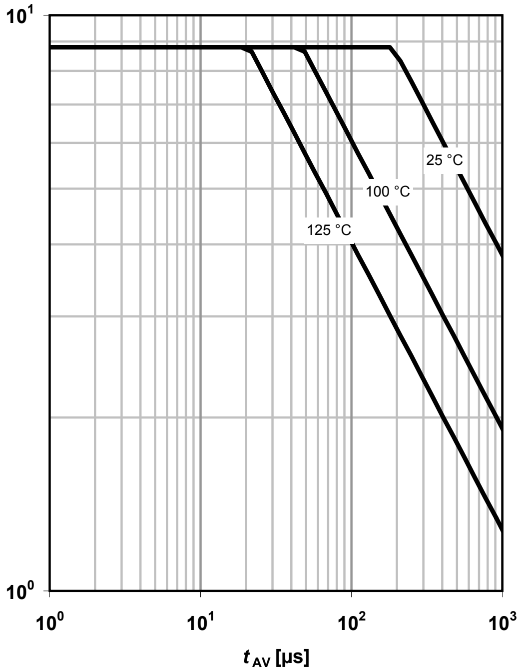
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

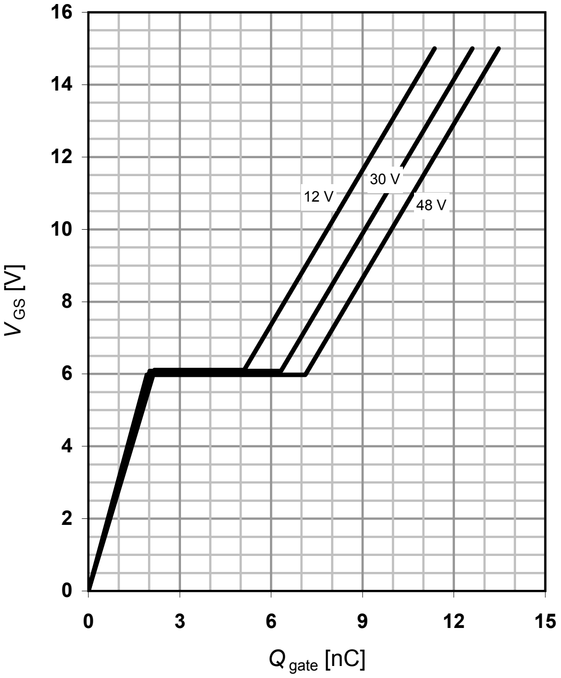
parameter: $T_{j(start)}$



14 Typ. gate charge

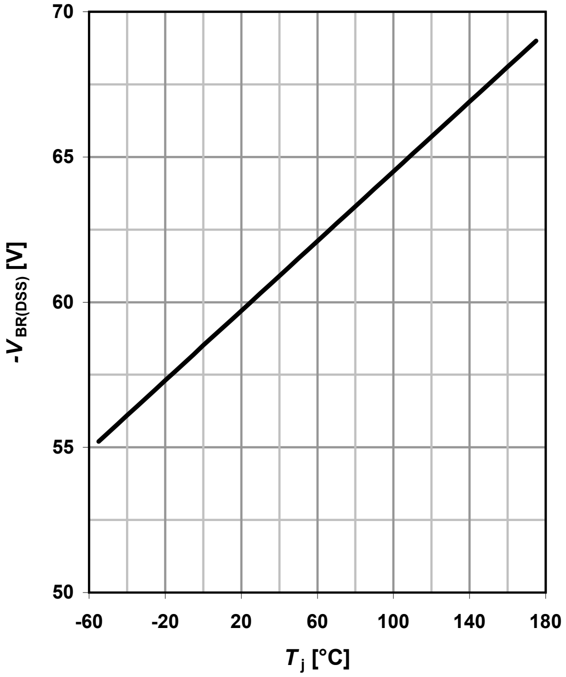
V_{GS}=f(Q_{gate}); I_D=-8.8 A pulsed

parameter: V_{DD}

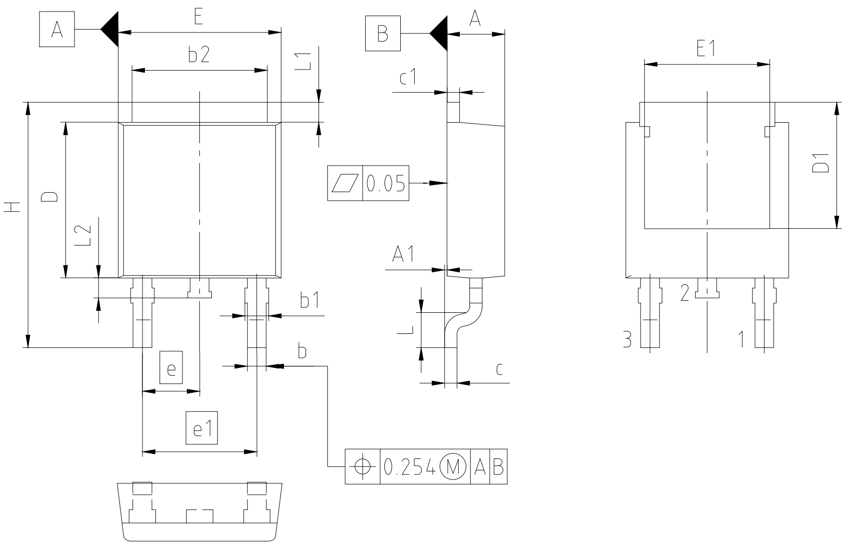


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=-250 µA



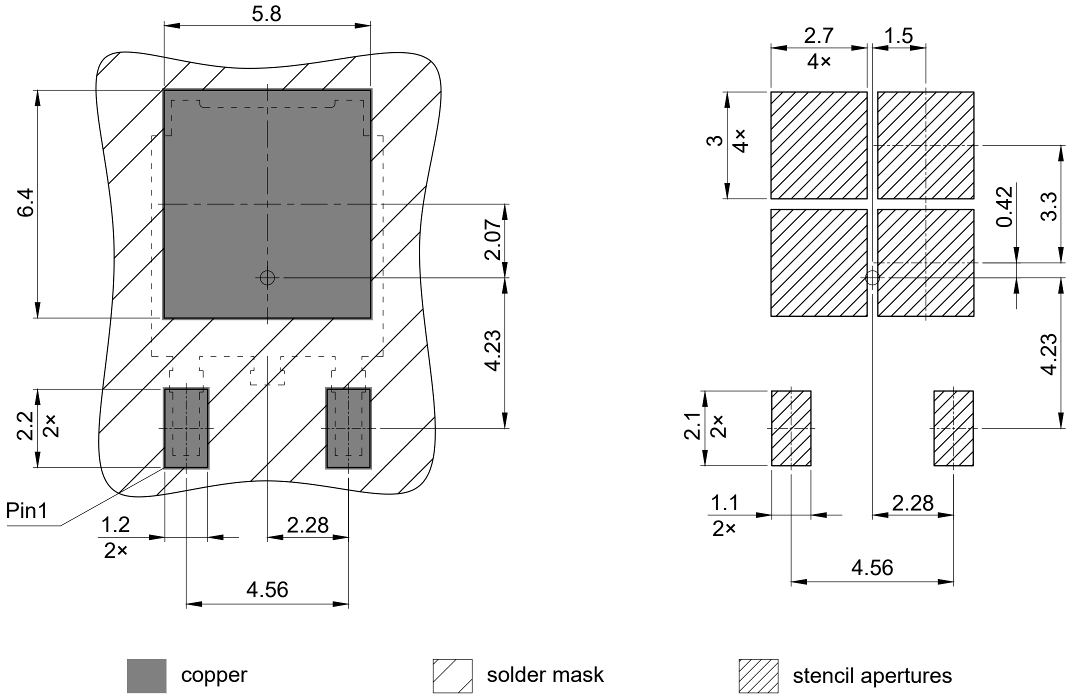
5 Package outlines



PACKAGE - GROUP NUMBER:	PG-TO252-3-U02	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.16	2.41
A1	0.00	0.15
b	0.64	0.89
b1	0.65	1.15
b2	4.95	5.50
c	0.46	0.61
c1	0.40	0.98
D	5.97	6.22
D1	5.02	5.84
E	6.35	6.73
E1	4.32	5.50
e	2.29	
e1	4.57	
N	3	
H	9.40	10.48
L	1.18	1.78
L1	0.89	1.27
L2	0.51	1.02

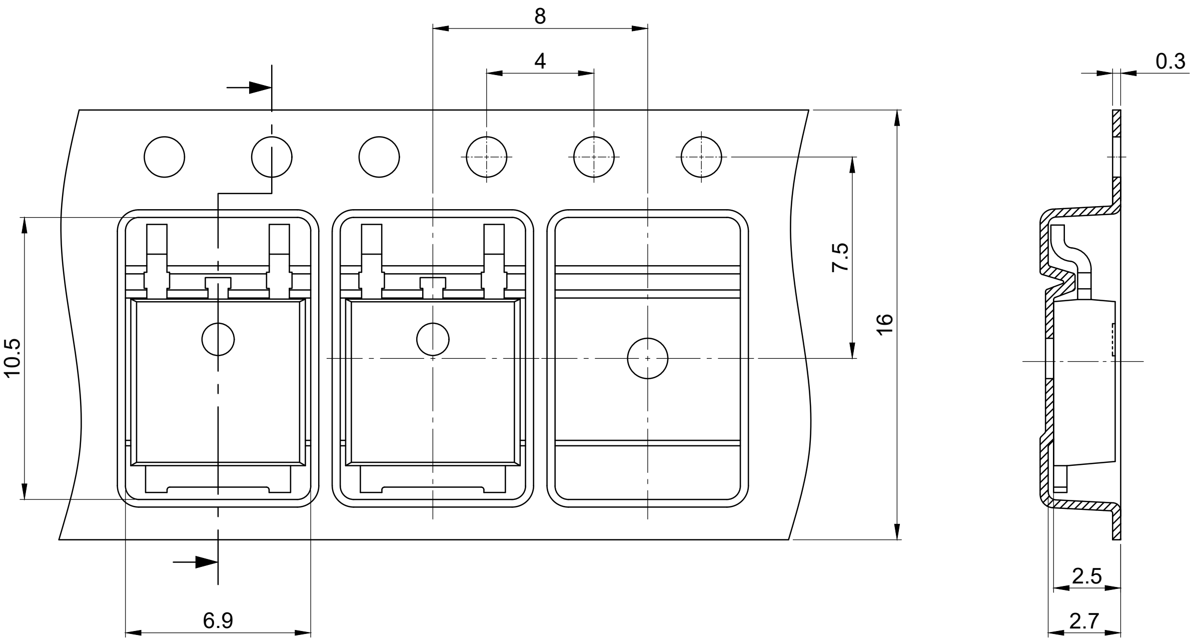
ALL DIMENSIONS REFER TO JEDEC
STANDARD TO-252 AND DO NOT INCLUDE MOLD
FLASH OR PROTRUSIONS.

Figure 1 Outline PG-TO252-3, dimensions in mm



All dimensions are in units mm
All pads are solder mask defined

Figure 2 Footprint drawing PG-TO252-3, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊲⊕]

Figure 3 Packaging variant PG-TO252-3, dimensions in mm

Revision history

SPD08P06P G

Revision 2026-03-05, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-03-05	Update to halogen-free, features and package drawings.

Trademarks

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