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RIC70849 - Rad hard buck controller with integrated gate drivers

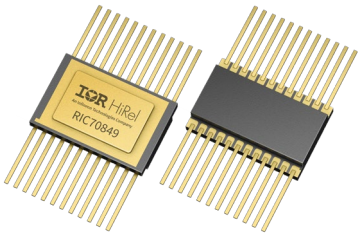
Features

- Wide input voltage range
- Accurate voltage reference over temperature and radiation
- Improved transient response with optional load line regulation
- Fixed frequency peak current mode control
- Wide programmable switching frequency enables optimization between solution size and performance
- Small minimum on time enables high step-down voltage ratio
- Integrated half bridge gate driver
- Integrated fault protections
- Integrated programmable soft start
- Radiation tolerance
  - High dose rate (50-300 rad(Si)/s) to 150 krad(Si) for 100 krad(Si) rating)
- Single event effect (SEE) hardness
  - No SEB or SEL up to LET of 81.9 MeV·cm^2/mg
  - SET characterized up to LET of 81.9 MeV·cm^2/mg
- Electrically screened and qualified to MIL-PRF-38535, Class V (DLA certification pending)

Product Summary

- V_{IN} (abs max) = 17.1 V
- V_{OUT} = 0.6 V to 5.25 V
- V_{REF} + V_{OSEA} = 600 mV ±1%
- f_{sw} = 100 kHz to 2 MHz
- t_{minon} (abs max) = 27 ns

Package



24 pin flatpack

Potential applications

- PoL converter for space grade FPGA, ASIC and DSP core rails
- Digital processing payload systems
- Distributed satellite power systems

Ordering information

Table 1 Ordering information

Orderable part number	Package type	Device level	Total ionizing dose level
5962R2320602VXA	24-lead flatpack	Level V[1]	100 krad(Si)
RIC70849F	24-lead flatpack	Engineering model[2]	

[1] Per MIL-PRF-38535 (DLA certification pending)

[2] Intended for engineering evaluation only, devices are only electrically tested at 25°C and for hermeticity

Description

RIC70849 is a radiation hardened synchronous buck controller with integrated gate drivers. It is intended for harsh radiation environments such as space, with electrical parameters specified pre and post-irradiation up to 100 krad(Si) and single effect effects (SEE) characterized up to a linear energy transfer (LET) of 81.9 MeV·cm^2/mg. RIC70849 is available in a hermetically sealed 24-lead flatpack and operates over the full military ambient temperature range of -55°C to 125°C.

The integrated half-bridge gate driver has a 4.8 V drive voltage and is intended to work with GaN HEMTs, such as IR HiRel Rad Hard GaN. RIC70849 supports a wide input voltage range including nominal inputs of 5 V and 12 V, and the output voltage can support from 0.6 V up to 5 V. This makes RIC70849 ideal for point of load (PoL) applications such as core rails of space rated FPGA and ASIC.

RIC70849 uses a fixed switching frequency peak current mode control algorithm. Externally adjustable slope compensation ensures stable operation over a wide range of conditions. The switching frequency is programmable from 100 kHz to 2 MHz with a single resistor, or it can be synchronized to an external clock or another RIC70849 for multiphase operation. It includes multiple integrated fault protections for increased reliability. It also has optional load-line regulation (also referred to as adaptive voltage positioning (AVP) or droop regulation), where the output voltage is dynamically adjusted based on the load current. This provides a system benefit of significantly reducing output capacitance.

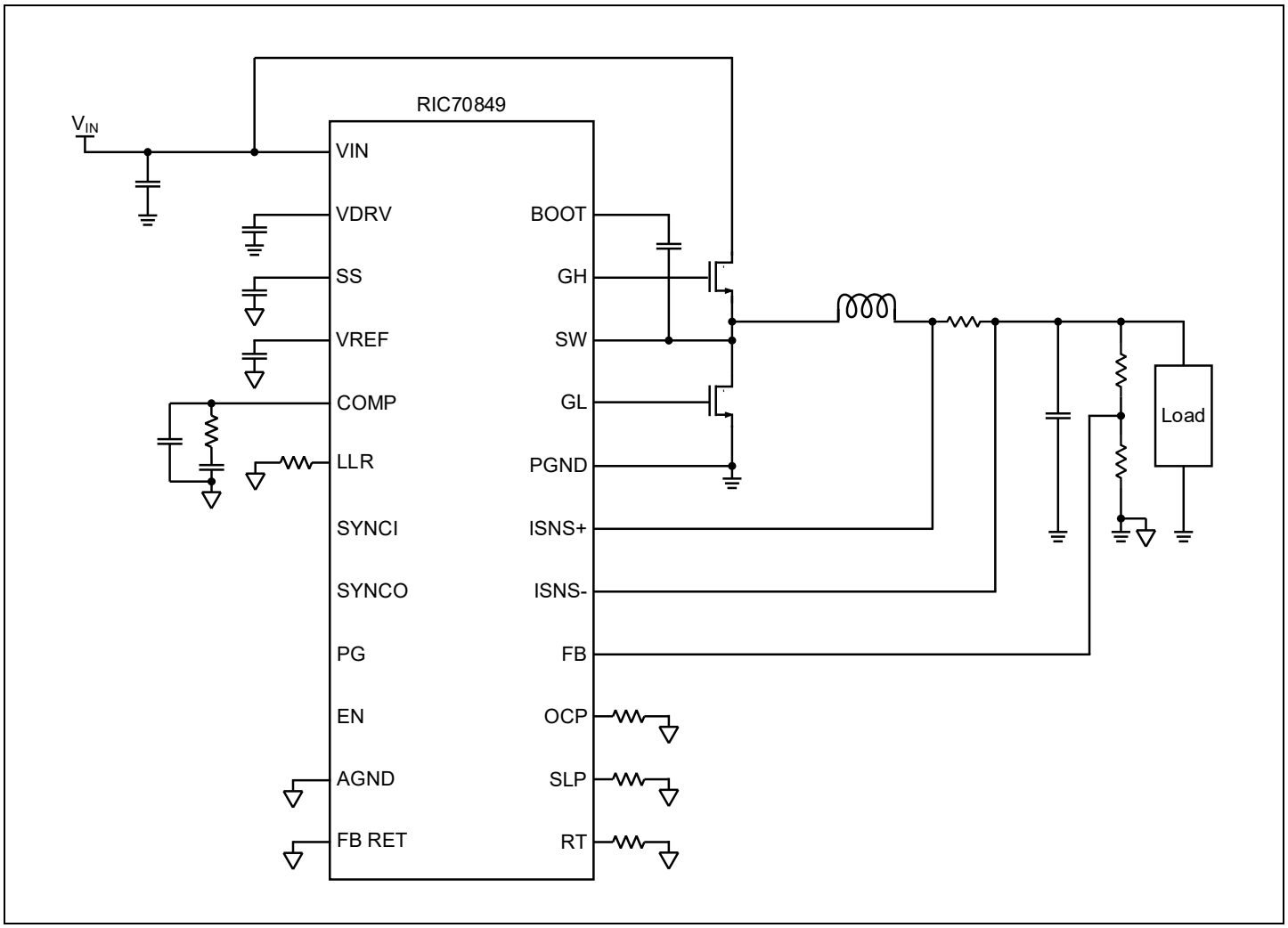


Figure 1 Typical PoL application block diagram

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1 Block diagram

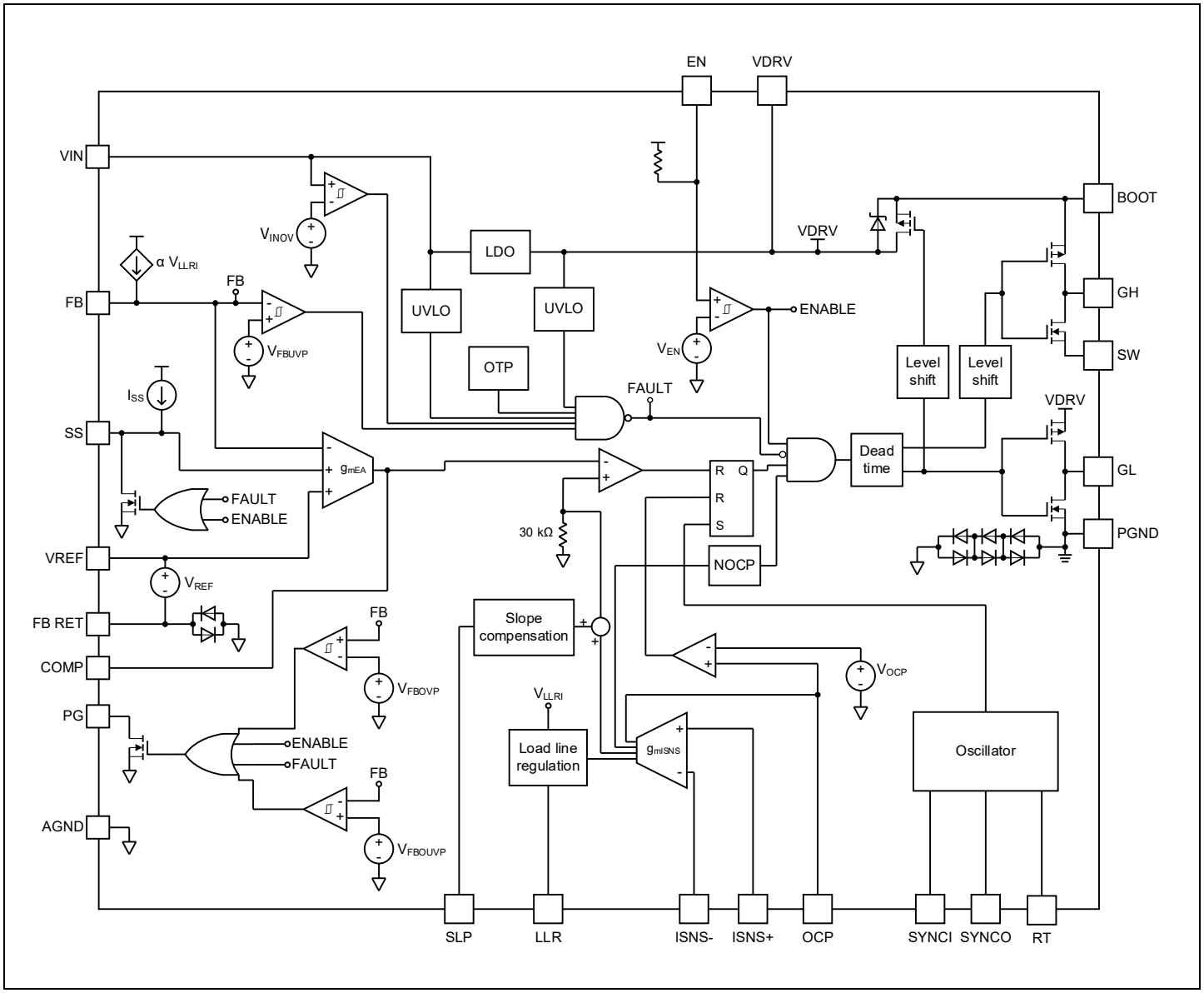


Figure 2 RIC70849 block diagram

2 Pin configuration and functionality

2.1 Pin configuration

24 lead flatpack

Figure 3 RIC70849 pin assignments (top view)

2.2 Pin functionality

Table 2 Pin functionality

Pin	Symbol	Description
1	SYNCI	Input for external clock. Clock on this pin will determine switching frequency if higher than frequency set on RT.
2	RT	Switching frequency selection. Connect a resistor from this pin to FB RET to set the switching frequency when in standalone operation.
3	SYNCO	Output of external clock for synchronization.
4	ISNS+	Positive input pin for inductor current sensing
5	ISNS-	Negative input pin for inductor current sensing
6, Lid	AGND	Analog ground. Logic signals are referenced to this pin.
7	FB RET	Feedback return ground. Feedback signals are referenced to this pin.
8	VREF	Output of internal 600 mV reference voltage. A ceramic capacitor is recommended between this pin and FB RET.
9	FB	Feedback pin for output voltage sensing
10	COMP	Output of internal transconductance error amplifier. Connect compensation network from this pin to AGND.

Pin	Symbol	Description
11	SLP	Slope compensation pin. Connect a resistor from this pin to FB RET to set slope compensation ramp.
12	SS	Soft start pin. A capacitor connected from this pin to FB RET sets the soft start ramp time.
13	LLR	Load line regulation. To enable load line regulation, connect a resistor from this pin to AGND. For no load line regulation leave the pin unconnected.
14	OCP	Over current protection. Connect a resistor from this pin to FB RET to set overcurrent, short circuit and negative current protection threshold. This pin can additionally be used as an output for the sensed inductor current (ISNS+ to ISNS-).
15	VIN	Input for internal LDO. A ceramic capacitor is recommended between this pin and PGND.
16	GH	High side FET gate driver output
17	SW	Switch node. Connect the high side FET source, low side FET drain and output inductor to this pin.
18	BOOT	Bootstrap supply for the high side FET gate driver. A ceramic capacitor is required between this pin and SW.
19	GL	Low side FET gate driver output
20, 22	PGND	Power ground. Connect to the source of the low side FET and negative terminal of input and output capacitors.
21	VDRV	Output of 4.8V internal LDO. A ceramic capacitor of at least 1 µF is required between VDRV and PGND
23	PG	Open drain power good signal. pulled low when fault triggers, EN is pulled low or output voltage is outside regulation window
24	EN	Enable. Forcing low disables PWM on GH and GL and holds both driver outputs low.

3 Electrical parameters

3.1 Absolute maximum ratings

Absolute maximum ratings indicate limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to AGND unless otherwise stated in the table.

Table 3 Absolute maximum ratings

Symbol	Definition	Min	Max	Units
V_{IN}	VIN	-0.3	17.1	V
V_{DRV}	VDRV to PGND	-0.3	6.5	V
BOOT	BOOT to SW	-0.3	6.5	V
SW	SW to PGND (DC)	-1.3	17.1	V
	SW to PGND (Pulse width < 20 ns)	-2.5		V
	SW to PGND (Pulse width < 10 ns)	-6.0		V
G_H	GH to SW (DC)	-0.3	VDRV+0.3	V
	GH to SW (Pulse width < 20 ns)	-1.0		V
	GH to SW (Pulse width < 10 ns)	-4.0		V
G_L	GL to PGND (DC)	-0.3	VDRV+0.3	V
	GL to PGND (Pulse width < 20 ns)	-1.0		V
	GL to PGND (Pulse width < 10 ns)	-4.0		V
V_{EN}	EN	-0.3	17.1	V
IN	SYNCI, PG	-0.3	6.5	V
ISNS	ISNS-, ISNS+ (DC)	-0.3	6.5	V
	ISNS-, ISNS+ (Pulse width < 20 ns)	-1.0		V
LGC	SLP, RT, SYNCO, OCP, LLR, COMP, VREF, SS, FB	-0.3	3.6	V
LGC	SLP, RT, SYNCO, OCP, LLR, COMP, VREF, SS, FB (LET ≤ 81.9 MeV·cm^2/mg)	-0.3	3.1	V
GND_A	FB RET to AGND (DC)	-0.3	0.3	V
	FB RET to AGND (Pulse width < 20 ns)	-0.5	0.5	V
GND_P	PGND to AGND (DC)	-0.9	0.9	V
	PGND to AGND (Pulse width < 20 ns)	-3.0	3.0	V
T_J	Operating junction temperature	-55	150	°C
T_S	Storage temperature	-65	150	°C
T_L	Lead temp (soldering, 10s, 0.063 in (1.6 mm) from case)		300	°C

3.2 ESD ratings

Table 4 ESD ratings

Symbol	Definition	Value	Units
V_{ESDHBM}	ESD Human Body Model (HBM)[1], Class 3A per MIL-STD-883, Method 3015	4	kV
V_{ESDCDM}	ESD Charged device model (CDM)[2]	1	kV

[1] Per ANSI/ESDA/ JEDEC JS-001

[2] Per ANSI/ESDA/JEDEC JS-002

3.3 Thermal characteristics

All ratings are specified under board mounted and still air conditions.

Table 5 Thermal characteristics

Symbol	Definition	Min	Typ	Max	Units
$R_{\Theta JC}$	Thermal resistance, junction to case		1.7		°C/W
$R_{\Theta JA}$	Thermal resistance, junction to ambient		27		°C/W

3.4 Recommended operating conditions

For proper operation the device should be used within the recommended operating conditions. All voltage parameters are absolute voltages referenced to AGND unless otherwise stated.

Table 6 Recommended operating conditions

Symbol	Definition	Min	Max	Units
V_{IN}	VIN bias voltage[1]	4.75	13.2	V
V_{DRV}	External voltage on VDRV pin (VIN=VDRV)[1]	4.6	5	V
V_{OUT}	Output voltage	0.6	5.25	V
f_{SW}	Switching frequency (RT or SYNCI)	100	2,000	kHz
T_A	Operating ambient temperature	-55	125	°C

[1] When voltage on VIN is less than 5 V, internal LDO in RIC70849 is in dropout which may cause VDRV voltage to drop too low under some operating conditions. When operating with low voltage input it is recommended to short VDRV to VIN pin.

3.5 Electrical characteristics

VIN = 4.75 V to 13.2 V and $T_A = T_J$ = -55 to 125°C unless otherwise stated. Logic pins (EN, SLP, RT, SYNCO, SYNCI, ISNS-, ISNS+, OCP, LLR, PG, COMP, VREF, SS, FB) are with respect to AGND = FB RET, power pins (VIN, VDRV, GL) are with respect to PGND and bootstrap pins (BOOT, GH) are with respect to SW. **All parameter ratings apply over a total ionizing dose (TID) of 100 krad(Si) with exposure at a high dose rate (HDR) of 50-300 rad(Si)/s**

Table 7 Electrical characteristics

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Bias input power						
I_{INQNL}	VIN operating current unloaded (500 kHz switching frequency)	5	7	9	mA	EN=5 V, RT=28.6kΩ, No load on GL and GH
I_{INSD}	VIN standby current	2	4	7	mA	EN=0 V
V_{INOV+}	Input overvoltage shutdown rising	15.5	16.6	17.1	V	
V_{INOV-}	Input overvoltage shutdown falling	15.2	16.2	17.1	V	
V_{INOVH}	Input OVP hysteresis		0.4		V	
V_{INUV+}	VIN UVLO rising threshold	4.2	4.4	4.6	V	
V_{INUV-}	VIN UVLO falling threshold	4.1	4.3	4.5	V	
V_{INUVH}	VIN UVLO hysteresis		100		mV	
Linear dropout regulator (LDO)						
V_{DRV}	VDRV voltage from LDO	4.6	4.8	5	V	VIN=9 V
V_{DRVD}	Dropout voltage (VIN-VDRV)	3	13	18	mV	VIN=4.5 V
I_{DRV}	Current limit from VDRV pin	130	148	280	mA	EN=0 V, VIN=4.75 V
		170	203	310	mA	EN=0 V, VIN=13.2 V
V_{DRVUV+}	VDRV UVLO rising threshold	4.2	4.4	4.6	V	
V_{DRVUV-}	VDRV UVLO falling threshold	4	4.2	4.4	V	
V_{DRVUVH}	VDRV UVLO hysteresis		130		mV	
Driver						
V_{OHGH}	GH high output drive	4.95			V	I_{GH}=20 mA, BOOT=5 V
V_{OHGL}	GL high output drive	4.96			V	I_{GL}=20 mA, VDRV=5 V
V_{OLGH}	GH low output drive			0.04	V	I_{GH}=20 mA, BOOT=5 V
V_{OLGL}	GL low output drive			0.04	V	I_{GL}=20 mA, VDRV=5 V
R_{GHH}	GH turn on resistance	0.7	1.4	2.1	Ω	I_{GL}=20 mA
R_{GHL}	GH turn off resistance	0.6	1.0	1.65	Ω	I_{GL}=20 mA
R_{GLH}	GL turn on resistance	0.6	1.1	1.8	Ω	I_{GL}=20 mA
R_{GLL}	GL turn off resistance	0.6	1.0	1.8	Ω	I_{GL} = 20 mA

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
I_{GHH}	GH turn on peak current[1]		2		A	
I_{GHL}	GH turn off peak current[1]		2		A	
I_{GLH}	GL turn on peak current[1]		2		A	
I_{GLL}	GL turn off peak current[1]		2		A	
$t_{minonGH}$	Minimum on time GH		24	27	ns	
$t_{minonGL}$	Minimum on time GL		24.5	30	ns	
t_{dt}	Dead time[1]			8	ns	
Oscillator						
f_{RT}	Internal oscillator frequency	450	500	550	kHz	RT = 28.6 kΩ
		900	1000	1100	kHz	RT = 13.7 kΩ
V_{SYNCI}	SYNCI input threshold (rising edge)	0.85	0.9	0.97	V	
$t_{SYNCION}$	SYNCI input minimum on and off pulse width[1]			100	ns	
I_{SYNCI}	SYNCI input current	-70		60	µA	V_{SYNCI} = 0 V or 5 V
V_{SYNCOH}	SYNCO voltage, logic high	2.7	2.9	3.1	V	
V_{SYNCOL}	SYNCO voltage, logic low			0.1	V	
P_{SYNCO}	SYNCO phase delay (GH to SYNCO)[1]		$0.5/f_{RT}$		°	180° phase shift
Feedback and error amplifier						
V_{FB}	Reference voltage (V_{REF}) + EA offset (V_{OSEA})	594	600	606	mV	
V_{REF}	Reference voltage	594	600	606	mV	
I_{FB}	FB input leakage current	-1		1	µA	V_{FB} = 600 mV, LLR = open
V_{FBOVP}	FB pin overvoltage protection	0.64	0.66	0.69	V	
V_{FBUVP}	FB pin undervoltage protection	0.51	0.54	0.57	V	
t_{VFBUVP}	FB pin undervoltage propagation delay	0.3	0.5	0.7	µs	
A_{EA}	EA DC gain[1]		126		dB	
g_{mEA}	EA transconductance	0.6	1	1.6	mS	
V_{OSEA}	EA offset voltage	-6		6	mV	
G_{BWEA}	EA gain bandwidth product[1]		155		MHz	
Soft start						
I_{SS}	Soft start current source	6.1	10	13.9	µA	
Current sense						
A_{ISNS}	Current sense amplifier DC gain	9.5	10	10.5	V/V	ISNS+ to ISNS- = ±5mV

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
g_{mISNS}	Current sense amplifier transconductance	280	333	380	µS	Measured on OCP pin
G_{BWISNS}	Current sense amplifier gain bandwidth product[1]		30		MHz	
I_{ISNS}	ISNS+ and ISNS- leakage current			17	µA	ISNS+ = 0.6 V, 3.6 V, ISNS- = 0.6 V, 3.6 V
V_{OCP}	Overcurrent threshold	1.195	1.215	1.235	V	
V_{NOCP}	Negative overcurrent threshold	-40	-20	-13	mV	Pre-irradiation
		-40	-20	-10	mV	Post-irradiation
t_{OCP}	Overcurrent threshold propagation delay	0.2	0.4	0.5	µs	ISNS+ to ISNS- = 20mV
Load line regulation						
I_{LLRIN}	Load line regulation current source from FB pin no load	-0.008		0.008	µA	R_{LLR} = 7.15 kΩ, ISNS+ to ISNS- =0 mV
I_{LLRL}	Load line regulation current source from FB pin, with load	-1.7	-1.1	-0.5	µA	R_{LLR} = 7.15 kΩ, ISNS+ to ISNS- = 20 mV
I_{LLRM}	Load line regulation current source maximum[1]		10		µA	
BW_{LLR}	LLR bandwidth[1]		250		kHz	
Enable						
V_{EN+}	EN rising threshold	0.88	0.92	0.98	V	
V_{EN-}	EN falling threshold	0.7	0.77	0.84	V	
V_{ENHYS}	EN pin hysteresis		200		mV	
I_{EN}	EN pin leakage current	-5		20	nA	EN = 0 V and 5 V
Power good						
V_{PGOV}	V_{PG} high limit for PG	0.63	0.66	0.7	V	
V_{PGOVH}	V_{PG} high limit hysteresis		21		mV	
V_{PGUV}	V_{PG} low limit for PG	0.51	0.54	0.57	V	
V_{PGUVH}	V_{PG} low limit hysteresis		31		mV	
V_{PGL}	PG low output	0.145	0.25	0.34	V	I_{PGOUT} = 2 mA
I_{PG}	PG active source current limit[1]			4	mA	
I_{PGLK}	PG high leakage current			100	nA	
Overtemperature						
T_{SD}	Overtemperature shutdown[1]	155			°C	
T_{HYS}	Overtemperature hysteresis[1]		25		°C	

[1] Parameter not subject to production test. Parameter guaranteed by design and characterization.

4 Typical characteristics

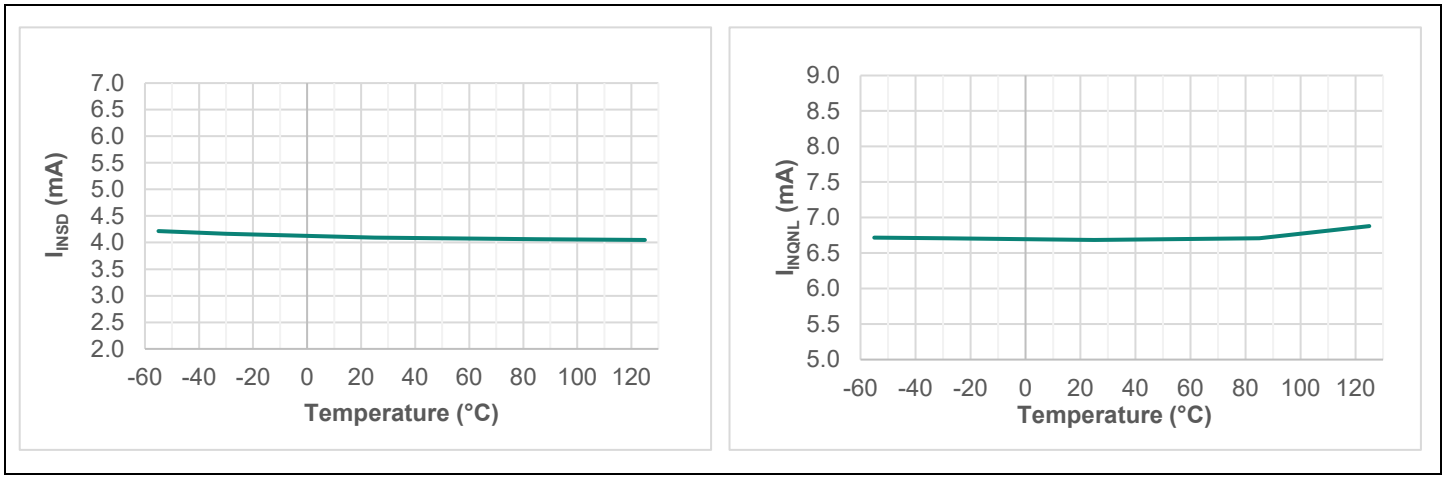


Figure 4 VIN standby current (I_{INSD}) and VIN operating current at 500 kHz unloaded (I_{INQNL}) over temperature

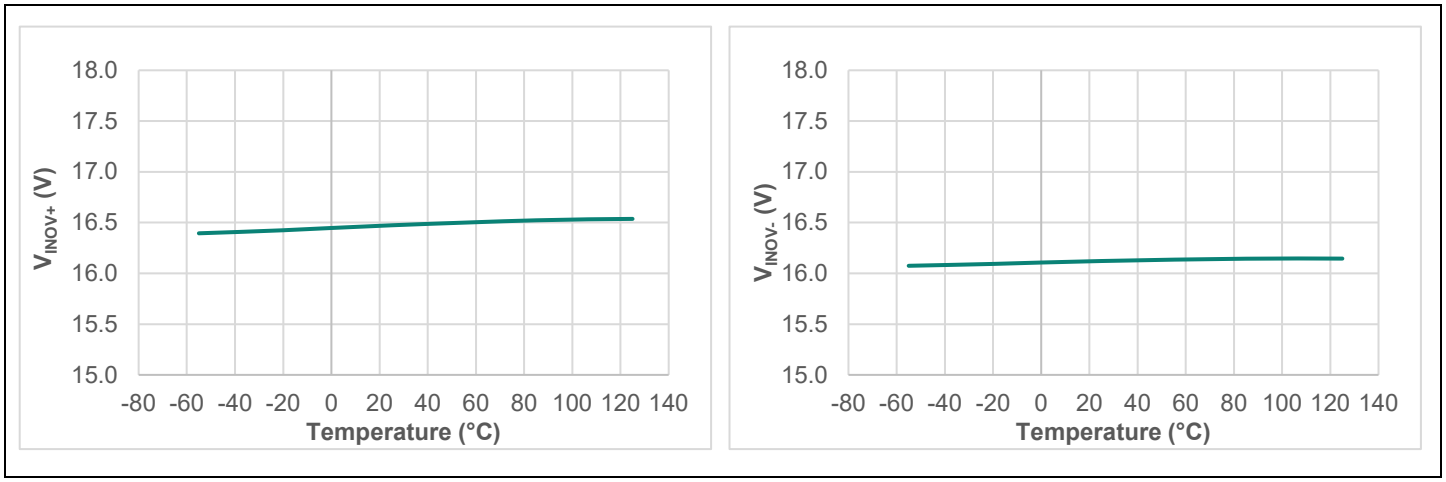


Figure 5 Input overvoltage shutdown rise (V_{INOV+}) and fall (V_{INOV-}) over temperature

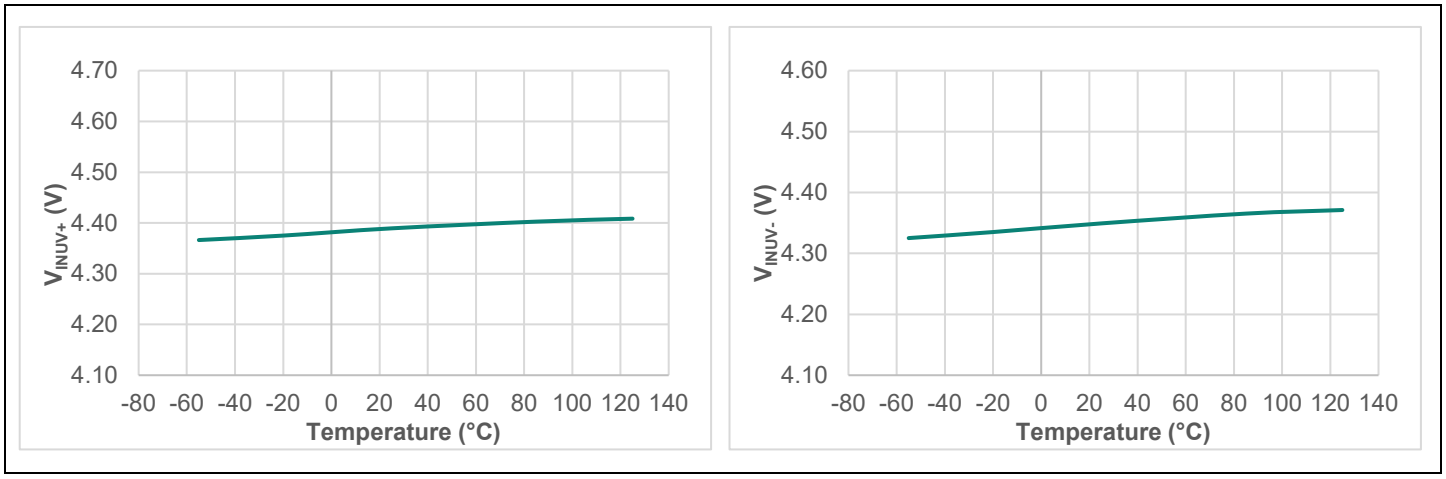


Figure 6 Input undervoltage lockout rise (V_{INUV+}) and fall (V_{INUV-}) over temperature

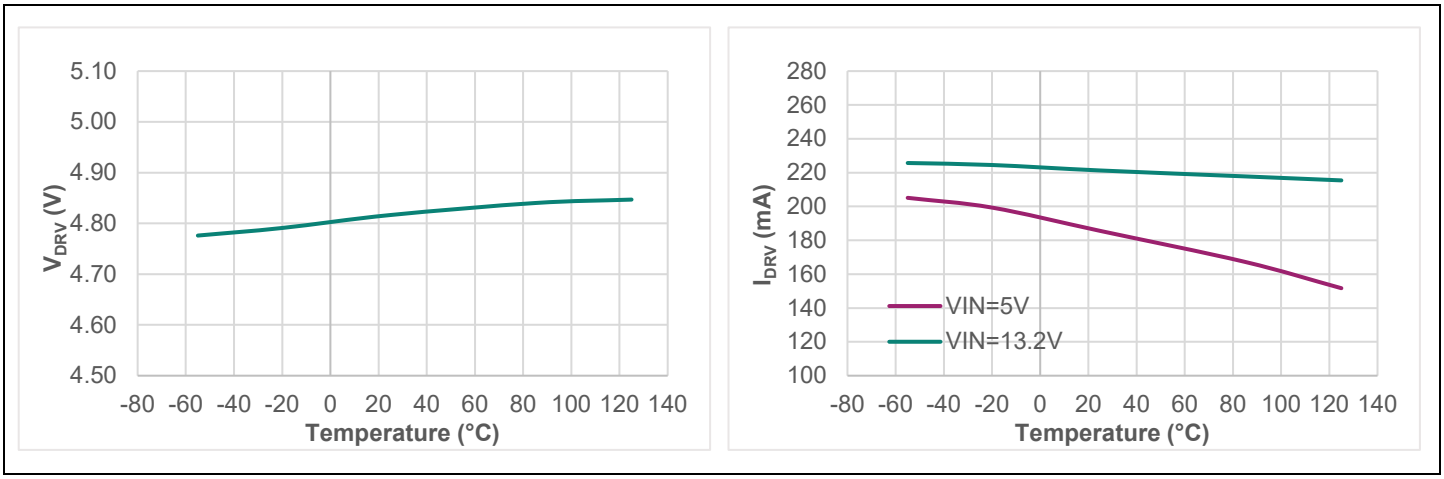


Figure 7 VDRV voltage (V_{DRV}) and VDRV current limit (I_{DRV}) over temperature

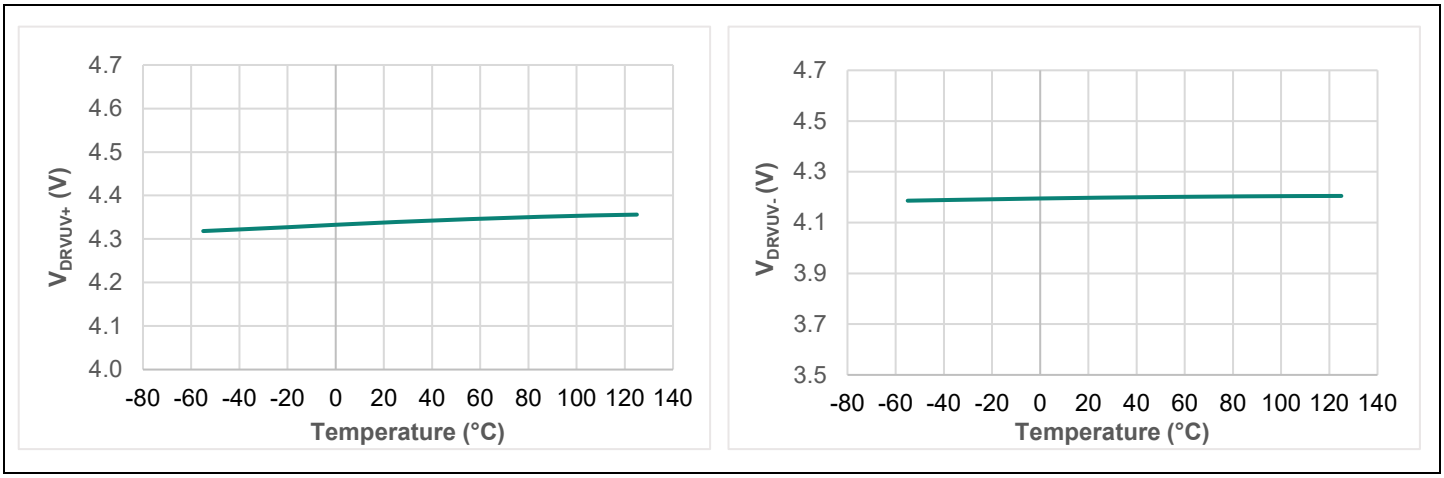


Figure 8 VDRV undervoltage lockout rise (V_{DRVUV+}) and fall (V_{DRVUV-}) over temperature

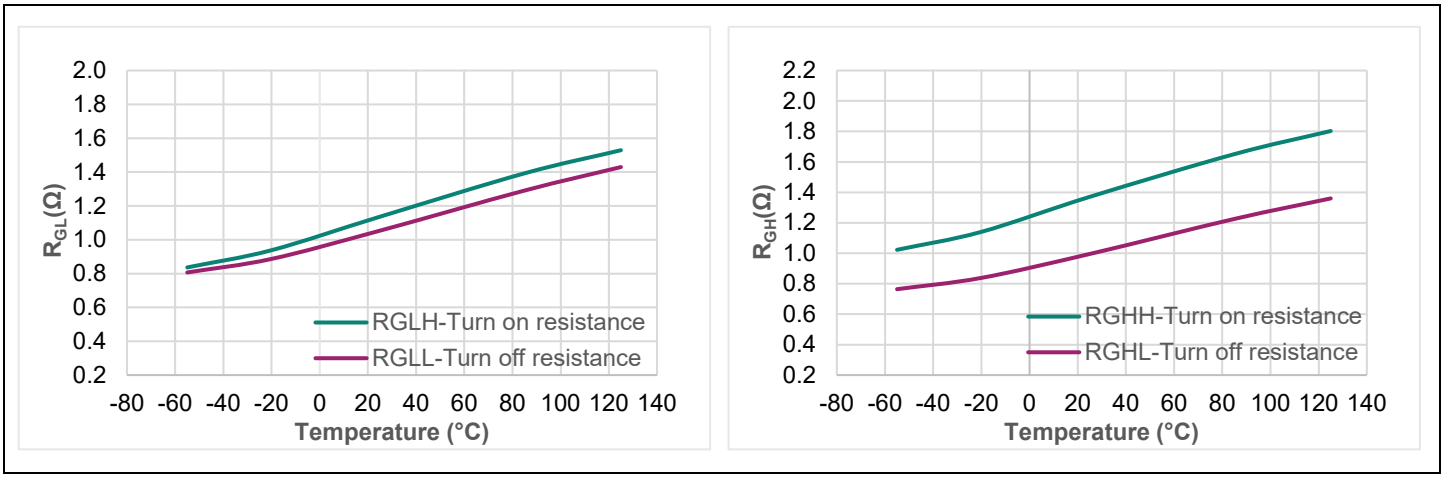


Figure 9 GL turn on and turn off resistance (R_{GL}) and GH turn on and turn off resistance (R_{GH}) over temperature

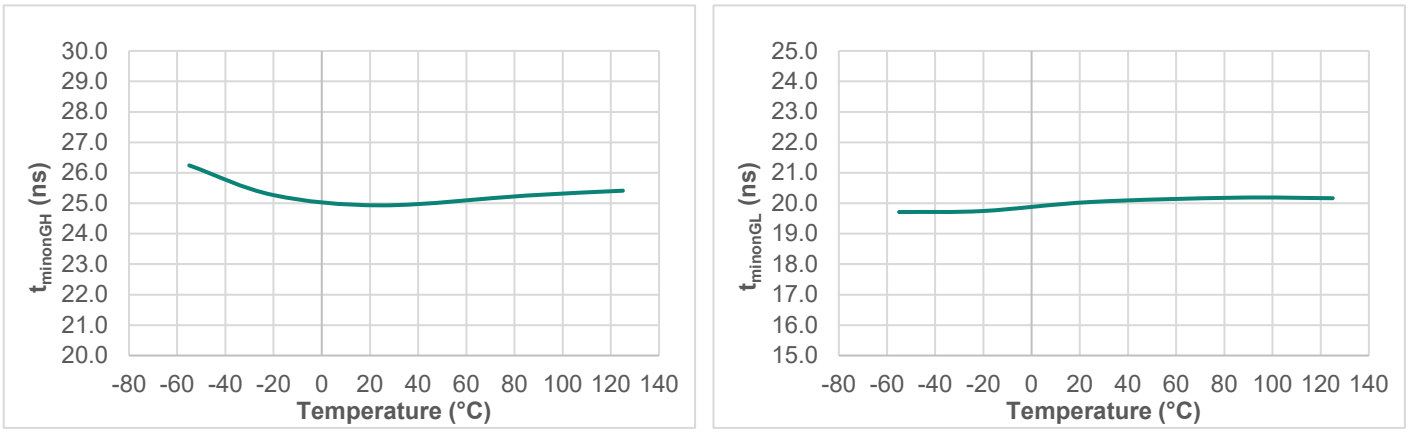


Figure 10 Minimum on time GH ($t_{onminGH}$) and minimum on time GL ($t_{onminGL}$) over temperature

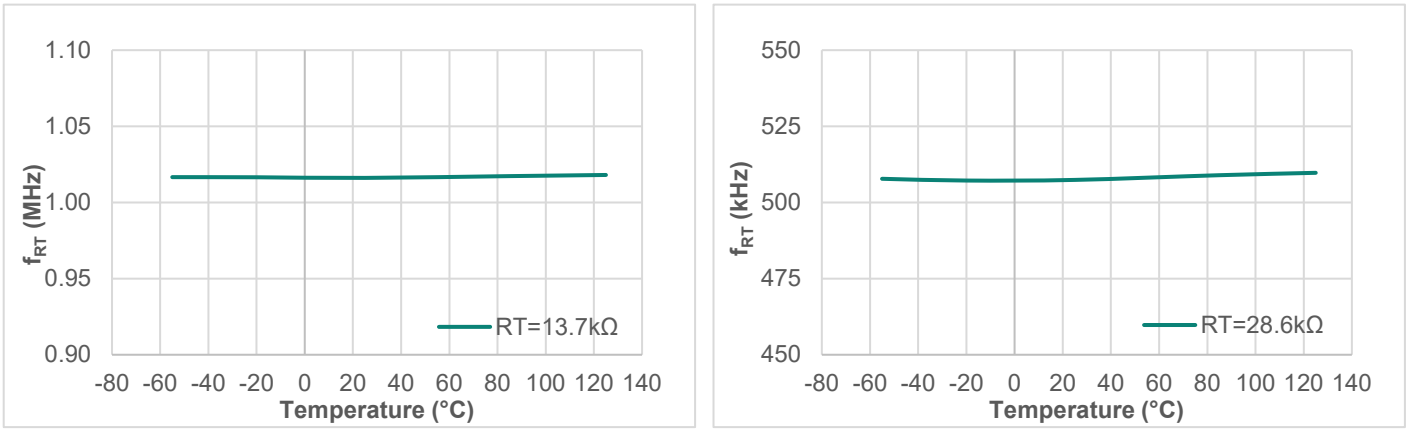


Figure 11 Internal oscillator frequency (f_{RT}) over temperature

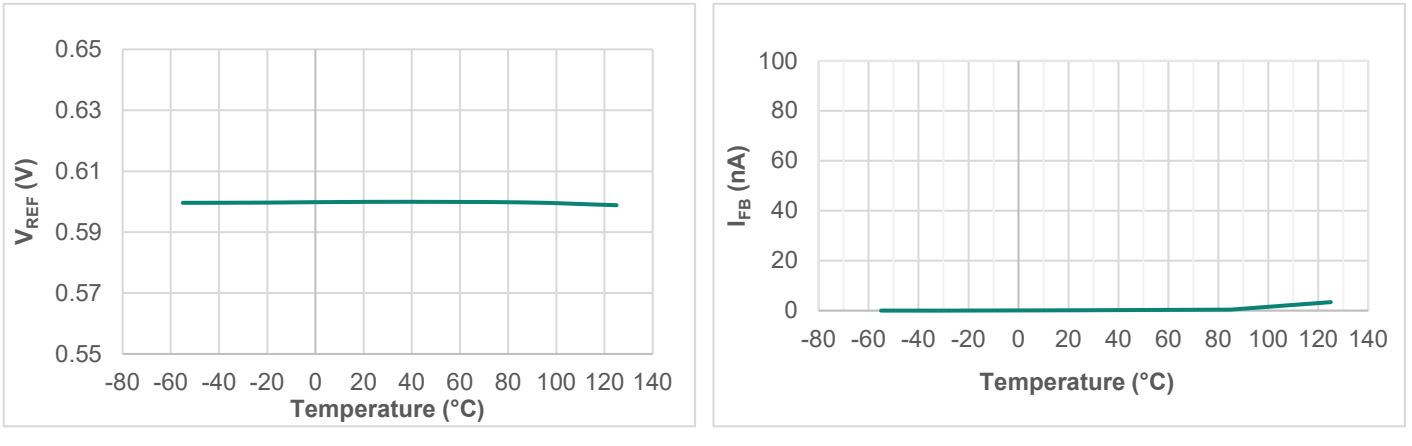


Figure 12 Reference voltage (V_{REF}) and FB input leakage current (I_{FB}) over temperature

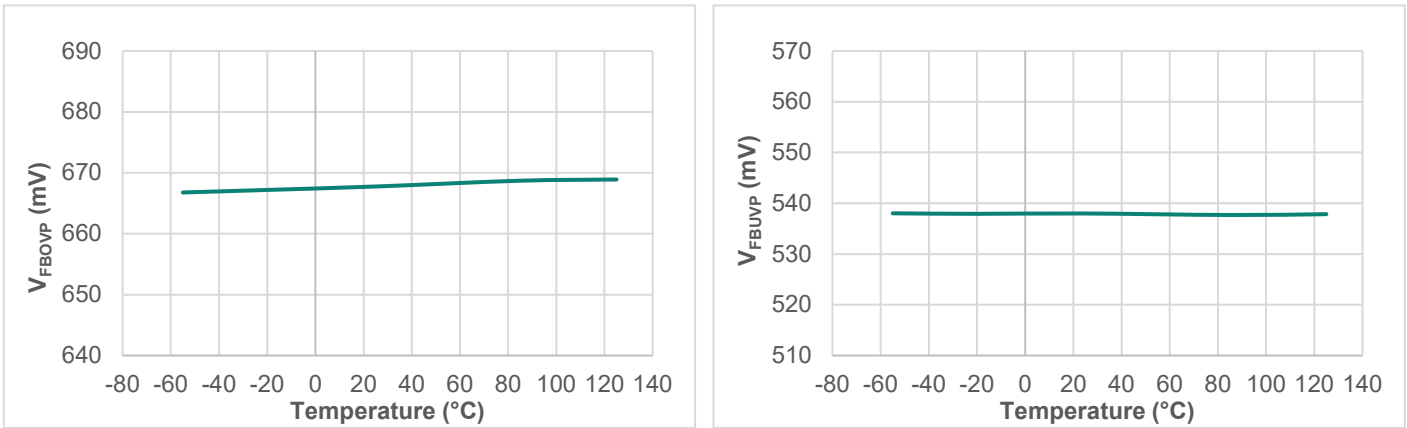


Figure 13 FB overvoltage protection (V_{FBOVP}) and undervoltage protection (V_{FBUVP}) over temperature

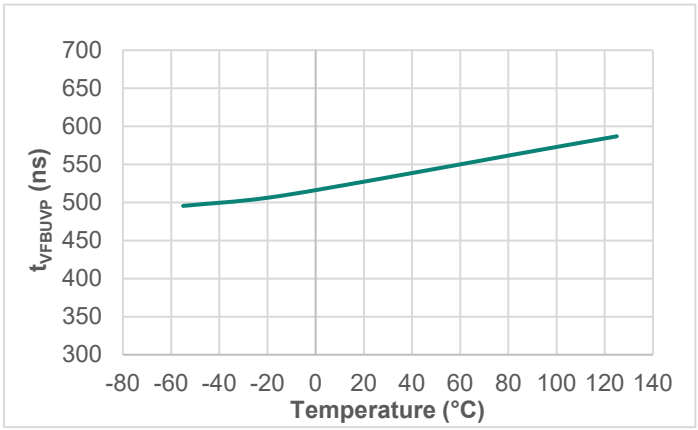


Figure 14 FB pin undervoltage propagation delay (t_{VFBUVP}) and EA transconductance (g_{mEA}) over temperature

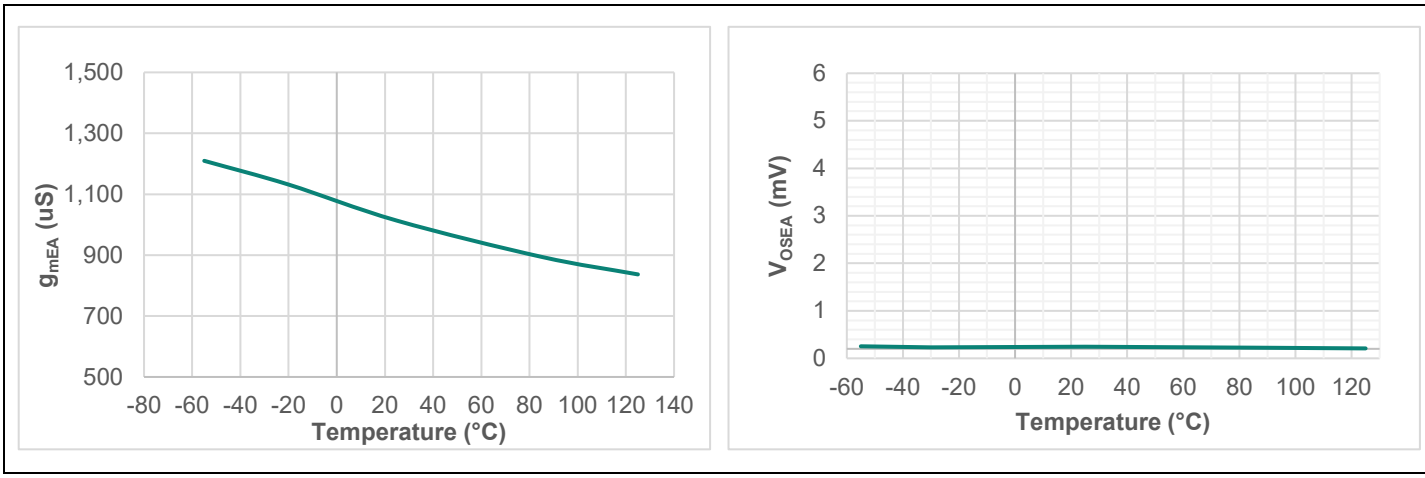


Figure 15 EA transconductance (g_{mEA}) and offset voltage (V_{OSEA}) over temperature

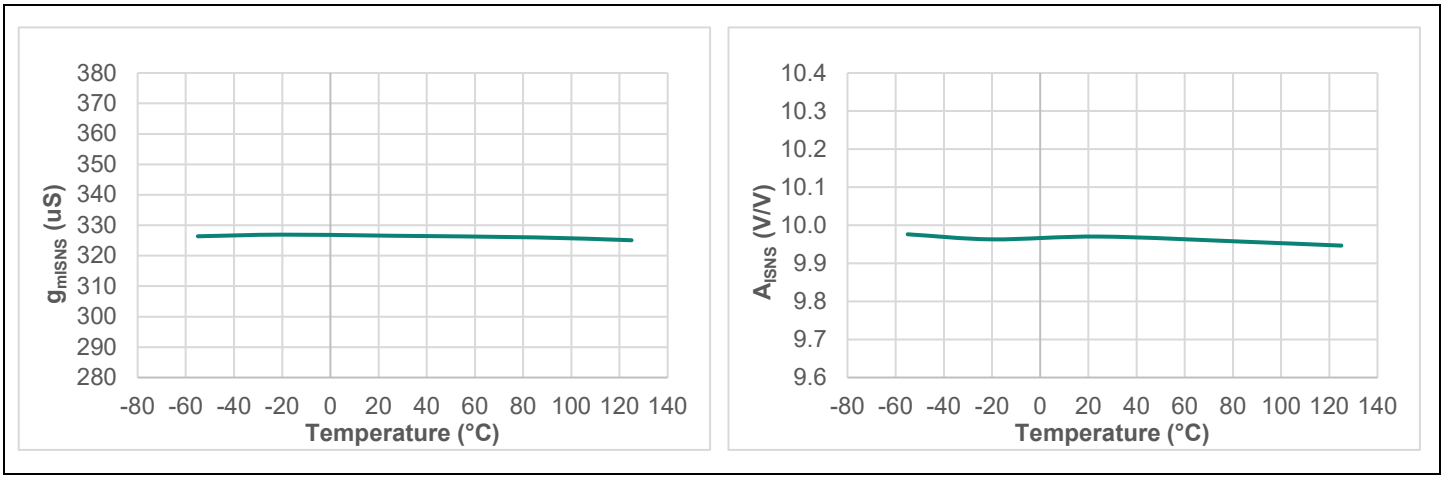


Figure 16 Current sense amplifier transduction (g_{mISNS})and DC gain (A_{ISNS}) over temperature

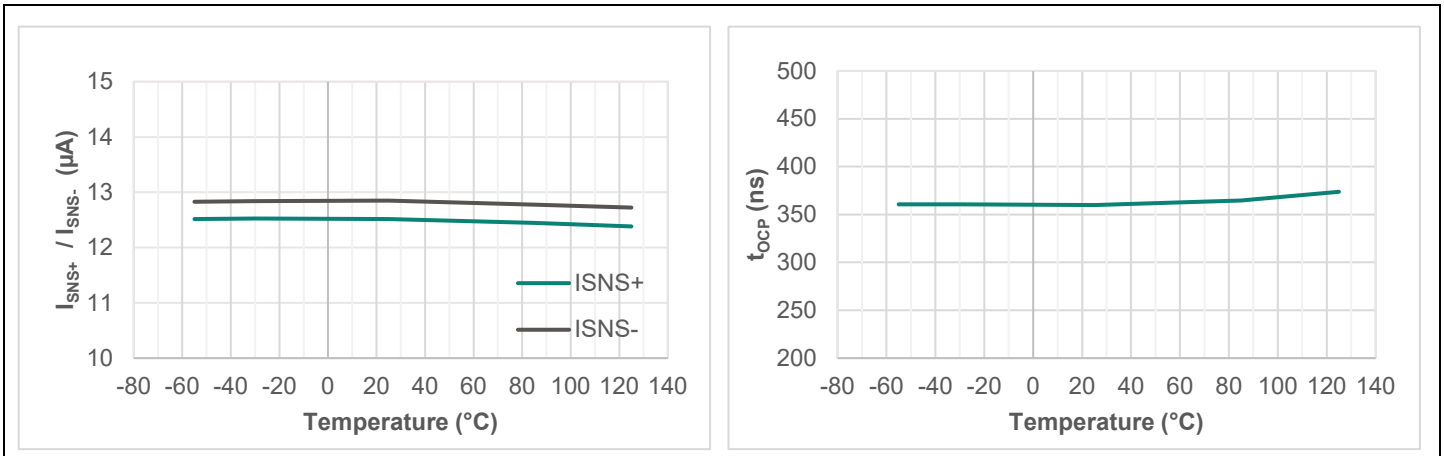


Figure 17 ISNS+(I_{SNS+}) and ISNS- (I_{SNS-}) leakage current and overcurrent threshold propagation delay (t_{OCP}) over temperature

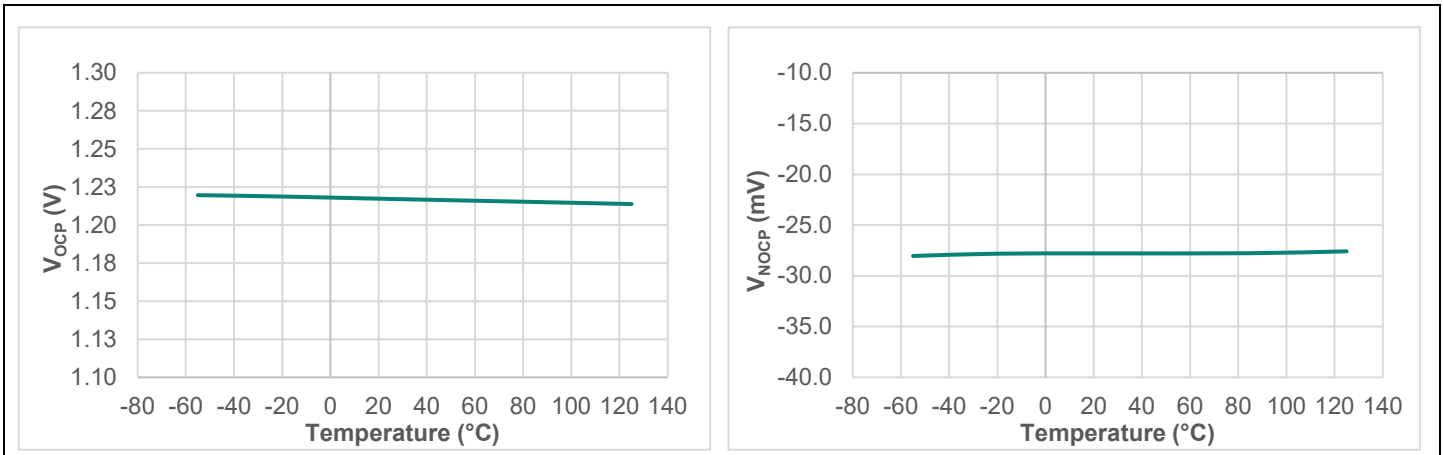


Figure 18 Overcurrent threshold (V_{OCP}) and negative overcurrent threshold (V_{NOCP}) over temperature

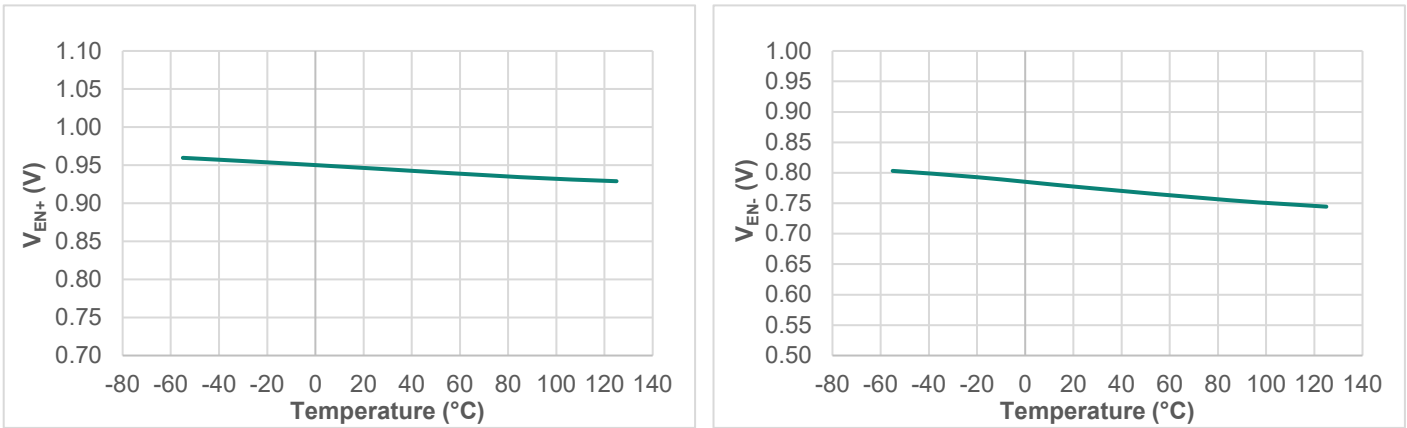


Figure 19 EN rising (V_{EN+}) and EN falling (V_{EN-}) over temperature

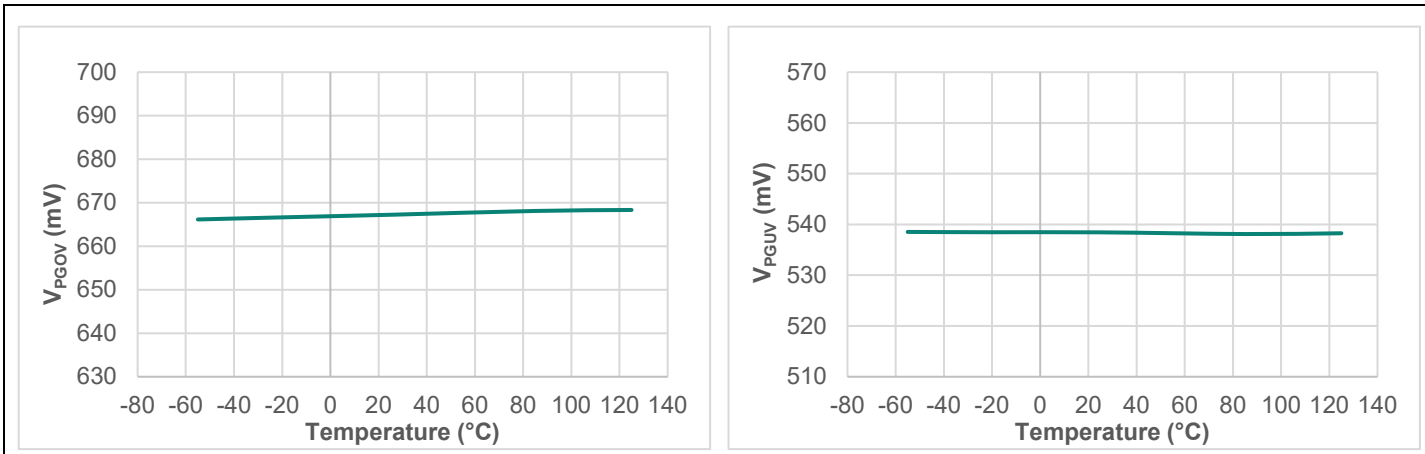


Figure 20 VFB high limit for PG (V_{PGOV}) and low limit for PG (V_{PGUV}) over temperature

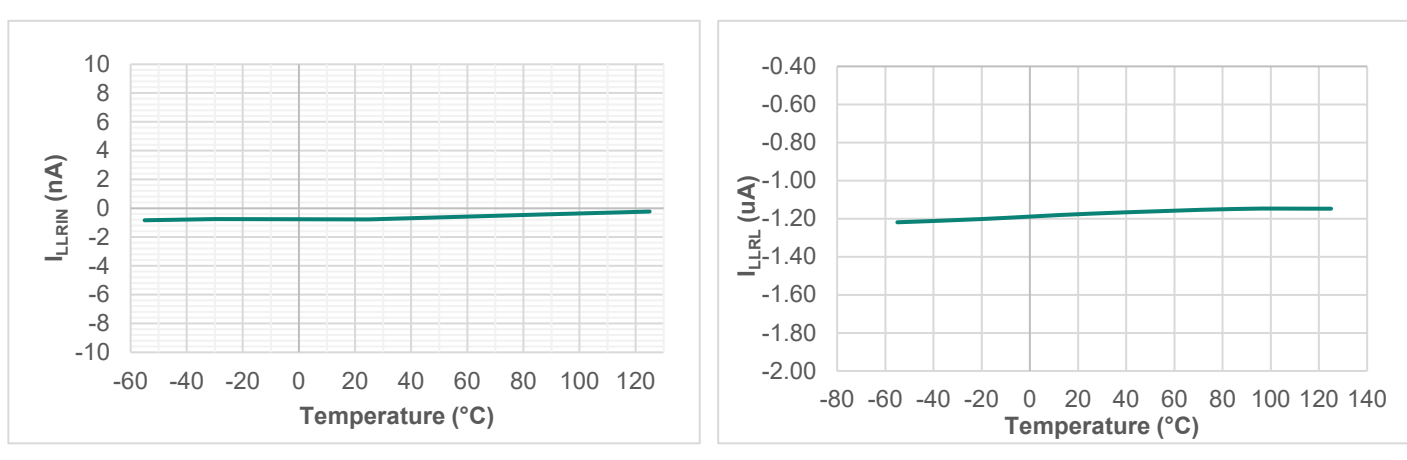


Figure 21 Load line regulation current source from FB pin loaded (I_{LLRL}) over temperature

5 General description

RIC70849 is a fixed switching frequency peak current mode buck controller intended for applications such as point of load (PoL) power conversion for space grade field programmable gate array (FPGA) core rails, microcontrollers and application-specific integrated circuits (ASICs). It is designed to work with radiation hardened GaN HEMTs, such as Rad Hard GaN. RIC70849 is certified for use in space applications per the Defense Logistics Agency (DLA) MIL-PRF-38535 Class V (DLA certification pending).

5.1 Radiation performance

RIC70849 is designed to work in space and other applications where there is significant ionizing radiation and energetic particles in the environment that can affect microcircuit performance. RIC70849 is characterized for operation up to a total ionizing dose (TID) of 100 krad(Si), with electrical parameters including limits post-irradiation. It is also characterized for single event effects (SEE) up to 81.9 MeV·cm^2/mg.

The packaged versions of RIC70849 do not have any electrically floating metal, with all metal (including the lid) internally connected to a known, controlled potential. This allows for compliance with system level requirements prohibiting electrically floating metal without the need for additional wires.

5.1.1 Total ionizing dose (TID)

RIC70849 is tested over total ionizing dose (TID) to verify robustness to ionizing proton and electron radiation environments, such as space. The radiation hardness assurance (RHA) program at IR HiRel uses a Cobalt-60 (60 Co) source and heavy ion irradiation. Every wafer is tested per MIL-STD-883, Method 1019, test condition A “Ionizing Radiation (Total Dose) Test Procedure.” Both pre- and post-irradiation performance are tested to the limits specified in the electrical characteristics.

5.1.2 Single event effects (SEE)

RIC70849 is characterized in heavy ion environment for single event effects (SEE) up to a linear energy transfer (LET) of 81.9 MeV·cm^2/mg. RIC70849 is found to be immune to destructive events single event burnout (SEB), single event gate rupture (SEGR) and single event latch-up (SEL) to a bias voltage of 16.7 V up to an LET of 81.9 MeV·cm^2/mg. RIC70849 is also characterized for single event transient (SET) up to an LET of 81.9 MeV·cm^2/mg.

5.2 Input power and bias

5.2.1 Power input

RIC70849 has an absolute maximum rating of 17.1 V on the VIN pin. This enables support of common input voltages such as 5 V or 12 V while meeting various tolerance and derating requirements typical of space applications. It is recommended that during initial startup the applied voltage on the VIN pin has a turn on slew rate of 0.1 V/ms or faster.

5.2.2 Drive voltage

RIC70849 features an internal linear low-dropout regulator (LDO) from VIN pin to VDRV pin. This internal LDO generates a 4.8 V (typical) supply. It is used for the internal logic and internal half bridge gate driver of RIC70849. It can additionally be used as a power rail for additional functions, such as a logic high voltage for the PG and EN pins. This LDO has a current limit I_{DRV}, which if reached will cause the LDO to enter constant current mode and the output voltage to decrease. If the voltage on VDRV decreases below the undervoltage lockout threshold, RIC70849 will enter undervoltage lockout and stop PWM operation. A capacitance of at least 1 µF from VDRV to PGND is required for proper operation.

When VIN=5 V and the VDRV pin is under heavy load (such as high switching frequency or large external load), the voltage drop of the internal LDO may cause the VDRV voltage to be lower than desired. To overcome this, an external voltage can be applied to VDRV. If an external voltage is applied to VDRV, it is recommended to apply the same voltage to VIN as well. If this is done it is recommended to keep VDRV pin voltage within the recommended limits specified in the electrical characteristics.

5.2.3 High side bootstrap circuit

RIC70849 features an integrated bootstrap circuit to provide bias for the integrated high side gate driver. The input for this bootstrap comes from VDRV. For proper operation, a ceramic capacitor of at least 100 nF is recommended from BOOT to SW pin.

5.3 Return pins

RIC70849 features 3 return pins, PGND, AGND and FB RET, along with a high side floating power return SW. PGND is intended for the power stage, where there are high amounts of ringing and electrical noise, and is used with VIN, VDRV and GL. SW is a power return for the high side gate driver and is used with BOOT and GH. AGND is intended for analog logic and is used with SYNCI, SYNCO, COMP, LLR, PG and EN pins. FB RET is a return for the feedback network that ties directly to the ground of the internal reference voltage. By providing a separate return for FB RET, RIC70849 has pseudo-differential output voltage sensing, which improves DC regulation accuracy over load. FB RET is intended for feedback circuitry that is referenced to the reference voltage, and is used with VREF, SLP, SS, RT and OCP pins.

All 3 return pins (PGND, AGND, FB RET) are internally connected in RIC70849 through diodes. These diodes clamp ringing, and potential noise coupling, across various returns. It is recommended to connect all 3 return pins (PGND, AGND, FB RET) externally together at the resistor divider network, which should be as close as possible to the load.

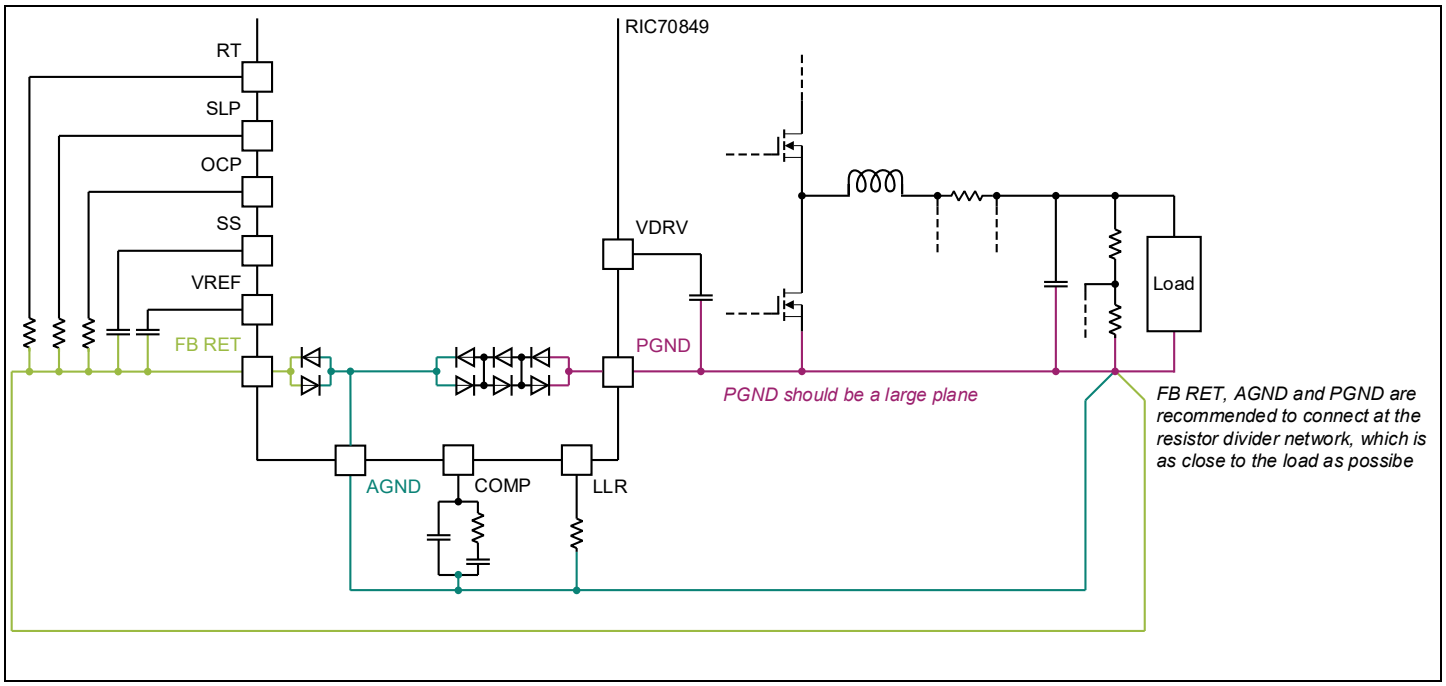


Figure 22 Example external connections for return pins PGND, AGND and FB RET

5.4 Gate drive

RIC70849 features and integrated half bridge driver with bootstrap and level shift. The drive voltage for both the high and low side is typically 4.8 V and is supplied from VDRV. The low side (GL) and high side (GH) have a gate drive strength of 2 A source and sink. Both drivers are intended to work with GaN HEMTs such as Rad Hard GaN.

In some instances, it may be desired to slow down the switching speed of the switches to reduce the voltage overshoot and ringing on the switch node or generated electromagnetic interference (EMI). This can be achieved by adding a resistor in series from GH (R_{GH}) or GL (R_{GL}) to the respective FET gate to slow down both the turn on and turn off switching time. Additionally, for the high side GH, a resistor (R_{GHON}) can be added in series with the bootstrap capacitor to slow down turn on time but maintain fast turn off speed.

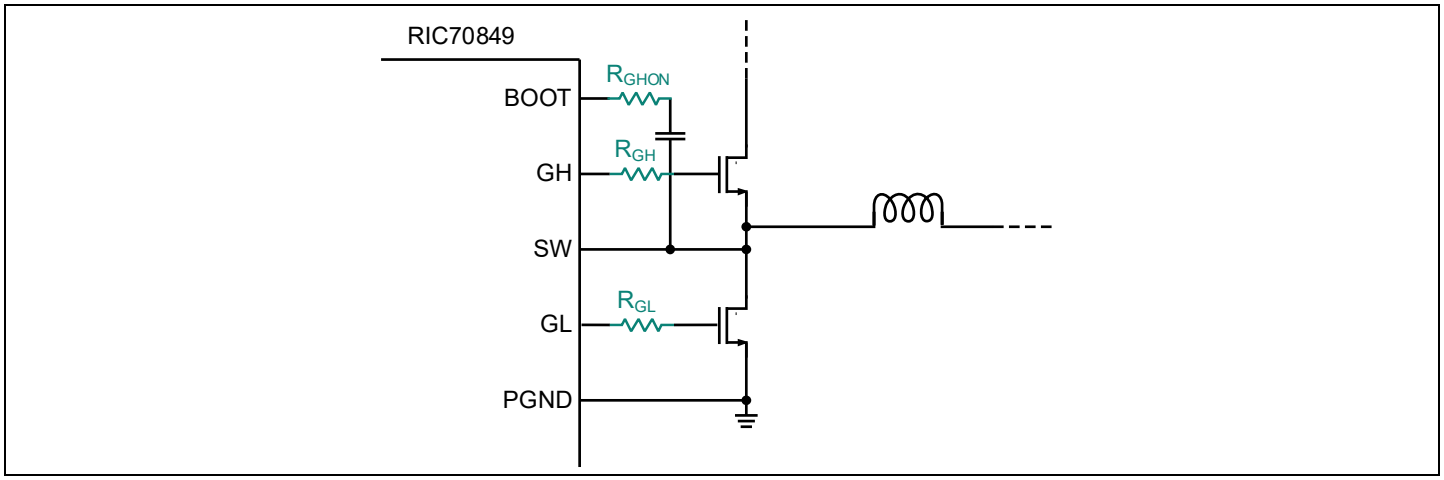


Figure 23 Optional external gate drive resistors

When the internal LDO is used to power the IC (bias power only applied to VIN), if large gate capacitance transistors are used at high switching frequencies (1 MHz and above), the internal LDO current limit I_{DRV} may be reached, reducing the effective maximum switching frequency. This occurs since the I_{DRV} limit includes the internal gate driver. The current draw from the gate driver operation can be approximated with the following equation.

$$I_{gate\ driver} = (Q_{G\ HS} + Q_{G\ LS}) \cdot f_{sw}$$

Where,

- $I_{gate\ driver}$ is the current draw from the gate driver in amperes (A)
- $Q_{G\ HS}$ is the total gate charge of the high side transistor in Columb (C)
- $Q_{G\ LS}$ is the total gate charge of the low side transistor in Columb (C)
- f_{sw} is the switching frequency in hertz (Hz)

It is recommended that $I_{gate\ driver}$ and any external load powered off of VDRV should always be less than I_{DRV} when the internal LDO is used to generate VDRV (bias power only applied to VIN).

5.5 Switching frequency

RIC70849 operates in fixed switching frequency operation, where the switching frequency stays at a fixed value and the duty cycle is modulated to regulate the output voltage. The clock that sets the switching frequency can either come from an internal oscillator or from an external clock.

5.5.1 Internal oscillator

To operate from the internal oscillator, the switching frequency can be set from 100 kHz to 2 MHz with an external resistor R_{RT} from RT to FB RET. The switching frequency f_{sw} for R_{RT} can be calculated with the following equation.

$$f_{sw} = \frac{1}{66.12 \cdot 10^{-12} \cdot RT + 76 \cdot 10^{-9}}$$

Where,

- RT is resistor on RT pin to FB RET pin in ohms (Ω)
- f_{sw} is the switching frequency in hertz (Hz)

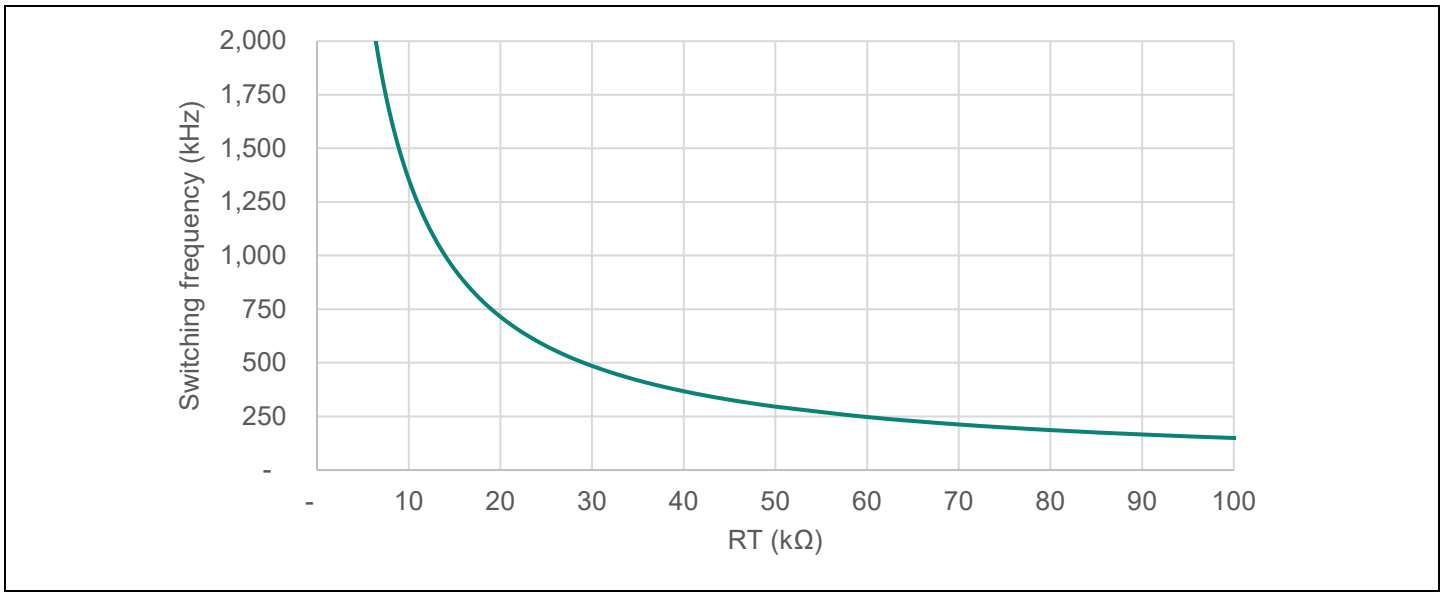


Figure 24 Switching frequency vs. resistor on RT pin

5.5.2 External clock

To operate RIC70849 from an external clock, the external clock needs to be applied from SYNCI to AGND. The clock is intended to be a square wave with amplitude anywhere between 1.8 V to 5 V logic with a logic high pulse width that is at least 100 ns long and logic low pulse width that is at least 100 ns long. The switching frequency is set by the period between rising edges of the external clock. When operating from an external clock applied to the SYNCI pin, the internal oscillator frequency on the RT pin must be set to at least 90% of the external clock frequency applied to SYNCI pin for proper operation. For example, if the external clock on SYNCI is 500 kHz, the internal oscillator frequency on the RT pin must be set at 450 kHz or greater.

RIC70849 selects operation from either the internal oscillator or external clock by whichever frequency is higher. If an external clock is applied to SYNCI at a frequency higher than RT, RIC70849 will follow the external clock. If there is no external clock applied to SYNCI (f_{SW}=0 Hz) or the external clock frequency is lower than the internal oscillator, RIC70849 will operate at the internal oscillator frequency. This allows for RIC70849 operation to be uninterrupted if it is following an external clock signal that either momentarily drops out or stops altogether.

5.5.3 Synchronization output

When operating from the internal oscillator (switching frequency set by RT pin), RIC70849 generates a 5 V PWM signal with a frequency equal to and phase 180° offset from the switching frequency on the SYNCO pin. This signal is

intended to connect to the SYNCI pin of another RIC70849 to allow them to operate in 2 phase interleaved operation. When an external clock is applied to SYNCI where the frequency is higher than the internal oscillator frequency set by a resistor on the RT pin and RIC70849 is in slave/follower mode, SYNCO output is disabled and is always held low.

5.6 Control

RIC70849 features peak current mode control for operation. As a result, it has both current sense and voltage sense along with compensation and control features.

5.6.1 Current sense amplifier

For the current sensing, which is used for both regulation and fault protection, RIC70849 has a differential transconductance amplifier with input from ISNS+ pin to ISNS- pin. This sensed current is intended to come from either a current sense resistor in series with the output inductor or inductor DC resistance (DCR) current sensing. The transconductance amplifier has a typical gain g_{mISNS} of 333 µS and an offset of 30 µA. For the control loop, the output of this transconductance amplifier has a 30 kΩ resistor on the output, which provides an overall current sense amplifier gain G_{CSA} of 10. A simplified block schematic showing the key components for the control current sense are shown in Figure 7.

$$G_{CSA} = g_{mISNS} \cdot R = 333\ \mu S \cdot 30\ k\Omega = 10$$

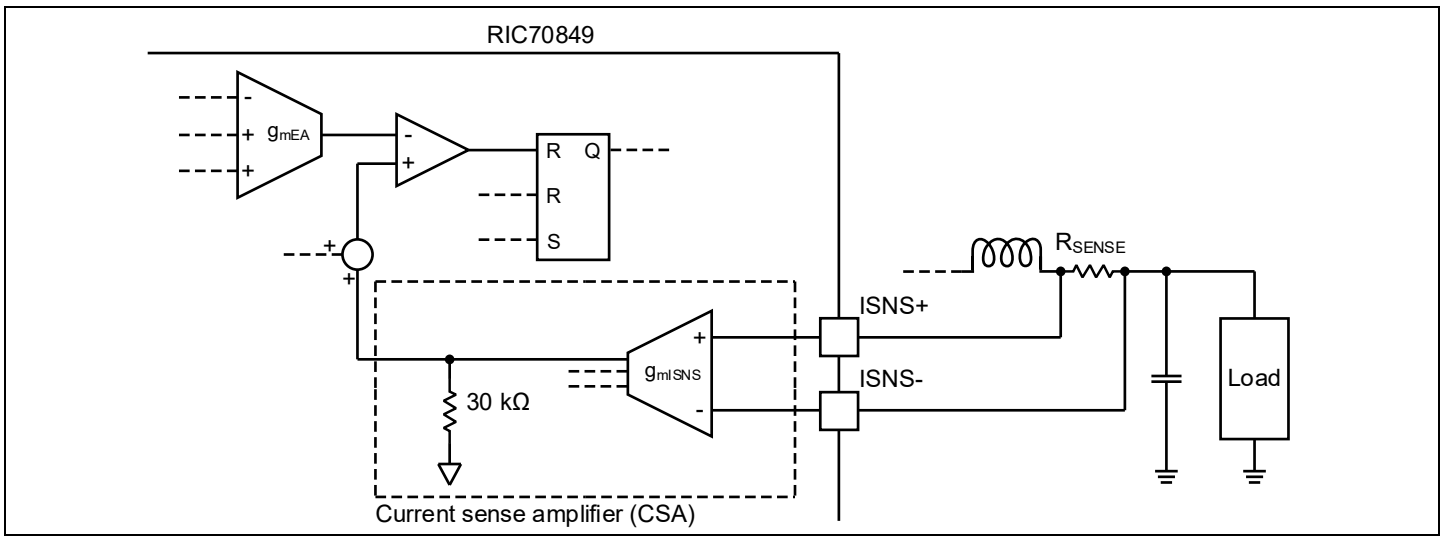


Figure 25 Simplified schematic of RIC70849 current sense amplifier

5.6.1.1 Current sense monitoring

For some applications, such as telemetry and fault monitoring, it may be desired to monitor the output current. This can be achieved with the RIC70849 OCP pin. This pin is connected to the output of the current sense amplifier and creates a voltage that is proportional to the sensed current from ISNS+ to ISNS-. More information on this is in section 5.10.1.

5.6.1.2 Current sense resistor

When a current sense resistor is used, it is recommended to have a kelvin connection from the ISNS+ and ISNS- pins to the current sense resistor. The resistance used will control the gain of the inner current control loop and is intended to be around 0.5 mΩ. It is required to keep the sense resistor connected on the output side of the inductor

(between the inductor and output capacitors) to limit the voltage magnitude and electrical noise on the ISNS+ and ISNS- pins.

5.6.1.3 Inductor DCR current sensing

Inductor DCR current sensing is a technique where the DC resistance of the output inductor is used to sense the current. This allows for the current sense resistor to be eliminated, which improves the efficiency of the power supply. To implement DCR current sensing, an RC network must be added in parallel with the output inductor and ISNS+ and ISNS- pins connected across the capacitor, as shown in Figure 8, where DCR is the DC resistance of the inductor and R_{DCR} and C_{DCR} are added external components.

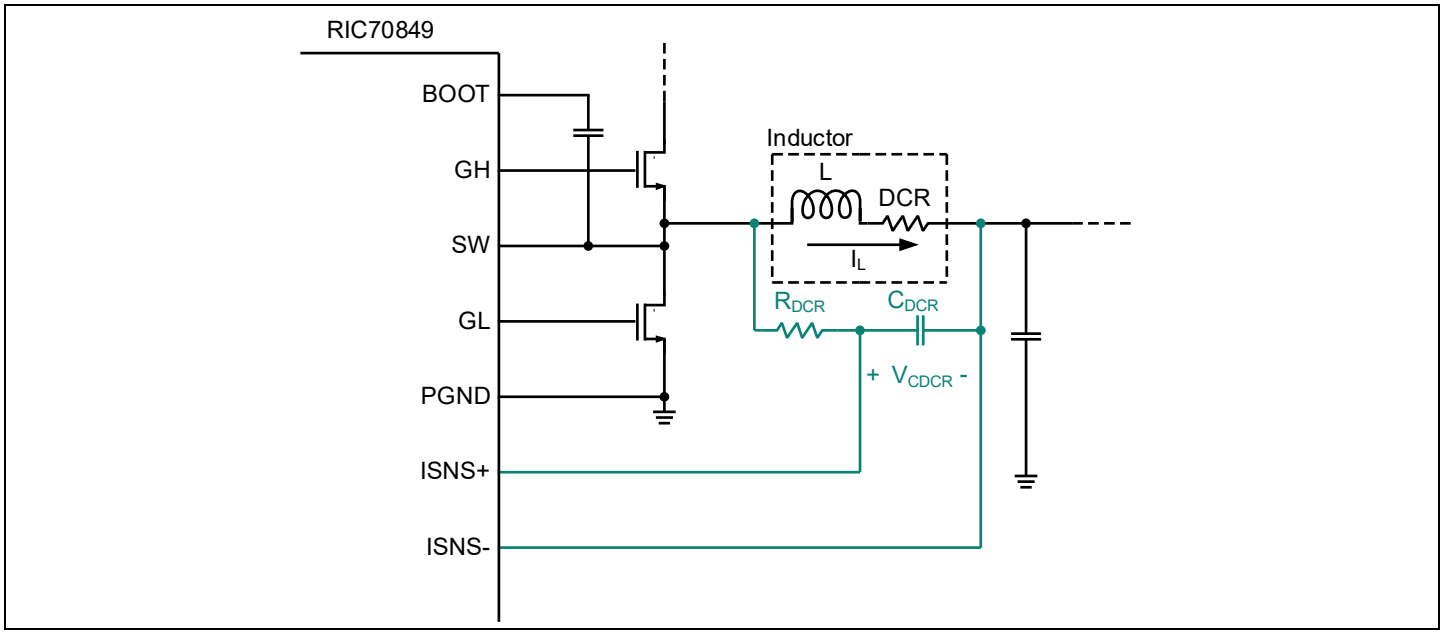


Figure 26 RIC70849 with inductor DCR current sensing

R_{DCR} and C_{DCR} can be calculated from the following equation.

$$R_{DCR} \cdot C_{DCR} = \frac{L}{DCR}$$

Where,

- R_{DCR} is the added resistor in ohms (Ω), recommended resistor value between 1kΩ - 10kΩ
- C_{DCR} is the added capacitor in farads (F)
- L is the inductance of the output inductor in henry (H)
- DCR is the DC winding resistance of the inductor in in ohms (Ω)

The voltage on C_{DCR} (V_{CDCR}) can be calculated with the following equation.

$$V_{CDCR} = I_L \cdot DCR$$

Where,

- V_{CDCR} is the voltage across C_{DCR} in volts (V)
- I_L is the current in the output inductor in amperes (A)
- DCR is the DC winding resistance of the inductor in in ohms (Ω)

For general design guidelines, it is recommended to limit V_{CDCR} so that voltage on ISNS+ and ISNS- do not exceed the absolute maximum limits of these pins.

5.6.2 Slope compensation

Due to the peak current mode control operation, there is the potential for subharmonic oscillation, especially if the duty cycle exceeds 50%. This subharmonic oscillation can cause the duty cycle to have large variation between switching cycles and appear unstable. To eliminate this, RIC70849 features programmable integrated slope compensation. Key waveforms for this integrated slope compensation are shown in Figure 9, where S_n is the on-time ramp slope of the sensed inductor current, S_f is the off-time ramp slope of the sensed inductor current, s_e is the ramp slope of the slope compensation and V_C is the control voltage (output of the compensator).

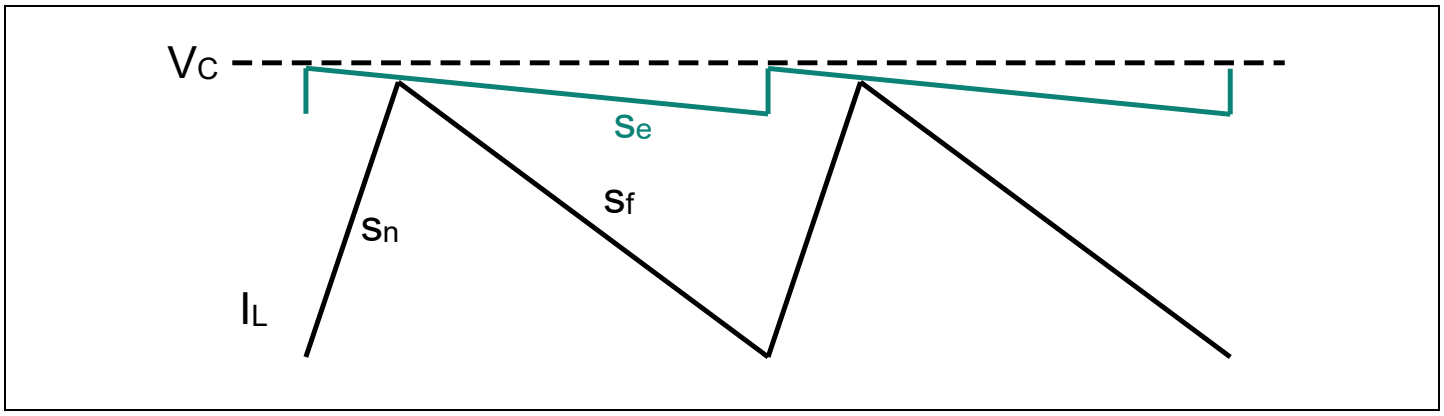


Figure 27 Key waveforms for integrated slope compensation in RIC70849

To maintain stability for a fixed frequency controller where the clock initiates the on time like RIC70849, the following equation is used.

$$\alpha = \frac{S_f - S_e}{S_n + S_e}$$

Where,

- α is the ratio of change of inductor current from one switching cycle to the next, where values greater than 1 represent instability
- S_F is the off-time ramp slope in amperes per microsecond (A/µs)
- S_n is the on-time ramp slope amperes per microsecond (A/µs)
- S_e is the slope of the external ramp (internal to the IC) in amperes per microsecond (A/µs)

If the duty cycle is above 50% (on time is longer than off time) and there is no external ramp (S_e=0), S_F is larger than S_N, resulting in α being greater than 1 and an unstable system. To mitigate this, external slope compensation S_e is added to reduce α below 0.5. Generation of S_e is integrated in RIC70849, where the ramp slope is set with a resistor R_{SLP} from SLP to FB RET and corresponding ramp slope calculated with the following equation

$$s_e = \frac{3{,}600}{R_{SENSE} * R_{SLP}}$$

Where,

- s_e is the slope of the external ramp (internal to RIC70849) in amperes per microsecond (A/µs)
- R_{SENSE} is the current sense resistor in series with the output inductor in ohms (Ω)

- R_{SLP} is the resistor on the SLP pin to FB RET pin in ohms (Ω)

More information on slope compensation, including how these equations and theory were derived, is available in [1].

5.7 Feedback

For output voltage regulation, the sensed output voltage is compared to an internal 600 mV reference voltage through the FB pin. To set the regulated output voltage, a resistor divider is recommended from the output voltage to ground. It is recommended to externally connect all returns for RIC70849 (PGND, AGND, FB RET) at this feedback divider network.

5.7.1 Reference voltage

RIC70849 features a precise 600 mV reference voltage to maintain high accuracy of the output voltage. The two parameters of RIC70849 that account for offset, tolerance of reference voltage V_{REF} and error amplifier (EA) offset voltage V_{OSEA} are combined in a single parameter voltage feedback V_{FB}, which has its own guaranteed minimum and maximum limit in the electrical characteristics. For aspects of design that depend on these tolerances, like output voltage DC regulation accuracy, it is recommended to use the combined parameter V_{FB}.

To improve robustness against single event effects, a 1 nF ceramic capacitor is recommended between VREF pin and FB RET as close to the pins as possible. It is not recommended to apply any external load to this pin.

5.7.2 Compensation

RIC70849 has an integrated transconductance amplifier for the compensation of the outer voltage control loop. The transconductance amplifier has a typical gain g_{mEA} of 1 mS. It can be used with a type 2 compensator, as shown in Figure 10.

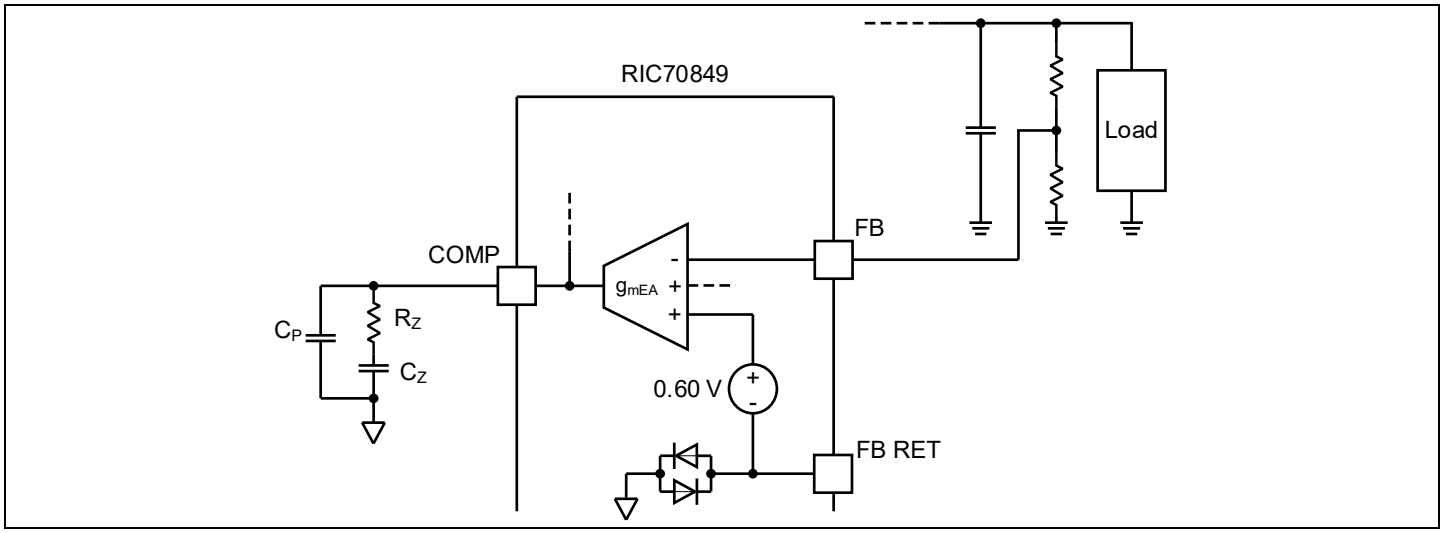


Figure 28 Simplified schematic of RIC70849 compensation with type 2 compensation

5.8 Soft start

RIC70849 features soft start to allows for a monotonic ramp of the output voltage, regardless of any pre-bias voltage on the output, within a programmable time t_{ss}. The soft start functionality works by charging an external capacitor C_{SS} from the SS to FB RET pin with a 10 µA (typical) current source I_{SS}. When the voltage on SS pin is less than the 600 mV reference, the voltage on the soft start pin is used as the reference voltage to regulate the output voltage. Once

the voltage on the SS pin exceeds 600 mV, the internal 600 mV reference takes over and is used for regulation. The capacitance on SS pin to FB RET pin to achieve a desired startup time can be calculated with the following equation.

$$C_{SS} = \frac{t_{ss} \cdot I_{ss}}{V_{ref}} = \frac{t_{ss} \cdot 10\ \mu A}{0.6\ V}$$

Where,

- C_{SS} is the capacitor on SS pin to FB RET pin in farads (F)
- t_{SS} is the desired startup time in seconds (s)
- I_{SS} is the internal current source on the SS pin, which is typically 10 µA
- V_{ref} is the internal reference voltage, which is typically 0.6 V

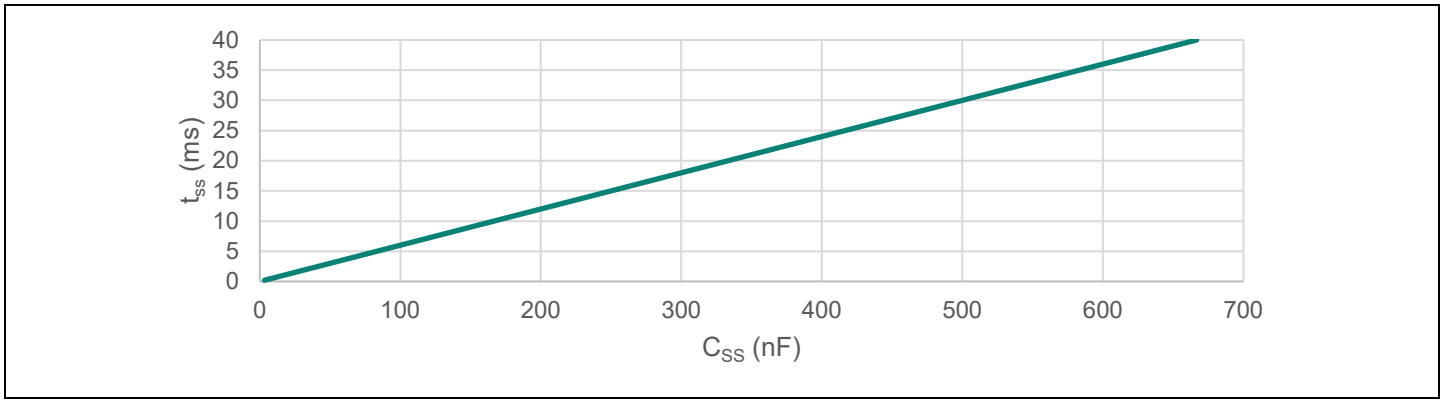


Figure 29 Soft start ramp time t_{ss} vs. SS pin capacitance C_{ss}

5.9 Load-line regulation

Load-line regulation (LLR), also called droop regulation or adaptive voltage positioning (AVP), is an output voltage regulation control technique where the output voltage is adjusted based on the load current. This adjustment in the output voltage reduces the voltage overshoot and undershoot during transient load steps, which can enable a reduction in required output capacitance. For more information on LLR refer to the application note How load-line will help the application.

LLR for RIC70849 works by injecting a current out of the FB pin, which goes through the bottom feedback resistor R_{FBB} to ground. Since RIC70849 regulation forces the voltage on FB pin to stay at the 600 mV reference voltage, this injected current causes the current through the top feedback resistor R_{FBT} to decrease, which correspondingly causes the output voltage to decrease. To achieve LLR, the magnitude of this injected current increases with higher load current as sensed across ISNS+ and ISNS- pins. The magnitude of the output voltage drop from LLR is dependent on the ratio between R_{FBT} and R_{LLR}, which is the resistor on the LLR to AGND pin which sets the magnitude of the current source. Note that when LLR is enabled the feedback resistor divider network may need to be adjusted slightly to account for an output voltage level offset, since “no load” for the design may not be 0 A load as sensed on ISNS+ and ISNS- pins (for example a preload resistor). This can most easily be achieved by reducing the resistance of R_{FBB}.

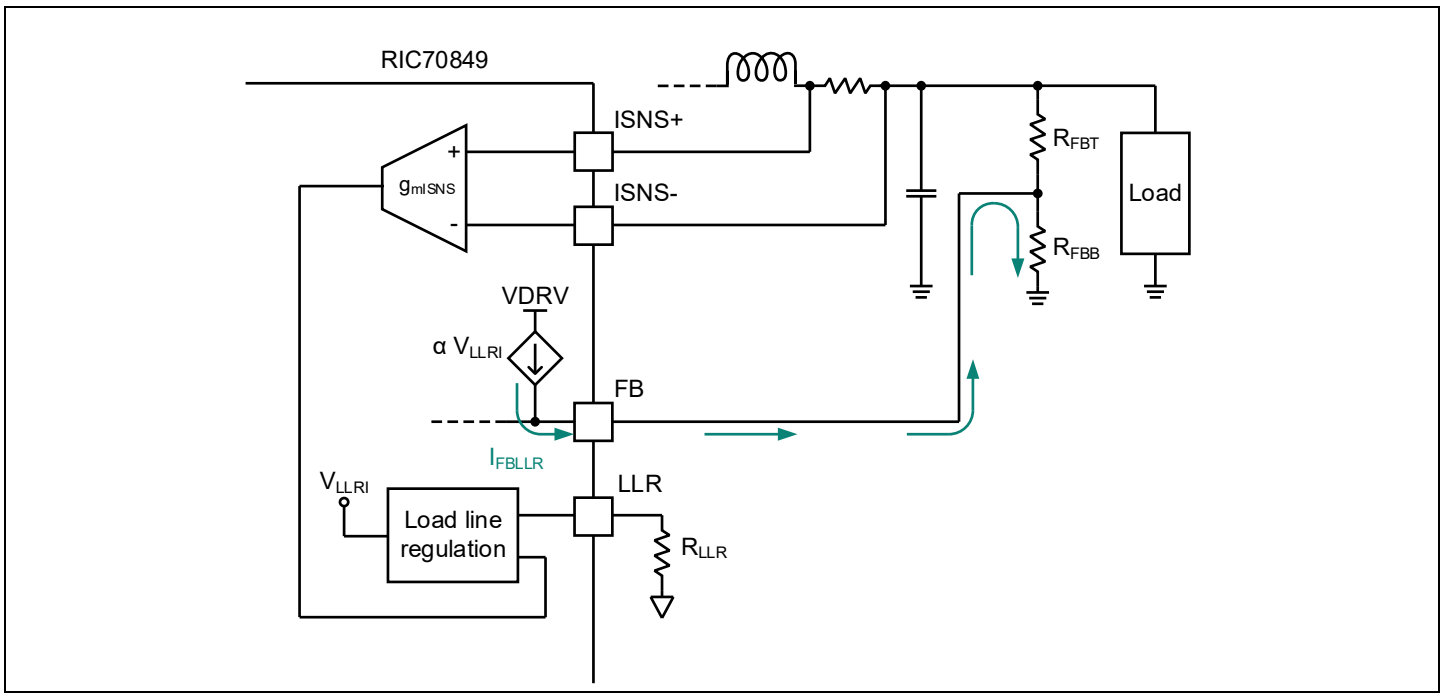


Figure 30 Simplified schematic of LLR operation in RIC70849

The injected current out of the FB pin can be calculated with the following equation.

$$I_{FBLLR} = \frac{6.665 \cdot R_{SENSE} \cdot I_L}{16 \cdot R_{LLR}}$$

Where,

- I_{FBLLR} is the current out of the FB pin from the LLR circuit in amperes (A)
- R_{SENSE} is the current sense resistor in series with the output inductor in ohms (Ω)
- I_L is the desired output overcurrent limit in amperes (A)
- R_{LLR} is the resistor on the LLR pin to AGND pin in ohms (Ω)

With I_{FBLLR}, the change in output voltage can be calculated with the following equation

$$V_{OUTOS} = I_{FBLLR} \cdot R_{FBT}$$

Where,

- V_{OUTOS} is the shift in output voltage in volts (V)
- R_{FBT} is the top resistor in the output resistor divider network in ohms (Ω)

Alternately, the desired load-line resistance can be calculated with the following equation

$$LL = \frac{R_{SENSE} \cdot R_{FBT}}{1.2 \cdot R_{LLR}}$$

Where,

- LL is the desired load line resistance in ohms (Ω)
- R_{SENSE} is the current sense resistor in series with the output inductor in ohms (Ω)
- R_{FBT} is the top resistor in the output resistor divider network in ohms (Ω)

- R_{LLR} is the resistor on the LLR pin to AGND pin in ohms (Ω)

For best operation of LLR, it is recommended to select R_{FBB} resistance value that is less than around 25 kΩ. Additionally, the internal LLR bandwidth is 250 kHz. It is recommended that the outer voltage loop control bandwidth is below 250 kHz, otherwise the LLR operation will cause additional ringing during load steps.

If LLR operation is not desired, LLR can be disabled by leaving the LLR pin open circuit. This will disable the injected current source on the FB pin. In this case the LLR pin is still electrically connected to internal circuitry, so it is not floating metal. If output voltage regulation is desired at 0.6 V and FB is connected directly to the output voltage, LLR feature can still be implemented with a R_{FBT} resistor, while the bottom feedback resistor is not populated.

5.10 Fault protections

RIC70849 features multiple integrated fault protections, which are summarized in Table 8. Fault protections include VIN undervoltage lockout (UVLO), VIN overvoltage (OVP), VDRV undervoltage lockout (VDRV UVLO), output voltage overvoltage (VOUT OVP), overcurrent protection (OCP), negative overcurrent protection (NOCP), overtemperature protection (OTP) and loss of SYNCI signal.

Table 8 Fault response summary

Fault type	Description	Response
VIN UVLO	Voltage on VIN pin decreases below UVLO threshold	Shutdown (GH and GL both go low) until VIN voltage increases above UVLO turn on, then attempt startup with soft start sequence
VIN OVP	Voltage on VIN pin exceeds OVP threshold	Shutdown (GH and GL both go low) until voltage on VIN reduces below OVP falling threshold, then attempt startup with soft start sequence
VDRV UVLO	Voltage on VDRV pin decreases below UVLO threshold	Shutdown (GH and GL both go low) until VDRV voltage increases above UVLO turn on, then attempt startup with soft start sequence
VOUT OVP	Overvoltage threshold on FB pin exceeded	Shutdown (GH and GL both go low) then attempt startup with soft start sequence
OCP	Sensed current from ISNS+ to ISNS- pin exceeds positive limit set on OCP pin	Truncate PWM pulse for current switching cycle (GH goes low, GL goes high), continue normal operation for next switching cycle
NOCP	Sensed current from ISNS+ to ISNS- pin exceeds negative limit set on OCP pin	Truncate GL for current switching cycle (GL goes low), continue normal operation for next switching cycle
OTP	Junction temperature exceeds T_{SD}	Shutdown (GH and GL both go low) until die temperature reduces by $T_{HYS,}$ then attempt startup with soft start sequence
Loss of SYNCI signal	While in follow mode lose signal on SYNCI	Run at frequency of internal oscillator set by resistor on RT pin

5.10.1 Overcurrent protection

The threshold for OCP is set with a resistor from OCP to FB RET. Similar to the current sense for the control loop, the current sense for OCP is sensed from the ISNS+ to ISNS- pins to a transconductance amplifier with a gain g_{mISNS} of 333 µS. The output of this transconductance amplifier is connected to the OCP pin, where a resistor R_{OCP} on the OCP pin will convert the output to a voltage. This voltage is compared to V_{OCP}, and if the voltage exceeds V_{OCP} the switching

cycle is truncated for that switching cycle from OCP protection. The same output is compared to V_{NOCP}, and if the voltage exceeds V_{NOCP} the GL gate drive is truncated for that switching cycle from NOCP protection. The resistor R_{OCP} sets the overall gain of the overcurrent protection current sense amplifier and corresponding overcurrent limit.

5.10.1.1 OCP with current sense resistor

For current sense resistor sensing, the following equation can be used to determine the R_{OCP}, where I_{OCP} is the desired peak current limit and R_{SENSE} is the current sense resistor resistance.

$$R_{OCP} = \frac{V_{OCP}}{(333\ \mu S \cdot R_{SENSE} \cdot I_{OCP}) + 30\ \mu A}$$

Where,

- R_{OCP} is the resistor on the OCP pin to FB RET pin in ohms (Ω)
- V_{OCP} is the internal threshold voltage which exceeding results in OCP protection in volts (V)
- R_{SENSE} is the current sense resistor in series with the output inductor in ohms (Ω)
- I_{OCP} is the peak inductor current that triggers OCP in amperes (A)

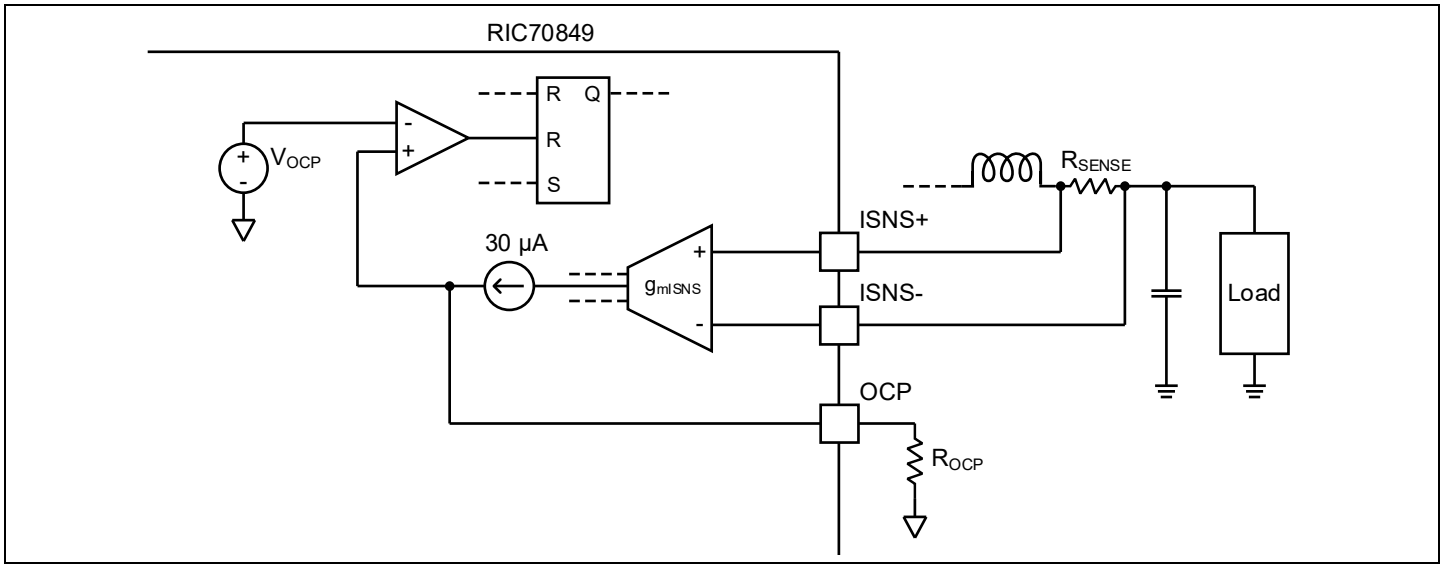


Figure 31 Simplified schematic of RIC70849 overcurrent protection with current sense resistor, with offset current of 30 µA shown externally for clarity

5.10.1.2 OCP with DCR sensing

For DCR current sensing, the following equation can be used to determine the R_{OCP}, where I_{OCP} is the desired peak current limit and V_{CDCR} is the sensed voltage across the DCR sensing capacitor. Calculations for the DCR current sensing resistor R_{DCR} and capacitor C_{DCR} are in section 5.6.1.3.

$$R_{OCP} = \frac{V_{OCP}}{(333\ \mu S \cdot V_{CDCR}) + 30\ \mu A}$$

$$V_{CDCR} = I_{OCP} \cdot DCR$$

Where,

- R_{OCP} is the resistor on the OCP pin to FB RET pin in ohms (Ω)
- V_{OCP} is the internal threshold voltage which exceeding results in OCP protection in volts (V)
- V_{CDCR} is the voltage across C_{DCR} in volts (V)
- DCR is the DC winding resistance of the inductor in in ohms (Ω)
- I_{OCP} is the peak inductor current that triggers OCP in amperes (A)

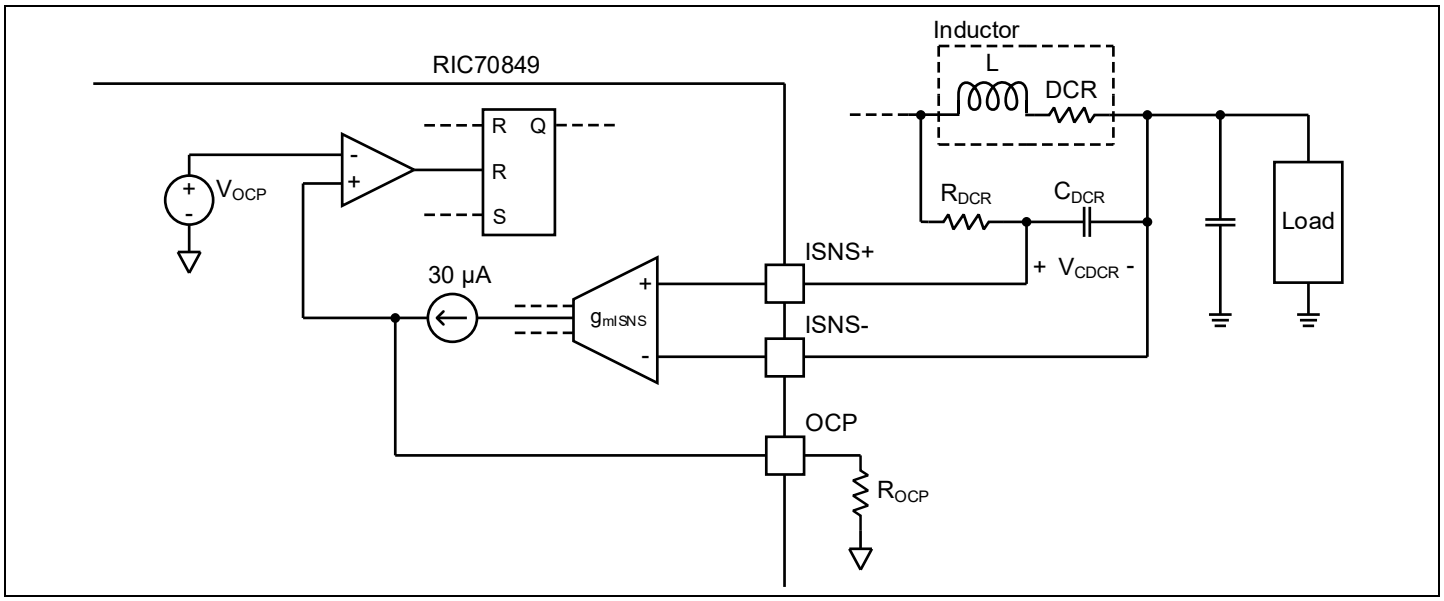


Figure 32 Simplified schematic of RIC70849 overcurrent protection with DCR sensing, with offset current of 30 µA shown externally for clarity

5.11 Power good

RIC70849 has a power good signal from the PG pin. This pin is an open drain configuration, where the pin is actively pulled to AGND when any of the following criteria are met.

- Fault VIN UVLO, VIN OVP, VDRV UVLO, VOUT OVP or OTP active
- Operation disabled by pulling EN pin low
- Sensed output voltage exceeds limits

When none of the event criteria are met, the PG pin is high impedance. It can be connected to an external voltage source, such as VDRV, with a pull up resistor, to create a logic high signal.

5.12 Enable

RIC70849 operation can be externally controlled with the EN pin. If this pin is held low, PWM operation is disabled with both GL and GH held low and voltage on SS pin discharged. If the voltage on the EN pin is above V_{EN}, RIC70849 initiates a soft start sequence and operates as expected. There is hysteresis on EN threshold to prevent chatter during state change. If there is no external voltage to apply on EN pin, or EN functionality is not desired, EN pin can be connected to VDRV through a pull up resistor.

6 Application information and additional details

6.1.1 Two phase operation

RIC70849 can synchronize with other RIC70849 for two phase operation, where one RIC70849 acts in a master/leader mode and another RIC70849 operates in slave/follower mode. The master/leader RIC70849 sets the switching frequency and performs the outer voltage loop regulation. The slave/follower RIC70849 follows the switching frequency and duty cycle set by the master/leader RIC70849, but it performs its own inner current control and fault protection.

RIC70849 can be configured to work in two phase mode with the following

- SYNCO pin of master/leader RIC70849 is connected to SYNCI pin of follower/slave RIC70849
- SS pin of master/leader RIC70849 is connected to SS pin of follower/slave RIC70849
- COMP pin of master/leader RIC70849 is connected to COMP pin of follower/slave RIC70849
- FB pin of follower/slave RIC70849 is connected to VREF pin of follower/slave RIC70849

An example schematic of two RIC70849 configured in 2 phase operation is shown in Figure 15.

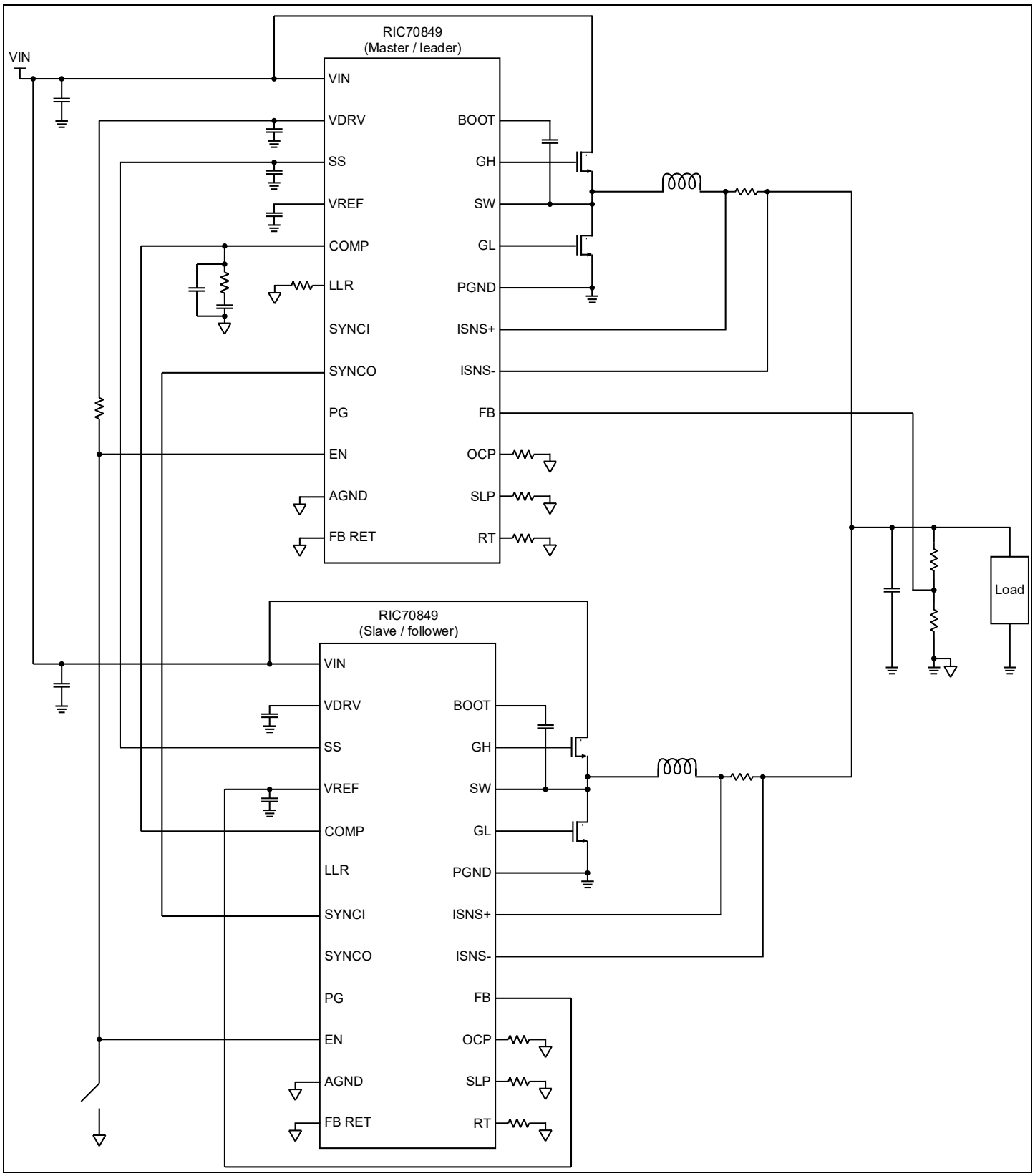


Figure 33 Simplified schematic of two-phase stand-alone operation

6.2 Power sequencing

The PG and EN pins of RIC70849 are rated such that they can be connected in tandem for power sequencing, where the PG pin of one RIC70849 can drive the EN pin of another RIC70849.

6.3 Recommended layout

To achieve high performance a good PCB layout is required. A poor layout can introduce parasitic inductance and capacitance, which couple with electrical noise that interferes with operation. Below are some recommendations to reduce these undesired effects.

1. For the bypass capacitor for power rails VIN to PGND, VDRV to PGND and BOOT to SW, use a ceramic capacitor and place as close to the pins as possible
2. For external FETs, place as close to their respective gate drive output and gate drive return as possible (high side FET with GH, SW and low side FET with GL, PGND)
3. For bypass capacitor for VREF, place as close as possible to VREF and FB RET pins
4. If current sense resistor is used, place the resistor on the output side of the inductor (between the inductor and output capacitors) to reduce noise on signal and peak voltage applied to ISNS+ and ISNS- pins
5. Externally connect returns PGND, AGND and FB RET at feedback network, which is as close to the load as possible to improve output voltage regulation accuracy over load
6. Use a mix of tantalum and ceramic capacitors for output capacitance, especially if there is a transient load step with high slew rate

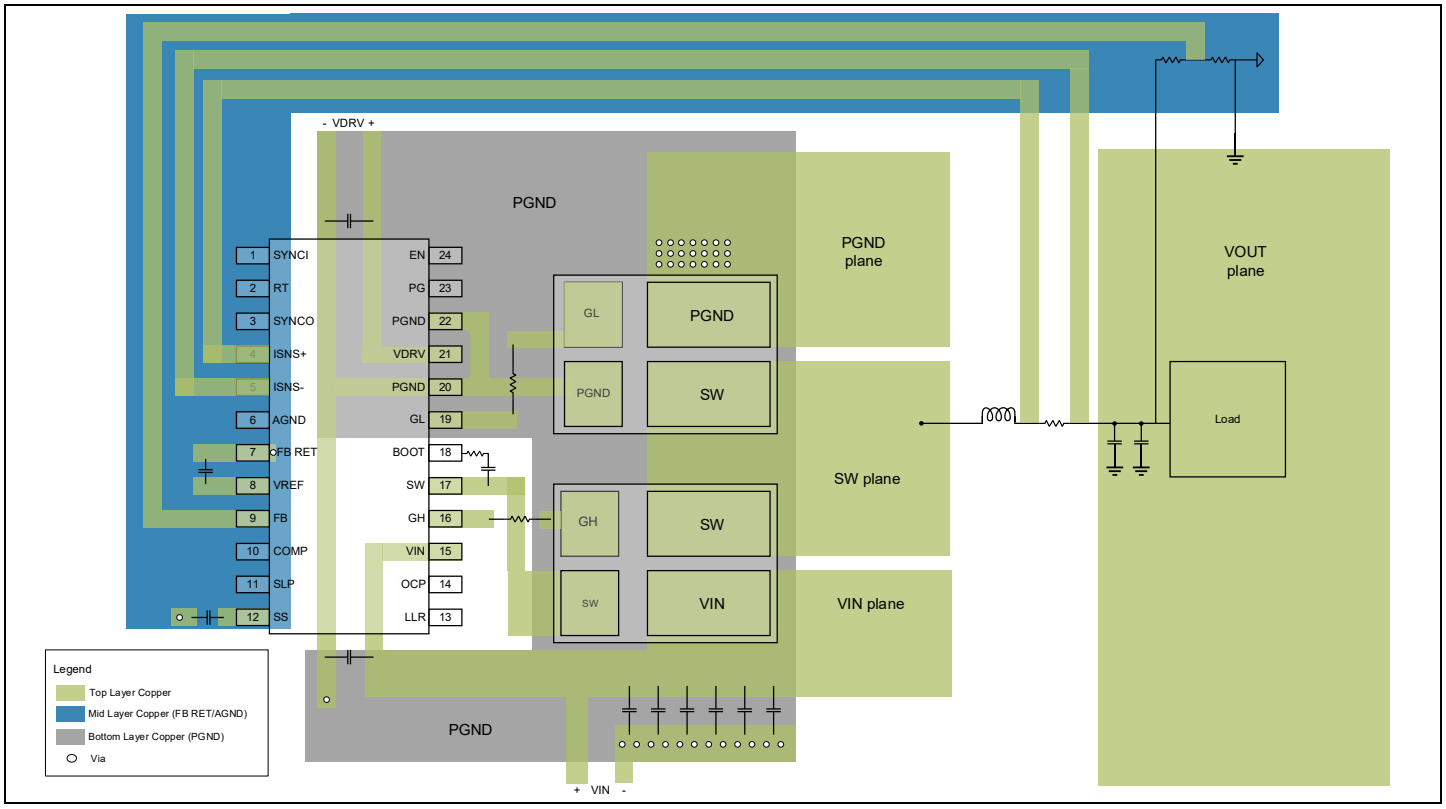
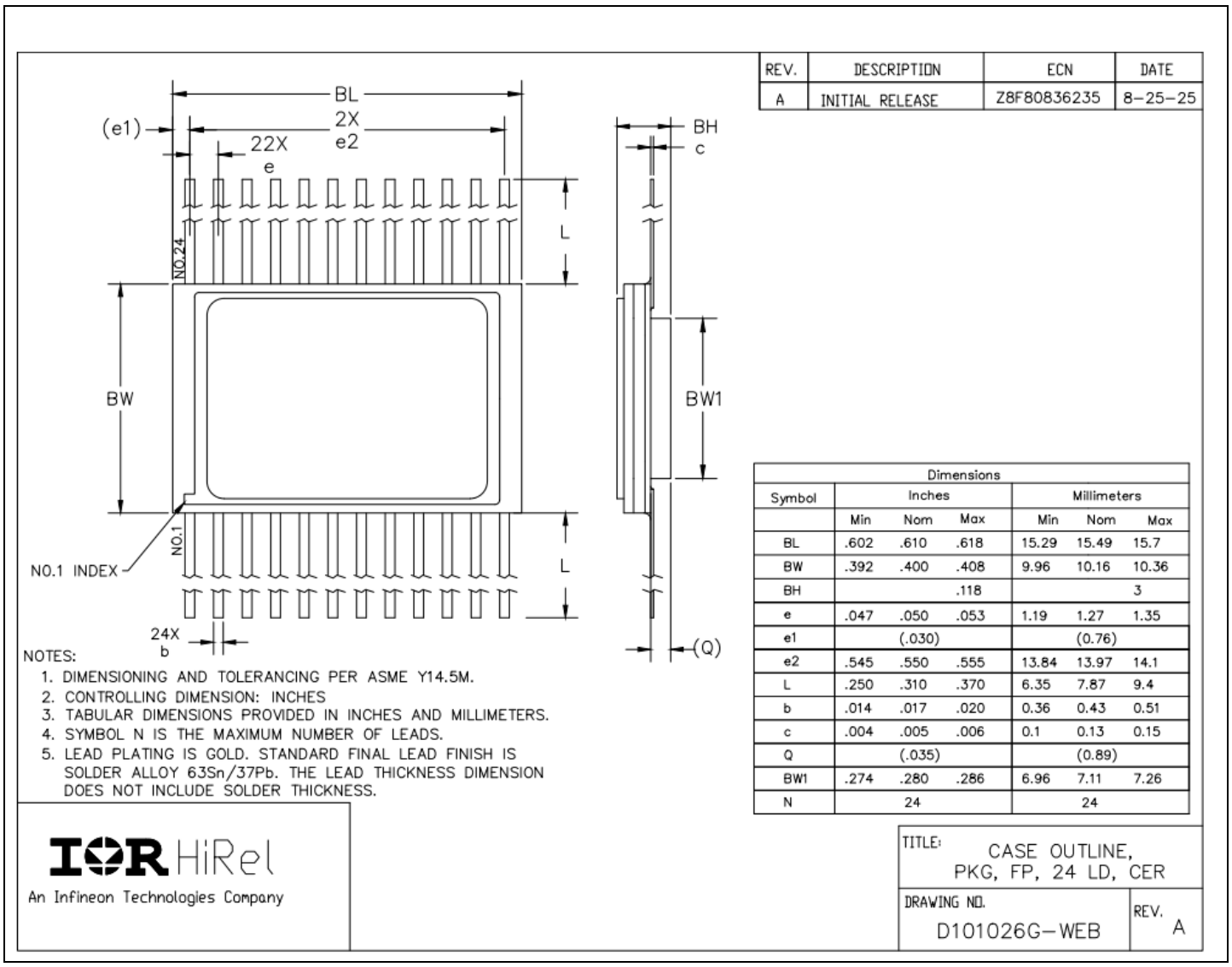


Figure 34 Recommended PCB layout for RIC70849

7 Package details

7.1 Flatpack

For our latest package drawing please refer to 24 Pin Hermetic Flatpack.



Dimensions						
Symbol	Inches			Millimeters		
	Min	Nom	Max	Min	Nom	Max
BL	.602	.610	.618	15.29	15.49	15.7
BW	.392	.400	.408	9.96	10.16	10.36
BH			.118			3
e	.047	.050	.053	1.19	1.27	1.35
e1		(.030)			(0.76)	
e2	.545	.550	.555	13.84	13.97	14.1
L	.250	.310	.370	6.35	7.87	9.4
b	.014	.017	.020	0.36	0.43	0.51
c	.004	.005	.006	0.1	0.13	0.15
Q		(.035)			(0.89)	
BW1	.274	.280	.286	6.96	7.11	7.26
N		24			24	

Figure 35 24-lead flatpack package outline

Revision history

Document revision	Date	Description of changes
1.0	07/13/2026	Initial revision

References

[1] R.B. Ridley, “A New Small-Signal Model for Current-Mode Control”, PhD Dissertation, Virginia Polytechnic Institute and State University, November

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