

RDHA701CD10A2NX

PD-97578C

Radiation Hardened Dual Solid State Relay 100V, 1.0A, R5 Technology

Features

- Total dose capability to 100kRads(Si)
- Optically coupled
- 1000VDC input-to-output, channel-to-channel, and pin-to-case isolation
- Hermetically sealed
- Ceramic package

Typical applications

- Solar array management, heater controls, bus switching, ground power isolation, generic load switching

Product validation

Screened to MIL-PRF-38534, and meets Qualification Conformance Inspection per MIL-PRF-38534 for Class K product

Description

The RDHA701CD10A2NX is a radiation hardened dual Solid State Relay in a hermetic package. It is configured as dual single pole single throw (SPST) normally open relay. This device is characterized for 100KRad (Si) total ionizing dose. The output MOSFET utilizes IR HiRel R5 technology.

Ordering Information

Table 1 **Ordering options**

Part number	Package	Screening Level	TID Level
RDHA701CD10A2NX	8 Pin Ceramic	Class K	100krad(Si)

Product Summary

- **Part number:** RDHA701CD10A2NX
- **Radiation level:** 100 kRads (Si)
- **Configuration:** Dual DC
- **Voltage:** 100V
- **I_b:** 1.0A



RDHA701CD10A2NX

Radiation Hardened Dual Solid State Relay

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Absolute Maximum Ratings

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Value	Unit
Output Withstand Voltage	$V_{O(OFF)}$	100	V
Output Current ¹	I_O	1.0	A
Input Forward Current	I_F	40	mA
Peak Input Forward Current ($t \leq 1.0\text{ms}$)	$I_{F(pk)}$	100	
Peak Input Reverse Voltage ($t \leq 1.0\text{ms}$)	V_R	5.0	V
Power Dissipation	P_{DISS}	1.0	W
Operating Temperature Range	T_J	-55 to +125	$^\circ\text{C}$
Storage Temperature Range	T_S	-65 to +150	
Lead Temperature (soldering $\leq 10\text{sec}$)	T_L	300	
Weight		0.8 (Typical)	g

¹ While the SSR design meets the design, requirements specified in MIL-PRF-38534, the end user is responsible for product derating as applicable for the application.

Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics (Per Channel)

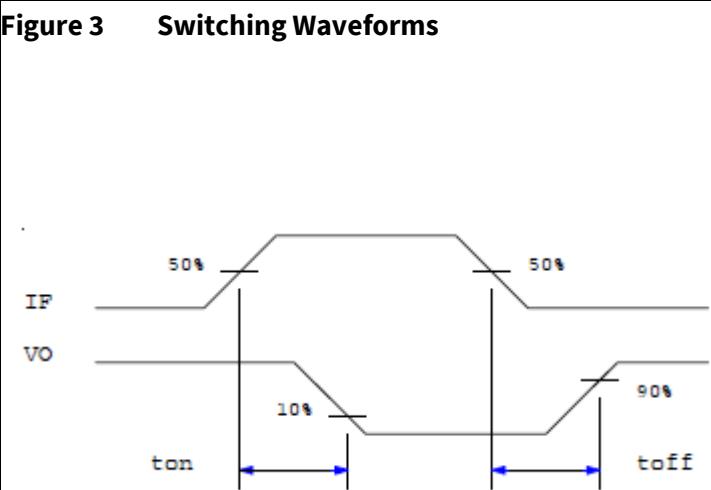
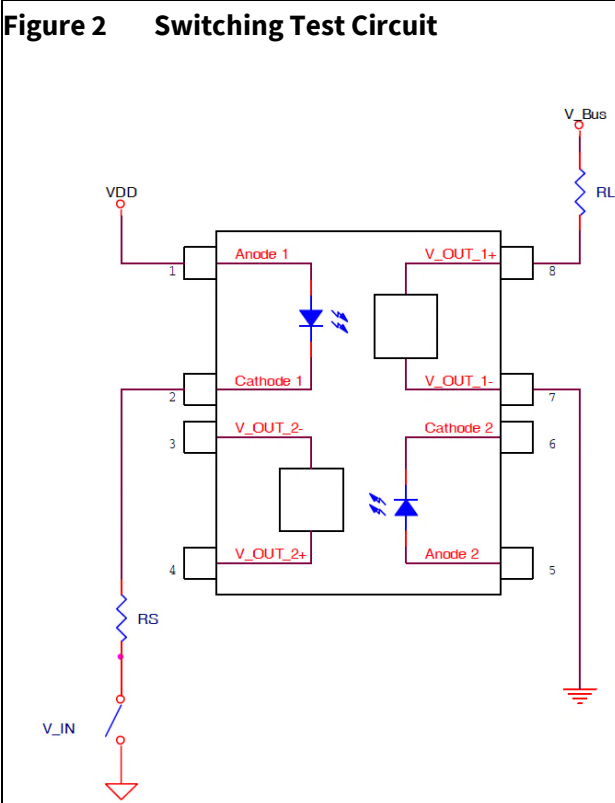
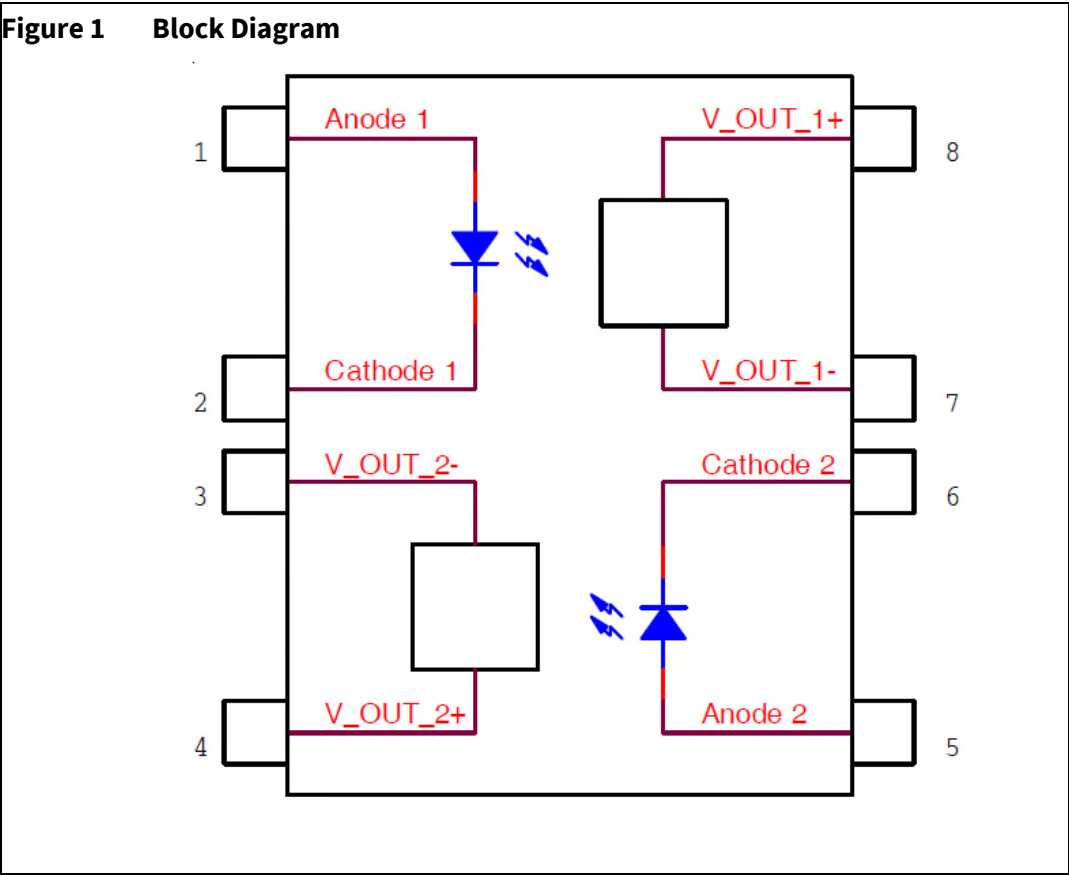
Table 3 Electrical Characteristics per Channel @ $-55^{\circ}\text{C} \leq T_c \leq +125^{\circ}\text{C}$ (Unless Otherwise Specified) ¹

Parameter	Group A Subgroups	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Output On-Resistance	1	$I_F = 10\text{mA}$, $I_O = 1.0\text{A}$	$R_{DS(ON)}$	—	0.25	0.40	Ω
	2			—	0.39	0.80	
Output Leakage Current	1	$I_F = 0$, $V_{OUT} = 100\text{V}$	I_O	—	—	10	μA
	2			—	—	25	
Input Forward Voltage	1, 2, 3	$I_F = 10\text{mA}$	V_F	1.0	—	1.85	V
Input-to-Output Leakage Current	1	$V_{I-O} = 1000\text{Vdc}$, dwell = 5s	I_{I-O}	—	—	1.0	μA
Channel-to-Channel Leakage Current			I_{CH-CH}				
Pin-to-Case Leakage Current			I_{CASE}				
Turn-On Time ^{3 4 5 6}	9, 10, 11	$I_F = 0$ to 10mA , $V_{BUS} = 28\text{V}$, $I_O = 1.0\text{A}$, Duty Cycle $\leq 1.0\%$	t_{on}	—	—	4.0	ms
Turn-Off Time ^{2 3 4 5}	9, 10, 11	$I_F = 10\text{mA}$ to 0 , $V_{BUS} = 28\text{V}$, $I_O = 1.0\text{A}$, Duty Cycle $\leq 1.0\%$	t_{off}	—	—	2.0	
Output Capacitance ⁷		$I_F = 0$, $V = +25\text{V}$, $f = 1\text{MHz}$, $T_c = 25^{\circ}\text{C}$	C_{OSS}	—	110	—	pF
Thermal Resistance ⁶		Per Channel	R_{THJC}	—	—	15	$^{\circ}\text{C/W}$
MTBF		MIL-HDBK-217F, SF@ $T_c = 25^{\circ}\text{C}$		22.7	—	—	MHrs

¹ IR HiRel does not currently have a DLA Certified Radiation Hardness Assurance Program.² Turn-On Time (t_{on}) includes the turn-on delay and rise time; Turn-Off Time (t_{off}) includes the turn-off delay and fall time.³ Reference Fig. 2 for Switching Test Circuits and Fig. 3 for Switching Test Wave Form.⁴ Optically coupled Solid State Relays (SSRs) have relatively slow turn on and turn off times. Care must be taken to ensure that transient currents do not cause a violation of SOA. If transient conditions are present, IR HiRel recommends a complete simulation to be performed by the end user to ensure compliance with SOA requirements as specified in the IRHQ57110 datasheet.⁵ Rise and fall time are controlled internally.⁶ Specification is guaranteed by design.

Test Circuits

3 Test Circuits

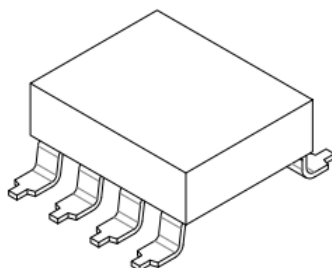


4 Package Outline

Note: For the most updated package outline, please see the website: [Package \(8 Pin Ceramic\)](#)

NOTES:

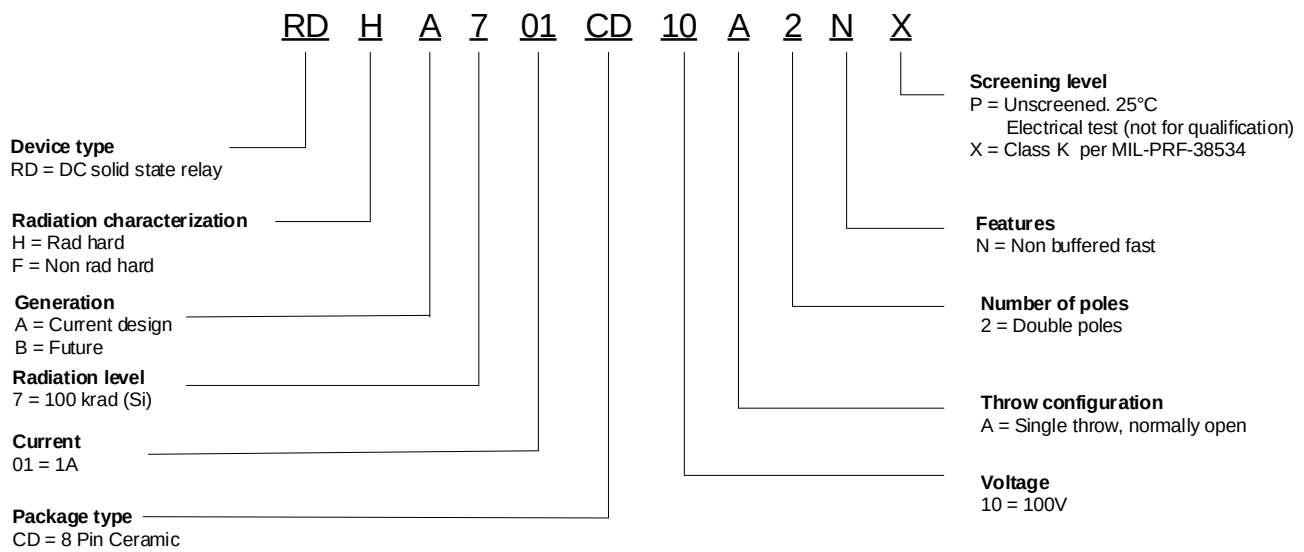
1. DIMENSIONING AND TOLERANCING PER
ASME Y14.5SM-1994
2. CONTROLLING DIMENSION: INCH
3. DIMENSIONS ARE IN INCHES [MILLIMETERS]
4. TOLERANCES ARE $\pm .005$ [0.13] UOS
5. STANDARD FINAL FINISH ON ALL TERMINALS
IS SOLDER ALLOY Sn/Pb



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TITLE: CASE OUTLINE: 8 PIN CERAMIC	
DRAWING NO. D100931G-WEB	REV C

5 Part Numbering Nomenclature



Revision history**Revision history**

Document version	Date of release	Description of changes
	10/19/2010	Final datasheet
Rev A	10/26/2010	Updated Package Picture with IR logo –page1
Rev C	05/25/2012	Updated per ECN-1120-00458
Rev C	09/02/2021	Updated per ECN-1120-8644

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Document reference

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