

IRF9130 (JANTX2N6804)

PD-90549F

**Repetitive Avalanche and dv/dt Rated Power MOSFET
Thru-Hole (TO-204AA)
-100V, -11A, P-channel**

Features

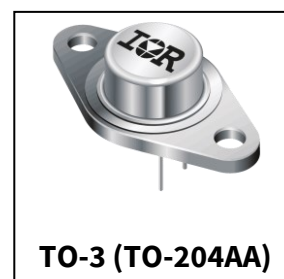
- Repetitive avalanche ratings
- Dynamic dv/dt rating
- Hermetically sealed
- Simple drive requirements
- ESD rating: Class 1C per MIL-STD-750, Method 1020

Potential Applications

- DC-DC converter
- Motor drives

Product Summary

- **BV_{DSS}** : -100V
- **I_D** : -11A
- **$R_{DS(on),max}$** : 0.30 Ω
- **$Q_{G,max}$** : 29nC
- **REF**: MIL-PRF-19500/562



Product Validation

Qualified to JANTX screening flow according to MIL-PRF-19500 for high-reliability applications

Description

HEXFET POWER MOSFET technology is the key to IR HiRel advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest “State of the Art” design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability. The HEXFET transistors also feature all of the well-established advantages of MOSFETs such as voltage control, very fast switching and temperature stability of the electrical parameters. They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

Ordering Information

Table 1 **Ordering options**

Part number	Package	Screening Level
IRF9130	TO-3 (TO-204AA)	COTS
JANTX2N6804	TO-3 (TO-204AA)	JANTX
JANTXV2N6804	TO-3 (TO-204AA)	JANTXV

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Absolute Maximum Ratings

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = -10V, T_C = 25^{\circ}C$	Continuous Drain Current	-11	A
$I_{D2} @ V_{GS} = -10V, T_C = 100^{\circ}C$	Continuous Drain Current	-7.0	A
$I_{DM} @ T_C = 25^{\circ}C$	Pulsed Drain Current ¹	-44	A
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.60	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ²	207	mJ
I_{AR}	Avalanche Current ¹	-11	A
E_{AR}	Repetitive Avalanche Energy ¹	7.5	mJ
dv/dt	Peak Diode Reverse Recovery ³	-5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	
	Weight	11.5 (Typical)	

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² $V_{DD} = -25V$, starting $T_J = 25^{\circ}C$, $L = 3.4mH$, Peak $I_L = -11A$, $V_{GS} = -10V$

³ $I_{SD} \leq -11A$, $di/dt \leq -140A/\mu s$, $V_{DD} \leq -100V$, $T_J \leq 150^{\circ}C$

Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics

Table 3 Static and Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	$V_{GS} = 0V, I_D = -1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.087	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.30	Ω	$V_{GS} = -10V, I_{D2} = -7.0A^1$
		—	—	0.36		$V_{GS} = -10V, I_{D2} = -11A^1$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	$V_{DS} = -80V, V_{GS} = 0V$
		—	—	-250		$V_{DS} = -80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Leakage Reverse	—	—	100		$V_{GS} = 20V$
Q_G	Total Gate Charge	—	—	29	nC	$I_{D1} = -11A$ $V_{DS} = -50V$ $V_{GS} = -10V$
Q_{GS}	Gate-to-Source Charge	—	—	7.1		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	21		
$t_{d(on)}$	Turn-On Delay Time	—	—	60	ns	$I_{D1} = -11A^{**}$ $V_{DD} = -50V$ $R_G = 7.5\Omega$ $V_{GS} = -10V$
t_r	Rise Time	—	—	140		
$t_{d(off)}$	Turn-Off Delay Time	—	—	140		
t_f	Fall Time	—	—	140		
$L_S + L_D$	Total Inductance	—	6.1	—	nH	Measured from Drain lead (6mm/0.25 in from package) to Source lead (6mm/0.25 in from package)
C_{iss}	Input Capacitance	—	860	—	pF	$V_{GS} = 0V$ $V_{DS} = -25V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	350	—		
C_{rss}	Reverse Transfer Capacitance	—	125	—		

****** Switching speed maximum limits are based on manufacturing test equipment and capability.

¹ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Device Characteristics

2.2 Source-Drain Diode Ratings and Characteristics

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-11	A	
I _{SM}	Pulsed Source Current (Body Diode) ¹	—	—	-44	A	
V _{SD}	Diode Forward Voltage	—	—	-4.7	V	T _J = 25°C, I _S = -11A, V _{GS} = 0V ²
t _{rr}	Reverse Recovery Time	—		250	ns	T _J = 25°C, I _F = -11A, V _{DD} ≤ -50V di/dt = -100A/μs ²
Q _{rr}	Reverse Recovery Charge	—	2.0	—	μC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	1.67	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	—	—	30	

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² Pulse width $\leq 300 \mu\text{s}$; Duty Cycle $\leq 2\%$

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Electrical Characteristics Curves

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Electrical Characteristics Curves

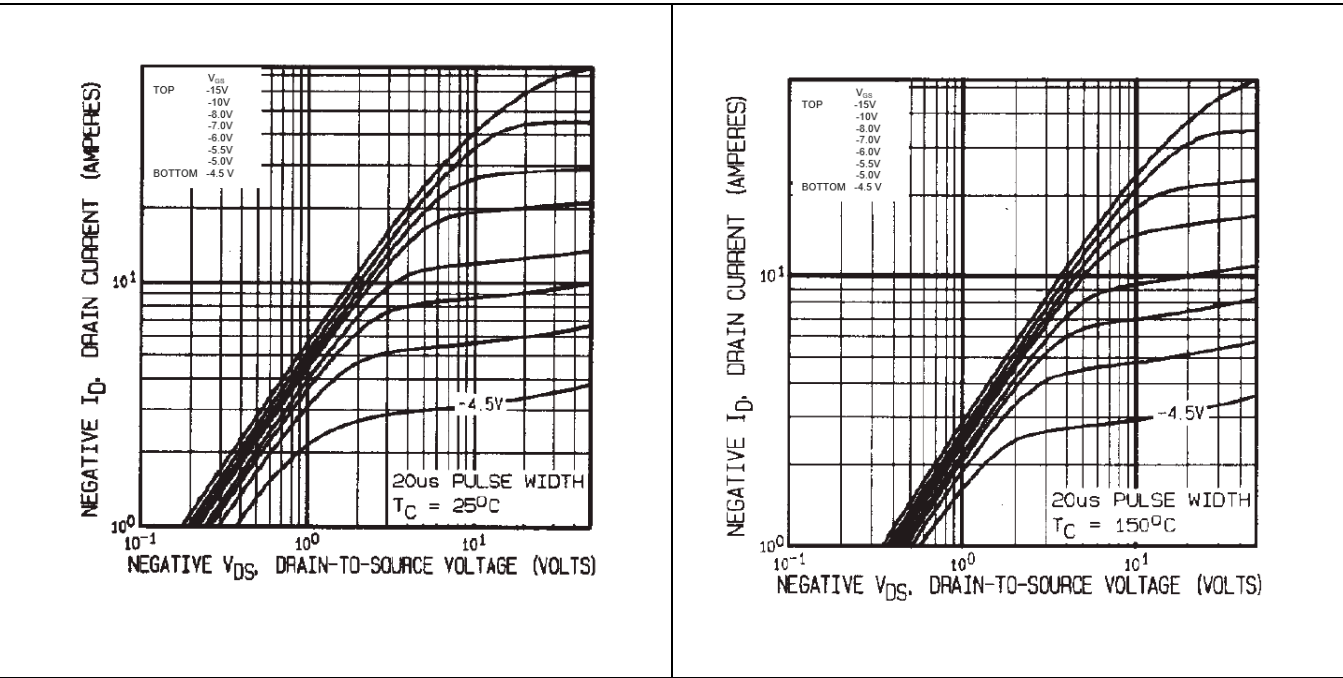


Figure 1 Typical Output Characteristics

Figure 2 Typical Output Characteristics

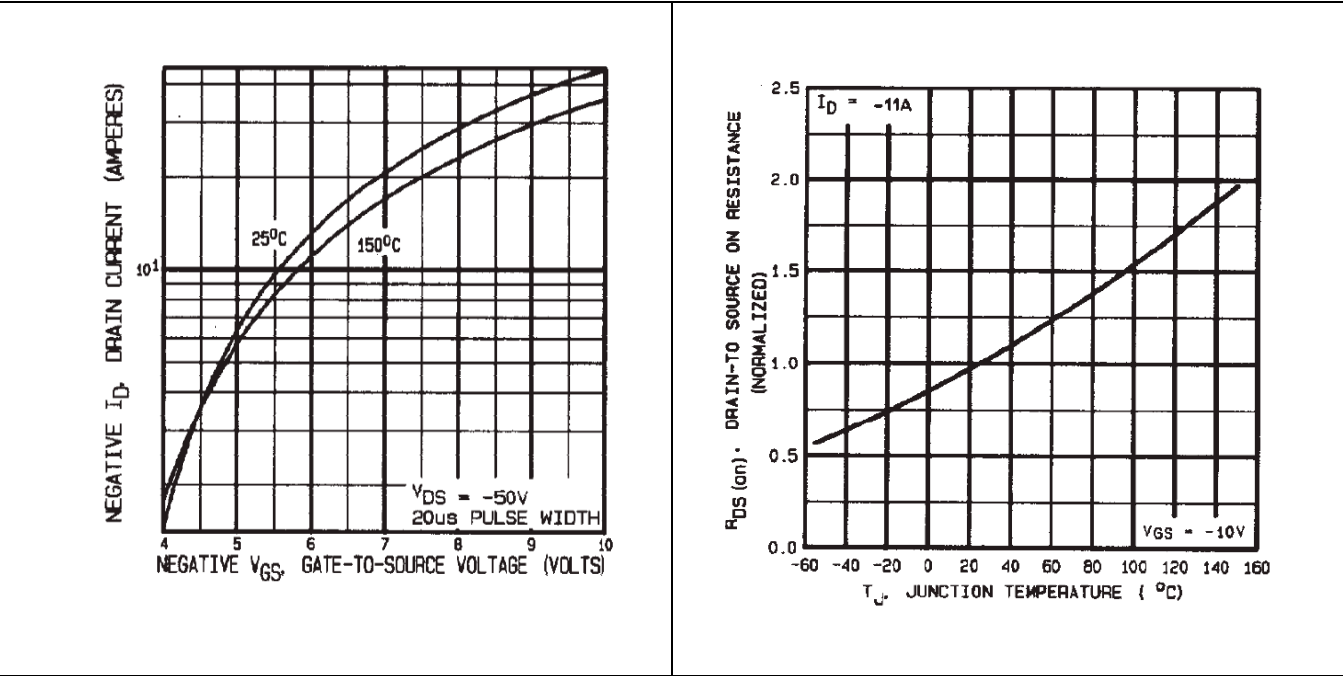


Figure 3 Typical Transfer Characteristics

Figure 4 Normalized On-Resistance Vs. Temperature

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Electrical Characteristics Curves

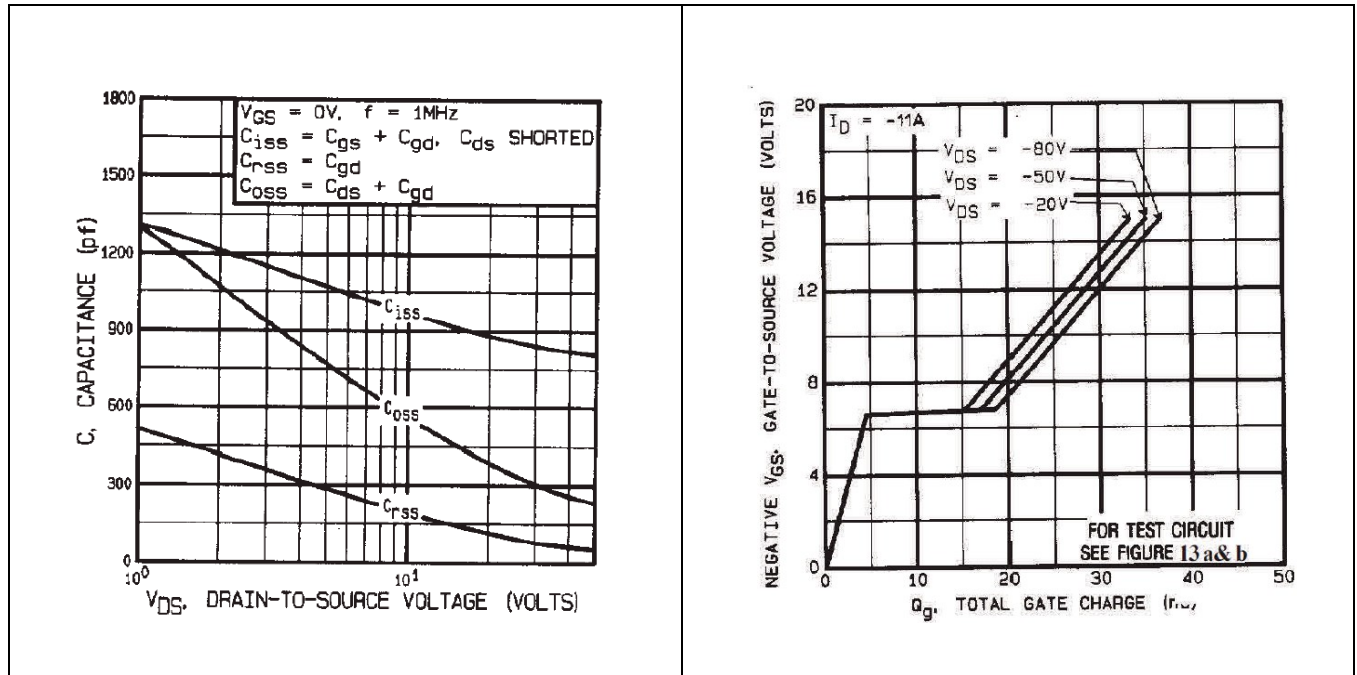


Figure 5 Typical Capacitance Vs. Drain-to-Source Voltage

Figure 6 Typical Gate Charge Vs. Gate-to-Source Voltage

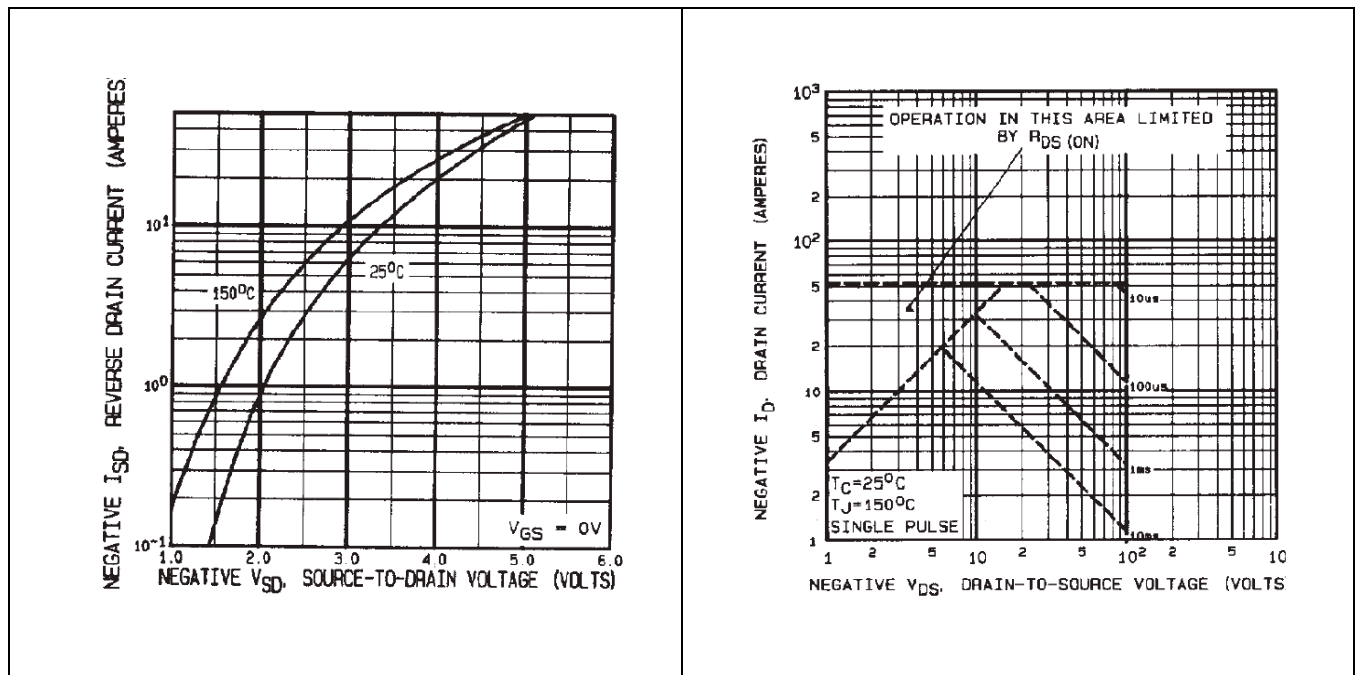


Figure 7 Typical Source-Drain Diode Forward Voltage

Figure 8 Maximum Safe Operating Area

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Electrical Characteristics Curves

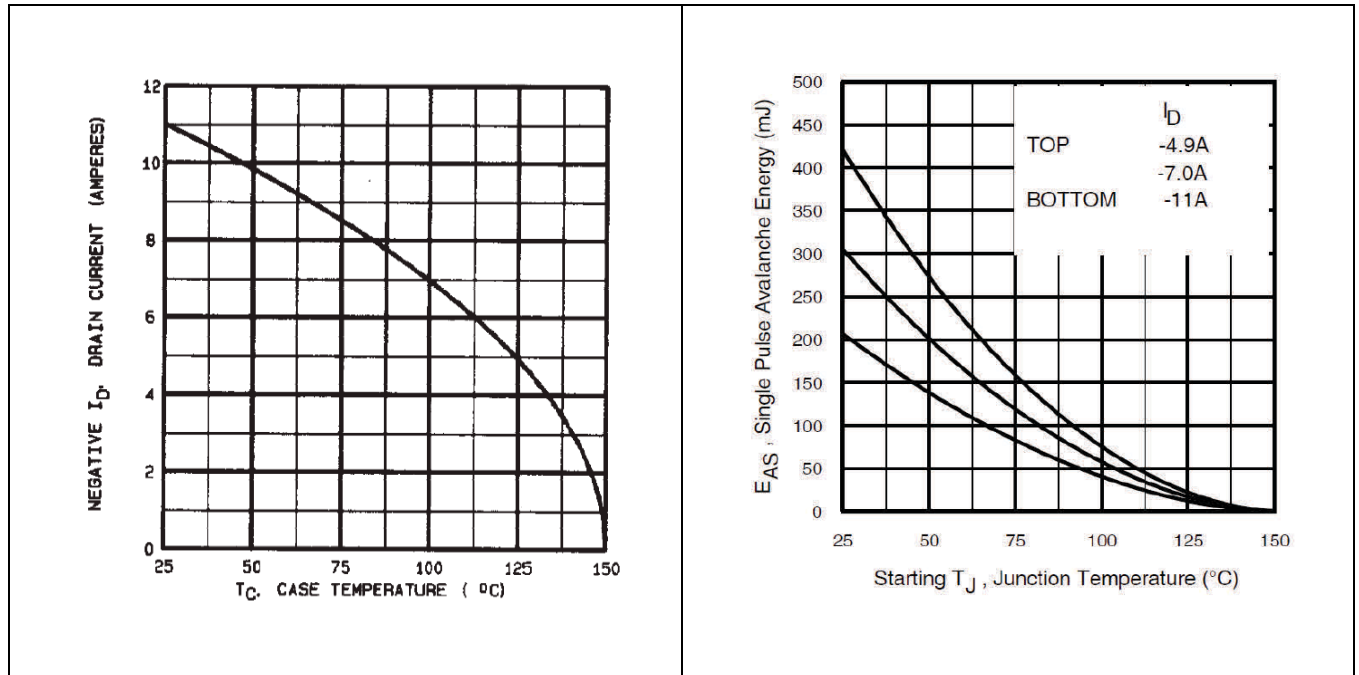


Figure 9 Maximum Drain Current Vs. Case Temperature

Figure 10 Maximum Avalanche Energy Vs. Junction Temperature

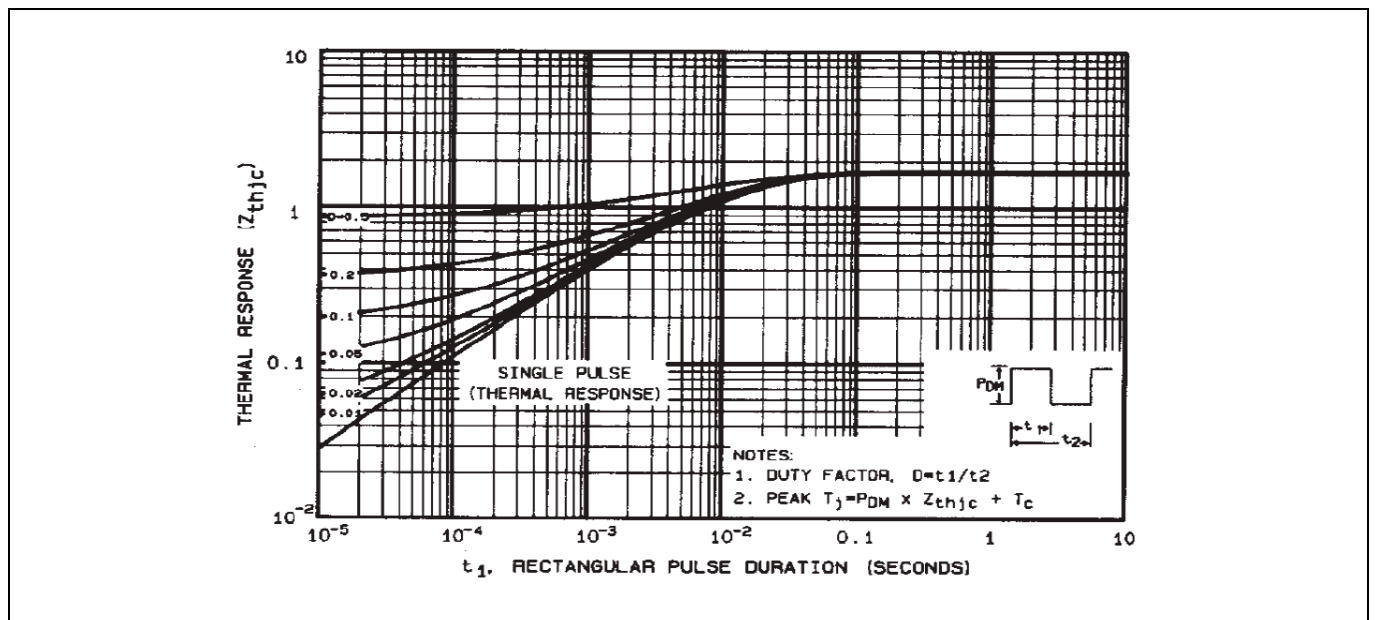


Figure 11 Maximum Effective Transient Thermal Impedance, Junction-to-Case

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Test Circuits

4 Test Circuits

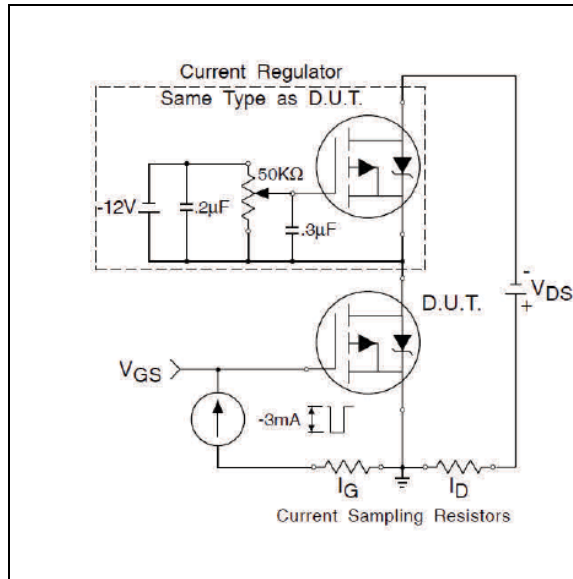


Figure 12 Gate Charge Test Circuit

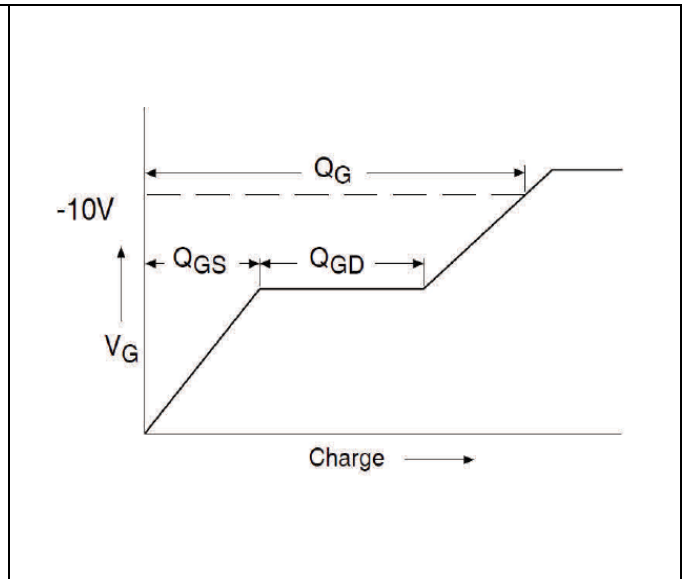


Figure 13 Gate Charge Waveform

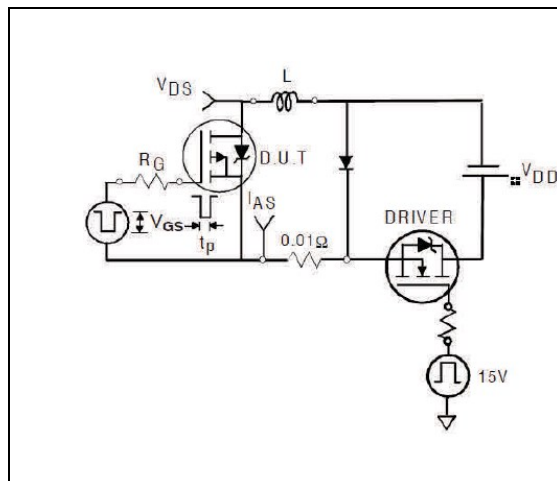


Figure 14 Unclamped Inductive Test Circuit

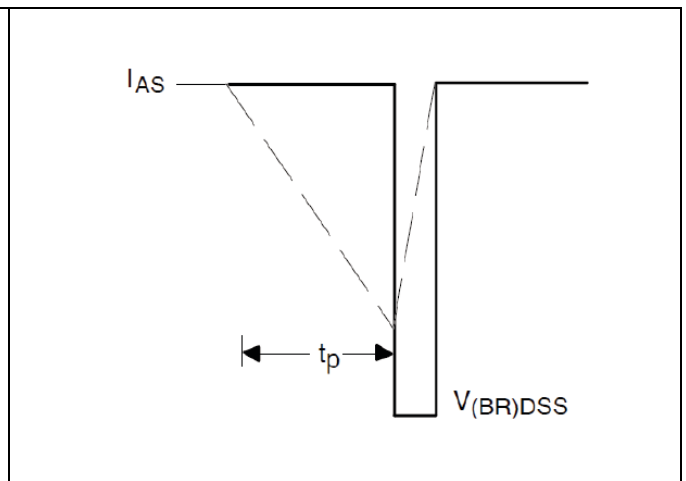


Figure 15 Unclamped Inductive Waveform

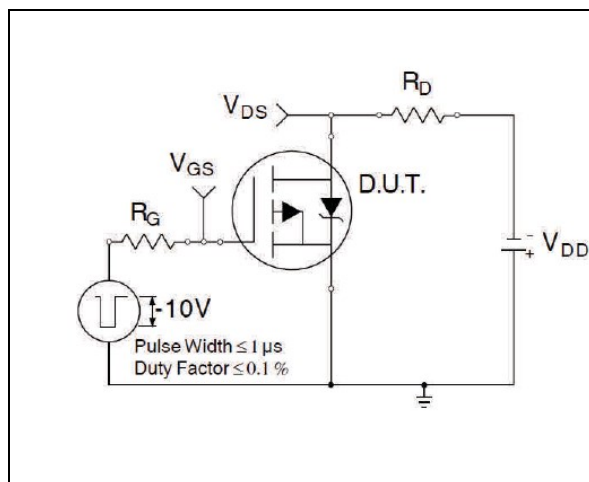


Figure 16 Switching Time Test Circuit

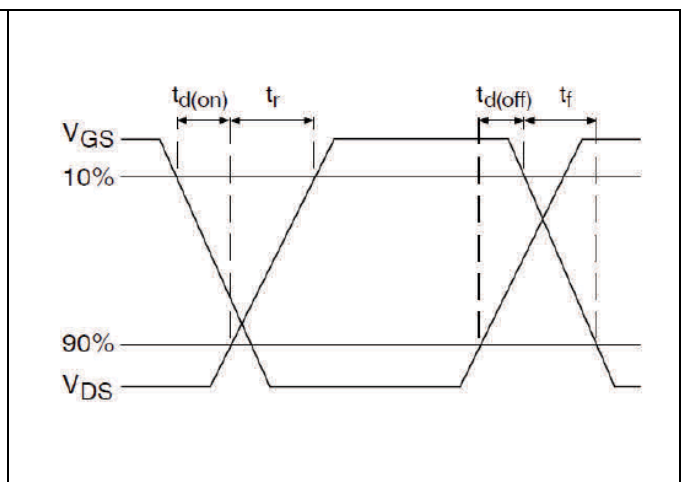


Figure 17 Switching Time Waveforms

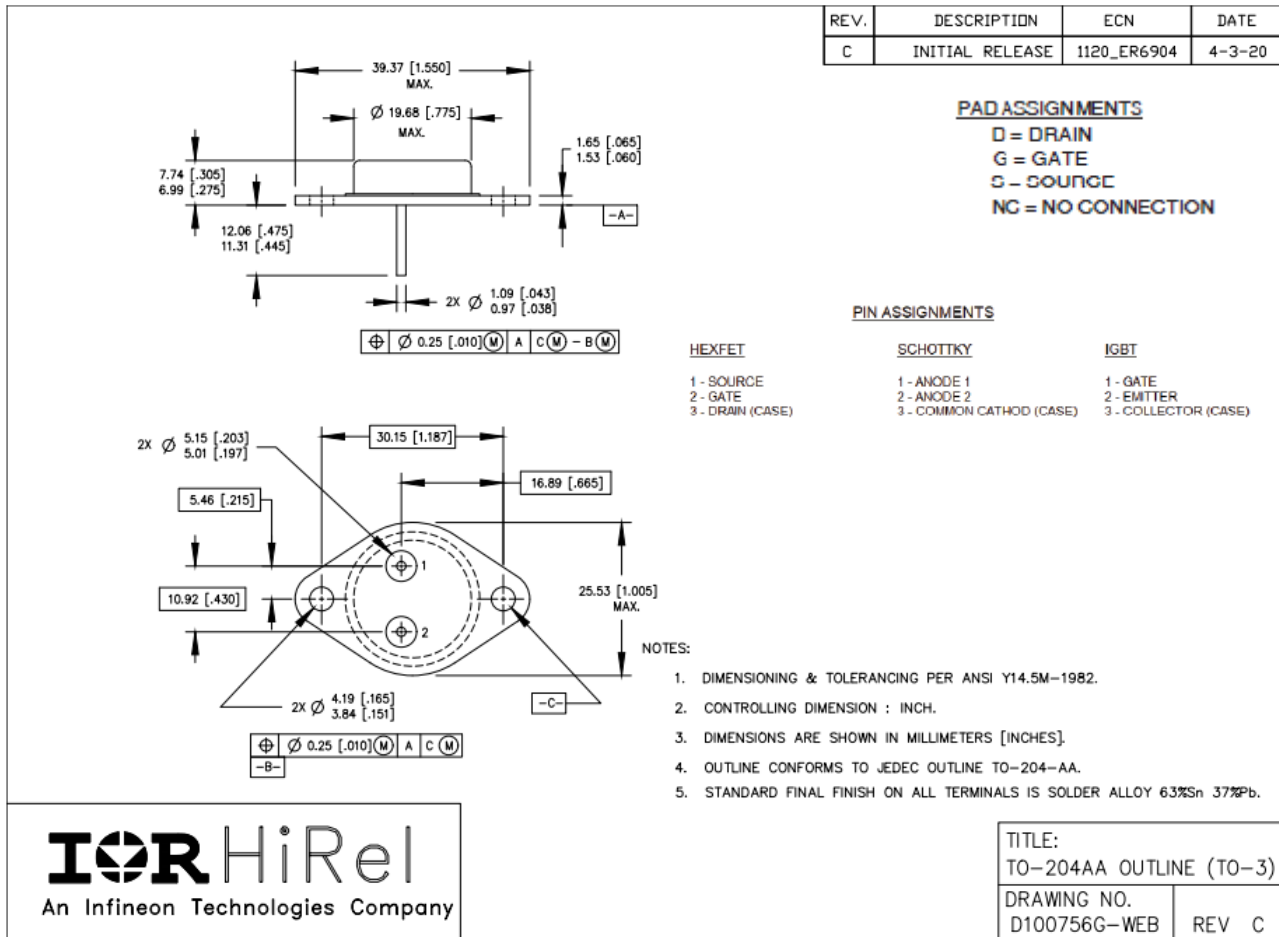
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Package Outline

5 Package Outline

Note: For the most updated package outline, please see the website: [TO-3 \(TO-204AA\)](#)



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Revision history

Revision history

Document version	Date of release	Description of changes
	01/26/2001	Datasheet (PD-90549C)
Rev D	09/28/2015	Updated based on ECN-1120_03206
Rev E	07/29/2019	Updated based on ECN-1120_06844
Rev F	12/06/2024	Updated based on ECN-1120_10116

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