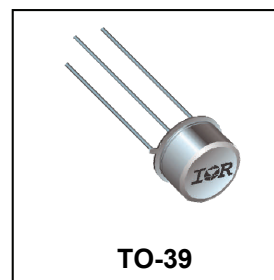


**REPETITIVE AVALANCHE AND dv/dt RATED
 HEXFET® TRANSISTORS
 THRU-HOLE TO-205AF (TO-39)**

500V, N-CHANNEL
REF: MIL-PRF-19500/555

Product Summary

Part Number	BVDSS	RDS(on)	I _D
IRFF420	500V	3.0Ω	1.5A



Description

The HEXFET® technology is the key to International Rectifier's HiRel advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on state resistance combined with high trans conductance.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

Features

- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Hermetically Sealed
- Simple Drive Requirements
- ESD Rating: Class 1B per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I _{D1} @ V _{GS} = 10V, T _C = 25°C	Continuous Drain Current	1.5	A
I _{D2} @ V _{GS} = 10V, T _C = 100°C	Continuous Drain Current	1.0	
I _{DM} @ T _C = 25°C	Pulsed Drain Current ①	6.0	
P _D @ T _C = 25°C	Maximum Power Dissipation	20	W
	Linear Derating Factor	0.16	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy ②	0.242	mJ
I _{AR}	Avalanche Current ①	2.2	A
E _{AR}	Repetitive Avalanche Energy ①	2.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	0.98 (Typical)	

For Footnotes, refer to the page 2.

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	500	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.43	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	3.0	Ω	V _{GS} = 10V, I _{D2} = 1.0A ④
		—	—	3.1		V _{GS} = 10V, I _{D1} = 1.5A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
G _{fs}	Forward Transconductance	1.0	—	—	S	V _{DS} = 15V, I _{D2} = 1.0A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	V _{DS} = 400 V, V _{GS} = 0V
		—	—	250		V _{DS} = 400V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _G	Total Gate Charge	7.3	—	25	nC	I _{D1} = 1.5A
Q _{GS}	Gate-to-Source Charge	0.1	—	6.0		V _{DS} = 250V
Q _{GD}	Gate-to-Drain ('Miller') Charge	3.7	—	18		V _{GS} = 10V
t _{d(on)}	Turn-On Delay Time	—	—	40	ns	V _{DD} = 225V
t _r	Rise Time	—	—	30		I _{D1} = 1.5A
t _{d(off)}	Turn-Off Delay Time	—	—	60		R _G = 7.5Ω
t _f	Fall Time	—	—	30		V _{GS} = 10V
L _S + L _D	Total Inductance	—	7.0	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm/ 0.25 in from package) with Source wire internally bonded from Source pin to Drain pin
C _{iss}	Input Capacitance	—	350	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	80	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	35	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	1.5	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	6.0		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 1.5A, V _{GS} = 0V④
t _{rr}	Reverse Recovery Time	—	—	900	ns	T _J = 25°C, I _F = 1.5A, V _{DD} ≤ 50V
Q _{rr}	Reverse Recovery Charge	—	—	5.9	μC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	—	6.25	°C/W
R _{θJA}	Junction-to-Ambient (Typical Socket Mount)	—	—	175	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V_{DD} = 50V, starting T_J = 25°C, L = 100μH, Peak I_L = 2.2A
- ③ I_{SD} ≤ 1.5A, di/dt ≤ 50A/μs, V_{DD} ≤ 500V, T_J ≤ 150°C, Suggested R_G = 7.5 Ω
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

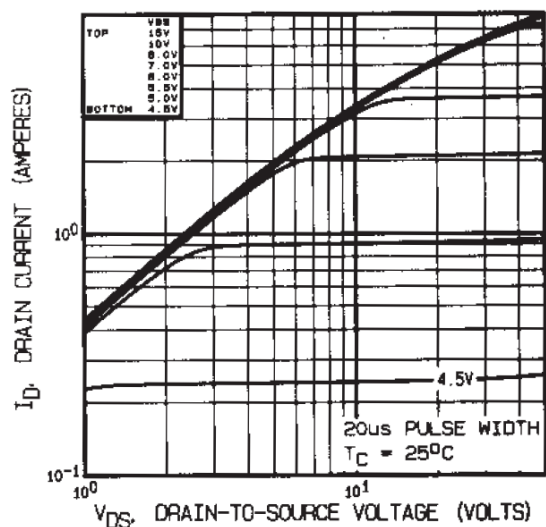


Fig 1. Typical Output Characteristics

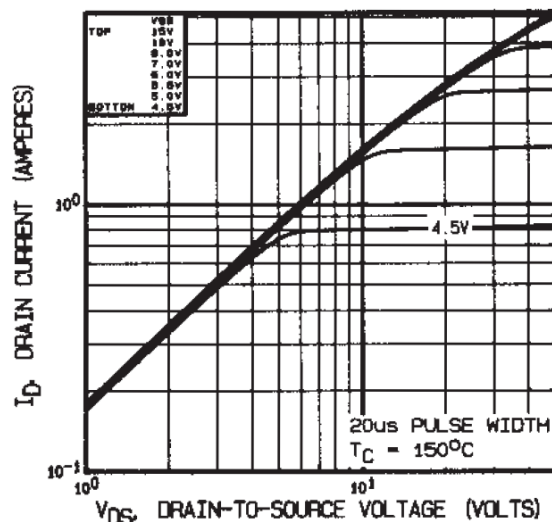


Fig 2. Typical Output Characteristics

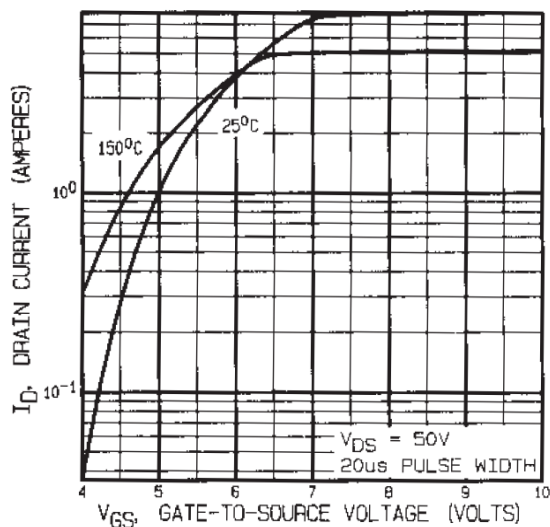


Fig 3. Typical Transfer Characteristics

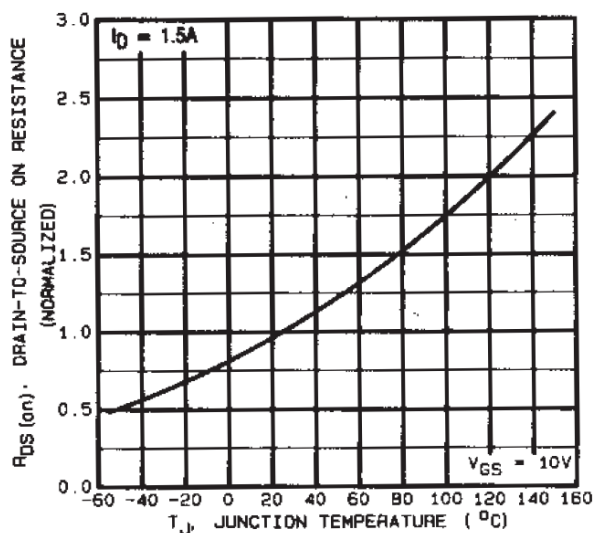


Fig 4. Normalized On-Resistance Vs. Temperature

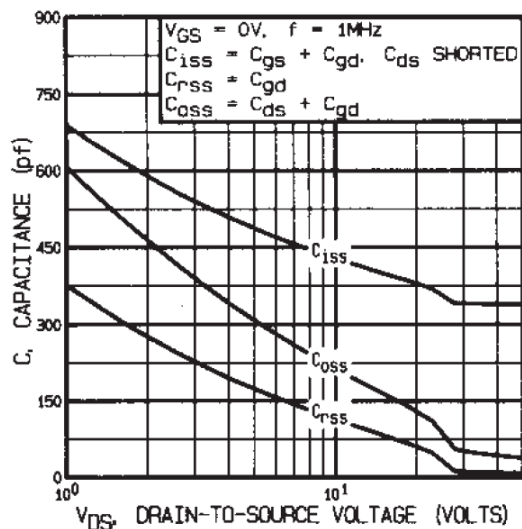


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

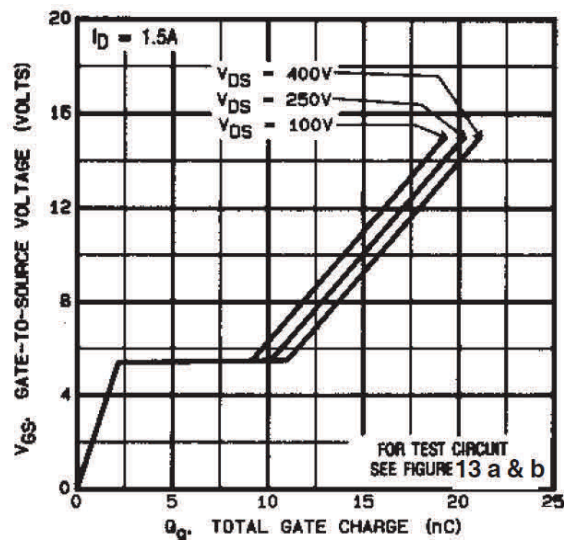


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

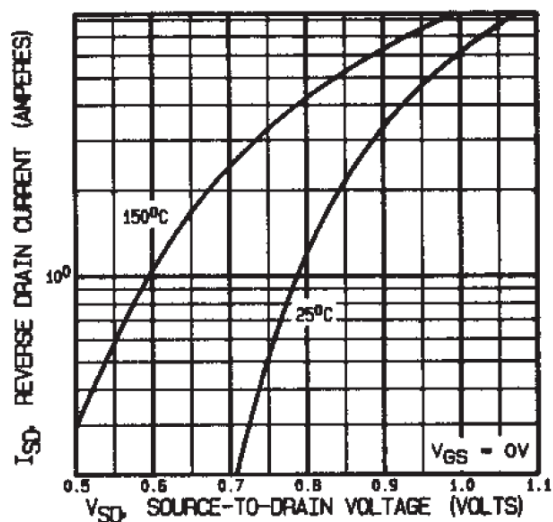


Fig 7. Typical Source-Drain Diode Forward Voltage

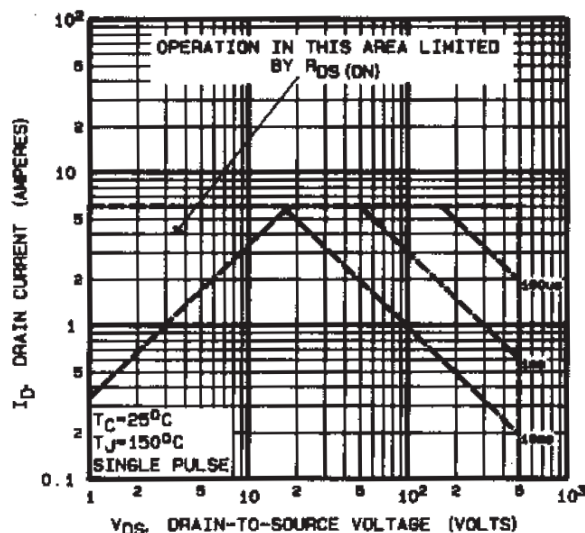


Fig 8. Maximum Safe Operating Area

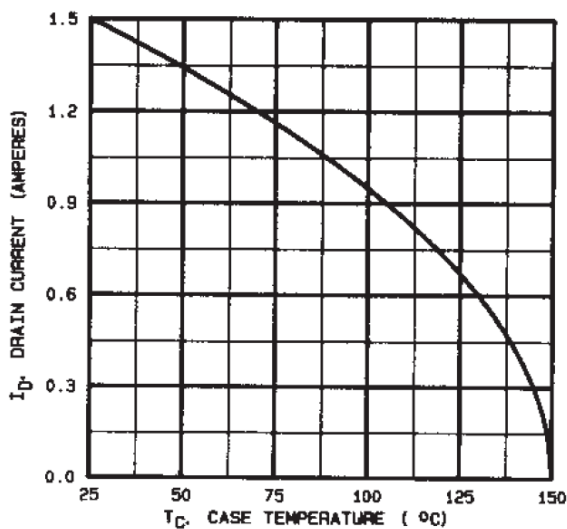


Fig 9. Maximum Drain Current Vs. Case Temperature

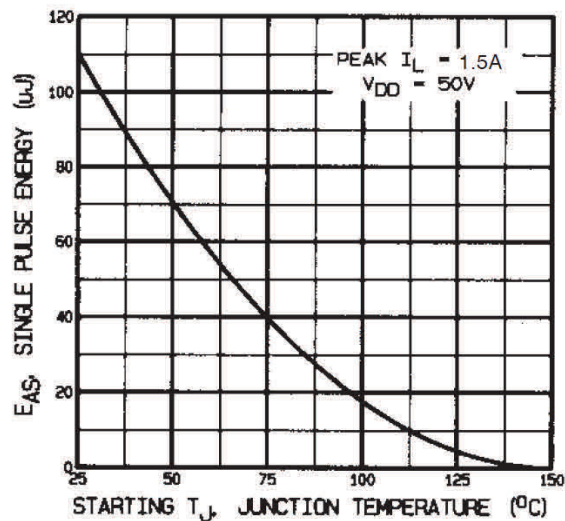


Fig 10. Maximum Avalanche Energy Vs. Drain Current

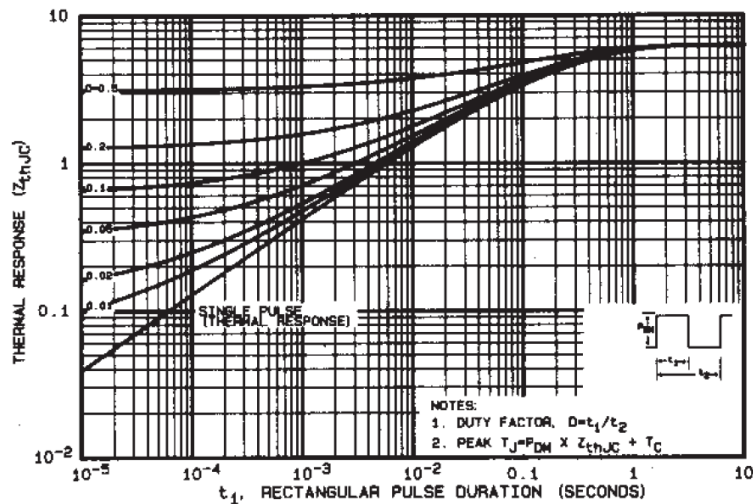


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

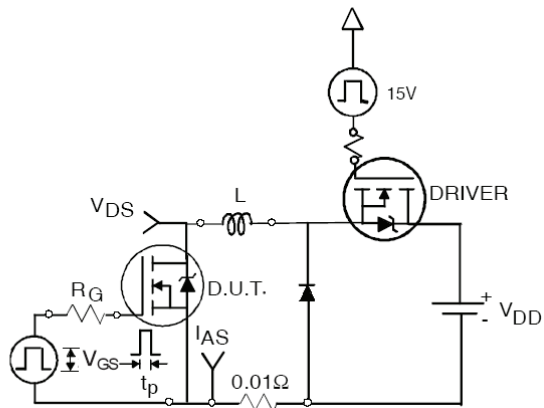


Fig 12a. Unclamped Inductive Test Circuit

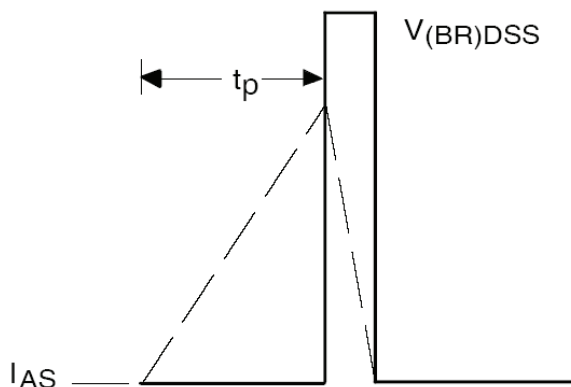


Fig 12b. Unclamped Inductive Waveforms

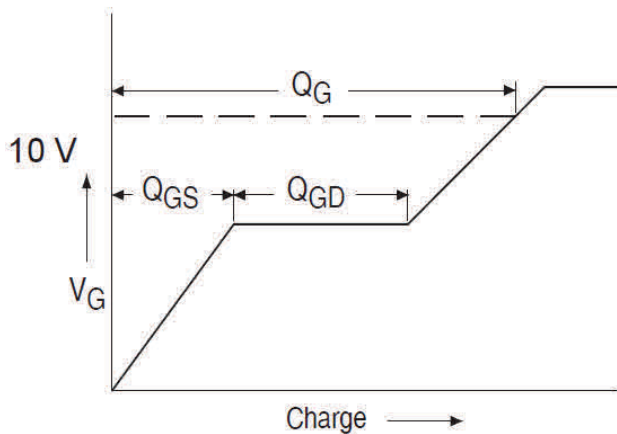


Fig 13a. Gate Charge Waveform

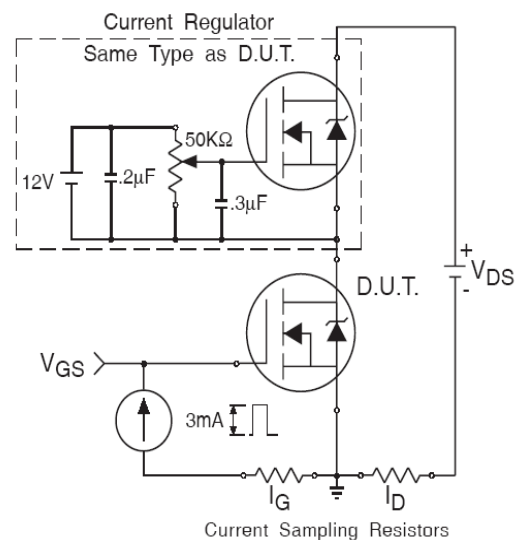


Fig 13b. Gate Charge Test Circuit

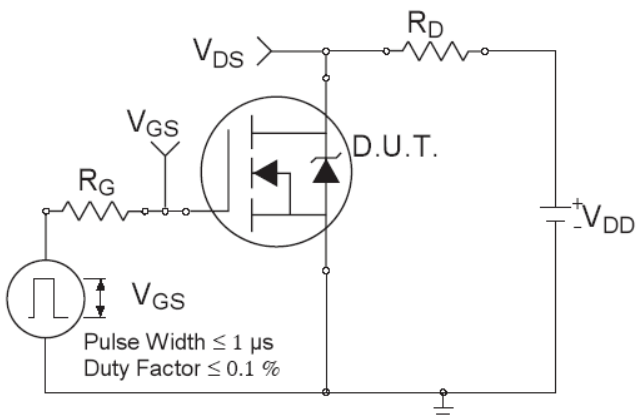


Fig 14a. Switching Time Test Circuit

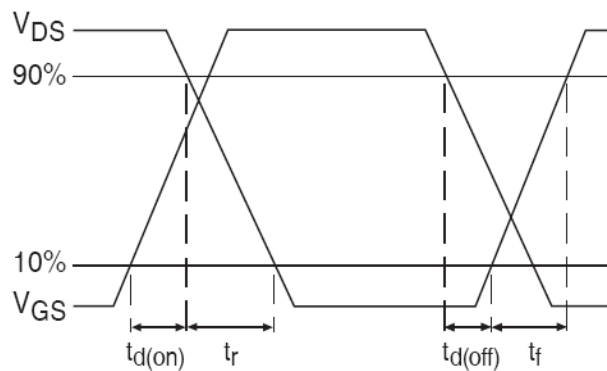
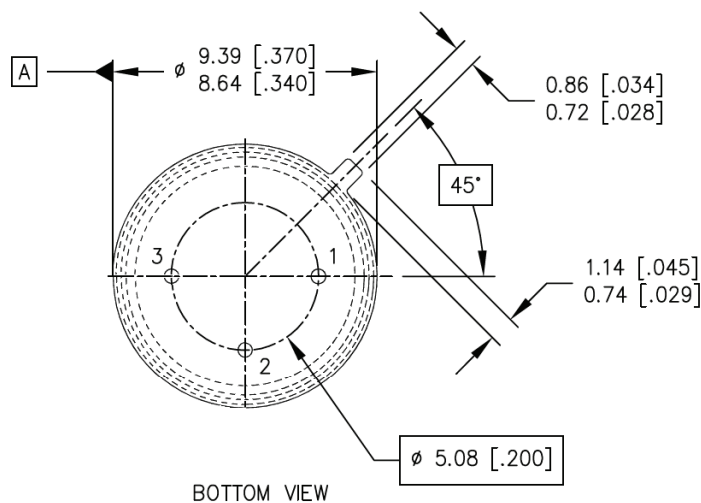
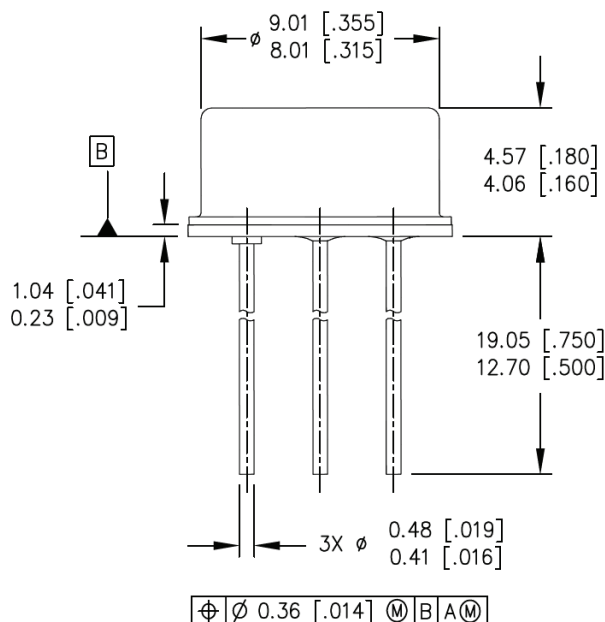


Fig 14b. Switching Time Waveforms

Case Outline and Dimensions - TO-205AF (TO-39)



NOTES:

SIDE VIEW

1. DIMENSIONING AND TOLERANCING PER ASME 14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-205AF (TO-39).

LEGEND

- 1- SOURCE
- 2- GATE
- 3- DRAIN (CONNECTED TO THE CASE)

IMPORTANT NOTICE

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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