

MOSFET
OptiMOS™ 6 Power-Transistor, 200 V

Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low reverse recovery charge (Q_{rr})
- High avalanche energy rating
- 175°C operating temperature
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020
- 100% avalanche tested

Product validation

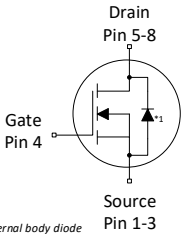
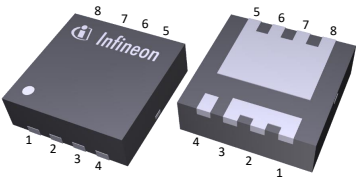
Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	200	V
$R_{DS(on),max}$	52	mΩ
I_D	26	A
Q_{oss}	29	nC
Q_G	9.9	nC
Q_{rr} (1000A/μs)	143	nC

Part number	Package	Marking	Related links
ISZ520N20NM6	PG-TSDSON-8	520N20N	-

PG-TSDSON-8 FL



*1: Internal body diode

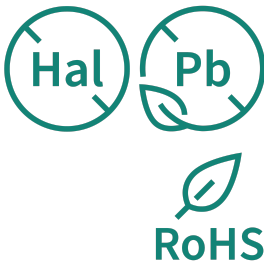




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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	26	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$
				18.7		$V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$
				19.5		$V_{GS}=15\text{ V}$, $T_C=100\text{ °C}$
				4.5		$V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=60\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	104	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	62	mJ	$I_D=9\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	88	W	$T_C=25\text{ °C}$
				2.5		$T_A=25\text{ °C}$, $R_{thJA}=60\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	1.05	1.7	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}		-	60		

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	200	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	3.0	3.7	4.5	V	$V_{DS}=V_{GS}$, $I_D=31\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1	1	μA	$V_{DS}=160\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
			10	100		$V_{DS}=160\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	44.1	52.0	m Ω	$V_{GS}=10\text{ V}$, $I_D=15\text{ A}$
			38.2	47.8		$V_{GS}=15\text{ V}$, $I_D=15\text{ A}$
Gate resistance	R_G	-	4.2	-	Ω	-
Transconductance ⁶⁾	g_{fs}	4.3	8.7	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=15\text{ A}$

⁶⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	740	960	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁷⁾	C_{oss}		120	160		
Reverse transfer capacitance ⁷⁾	C_{rss}		10	17		
Turn-on delay time	$t_{d(on)}$	-	5.7	-	ns	$V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=7.5\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r		3.8			
Turn-off delay time	$t_{d(off)}$		6.6			
Fall time	t_f		9.2			

⁷⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁸⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5.1	-	nC	$V_{DD}=100\text{ V}$, $I_D=7.5\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$		2.7	-	nC	
Gate to drain charge ⁹⁾	Q_{gd}		2.3	3.5	nC	
Switching charge	Q_{sw}		4.6	-	nC	
Gate charge total ⁹⁾	Q_g		9.9	14.9	nC	
Gate plateau voltage	$V_{plateau}$		6.8	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	8	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ⁹⁾	Q_{oss}	-	29	38	nC	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$

⁸⁾ See "Gate charge waveforms" for parameter definition

⁹⁾ Defined by design. Not subject to production test.

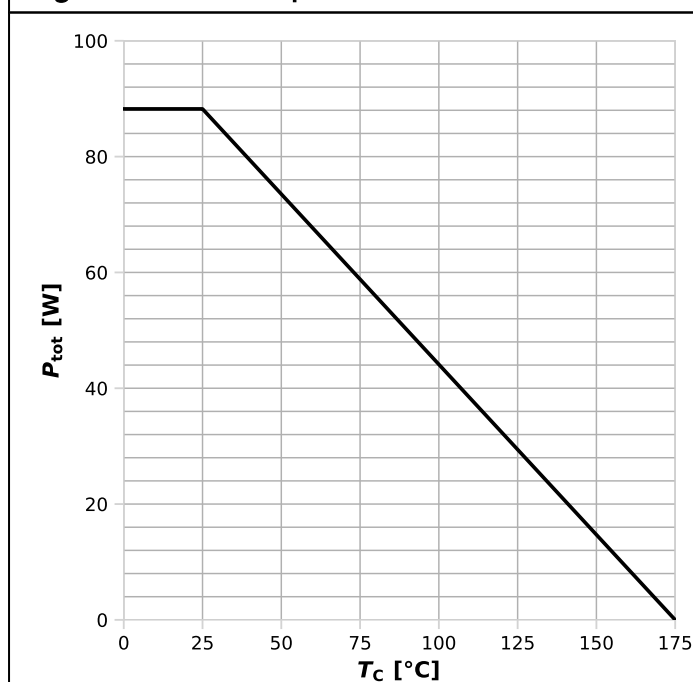
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	26	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$			104		
Diode forward voltage	V_{SD}	-	0.88	1.0	V	$V_{GS}=0\text{ V}$, $I_F=15\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time	t_{rr}	-	37	-	ns	$V_R=100\text{ V}$, $I_F=7.5\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁰⁾	Q_{rr}		30	60	nC	
Reverse recovery time	t_{rr}	-	18	-	ns	$V_R=100\text{ V}$, $I_F=7.5\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁰⁾	Q_{rr}		143	286	nC	

¹⁰⁾ Defined by design. Not subject to production test.

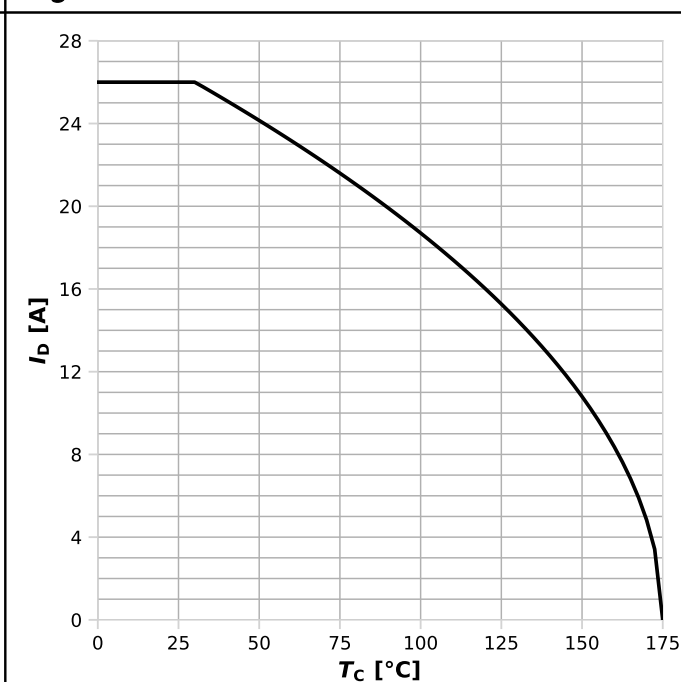
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



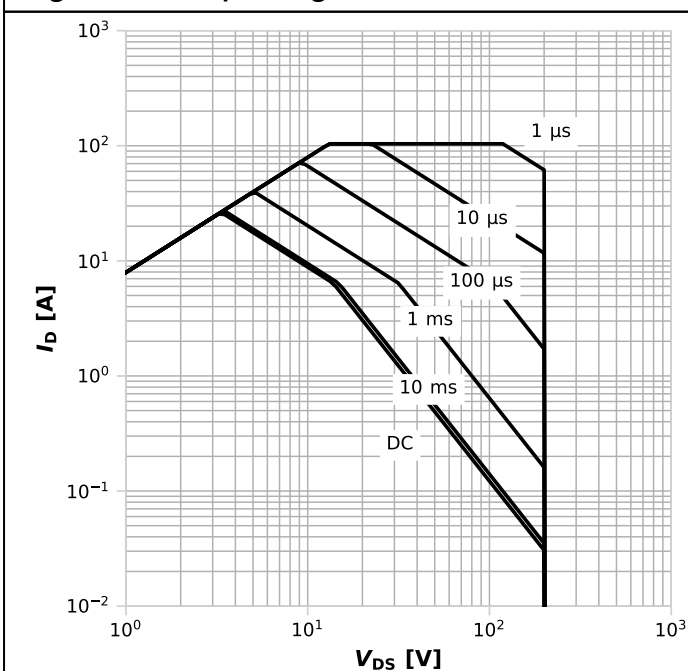
$$P_{\text{tot}} = f(T_c)$$

Diagram 2: Drain current



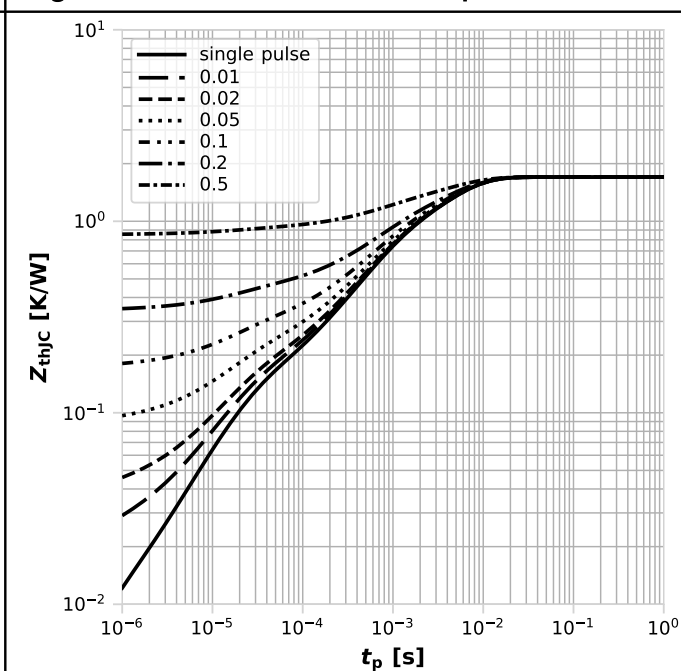
$$I_D = f(T_c); V_{GS} \geq 10 \text{ V}$$

Diagram 3: Safe operating area



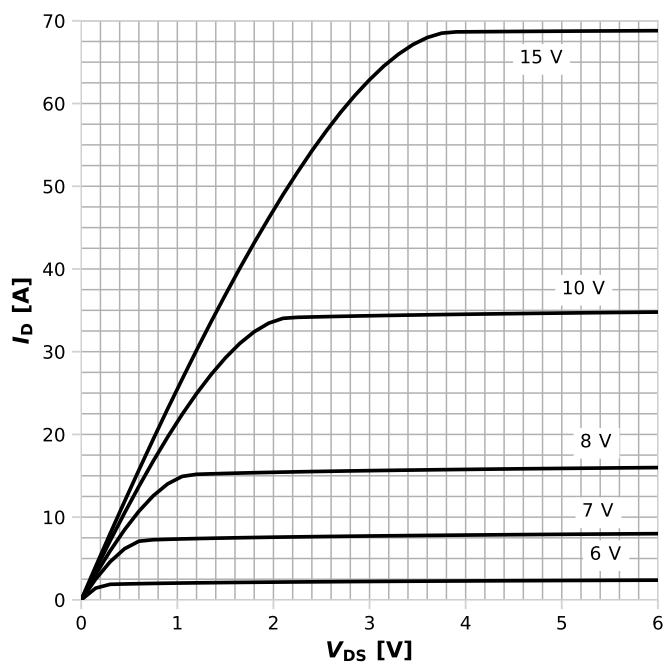
$$I_D = f(V_{DS}); T_c = 25 \text{ °C}; D = 0; \text{parameter: } t_p$$

Diagram 4: Max. transient thermal impedance



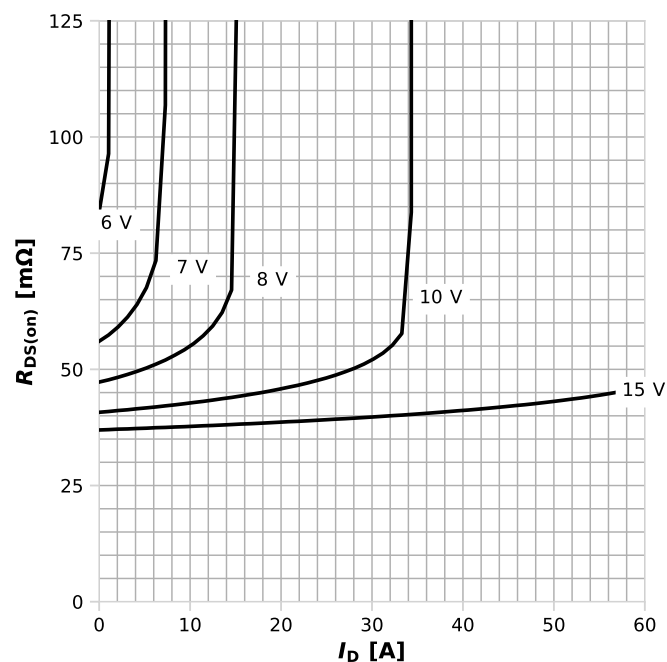
$$Z_{thJC} = f(t_p); \text{parameter: } D = t_p / T$$

Diagram 5: Typ. output characteristics



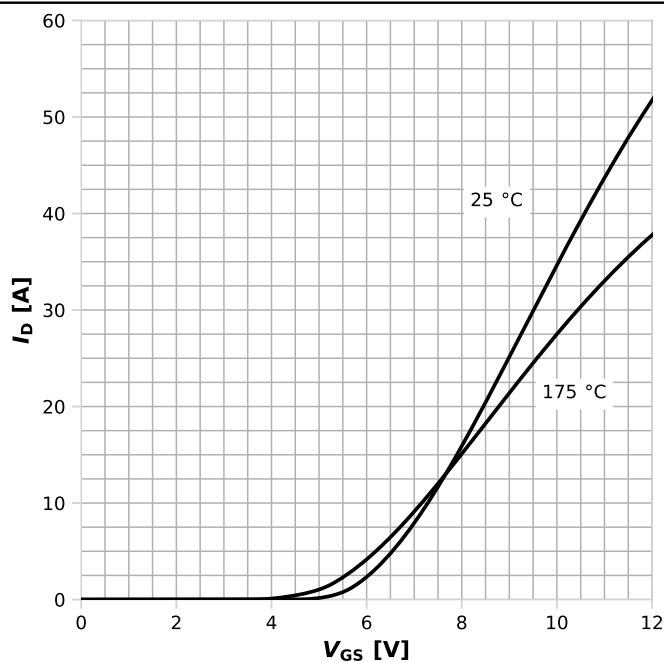
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



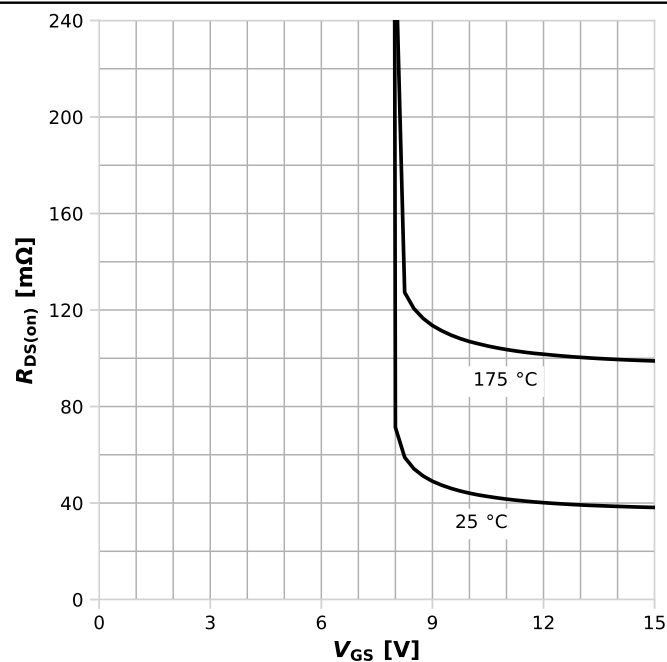
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



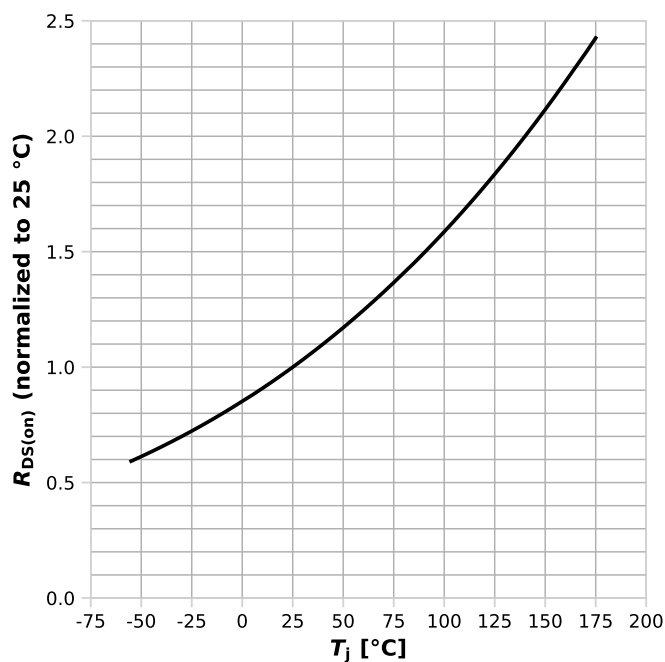
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



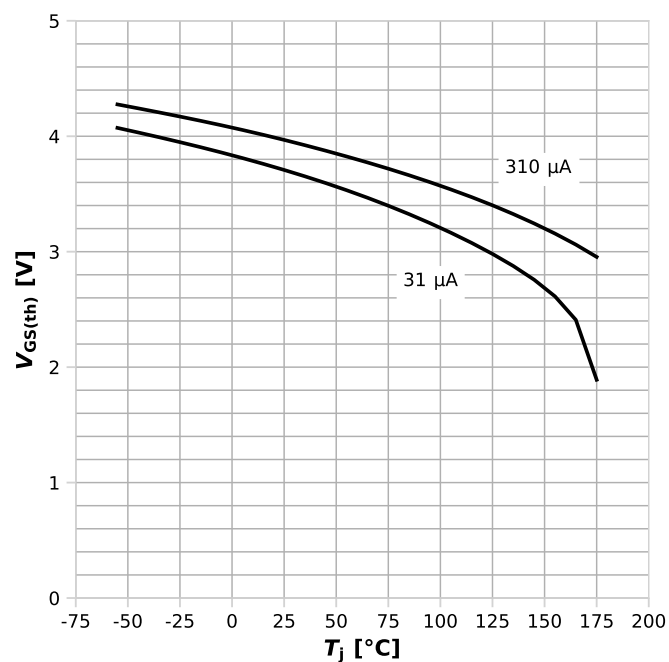
$R_{DS(on)} = f(V_{GS})$, $I_D = 15\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



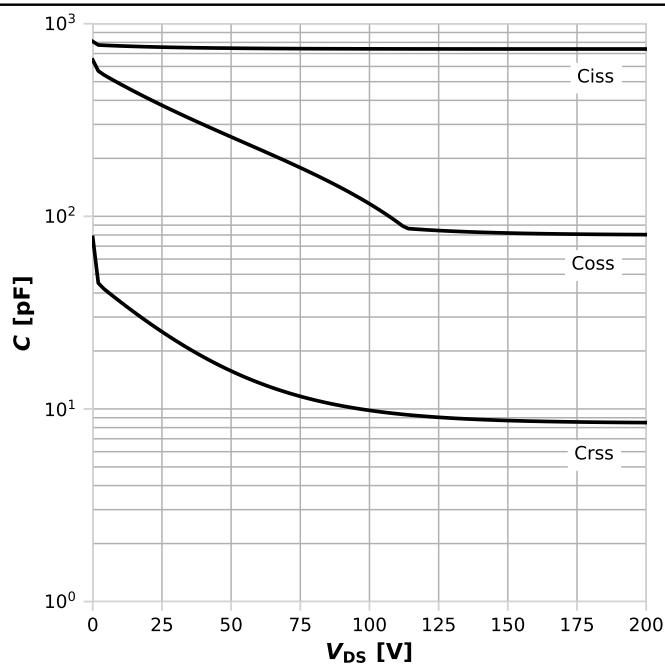
$$R_{DS(on)} = f(T_j), I_D = 15 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



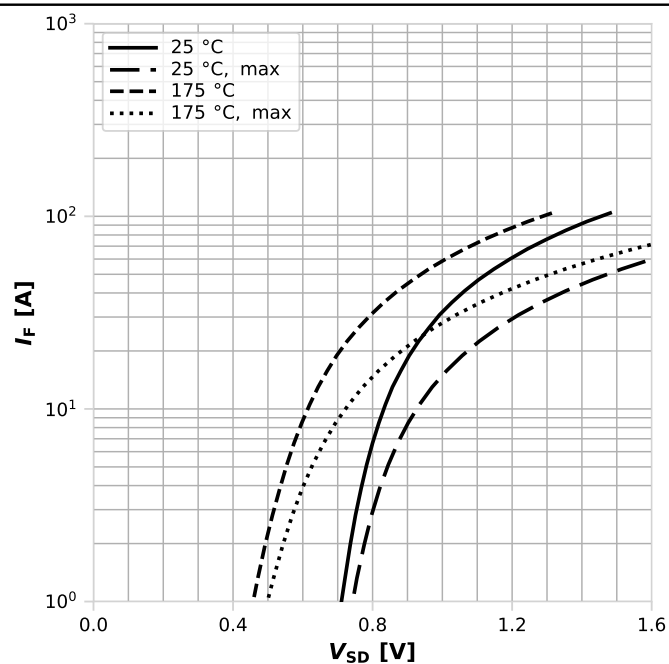
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances



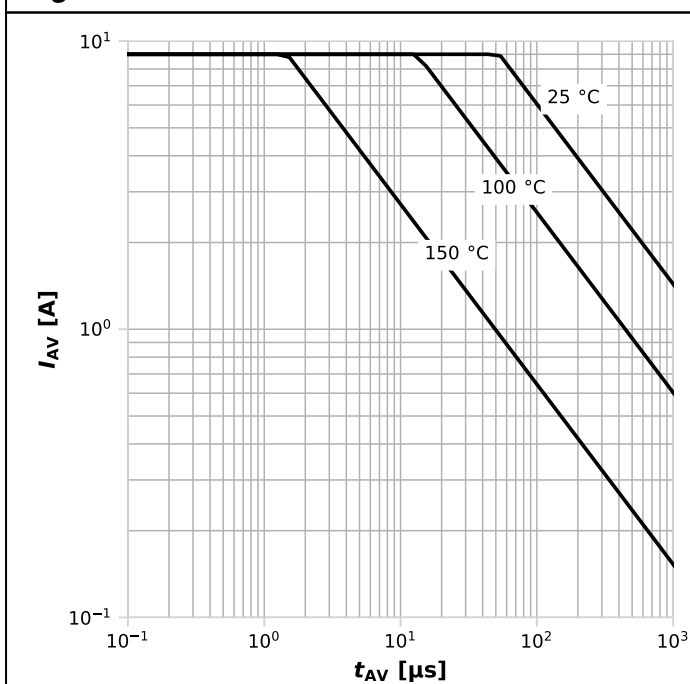
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



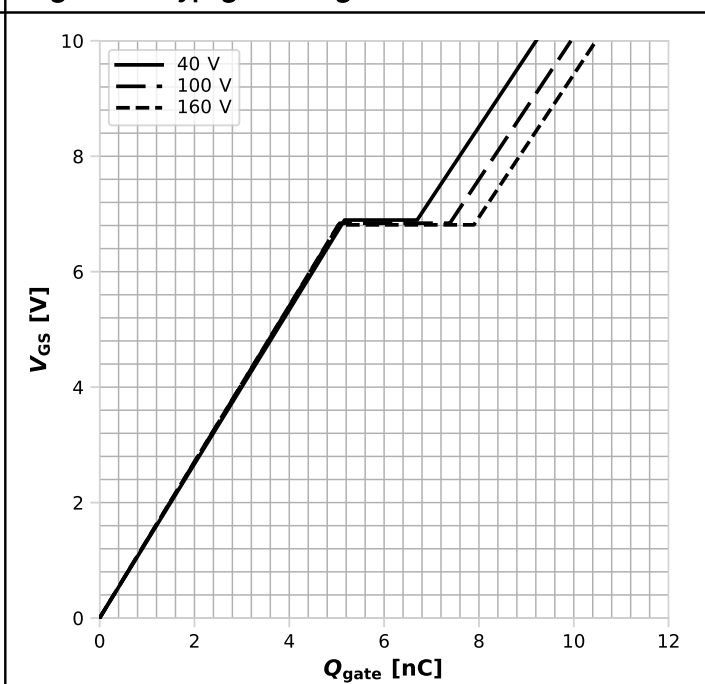
$$I_F = f(V_{SD}); \text{ parameter: } T_j$$

Diagram 13: Avalanche characteristics



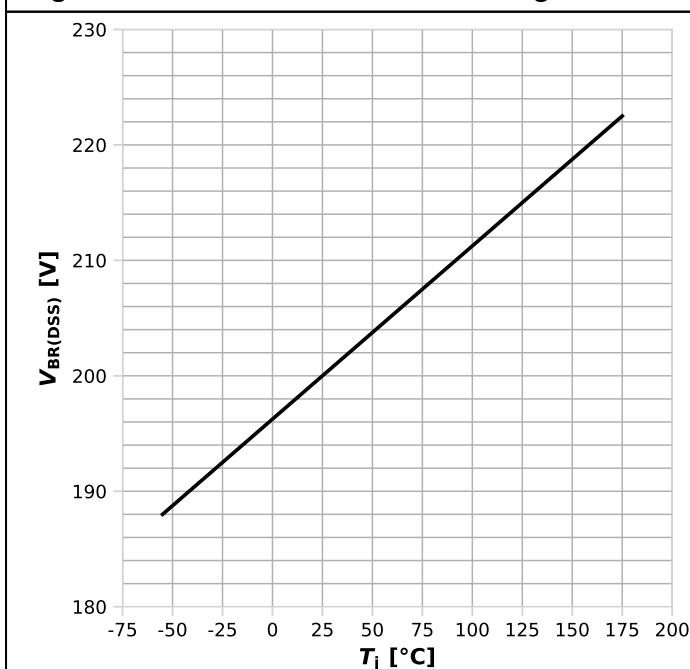
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



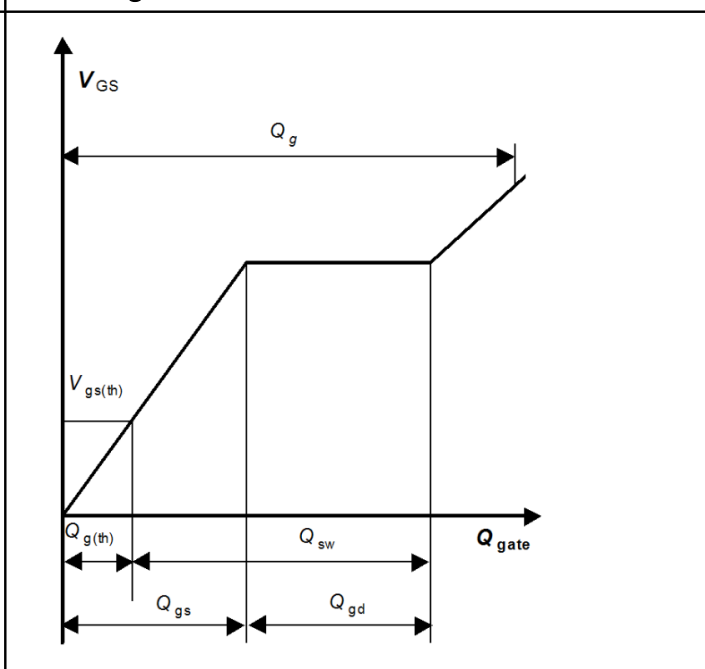
$V_{GS}=f(Q_{gate})$, $I_D=7.5\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



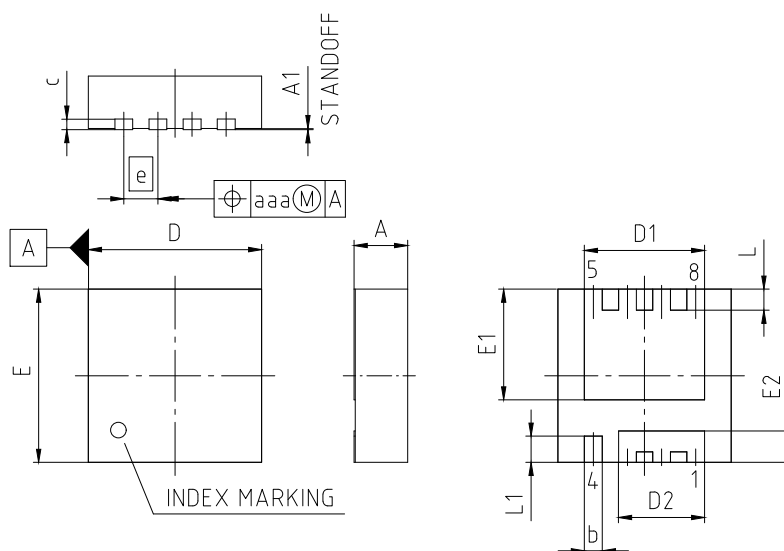
$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Gate charge waveforms



-

5 Package outlines



PACKAGE - GROUP NUMBER: PG-TSDSON-8-U03		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.10
A1	0	0.05
b	0.24	0.44
c	0.10	0.30
D	3.20	3.40
D1	2.19	2.39
D2	1.54	1.74
E	3.20	3.40
E1	2.01	2.21
E2	0.50	0.70
e	0.65	
L	0.30	0.50
L1	0.40	0.60
aaa	0.06	
N	8	

NOTE:

DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-TSDSON-8, dimensions in mm

Revision history

ISZ520N20NM6

Revision 2025-11-24, Rev. 2.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2023-12-07	Release of final version
2.1	2025-11-24	Update Rgext condition for timing

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