

MOSFET

OptiMOS™ 6 Power-Transistor, 60 V

Features

- Optimized for low voltage drives and battery powered applications
- Optimized for high performance SMPS
- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

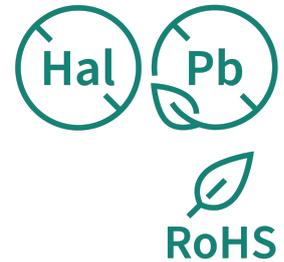
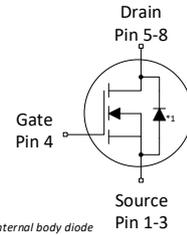
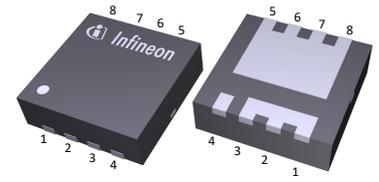
Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Table 1 Key performance parameters

| Parameter | Value | Unit |
|---------------------|-------|------|
| V_{DS} | 60 | V |
| $R_{DS(on),max}$ | 7.2 | mΩ |
| I_D | 57 | A |
| Q_{oss} | 20 | nC |
| Q_G | 12.3 | nC |
| Q_{rr} (1000A/μs) | 45 | nC |

PG-TSDSON-8 FL



| Part number | Package | Marking | Related links |
|--------------|-------------|---------|---------------|
| ISZ072N06NM6 | PG-TSDSON-8 | 072N6N6 | - |



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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|--|----------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Continuous drain current ¹⁾ | I_D | - | - | 57 | A | $V_{GS}=10\text{ V}, T_C=25\text{ °C}$ |
| | | | | 40 | | $V_{GS}=10\text{ V}, T_C=100\text{ °C}$ |
| | | | | 37 | | $V_{GS}=8\text{ V}, T_C=100\text{ °C}$ |
| | | | | 12.7 | | $V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=60\text{ °C/W}^2)$ |
| Pulsed drain current ³⁾ | $I_{D,pulse}$ | - | - | 228 | A | $T_C=25\text{ °C}$ |
| Avalanche energy, single pulse ⁴⁾ | E_{AS} | - | - | 41 | mJ | $I_D=10\text{ A}, R_{GS}=25\text{ }\Omega$ |
| Gate source voltage | V_{GS} | -20 | - | 20 | V | - |
| Power dissipation | P_{tot} | - | - | 50 | W | $T_C=25\text{ °C}$ |
| | | | | 2.5 | | $T_A=25\text{ °C}, R_{thJA}=60\text{ °C/W}^2)$ |
| Operating and storage temperature | T_j, T_{stg} | -55 | - | 175 | °C | - |

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | | 1.5 | 3.0 | °C/W | - |
| Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾ | R_{thJA} | - | - | 60 | | |

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|--|---------------|--------|------|------|---------------|--|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 60 | - | - | V | $V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$ |
| Gate threshold voltage | $V_{GS(th)}$ | 2.1 | 2.7 | 3.3 | V | $V_{DS}=V_{GS}$, $I_D=14\text{ }\mu\text{A}$ |
| Zero gate voltage drain current | I_{DSS} | - | 0.1 | 1.0 | μA | $V_{DS}=48\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ |
| | | | 10 | 100 | | $V_{DS}=48\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$ |
| Gate-source leakage current | I_{GSS} | - | 10 | 100 | nA | $V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 5.4 | 7.2 | m Ω | $V_{GS}=10\text{ V}$, $I_D=10\text{ A}$ |
| Drain-source on-state resistance ⁶⁾ | $R_{DS(on)}$ | - | 6.1 | 8.5 | m Ω | $V_{GS}=8\text{ V}$, $I_D=5\text{ A}$ |
| Gate resistance | R_G | - | 0.7 | - | Ω | - |
| Transconductance ⁶⁾ | g_{fs} | 18 | 36 | - | S | $ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=10\text{ A}$ |

⁶⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|--|--------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Input capacitance ⁷⁾ | C_{iss} | - | 790 | 1000 | pF | $V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$ |
| Output capacitance ⁷⁾ | C_{oss} | | 330 | 430 | | |
| Reverse transfer capacitance ⁷⁾ | C_{rss} | | 18 | 32 | | |
| Turn-on delay time | $t_{d(on)}$ | - | 5.6 | - | ns | $V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=10\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |
| Rise time | t_r | | 5.8 | | | |
| Turn-off delay time | $t_{d(off)}$ | | 7.5 | | | |
| Fall time | t_f | | 2.3 | | | |

⁷⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁸⁾

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|------------------------------------|---------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 3.5 | - | nC | $V_{DD}=30\text{ V}$, $I_D=10\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge at threshold | $Q_{g(th)}$ | - | 2.1 | - | nC | |
| Gate to drain charge ⁹⁾ | Q_{gd} | - | 2.9 | 4.4 | nC | |
| Switching charge | Q_{sw} | - | 4.3 | - | nC | |
| Gate charge total ⁹⁾ | Q_g | - | 12.3 | 15.4 | nC | |
| Gate plateau voltage | $V_{plateau}$ | - | 4.5 | - | V | |
| Output charge ⁹⁾ | Q_{oss} | - | 20 | 27 | nC | $V_{DS}=30\text{ V}$, $V_{GS}=0\text{ V}$ |

⁸⁾ See "Gate charge waveforms" for parameter definition

⁹⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|--|---------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | I_S | - | - | 45 | A | $T_C=25\text{ °C}$ |
| Diode pulse current | $I_{S,pulse}$ | - | - | 228 | | |
| Diode forward voltage | V_{SD} | - | 0.81 | 1.0 | V | $V_{GS}=0\text{ V}$, $I_F=10\text{ A}$, $T_J=25\text{ °C}$ |
| Reverse recovery time ¹⁰⁾ | t_{rr} | - | 20 | 40 | ns | $V_R=30\text{ V}$, $I_F=10\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$ |
| Reverse recovery charge ¹⁰⁾ | Q_{rr} | - | 10 | 20 | | |
| Reverse recovery time ¹⁰⁾ | t_{rr} | - | 13 | 26 | ns | $V_R=30\text{ V}$, $I_F=10\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$ |
| Reverse recovery charge ¹⁰⁾ | Q_{rr} | - | 45 | 90 | | |

¹⁰⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

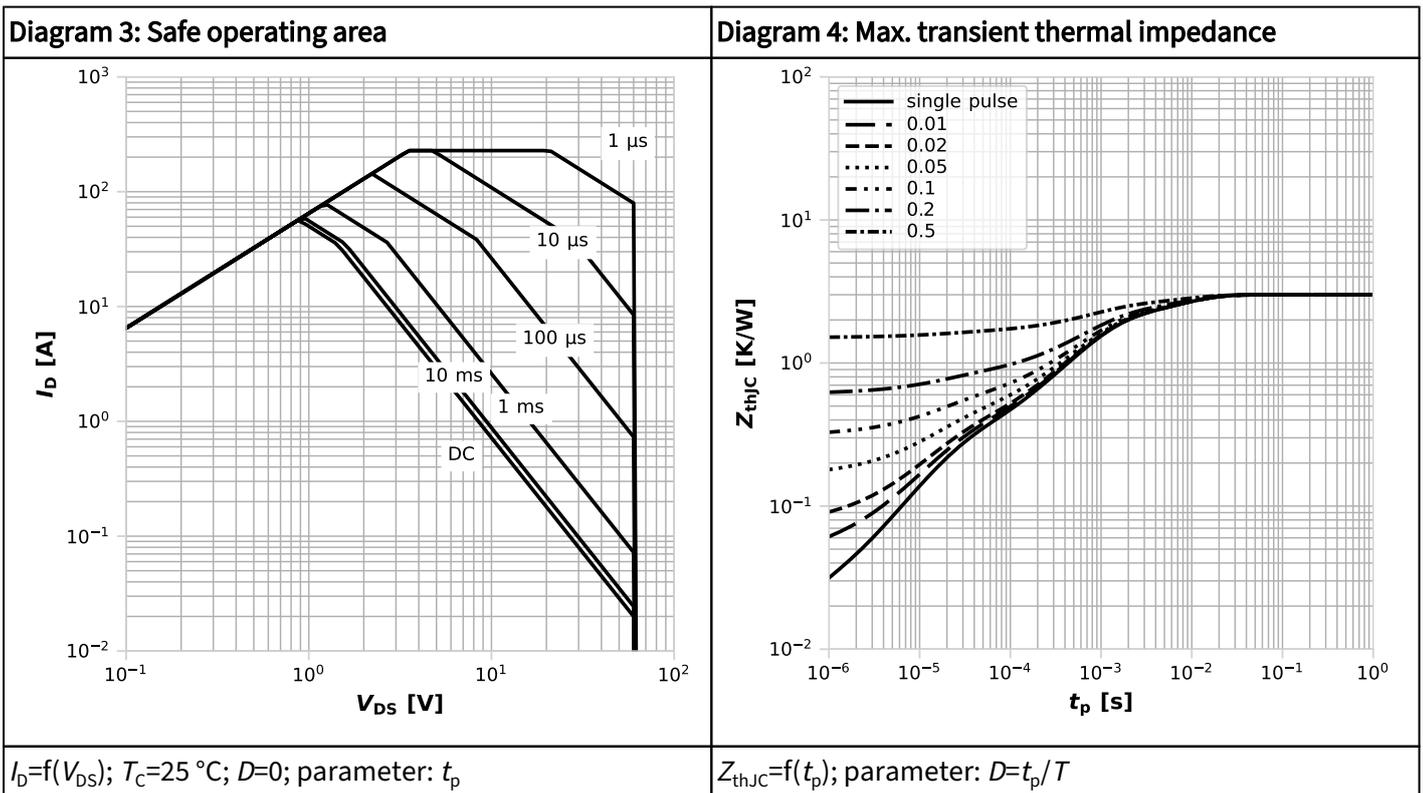
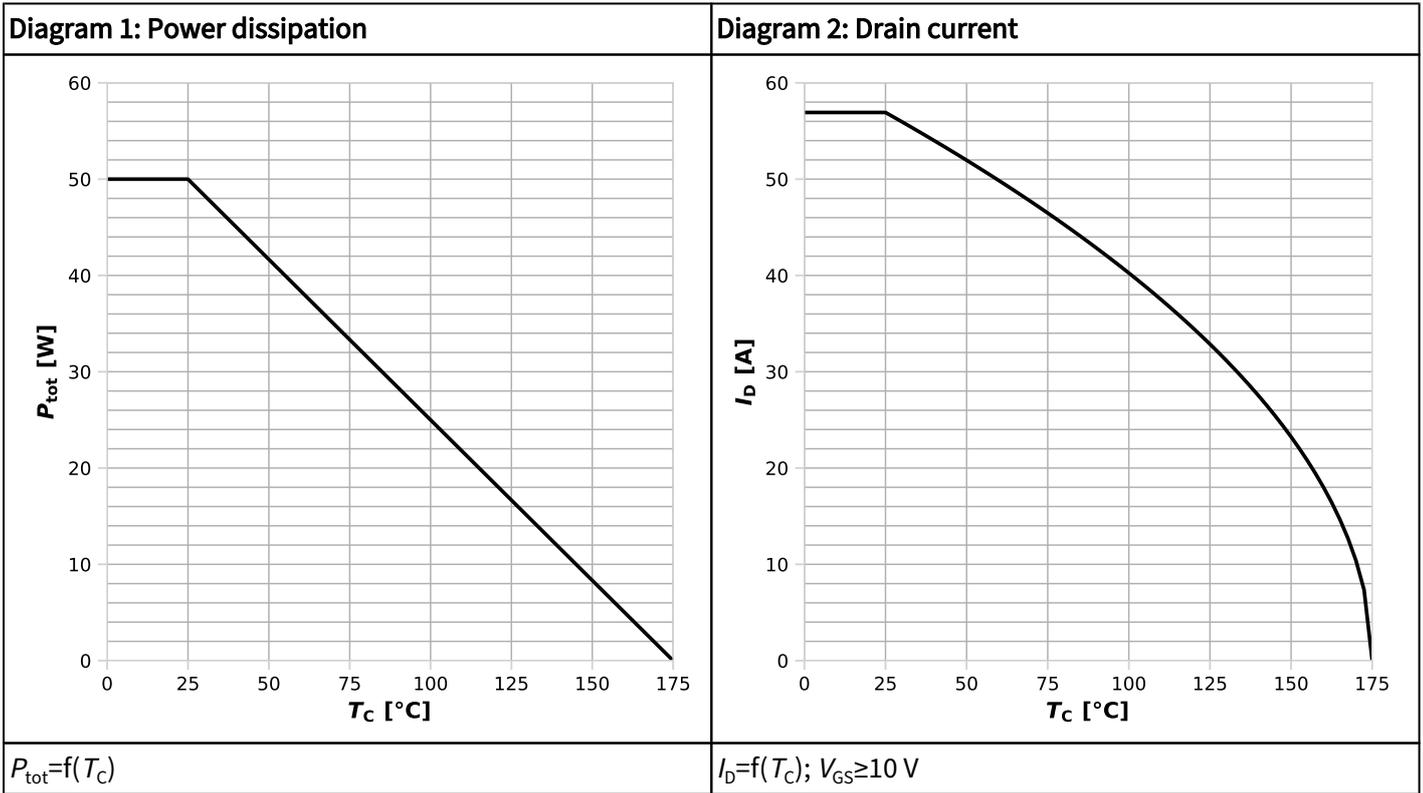
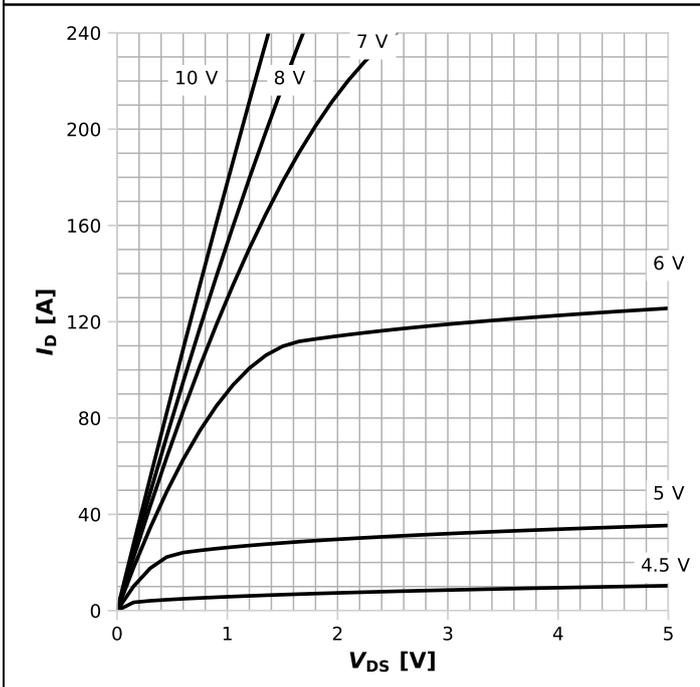
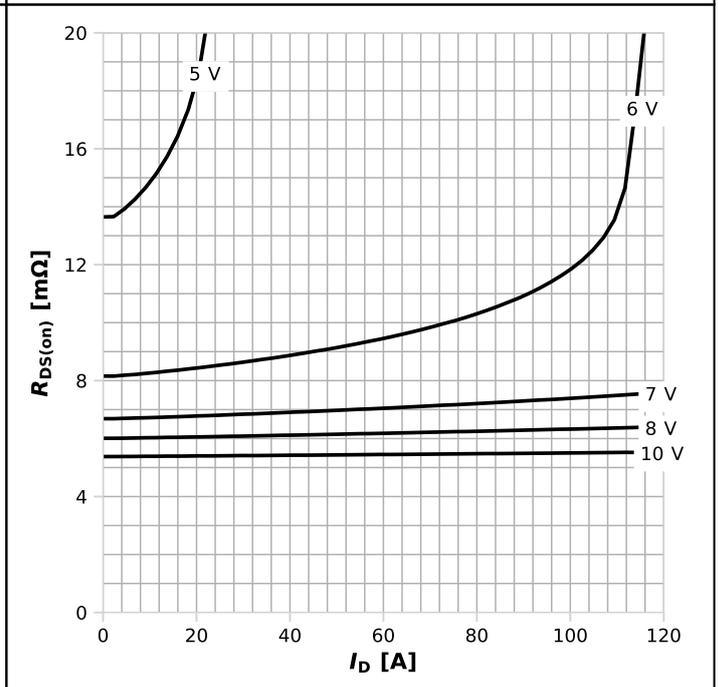


Diagram 5: Typ. output characteristics



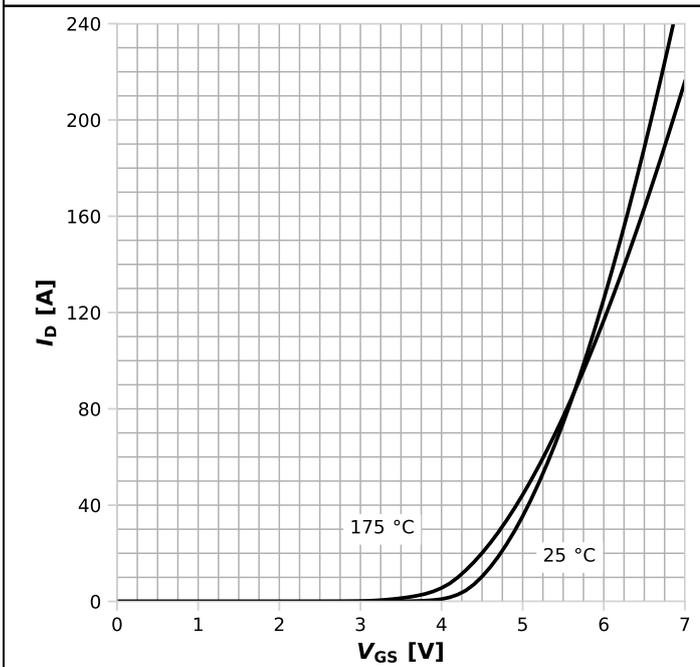
$I_D = f(V_{DS})$, $T_j = 25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



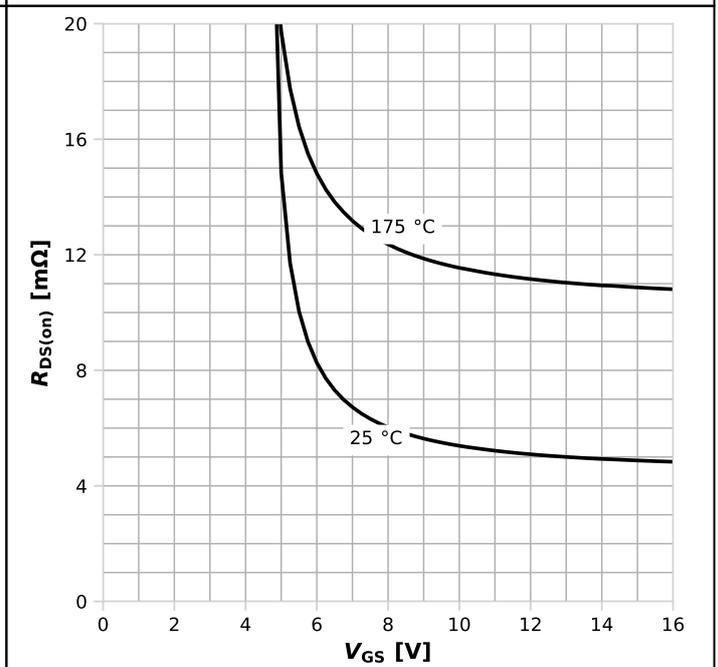
$R_{DS(on)} = f(I_D)$, $T_j = 25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



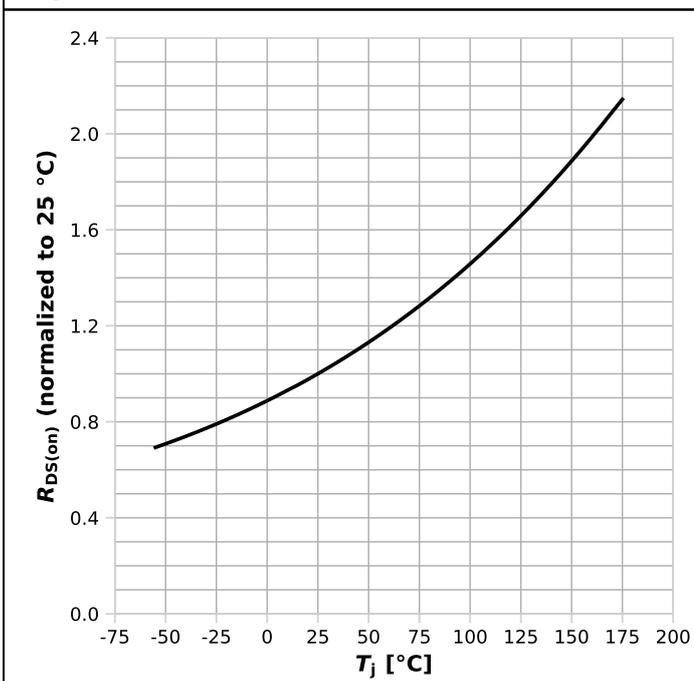
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



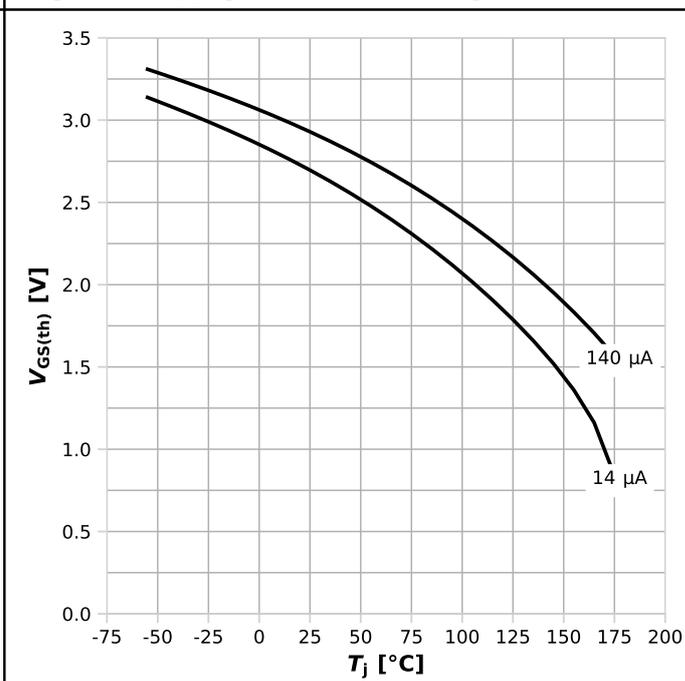
$R_{DS(on)} = f(V_{GS})$, $I_D = 10$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



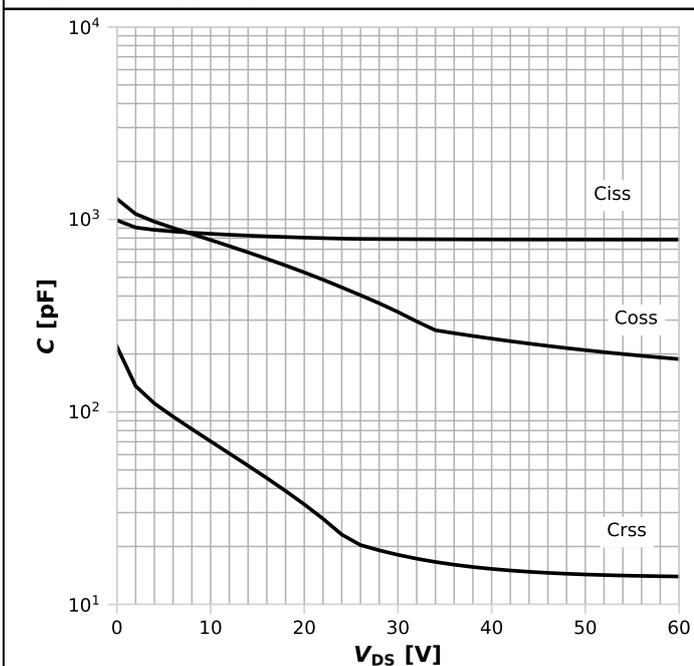
$R_{DS(on)}=f(T_j), I_D=10\text{ A}, V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



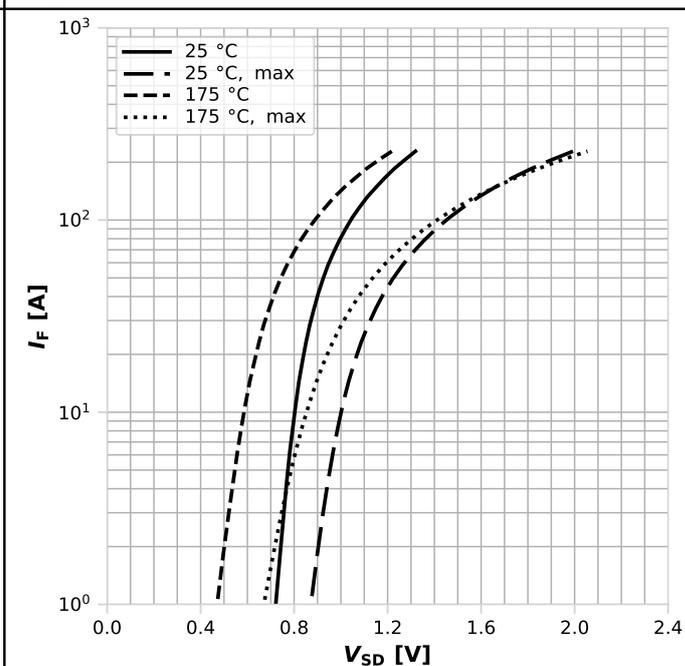
$V_{GS(th)}=f(T_j), V_{GS}=V_{DS}; \text{parameter: } I_D$

Diagram 11: Typ. capacitances



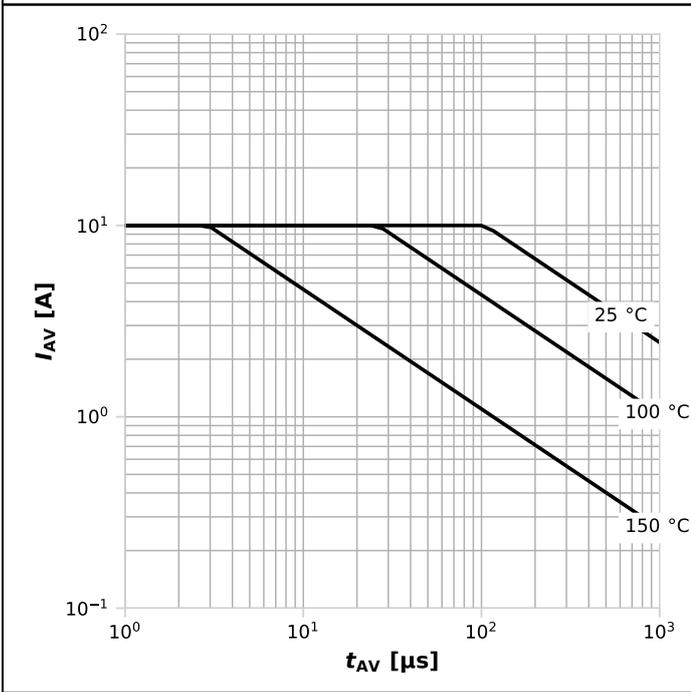
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



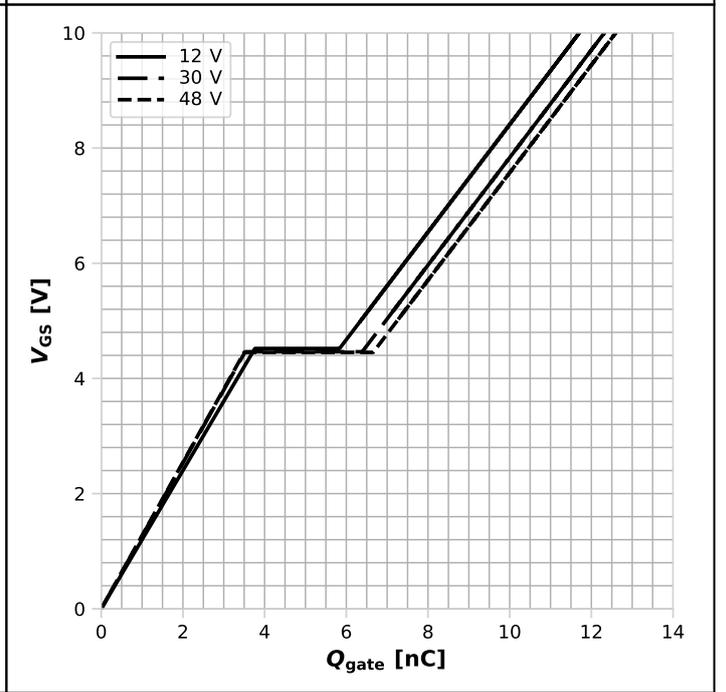
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 13: Avalanche characteristics



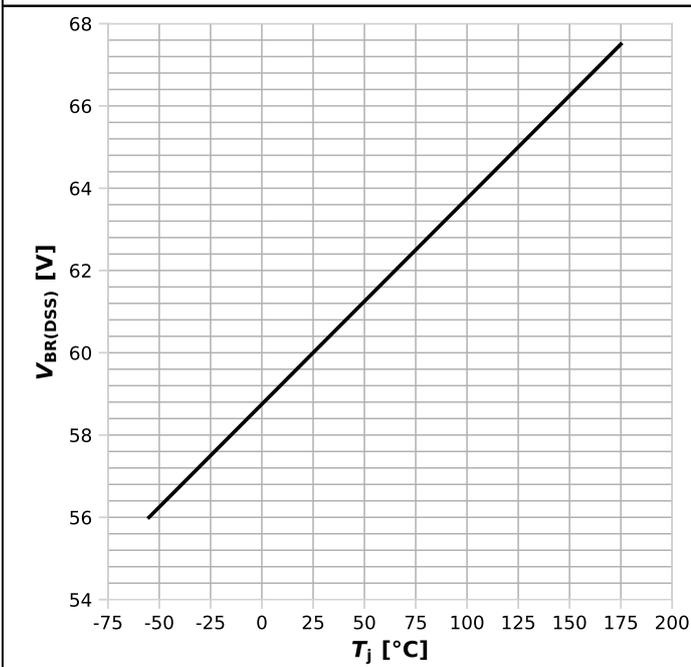
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



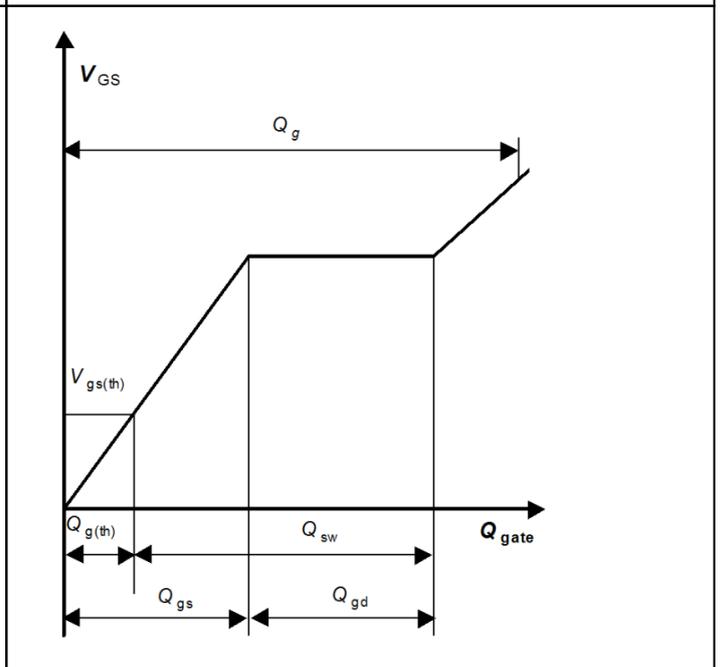
$V_{GS}=f(Q_{gate}), I_D=10 \text{ A pulsed}, T_j=25 \text{ °C}$; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



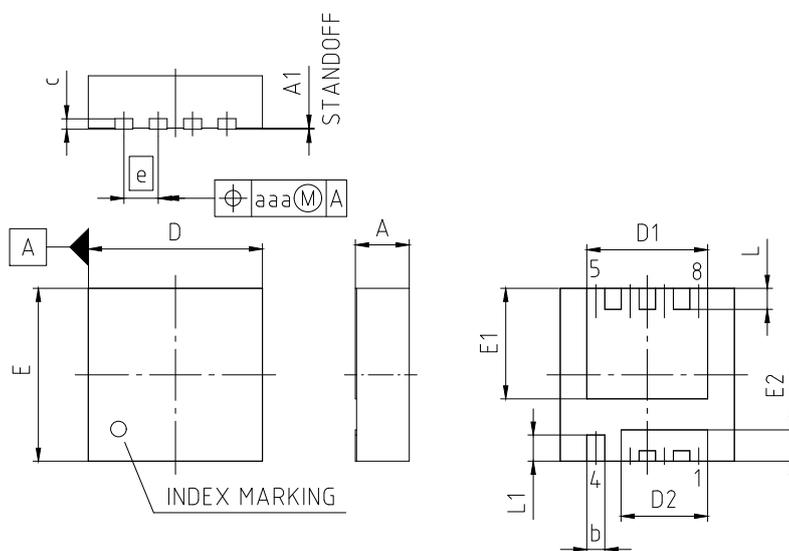
$V_{BR(DSS)}=f(T_j); I_D=10 \text{ mA}$

Gate charge waveforms



-

5 Package outlines



| PACKAGE - GROUP NUMBER: PG-TSDSON-8-U03 | | |
|---|-------------|------|
| DIMENSIONS | MILLIMETERS | |
| | MIN. | MAX. |
| A | 0.90 | 1.10 |
| A1 | 0 | 0.05 |
| b | 0.24 | 0.44 |
| c | 0.10 | 0.30 |
| D | 3.20 | 3.40 |
| D1 | 2.19 | 2.39 |
| D2 | 1.54 | 1.74 |
| E | 3.20 | 3.40 |
| E1 | 2.01 | 2.21 |
| E2 | 0.50 | 0.70 |
| e | 0.65 | |
| L | 0.30 | 0.50 |
| L1 | 0.40 | 0.60 |
| aaa | 0.06 | |
| N | 8 | |

NOTE:
 DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-TSDSON-8, dimensions in mm



Revision history

ISZ072N06NM6

Revision 2025-07-07, Rev. 2.1

Previous revisions

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.0 | 2024-05-07 | Release of final |
| 2.1 | 2025-07-07 | Revised Rdson at Vgs from 6V to 8V |

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