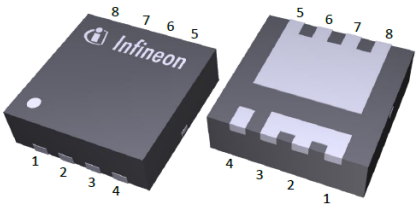
英飞凌MOSFET

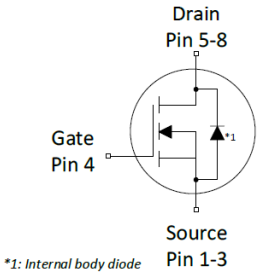
OptiMOS™ 7 功率晶体管，40 V

PG-TSDSON-8 FL



特性

- N沟道，标准电平
- 增强型 SOA
- 驱动优化
- 卓越的热阻
- 100% 雪崩测试
- 无铅镀层；符合 RoHS 标准
- 符合 IEC61249-2-21 标准的无卤素



*1: Internal body diode

产品验证

符合 JEDEC JESD47, JESD22 和 J-STD-020 相关测试的工业应用要求。

表 1　　主要性能参数

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),max}$	1.55	mΩ
I_D	177	A
Q_{OSS}	47	nC
$Q_G(0V..10V)$	37	nC
$Q_{rr}(100A/\mu s)$	24	nC

Part number	Package	Marking	Related links
ISZ015N04NM7V	PG-TSDSON-8	15N04NM7	-

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1 最大额定值

除非另有规定，T_A =25 °C

表 2 最大额定值

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	177	A	V_{GS}=10 V, T_C=25 °C
				125		V_{GS}=10 V, T_C=100 °C
				132		V_{GS}=15 V, T_C=100 °C
				32		V_{GS}=10 V, T_A=25 °C, R_{THJA}=50 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	708	A	T_C=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	68	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	94	W	T_C=25 °C
				3.0		T_A=25 °C, R_{thJA}=50 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

1) 额定值指产品仅具有数据手册指定的绝对最大值，保持外壳温度符合规定要求。其他外壳温度请参见图 2。需要根据实际环境条件降低额定值。

2) 器件置于40 mm × 40 mm × 1.5 mm 环氧树脂 PCB FR4 上，配有6 cm^2（单层，70 µm 厚）铜层面积用于漏极连接。PCB在静止空气中垂直放置。

3) 详细信息请参见图 3

4) 详细信息请参见图 13

2 热特性

表 3 热特性

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	1.6	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}			20		
Thermal resistance, junction - ambient, 6 cm^2 cooling area [5)]	R_{thJA}			50		

5) 器件置于40 mm × 40 mm × 1.5 mm 环氧树脂 PCB FR4 上，配有6 cm^2（单层，70 µm厚）铜层面积用于漏极连接。PCB 在静止空气中垂直放置。

3 电气特性

除非另有规定，T_j = 25°C

表 4 静态特性

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.35	2.75	3.15	V	V_{DS}=V_{GS}, I_D=36 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C
			10	100		V_{DS}=40 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.19	1.40	mΩ	V_{GS}=15 V, I_D=50 A
			1.35	1.55		V_{GS}=10 V, I_D=50 A
Gate resistance	R_G	-	0.8	-	Ω	-
Transconductance	g_{fs}	-	100	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=50 A

表 5 动态特性

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [6)]	C_{iss}	-	2400	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Output capacitance [6)]	C_{oss}		1300			
Reverse transfer capacitance [6)]	C_{rss}		30			
Turn-on delay time	$t_{d(on)}$	-	8.2	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r		2.6			
Turn-off delay time	$t_{d(off)}$		13			
Fall time	t_f		4.5			

6) 由设计指定，未经过生产测试。

表 6 栅极电荷特性[7)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	12	-	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$		6.7	-	nC	
Gate to drain charge	Q_{gd}		8.2	-	nC	
Switching charge	Q_{sw}		14	-	nC	
Gate charge total [8)]	Q_g		37	46	nC	
Gate plateau voltage	$V_{plateau}$		5.1	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	34	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	47	-	nC	V_{DS}=20 V, V_{GS}=0 V

7) 参数定义请参数见“栅极电荷波形”

8) 由设计指定，未经过生产测试。

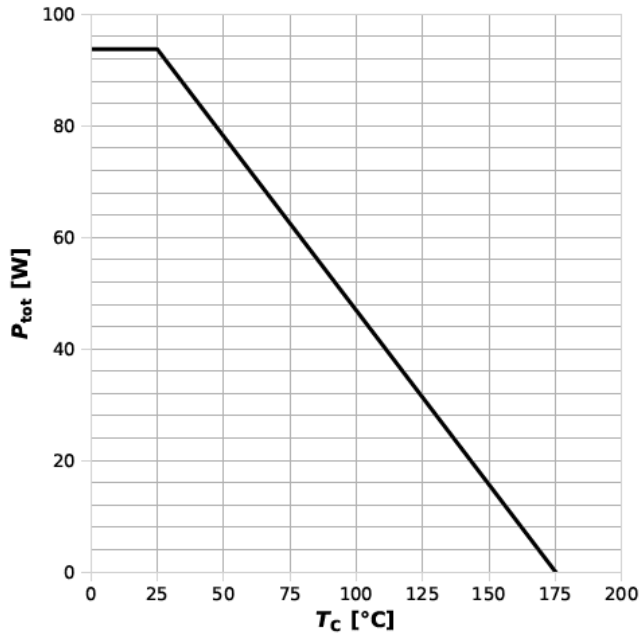
表 7 反向二极管

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	94	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			708		
Diode forward voltage	V_{SD}	-	0.83	1.0	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time [9)]	t_{rr}	-	34	-	ns	V_R=20 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge [9)]	Q_{rr}		24		nC	

9) 由设计指定，未经过生产测试。

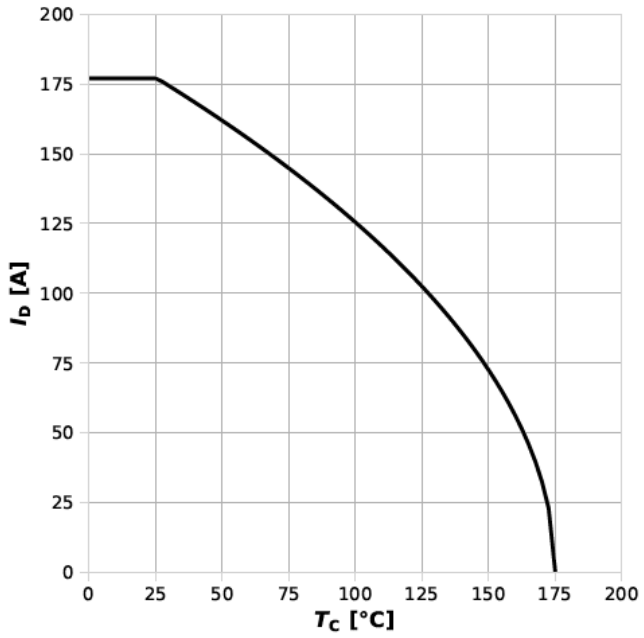
4 电气特性图

Diagram 1: Power dissipation



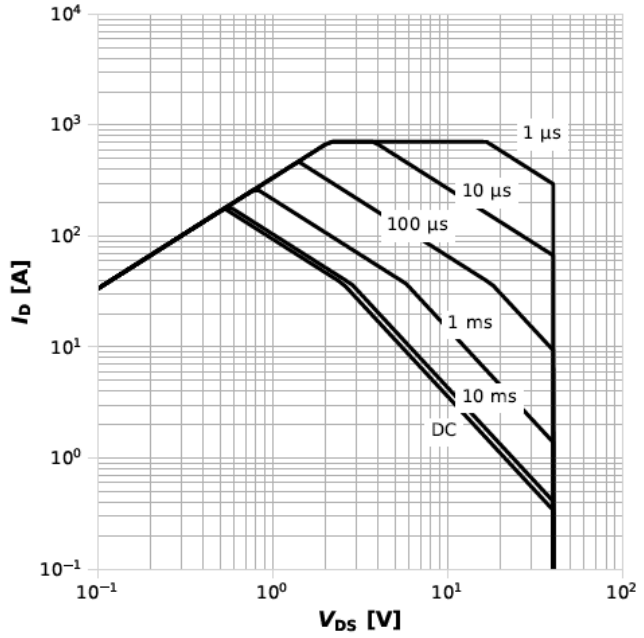
P_{tot}=f(T_C)

Diagram 2: Drain current



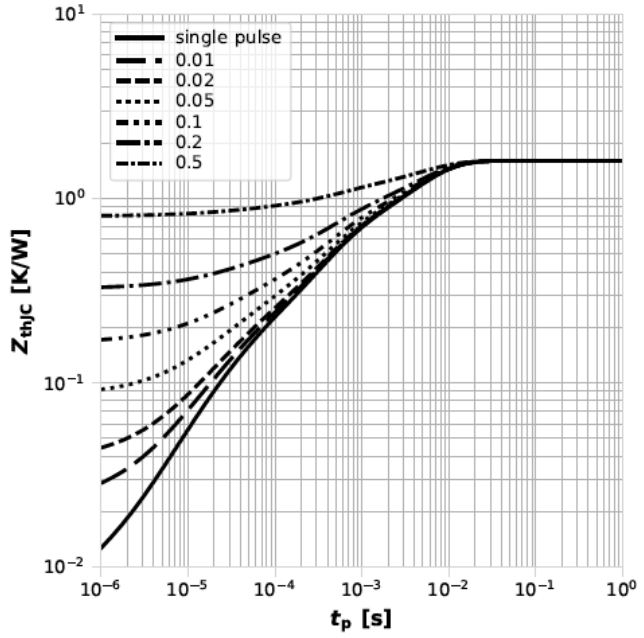
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



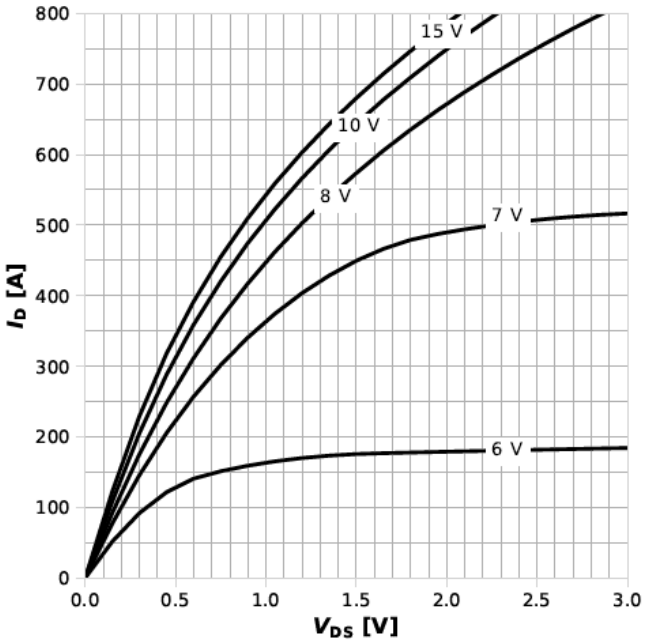
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



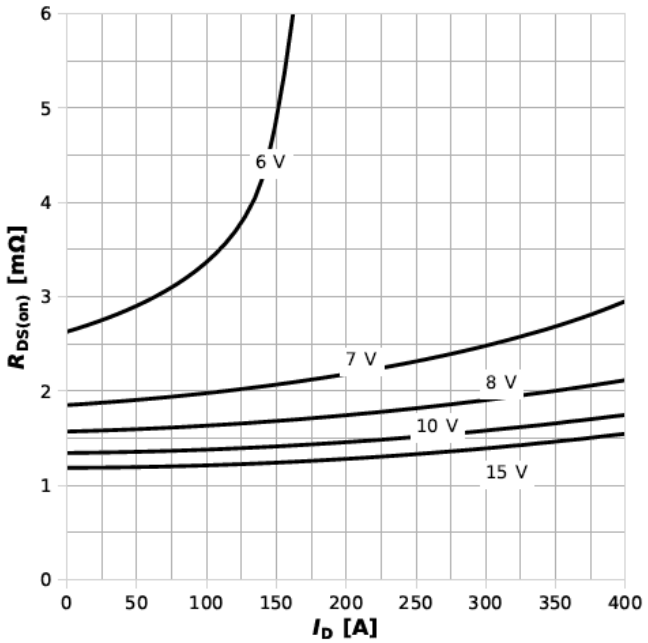
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



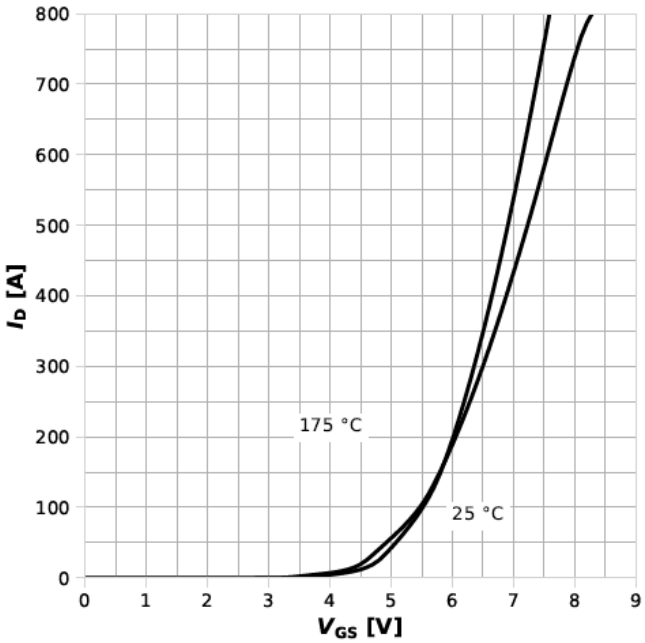
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



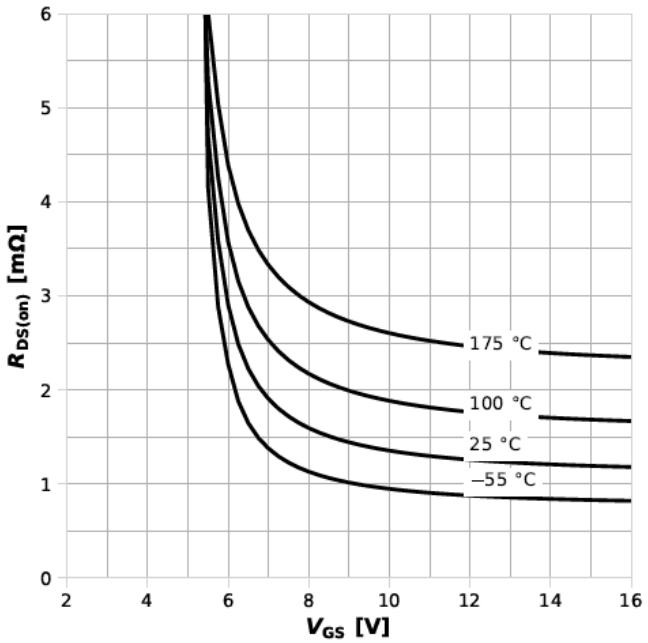
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



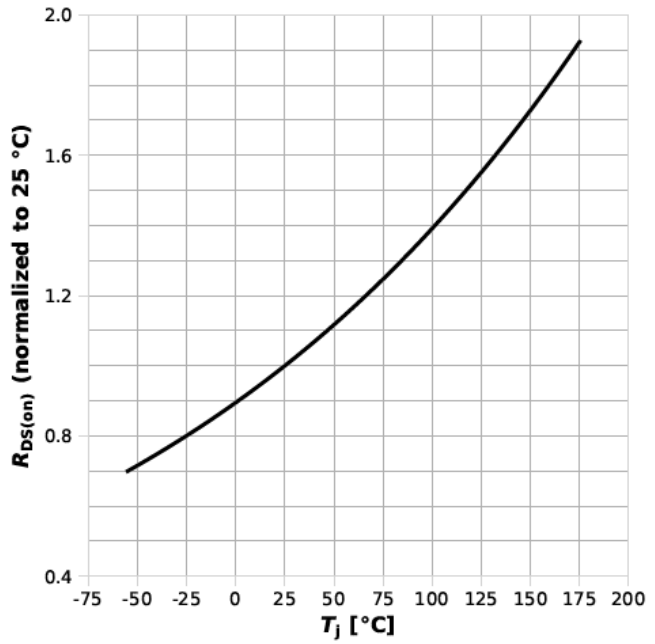
I_D=f(V_{GS}), $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



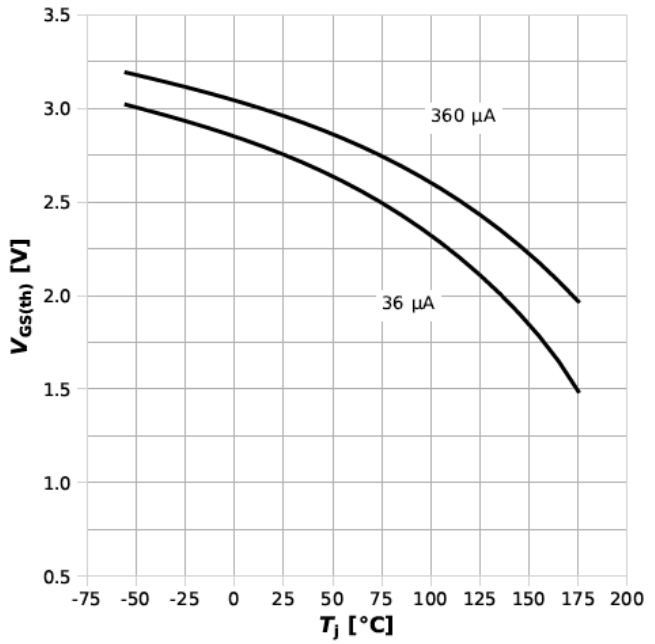
$R_{DS(on)}$=f(V_{GS}), I_D=50 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



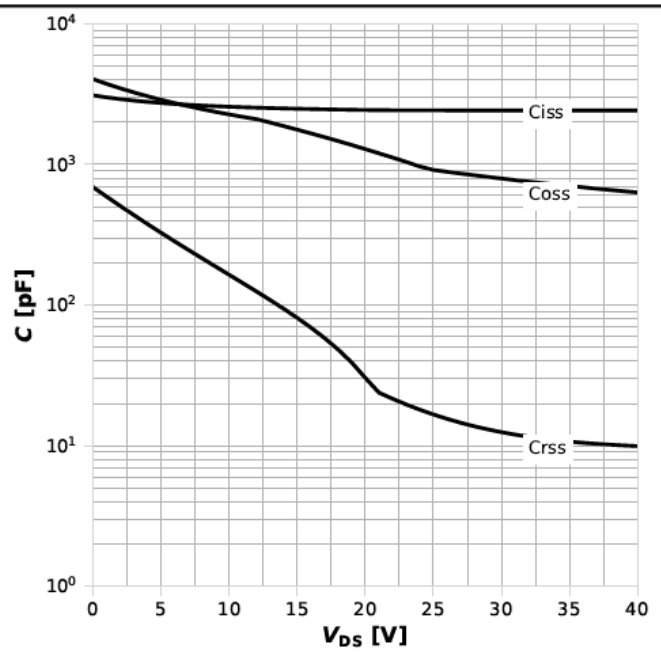
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



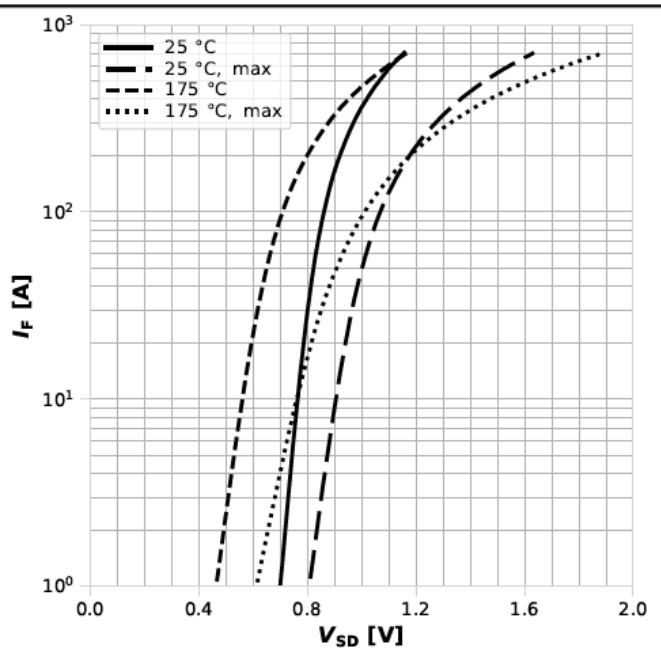
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

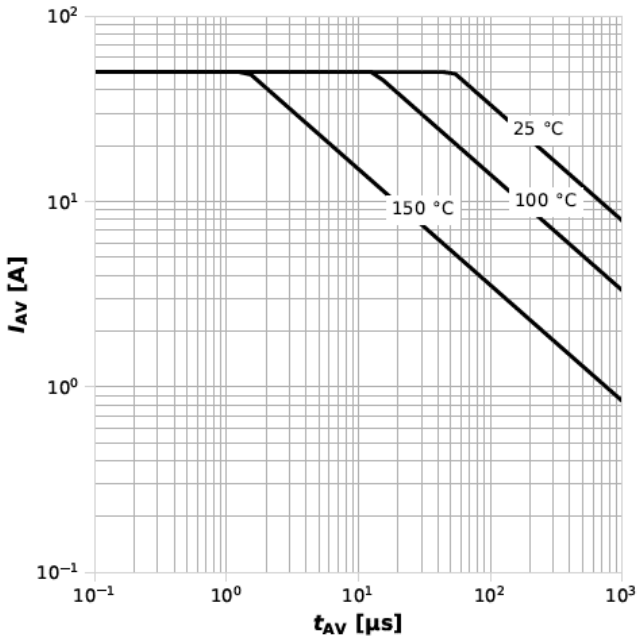
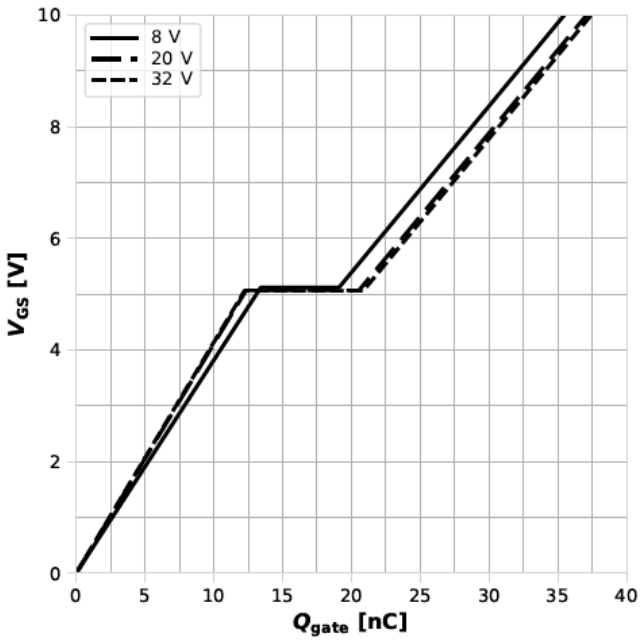
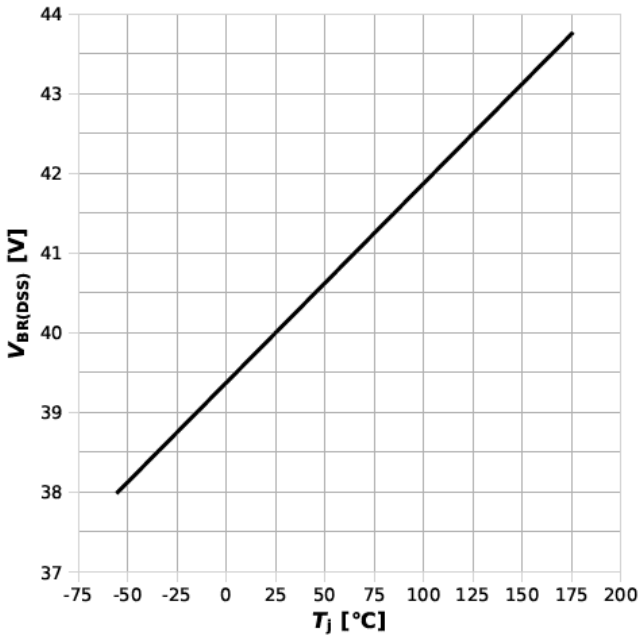
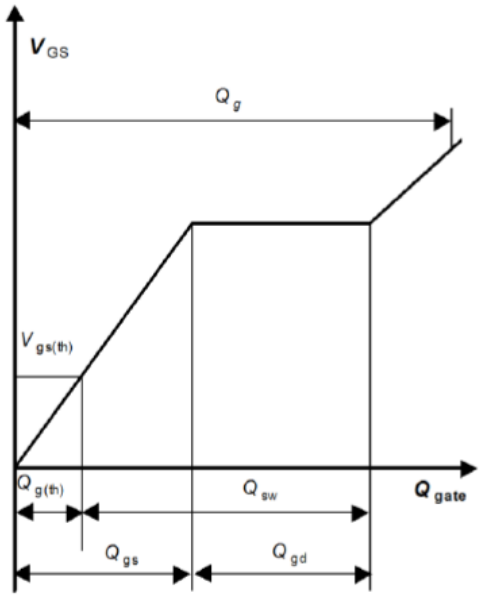
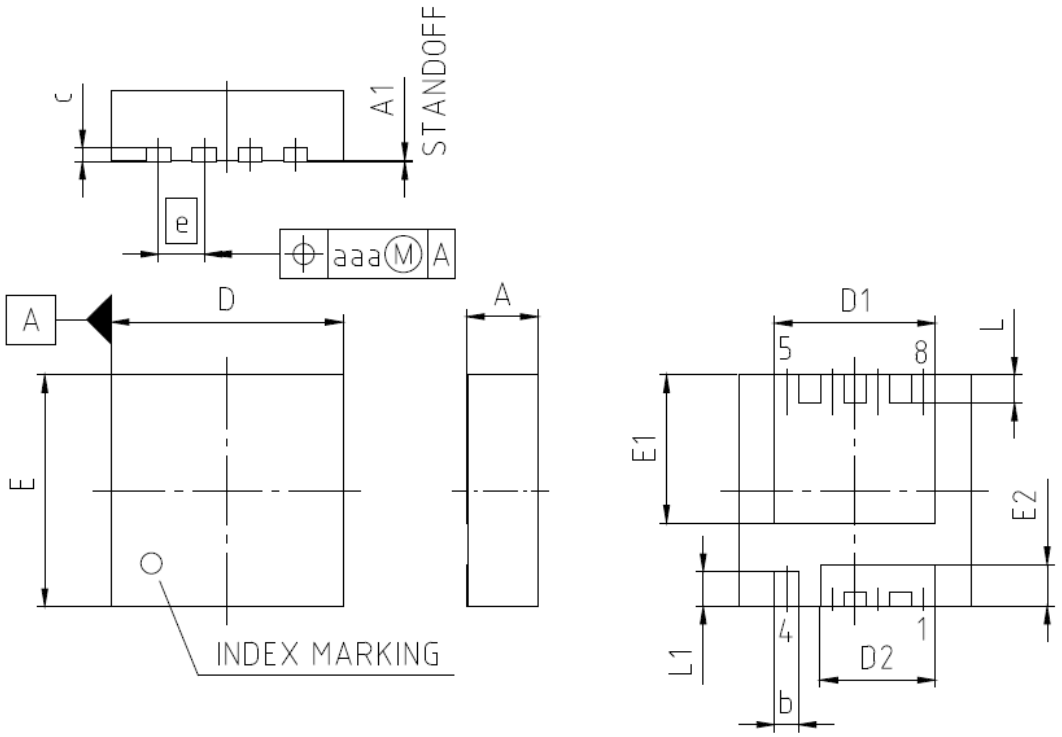
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 封装外形



PACKAGE - GROUP NUMBER:	PG-TSDSON-8-U03	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.10
A1	0	0.05
b	0.24	0.44
c	0.10	0.30
D	3.20	3.40
D1	2.19	2.39
D2	1.54	1.74
E	3.20	3.40
E1	2.01	2.21
E2	0.50	0.70
e	0.65	
L	0.30	0.50
L1	0.40	0.60
aaa	0.06	
N	8	

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

图 1　　PG-TSDSON-8 外形图，尺寸单位为毫米

修订记录

ISZ015N04NM7V

Revision 2025-04-22, Rev. 1. 0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-04-22	Release of final version

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