iSSR60V4A0R1H, iSSR60V2A5R1H
Infineon coreless-transformer advanced solid-state relay

Features

✓ RoHS

Green

- Single-channel solid-state relay
- For use in DC and AC applications with up to 380 V peak
- Typical output current up to 4 A (tbd) using CoolMOS™ S7 technology
- Logic-level control input
- Precise overtemperature protection
- Ultrafast overcurrent protection
- Dynamic Miller clamping
- High common-mode transient immunity CMTI > 200 kV/µs
- Suitable for 24 V supply using additional drop-out resistor
- Galvanically isolated input
- UL 1577 certification V_{ISO} = 5.7 kV (rms) for 1 min certification (planned)
- IEC 60747-17 certification V_{IOTM} = 8 kV (peak) for 1 min certification (planned)

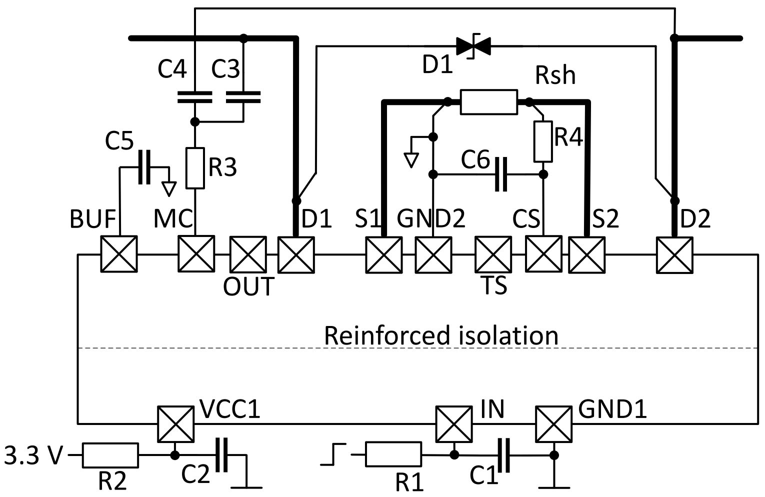
Potential applications

- Industrial automation I/O cards
- Smart home I/O cards
- Online UPS/Industrial UPS
- Residential and commercial HVAC
- Industrial and servo drives

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22, and J-STD-020.

Description



Typical application

iSSR60VxAxR1H Infineon solid-state relays are galvanically isolated solid-state relays using Infineon's benchmark CoolMOS™ transistors in PG-DSO-22-3 package. They provide a typical output current of up to 4 A AC. The input logic pin operates on a wide input voltage range from 3 V to 15 V using CMOS threshold levels to support 3.3 V microcontrollers. All variants have an input undervoltage lockout (UVLO).

Energy transfer across the isolation barrier is realized by Infineon's coreless transformer technology. All variants have ultra-fast acting protection features to protect against overcurrent and overtemperature. Active shutdown and dynamic Miller clamping enable to keep the relay in off-state even under demanding situations, such as electric fast transients.

Table 1 **Ordering information**

Product type	Output configuration	Typical load current	Certification	Package marking
iSSR60V4A0R1H	A (for AC and DC)	4 A	IEC 60747-17, UL 1577 (planned)	iSSR60V4A0R1H
iSSR60V2A5R1H	A (for AC and DC)	3 A	IEC 60747-17, UL 1577 (planned)	iSSR60V2A5R1H

Table 2 **Related evaluation board**

Board name	Solid-state relay	Load current (DC or RMS)	Short description
Eval-ISSR60V4A0R1H	iSSR60V4A0R1H	4 A ($T_{J,MOSFET}$ = 25°C)	An AC-current evaluation board with iSSR60V4A0R1H solid-state relay featuring shunt-based overcurrent protection, integrated MOSFET-sensor overtemperature protection, and dynamic Miller clamping. Its outstanding turn-on and turn-off performance enables the use for high inrush current systems.

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1 Block diagram reference

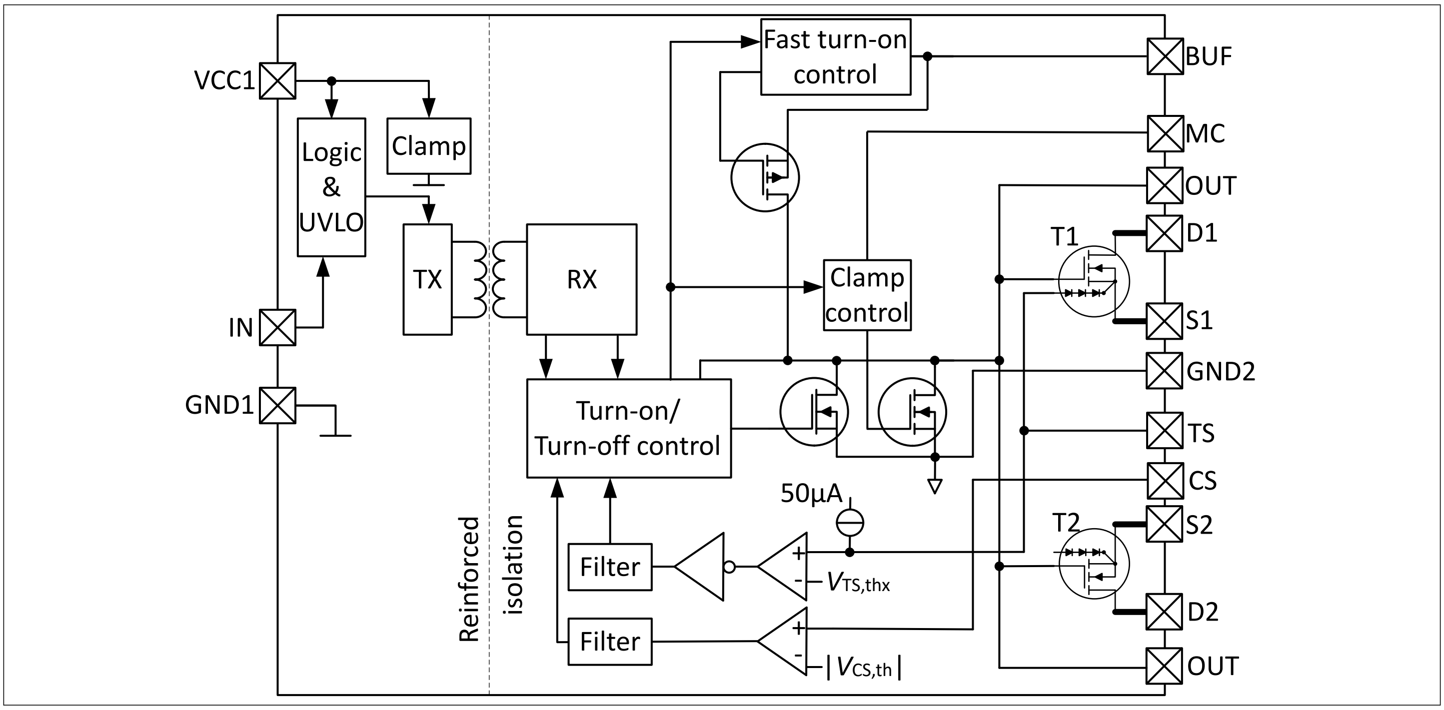

Figure 2 **Block diagram**

2 Pin configuration and description

Pin configuration PG-DSO-22-3

Table 3 **Pin configuration**

Pin No.	Name	Function
1	*NC*	Not connected
2	*NC*	Not connected
3	*IN*	IN
4	*VCC1*	VCC1
5	*GND1*	Reference for the input side
6	*GND1*	Reference for the input side
7	*NC*	Not connected
8	*NC*	Not connected
9	*D2*	Drain of MOSFET 2
10	*D2*	Drain of MOSFET 2
11	*S2*	Source of MOSFET 2
12	*NC*	Not connected
13	*GND2*	Reference for the output side
14	*OUT*	Gate voltage of the two switching MOSFETs (for productive testing only)
15	*MC*	Input for dynamic Miller clamping

(table continues...)

Table 3 (continued) Pin configuration

Pin No.	Name	Function
16	*BUF*	Connection to buffer capacitor
17	*CS*	Input for current sensor voltage
18	*GND2*	Reference for the output side
19	*TS*	Output for temperature sensor signal (for productive testing only)
20	*S1*	Source of MOSFET 1
21	*D1*	Drain of MOSFET 1
22	*D1*	Drain of MOSFET 1

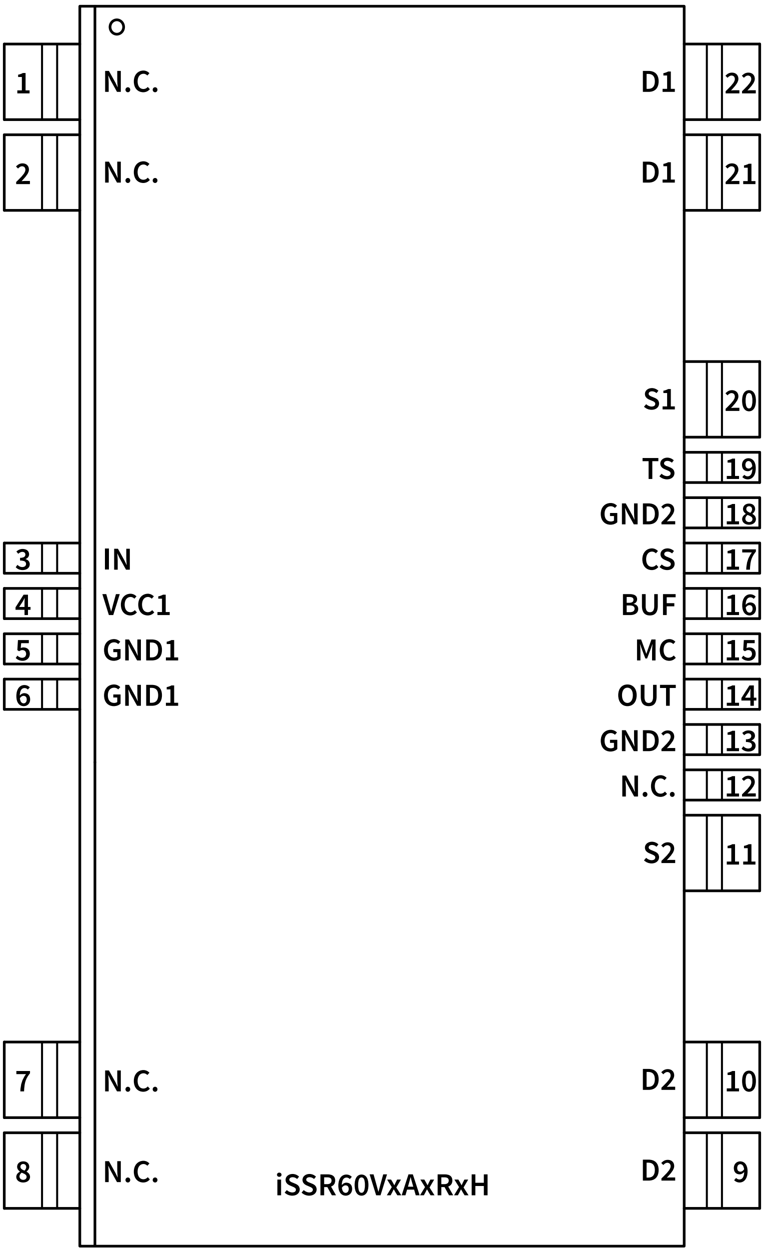

Figure 3 PG-DSO-22-3 (top view)

Pin description (iSSR60V4A0H1, iSSR60V2A5R1H)

- *IN*: Logic input control terminal, can be shorted with terminal *VCC1* for emulating a two-terminal input control.
- *VCC1*: Input side supply voltage.
- *GND1*: Input side reference voltage.
- *D1*: Drain of the switching MOSFET1. *D1* can be connected to *D2* for paralleling the two switching MOSFETs.
- *S1*: Source of the switching MOSFET1. *S1* can be connected to *S2* for paralleling the two switching MOSFETs.
- *GND2*: Output side reference voltage
- *OUT*: Gate voltage of the switching MOSFETs. This output is controlled by *IN*, *VCC1*, and potential triggering of the protection thresholds. Connecting any circuits to terminal *OUT* is not recommended
- *MC*: Connecting terminal of the coupling capacitor for dynamic Miller clamping. The terminal has to be kept floating, if the dynamic Miller clamp is not used
- *BUF*: Connecting terminal of the buffer capacitor for accumulating energy before turn-on
- *CS*: Input for the current sense signal. Terminal *CS* can be shorted to GND2 to disable overcurrent protection
- *TS*: A small capacitor value to GND2 can be added to this terminal for filtering the temperature sensor signal
- *S2*: Source of the switching MOSFET2. *S2* can be connected to *S1* for paralleling the two switching MOSFETs
- *D2*: Drain of the switching MOSFET2. *D2* can be connected to *D1* for paralleling the two switching MOSFETs

3 Electrical characteristics and parameters

3.1 Absolute maximum ratings

Table 4 **Absolute maximum ratings**

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only. Operating the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Device reliability may be affected by exposure to absolute-maximum-rated conditions for extended periods of time. All voltages are referenced to their respective GND (GND1 for input side pins and GND2 for output-side pins) unless specified otherwise.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input-to-output offset voltage	V_{OFFSET}	-1200		1200	V	[1] $V_{OFFSET} = \|V_{GND1} - V_{GND2}\|$
Input supply voltage	V_{VCC1}	-10		4.25	V	
Input logic voltage (terminal IN)	V_{IN}	-10		15	V	
Output voltage at terminal OUT	V_{OUT}	-0.3		20	V	Reference to GND2
Voltage at terminal MC	V_{MC}	-0.3		3.6	V	Reference to GND2
Voltage at terminals CS, S1, S2 and TS (static)	V_{CS} V_{S1} V_{S2} V_{TS}	-1.2		4	V	Reference to GND2
Voltage at terminals CS and TS (dynamic)	$V_{CS,dyn}$ $V_{S1,dyn}$ $V_{S2,dyn}$ $V_{TS,dyn}$	-2		6	V	Reference to GND2, $0 < I_{CS,dyn} <$ 10 mA, $t_p < 2$ µs, $d < 0.001$ $0 < I_{TS,dyn} < 10$ mA, $t_p < 2$ µs, $d < 0.001$
Voltage at terminal BUF	V_{BUF}	-0.3		20	V	Reference to GND2
Drain-source voltage per MOSFET	V_{DS}			600	V	$T_J = 25$ °C
Input supply current	I_{VCC1}	0		120	mA	
Input logic current (terminal IN)	I_{IN}			10	mA	
Current at terminal OUT (static)	I_{OUT}	-10		10	mA	$V_{VCC1} = V_{IN} = 0$
Current at terminal OUT (dynamic)	$I_{OUT,dyn}$	-100		100	mA	$V_{VCC1} = V_{IN} = 0$; $t_p < 10$ µs for negative current pulses; $t_p <$ 1 µs for positive current pulses
Current at terminal MC (static)	I_{MC}	-6		6	mA	Reference to GND2
Current at terminal MC (dynamic)	$I_{MC,dyn}$	-100		100	mA	$t_p < 1$ µs; $d < 1\%$
Current at terminals CS and TS	I_{CS}, I_{TS}	-1		1	mA	Reference to GND2
Current at terminal BUF (static)	I_{BUF}	-10		10	mA	
Current at terminal BUF (dynamic)	$I_{BUF,dyn}$	-1		1	A	$t_p < 1$ µs
Drain current per MOSFET	I_D	-4		4	A	$V_{VCC1} = V_{IN} = 3.3$ V, $T_a = 25$ °C, iSSR60V4A0R1H
Drain current per MOSFET	I_D	-3		3	A	$V_{VCC1} = V_{IN} = 3.3$ V, $T_a = 25$ °C , iSSR60V2A5R1H

(table continues...)

Table 4 (continued) Absolute maximum ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only. Operating the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Device reliability may be affected by exposure to absolute-maximum-rated conditions for extended periods of time. All voltages are referenced to their respective GND (GND1 for input side pins and GND2 for output-side pins) unless specified otherwise.

Parameter	**Symbol**	**Values**			**Unit**	**Note or condition**
		Min.	**Typ.**	**Max.**		
Reverse diode current per MOSFET	I_F			1	A	V_{IN} = 0 V, T_A = 85 °C
Non-repetitive pulsed drain current per MOSFET	$I_{D,pulse}$	-40		40	A	T_C = 25 °C, pulse width is limited by $T_{J,max}$, iSSI60V4A0R1H
Non-repetitive pulsed drain current per MOSFET	$I_{D,pulse}$	-20		20	A	T_C = 25 °C, pulse width is limited by $T_{j,max}$, iSSI60V2A5R1H
Avalanche current, single pulse per MOSFET	I_{AS}			2.7	A	
Avalanche energy, single pulse per MOSFET	E_{AS}			0.45	mJ	I_D = 2.7 A, V_{DD} = 50 V
MOSFET dv/dt ruggedness	dv_{DS}/dt			20	V/ns	[2] V_{DS} = 0 V to 300 V
Reverse diode dv/dt ruggedness	dv_{SD}/dt			5	V/ns	[2] V_{DS} = 0 V to 300 V, I_{SD} ≤ 4 A, T_j = 25 °C
Maximum diode-commutation speed	di_f/dt			800	A/µs	V_{DS} = 0 V to 300 V, I_{SD} ≤ 4 A, T_j = 25 °C
Power dissipation, input side	P_{DIN}			200	mW	T_A = 85°C [3]
Power dissipation, output part	P_{DOUT}			4.5	mW	Control IC only, T_A = 85 °C [4]
Power dissipation, MOSFETs	$P_{D,MOS}$			1.08	W	T_A = 85°, iSSR60V4A0R1H, power equally distributed on both MOSFETs
Power dissipation, MOSFETs	$P_{D,MOS}$			0.96	W	T_A = 85 °C, iSSR60V2A5R1H, power equally distributed on both MOSFETs
ESD robustness, human-body model	$\|V_{ESD,HBM}\|$	2			kV	[5]
ESD robustness, charged-device model	*ESD,CDM*			TC 1000	–	[6]
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_{ST}	-55		150	°C	

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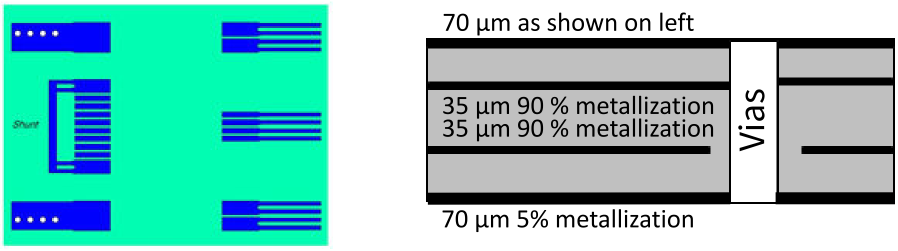
[1] For functional isolation operation only
[2] The dv/dt has to be limited through appropriate measures, e.g., snubbers.
[3] PG-DSO-22-3: derating of power above T_j = tbd°C with tbd mW/°C, layout 2s2p (JESD 51-5 / JESD 51-7).
[4] PG-DSO-52-xx: derating of power above T_j = tbd°C with tbd mW/°C, layout 2s2p (JESD 51-5 / JESD 51-7).
[5] According to ANSI/ESDA/JEDEC-JS-001-2017 (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).
[6] According to ANSI/ESDA/JEDEC-JS-002-2014 (TC = highest test condition passed according to AEC-Q100-011 Rev D).

3.2 Thermal specifications

Table 5 **Thermal specifications**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Characterization parameter, junction-to-package (top)	Ψ_{Jtop}		1.54		K/W	T_A = 85 °C, PG-DSO-22-3, reference design
Thermal resistance, junction-to-ambient	R_{THJA}			30	K/W	T_A = 85 °C, iSSR60V4A0R1H, reference design
Thermal resistance, junction-to-ambient	R_{THJA}			34	K/Wm	T_A = 85 °C, iSSR60V2A5R1H, reference design



Reference design PCB stack design

Figure 4 **Thermal reference design**

3.3 Recommended operating conditions

Table 6 **Recommended operating conditions**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input supply voltage	V_{VCC1}	2.85	3.3	3.5	V	V_{VCC1} - V_{GND1}
Voltage at terminals CS (static)	V_{CS}	-0.5		2.7	V	V_{CS} - V_{GND2}
External input-supply capacitance including tolerances of the capacitor	$C_{\mathrm{VCC1,ext}}$			4.7	nF	V_{VCC1} - V_{GND1}
External capacitance at terminal TS including tolerances of the capacitor	$C_{\mathrm{TS,ext}}$			1.5	nF	V_{TS} - V_{GND2}
Ambient temperature	T_A	-40		125	°C	–
Junction temperature of the solid-state isolator	T_J	-40		125	°C	–
Junction temperature of the power MOSFETs	T_J	-40		150	°C	–
High-level common-mode transient immunity of the solid-state isolator	$\lvert\mathrm{CM}_\mathrm{H}\rvert$			200	V/ns	V_{CM} = 1500 V
Low-level common-mode transient immunity of the solid-state isolator	$\lvert\mathrm{CM}_\mathrm{L}\rvert$			200	V/ns	V_{CM} = 1500 V

3.4 Electrical characteristics

The minimum and maximum electrical characteristics include the spread of values over supply voltages and temperatures within the operating parameters. Minimum and maximum characteristics are verified by characterization/design. Electrical characteristics are tested in production at T_A = 25°C. Typical values represent the median values measured at supply voltage V_{VCC1} = 3.3 V, and T_A = 25°C. All voltages are referenced to their respective GND (GND1 for input side pins and GND2 for output-side pins). This is valid for all electrical characteristics unless specified otherwise.

3.4.1 Power supply

Table 7 Power supply

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
UVLO threshold, input side (power up)	V_{UVLOH1}	2.7	2.775	2.85	V	V_{VCC1} - V_{GND1}
UVLO threshold, input side (power down)	V_{UVLOL1}	2.6	2.68	2.75	V	V_{VCC1} - V_{GND1}
UVLO hysteresis, input side	V_{HYS1}	70			mV	V_{UVLOH1}- V_{UVLOL1}
Supply current at terminal VCC1	I_{VCC1}	14	16	19	mA	V_{VCC1} = 3.3 V, I_{OUT} = 0 mA
Standby supply current at terminal VCC1	$I_{IN,STBY}$		1.4	2.5	mA	V_{VCC1} = 3.3 V, V_{IN} = 0 V
Off-time before turn-on	$t_{OFF,VCC1}$	25			µs	[1] $V_{VCC1} < V_{UVLOL1}$

1) Parameter is not subject to production test - verified by design/characterization.

3.4.2 Logic input

Table 8 Logic input

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
IN low-input threshold voltage	V_{IL}	1.0	1.2		V	V_{IN} - V_{GND1}
IN high-input threshold voltage	V_{IH}		2.1	2.3	V	V_{IN} - V_{GND1}
IN low/high hysteresis	$V_{IN,HYS}$	0.7			V	V_{IH} - V_{IL}
IN pull down resistor	$R_{IN,PD}$	200			kΩ	V_{IN} = 2.5 V
Off-time before turn-on	$t_{OFF,IN}$	25			µs	[1] V_{VCC1} = 3.3 V, $V_{IN} < V_{IL,min}$, C_{BUF} = 68 nF

1) Parameter is not subject to production test - verified by design/characterization.

3.4.3 Gate drive

Table 9 Gate drive

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output voltage	V_{OUT}	10	17	20	V	V_{OUT} - V_{GND2}, $V_{VCC1} = V_{IN} = 3.3$ V, $I_{OUT} = 0$ A
Low-level output resistance	R_{OL}	5	8.5	12	Ω	$V_{VCC1} = 0$, $V_{OUT} < 0.5$ V

3.4.4 Fast turn-on

Table 10 Fast turn-on

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fast turn-on threshold (power up)	$V_{BUF,th}$	10.0	10.4	10.8	V	V_{BUF} - V_{GND2}

3.4.5 Dynamic Miller clamping

Table 11 Dynamic Miller clamping

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Dynamic Miller-clamp saturation current	I_{CLAMP}	500	1700		mA	[1] $V_{MC} = 2.5$ V; $V_{OUT} = 3$ V
Low-level output resistance during dynamic Miller clamping	$R_{OL,MC}$	0.7	1.5	3.5	Ω	$V_{MC} = 2.5$ V, $I_{OUT} = 10$ mA
Input resistance terminal MC	R_{MC}	400	500	600	Ω	$V_{VCC1} = 0$ V, $V_{MC} = 0.5$ V

1) Parameter is not subject to production test - verified by design/characterization.

3.4.6 Overcurrent protection

Table 12 Overcurrent protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overcurrent comparator-shutdown threshold	$\lvert V_{CS,th}\rvert$	185	200	215	mV	V_{CS} - V_{GND2}, $V_{VCC1} = V_{IN} = 3.3$ V
Overcurrent shutdown delay	$t_{PD,CS}$		0.375	1	µs	$V_{CS} = 300$ mV, $V_{OUT} = 2.5$ V
Overcurrent filter time	$t_{CS,filter}$	120	150	200	ns	[1] $\lvert V_{CS}\rvert = 0.3$ V

1) Parameter is not subject to production test - verified by design/characterization.

3.4.7 Overtemperature protection

Table 13 Overtemperature protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overtemperature comparator threshold	$V_{TS,th1}$	1.056	1.095	1.120	V	V_{IN} = 3.3 V, V_{TS} - V_{GND2}
Temperature-sensor bias current	$I_{TS,bias}$	40	50	60	µA	V_{VCC1} = V_{IN} = 3.3 V
Overtemperature shutdown delay	$t_{PD,TS}$			5	µs	V_{IN} = 3.3 V, V_{TS} = $V_{TS,th2}$ - 20 mV
Temperature-sensor filter time	$t_{TS,filter}$	1.9	2.7	3.5	µs	1) V_{VCC1} = 3.3 V, V_{TS} = $V_{TS,th2}$ -20 mV

3.4.8 MOSFET

Table 14 MOSFET

For applications with applied blocking voltage > 420V, customers are required to evaluate the impact of cosmic radiation in all applications at an early design phase.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600			V	V_{Dx} - V_{GND2}, V_{GS} = 0 V, I_D = 1mA, T_J = 25 °C
Reverse diode forward voltage	V_{SD}		0.81		V	V_{VCC1} = V_{IN} = 0 V, I_F = 4 A, T_J = 25 °C, iSSR60V4A0R1H
Reverse diode forward voltage	V_{SD}		0.81		V	V_{VCC1} = V_{IN} = 0 V, I_F = 2.5 A, T_J = 25 °C, iSSR60V2A5R1H
Drain-to-drain a.c. leakage current	$I_{DSS,AC}$		370		µA	1) V_{IN} = 0 V, $V_{D1\text{-}D2}$ = 230 V, f = 50 Hz sine wave, T_J = 25 °C, iSSR60V4A0R1H
Drain-to-drain a.c. leakage current	$I_{DSS,AC}$		240		µA	1) V_{IN} = 0 V, $V_{D1\text{-}D2}$ = 230 V, f = 50 Hz sine wave, T_J = 25 °C, iSSR60V2A5R1H
Off-state drain current per MOSFET	$I_{DS,off}$	0		2	µA	V_{DS} = 600 V, V_{IN} = 0 V, T_J = 25 °C, iSSR60V4A0R1H
Off-state drain current per MOSFET	$I_{DS,off}$	0		2	µA	V_{DS} = 600 V, V_{IN} = 0 V, T_J = 25 °C, iSSR60V2A5R1H
Off-state drain current per MOSFET iSSR60V4A0R1H	$I_{DS,off}$		20		µA	1) V_{DS} = 600 V, V_{IN} = 0 V, T_J = 150 °C
Off-state drain current per MOSFET iSSR60V2A5R1H	$I_{DS,off}$		15		µA	1) V_{DS} = 600 V, V_{IN} = 0 V, T_J = 150 °C
Drain-source on-state resistance of a single MOSFET	$R_{DS(on)}$		50		mΩ	V_{VCC1} = V_{IN} = 3.3 V, I_D = 4 A, T_J = 25 °C, iSSR60V4A0R1H
Drain-source on-state resistance of a single MOSFET	$R_{DS(on)}$		80		mΩ	V_{VCC1} = V_{IN} = 3.3 V, I_D = 2.5 A, T_J = 25 °C, iSSR60V2A5R1H

(table continues...)

Table 14 (continued) MOSFET

For applications with applied blocking voltage > 420V, customers are required to evaluate the impact of cosmic radiation in all applications at an early design phase.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Turn-on propagation delay input-to-output	$t_{d(on)}$		4.2		ms	[1] C_{BUF} = 68 nF, V_{DS} = 300 V, I_D = 1.5 A, V_{VCC1} = V_{IN} = 3.3 V
Turn-on rise time	t_r		156		ns	[1] C_{BUF} = 68 nF, V_{DS} = 300 V, I_D = 4 A
Turn-off propagation delay input-to-output	$t_{d(off)}$		7.33		µs	[1] C_{BUF} = 68 nF, V_{DD} = 300 V, I_D = 4 A
Turn-off fall time	t_f		158		ns	[1] C_{BUF} = 68 nF, V_{DS} = 300 V, I_D = 4 A
Turn-off fall time after protection (OCP or OTP)	$t_{f,prot}$		157		ns	[1] C_{BUF} = 68 nF, V_{DS} = 300 V, I_D = 4 A

1) Parameter is not subject to production test - verified by design/characterization.

4 Insulation and safety-related specifications

4.1 Safety-limiting values

Note: safety-limiting values define the operating conditions under which the isolation barrier can be guaranteed to stay unaffected. This corresponds with the maximum allowed junction temperature, as temperature-induced failures might cause significant overheating and eventually damage the isolation barrier.

Parameter	**Symbol**	**Value**	**Unit**	**Note or condition**
Maximum ambient safety temperature	T_S	150	°C	
Safety input power dissipation	P_{SI}	200	mW	Derating required above T_A = 120.6°C with 6.8 mW/°C, T_J = 150 °C
Safety input supply current	I_{SI}	50	mA	Derating required above T_A = 122 °C with 1.79 mA/°C, T_J = 150 °C
Safety output power dissipation	P_{SO}	4.5	mW	Derating required above T_A = 149°C with 4.5 mW/°C, T_J = 150 °C

4.2 Insulation characteristics

Parameter	**Symbol**	**Value**	**Unit**	**Note or condition**
External clearance	*CLR*	>8	mm	Shortest distance in air from any input to any output pin according to IEC 60664-1$^{1)}$
External creepage	*CRP*	>8	mm	Shortest distance over package surface from any input pin to any output pin according to IEC 60664-1$^{1)}$
Comparative tracking index	*CTI*	>600	V	According to IEC 60112
Material group		I		According to IEC 60112
Pollution degree		2		According to IEC 60664-1
Overvoltage category (According to IEC 60664-1)		I - IV I - IV I - III I-II		Rated mains voltage ≤ 150 V (rms) Rated mains voltage ≤ 300 V (rms) Rated mains voltage ≤ 600 V (rms) Rated mains voltage ≤ 1000 V (rms)
Climatic category		40/125/21		
Input-to-output isolation according to UL1577 Ed. 5 (planned)				
Input-to-output isolation voltage	V_{ISO}	5700	V_{rms}	$V_{TEST} = V_{ISO}$ for $t = 60$ s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ for $t = 1$ s (100% productive tests)
Input-to-output isolation according to IEC 60747-17 (planned)				
Maximum rated transient isolation voltage	V_{IOTM}	8000	V_{pk}	$V_{TEST} = V_{IOTM}$ for $t_{ini} = 60$ s (type test and sample test) $V_{TEST} = 1.2 \times V_{IOTM}$ for $t_{ini} = 1$ s (routine test)
Maximum rated repetitive peak isolation voltage	V_{IORM}	1200	V_{pk}	According to Time Dependent Dielectric Breakdown (TDDB) test

Parameter	**Symbol**	**Value**	**Unit**	**Note or condition**
Apparent charge	q_{PD}	<5	pC	Method (b1) (routine test and type test pre-conditioning) $V_{PD(ini),b} = 1.2 \times V_{IOTM}$ for $t_{ini} = 1$ s $V_{PD(m)} = 1.875 \times V_{IORM}$ for $t_m = 1$ s Method (a) (type test, subgroup 1 final measurements) $V_{PD(ini),a} = V_{IOTM}$ for $t_{ini} = 60$ s $V_{PD(m)} = 1.6 \cdot V_{IORM}$ for $t_m = 10$ s3)
Impulse voltage	V_{IMP}	8000	V_{pk}	
Maximum surge isolation voltage	V_{IOSM}	11000	V_{pk}	$V_{TEST} \geq 1.3 \cdot V_{IMP}$ (type test)4)
Isolation resistance	R_{IO}	$>10^{12}$	Ω	$V_{IO} = 500\ V_{dc}$ for $t = 60$ s, $T_A = 25$ °C5)
Isolation resistance	R_{IO}	$>10^{11}$	Ω	$V_{IO} = 500\ V_{dc}$ for $t = 60$ s, $T_A = 125$ °C5)
Isolation resistance	R_{IO_S}	$>10^{9}$	Ω	$V_{IO} = 500\ V_{dc}$ for $t = 60$ s, $T_S = T_A = 150$ °C5)
Isolation capacitance	C_{IO}	2.9	pF	$f = 1$ MHz5)

1) Creepage and clearance requirements depend on the application and related end-equipment isolation standard. Care should be taken to keep the required creepage and clearance value on printed-circuit-board level.

2) Safety certification planned.

3) The partial discharge voltage $V_{PD(m)}$ applied during productive tests is greater (tbd $V_{pk} > 1.875 \times V_{IORM}$) to include the F_4 factor (1.1) required by end-equipment standards IEC 60664-1, IEC 62368-1, IEC 60950 ($V_{PD(m)} = F_1 \times F_2 \times F_3 \times F_4 \times V_{IORM} = 1.875 \times F_4 \times V_{IORM}$). The F_3 factor (1.25) is also considered for further stress of the insulation.

4) The surge test is performed in insulation oil to determine the intrinsic surge immunity of the insulation barrier.

5) The parameters apply to the product converted in a two terminals device with all terminals on side 1 connected together and all terminals on side 2 connected together.

5 Typical characteristics

Unless otherwise noted,the measurements are done with V_{VCC1}= 3.3 V.

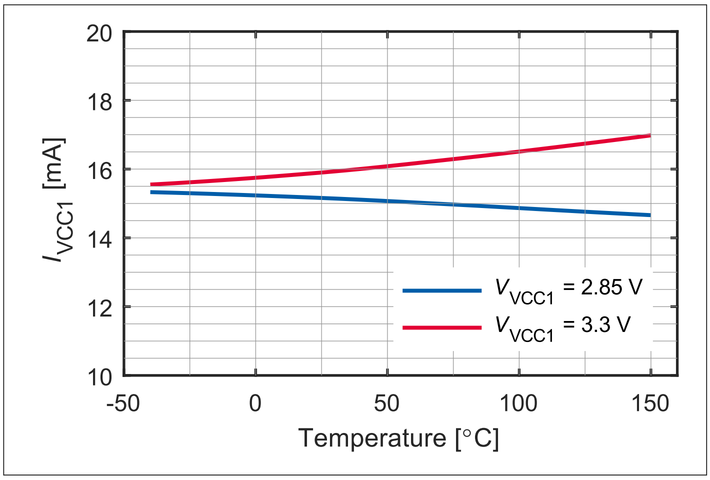


Figure 5 **Input supply current vs. temperature**

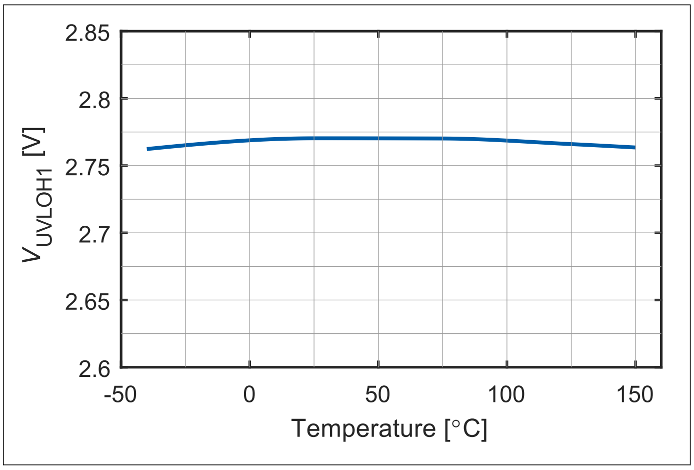


Figure 6 **UVLO threshold input side (power up) vs. temperature**

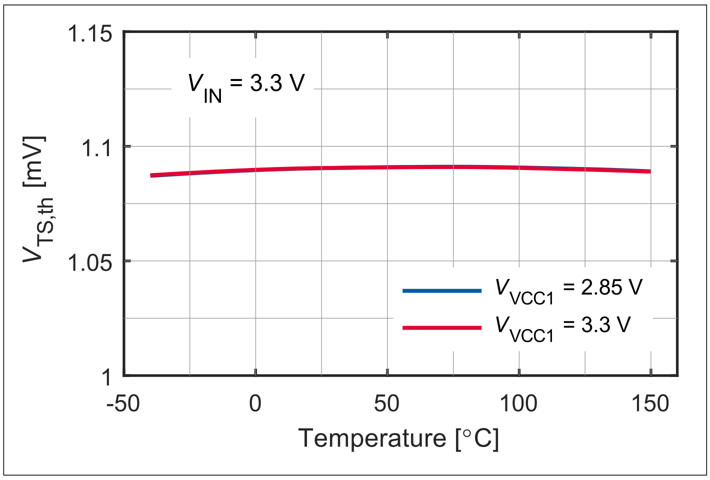


Figure 7 **Overtemperature comparator threshold voltage vs. temperature**

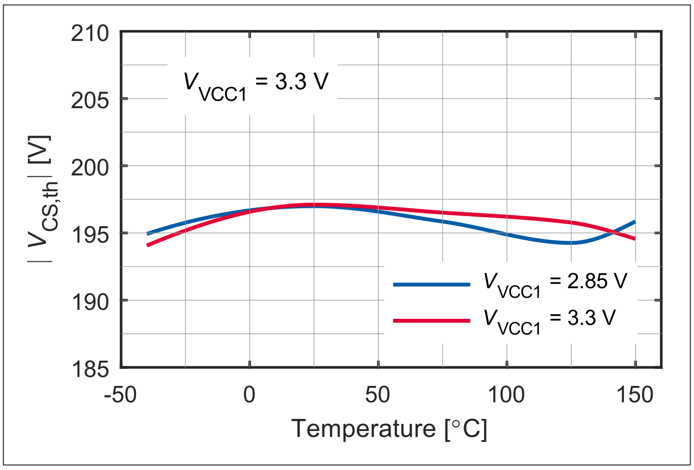


Figure 8 **Overcurrent comparator threshold voltage vs. temperature**

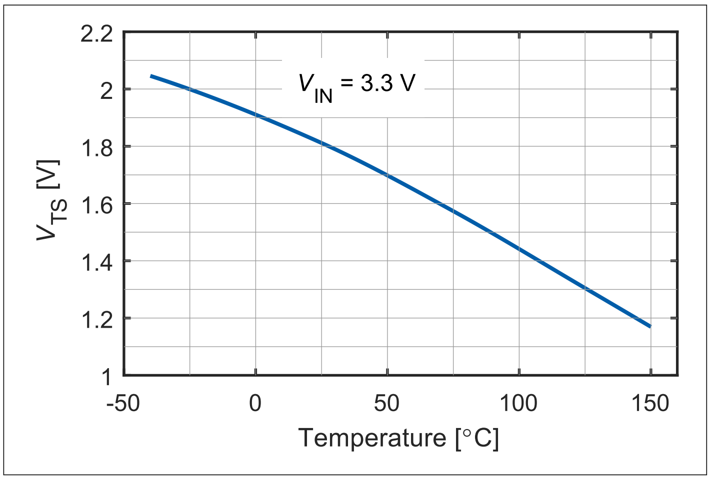


Figure 9 **Temperature sensor voltage vs. temperature**

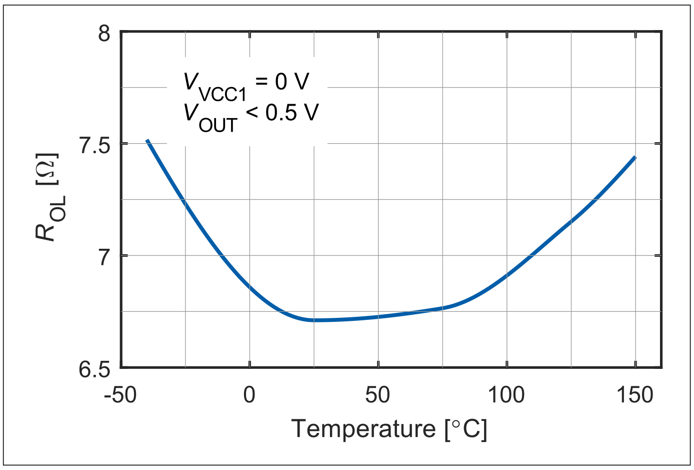


Figure 10 **Low level output resistance vs. temperature**

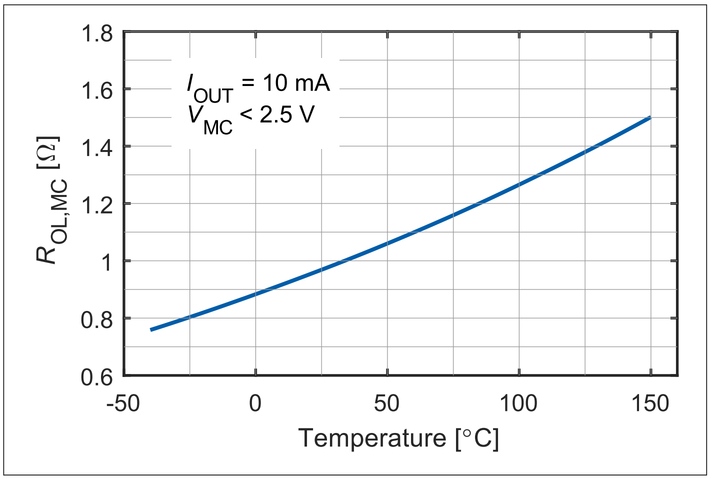


Figure 11 Low-level output resistance during dynamic Miller clamping vs. temperature

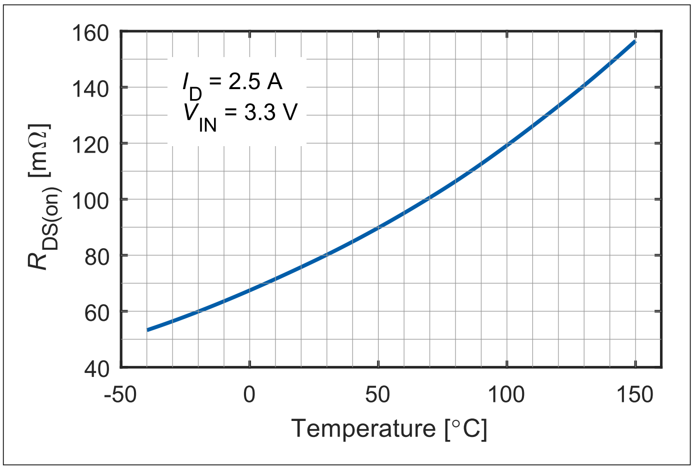


Figure 12 On-state resistance per MOSFET vs. temperature (iSSR60V2A5R1H)

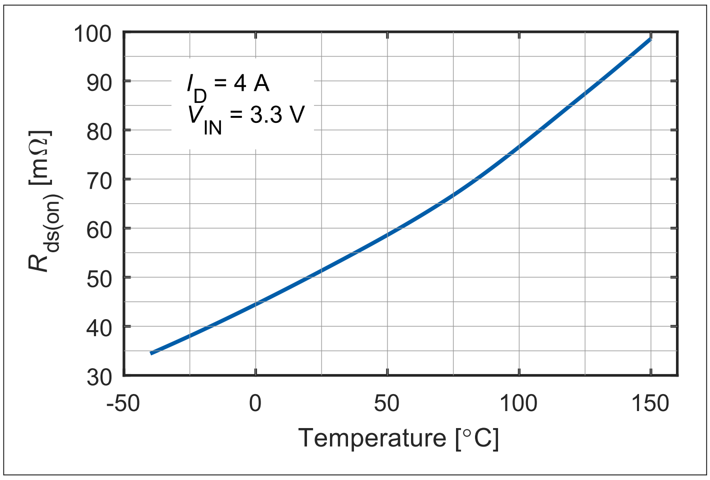


Figure 13 On-state resistance per MOSFET vs. temperature (iSSR60V4A0R1H)

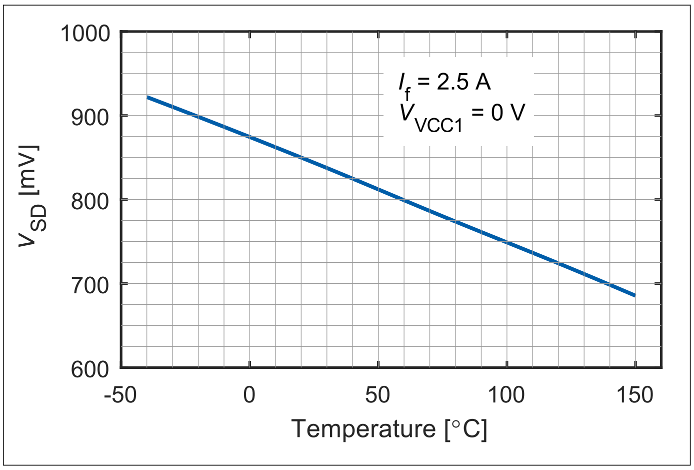


Figure 14 Reverse diode forward voltage vs. temperature (iSSR60V2A5R1H)

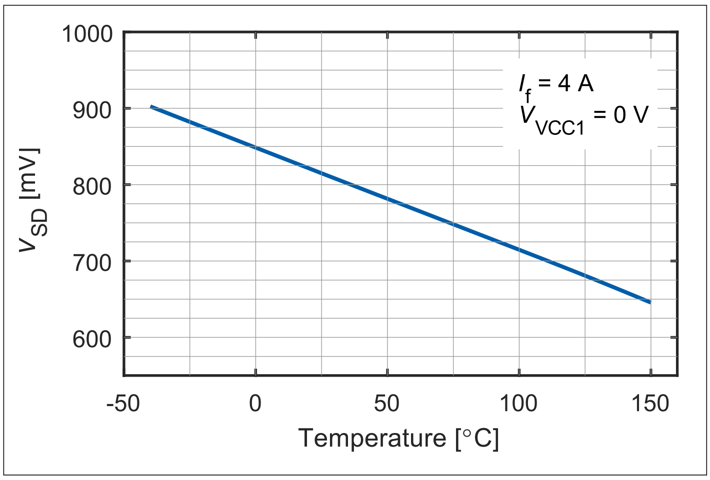


Figure 15 Reverse diode forward voltage vs. temperature (iSSR60V4A0R1H)

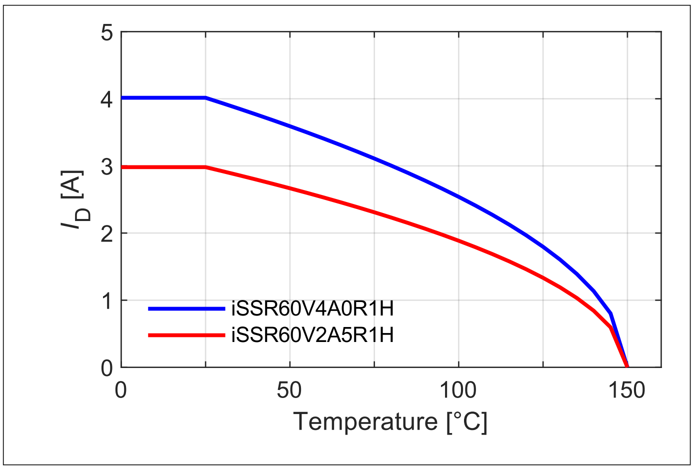


Figure 16 Maximum drain current per MOSFET (current equal in both MOSFETs)

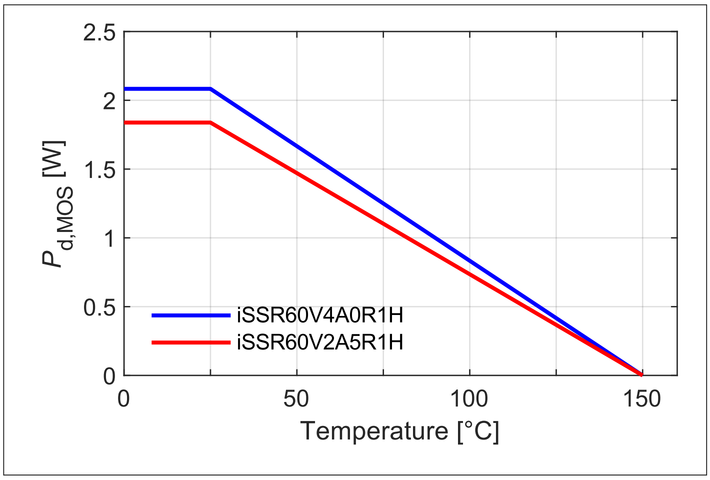


Figure 17 Maximum power dissipation per MOSFET (power dissipation equal in both MOSFETs)

6 Timing diagrams

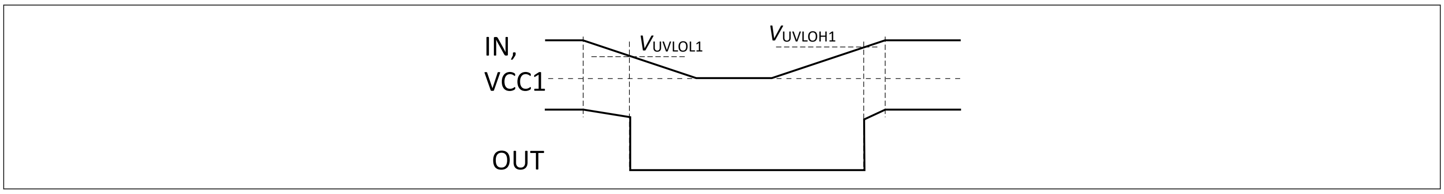


Figure 18 UVLO behavior

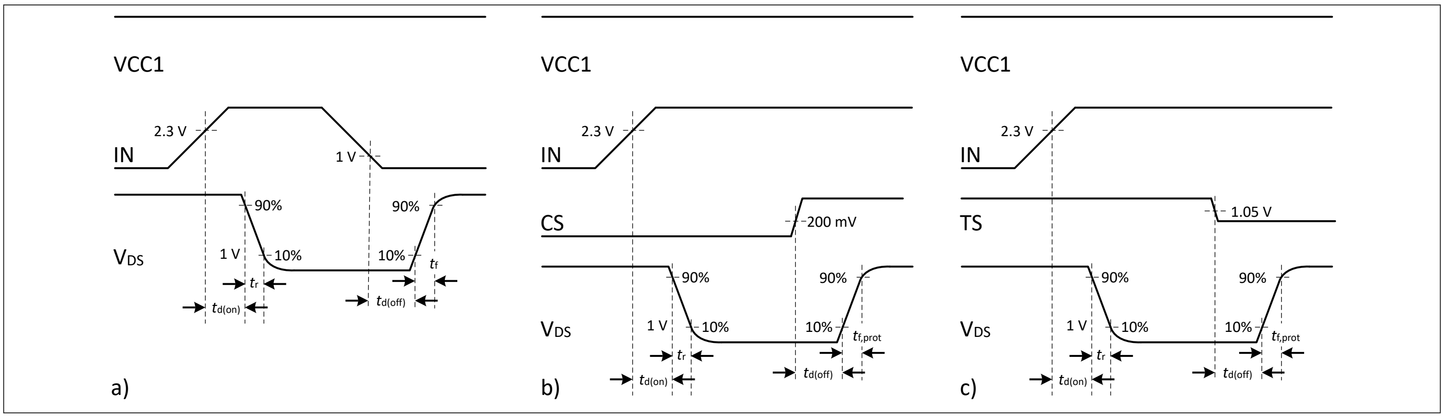


Figure 19 Turn-on and turn-off propagation delay, rise and fall time: a) normal switching, b) and c) protective turn-off with trigger at *CS* and *TS*

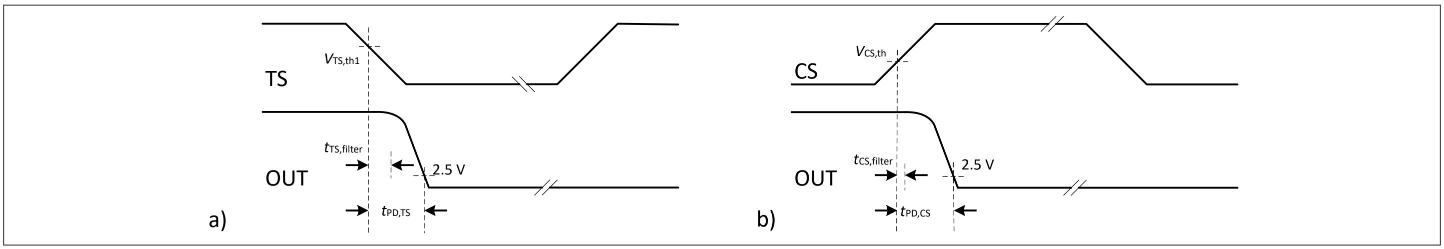


Figure 20 a) Over-temperature protection timing, b) Over-current protection timing

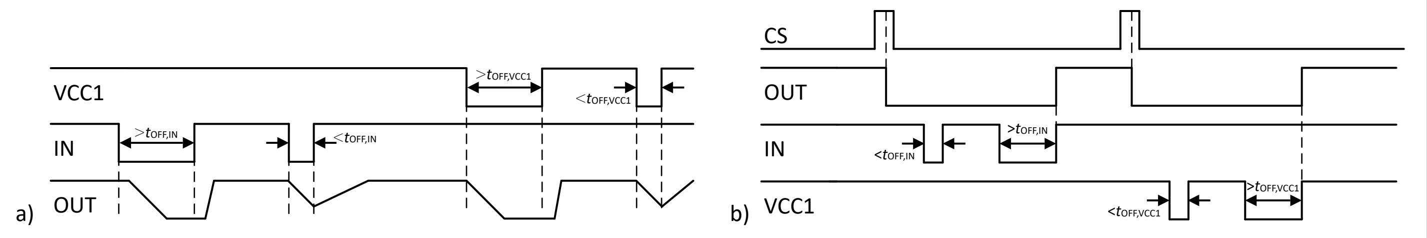


Figure 21 a) Off-time before turn-on, b) off-time after protection (example of overcurrent protection)

7 Functional description

The iSSR60VxAxR1H ICs from Infineon are compact, general-purpose solid-state relays. They are configured for use in both DC and AC applications. They offer advanced ultra-fast protection features enabling fast and easy design of highly reliable systems.

The integrated galvanic isolation between the input control side and the driving output stage grants additional safety. The solid-state relays ICs support direct connection of various signal sources like microcontrollers.

7.1 Input side

7.1.1 iSSR input-side supply

The input side of the iSSR product family is 3.3 V compatible and operates best with an input voltage tolerance of 5%. The power-up undervoltage threshold voltage is V_{UVLOH1}. It ensures sufficient output voltage for operating the output. The power-down undervoltage threshold is V_{UVLOL1}. The integrated supply is based on a shunt regulator that emulates a diode structure to simplify the designs. The device can then be supplied even by a voltage rail that exceeds the operating range by using a current-limiting resistor placed in series to the supply terminal *VCC1*. If no suitable resistor is used in series to the terminal *VCC1* for limiting the current, staying within the operating parameters is recommended to avoid unnecessary power dissipation in the input-side control IC.

The input side of the Infineon solid-state relay contains an integrated voltage supply buffer capacitor. External buffer capacitors for the supply voltage are not necessary, but can be used. The external buffer capacitance should not exceed $C_{\mathrm{VCC1,ext}}$ for supply voltages with large tolerances . However, if it can be guaranteed that the supply voltage never exceeds 3.5 V under any circumstance, the external capacitance can be higher.

In addition, the iSSR family provides a strong reverse-bias capability for the supply terminal *VCC1*. This enables all variants to operate in a differential operation with respect to their terminals *VCC1* and *GND1*.

A minimum off-time $t_{\mathrm{OFF,VCC1}}$ is required between the turn-off and turn-on signals to establish a defined "off" state on the output side of the isolator.

The products in the iSSR family can reset the protection at either terminal *VCC1* or terminal *IN*. Before any reset, ensure that the reset time is more than $t_{\mathrm{OFF,IN}}$ or $t_{\mathrm{OFF,VCC1}}$ before turning the protection event on again.

7.1.2 iSSR logic input

The iSSR family offers separate supply and control terminals. The control logic thresholds V_{IL} and V_{IH} at terminal *IN* are 3.3 V CMOS compliant and can be controlled directly from standard CMOS logic outputs. Note that the signal level at terminal *IN* can be substantially higher than the supply voltage at terminal *VCC1*. For example, it is possible to apply a 5 V signal while $V_{\mathrm{VCC1}} = 3.3$ V. The output acts in phase with the input control signal at terminal *IN*. Before turning on, a minimum off-time ($t_{\mathrm{OFF,IN}}$) must be considered for resetting the output side. If the equivalent input capacitance of the MOSFET is more than 100 pF, off times longer than $t_{\mathrm{OFF,IN}}$ might be needed.

The logic input is also safeguarded against reverse biasing. It can endure negative voltages with reference to *GND1* as stated in the absolute maximum ratings.

A new reset procedure has to be performed after a turn-off triggered by a protection event. The products in the iSSR family can perform this reset at either terminal *VCC1* or terminal *IN*. Before any reset, ensure that the reset time is more than $t_{\mathrm{OFF,IN}}$ before turning on again.

The solid-state relay can also operate with externally shorted terminals *VCC1* and *IN*. It is important to verify that sufficient current is supplied together with the 3.3 V control signal.

7.2 Output side

7.2.1 Fast turn-on

All variants of the iSSR products provide the fast turn-on feature. This further enforces the turn-on current by accumulating charge in an external buffer capacitor at terminal *BUF*. If the voltage at terminal *BUF* is equal or higher than the buffer threshold voltage $V_{BUF,th}$ and a turn-on condition is given on the control side, the accumulated charge is released to terminal *OUT*.

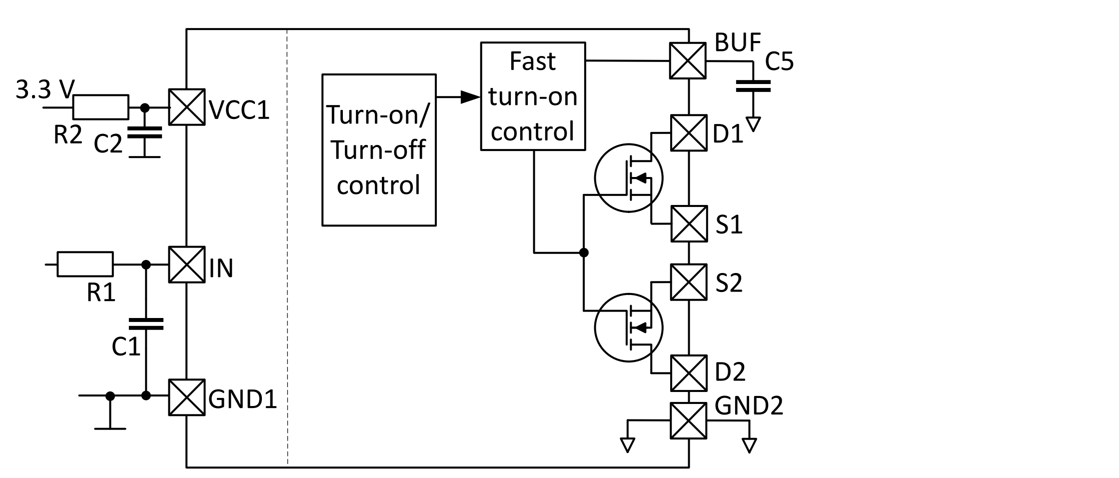


Figure 22 **Fast turn-on feature of iSSR60V4A0R1H and iSSR60V2A5R1H**

It is recommended to use a buffer capacitance of minimum 56 nF +/-10% to avoid a fast turn-on that yields an insufficient gate-source voltage for the power MOSFETs for iSSR60V4A0R1H. The related capacitance for iSSR60V2A5R1H should be a minimum of 39 nF +/-10%.

7.2.2 Normal turn-off

The normal turn-off feature is implemented in all variants. A turn-off signal from the input side activates the integrated depletion FET. The depletion FET discharges the gate node of the operating power transistors. The sink current of the iSSR family products is dimensioned to discharge the switching transistors within a few microseconds.

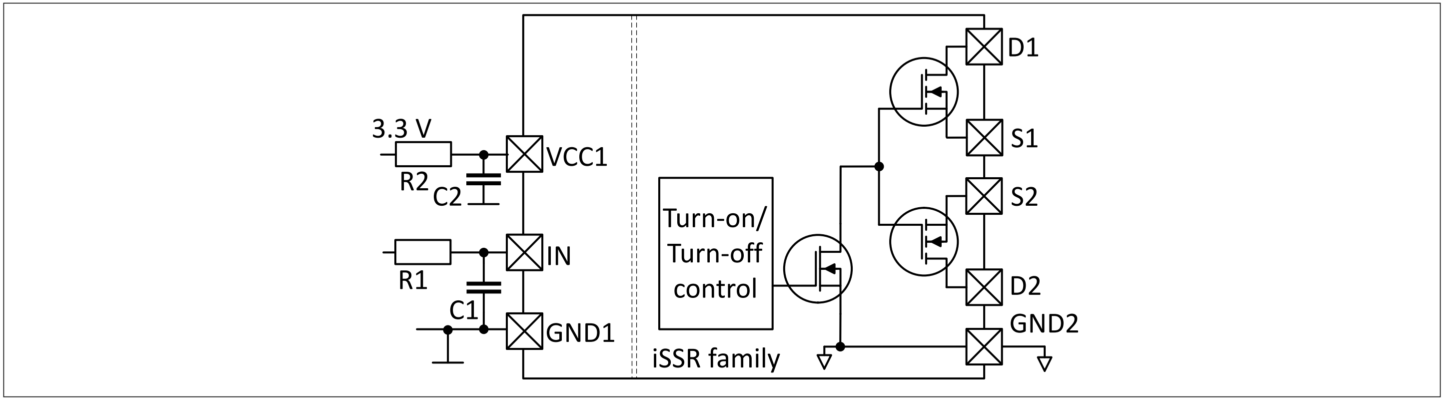


Figure 23 **Normal turn-off**

7.2.3 Fast turn-off

Overcurrent or overtemperature events trigger the fast turn-off feature of the products in the iSSR family. The fast turn-off feature enables these products to shut down the power transistors inside their safe operating area particularly during high-load operations. The iSSR family's saturation current of the fast turn-off is dimensioned to discharge the switching transistors faster than in a normal turn-off.

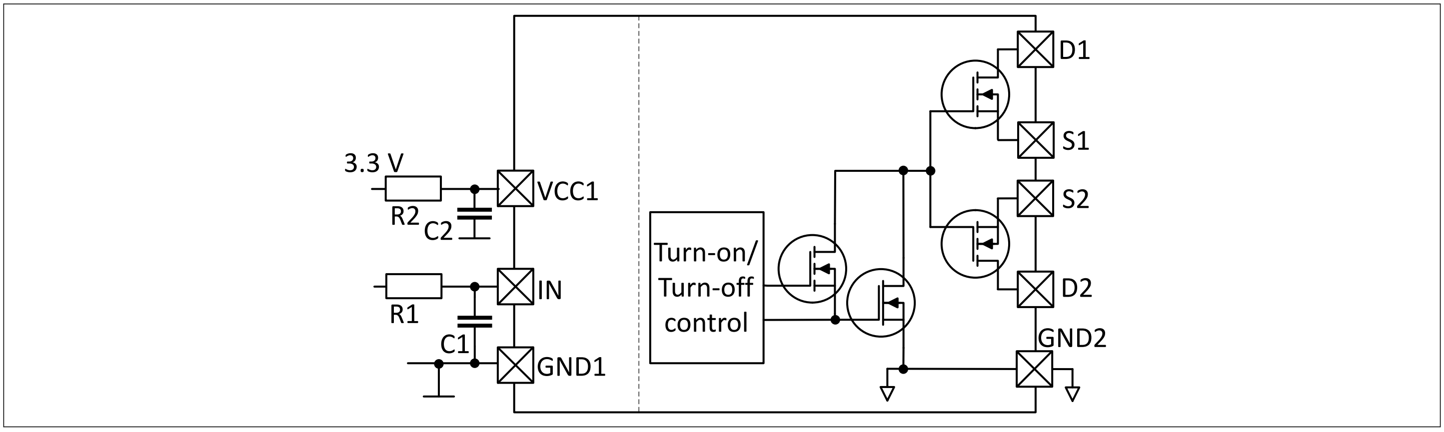


Figure 24 **Fast turn-off**

7.2.4 Dynamic Miller clamping (DMC)

The dV/dt applied by the connected AC voltage creates capacitive displacement currents through the parasitic capacitances of a power transistor. This can lead to a parasitic turn-on of the power switch during its "off"-state by increasing the voltage at the gate node of the power switch. The following three major effects can cause dV/dt to occur in installations:

- Surge voltages
- Fast electric transients (burst)
- dV/dt of the line voltage

  The dV/dt of the line voltage results in a relatively slow dV/dt of 320 V * 2*π * 50 Hz ~ 100 V/ms in 230 V AC grids. Many power transistors are inherently robust against parasitic turn-on under this condition. However, surge voltages and fast electric transients result in a much faster dV/dt and power transistors benefit from the dynamic Miller clamping feature

The dV/dt appearing at the drain also injects a current into the related terminals *MC* and activates the dynamic Miller clamp FET. The clamping FET ensures that the power switch is kept in the “off” state. It is activated by connecting the power switch's drain to terminal *MC* with a suitable capacitor.

Clamping elements such as Zener diodes between terminals *MC* and *GND2* ensures that the device stays below the absolute maximum ratings.

7.2.5 Overcurrent protection

The overcurrent protection feature detects excessive positive or negative current through the power transistor. It uses the voltage drop at an external shunt resistor to trigger a comparator with a fixed threshold $|V_{\mathrm{CS,th}}|$ at terminal *CS*. The dimensioning of the shunt follows this equation:

$$R_{\mathrm{sh}} = \frac{|V_{\mathrm{CS,\,th}}|}{I_{\mathrm{pk,\,max}}}$$

Note that $V_{\mathrm{CS,th}}$ can be positive or negative. Once triggered, the protection reacts quickly and turns off the iSSR power transistors in a very short time. This allows the iSSR family to support the AC15 system tests according to IEC 60947-5-1 under appropriate operating conditions. The integrated noise filter has a filter time of $t_{\mathrm{CS,filter}}$ and can be backed up by an external RC filter. However, having as little external filtering as possible is recommended to get a quick reaction time in case of an overcurrent condition.

The triggering of the overcurrent protection feature leads to the latched turn-off of the power switch and requires a reset on the input side.

7.2.6 Overtemperature protection

The overtemperature protection feature of the Infineon iSSR family uses the on-chip integrated temperature sensor of the iSSR's power MOSFETs.

The iSSR family products provide a constant bias current $I_{TS,bias}$ for the temperature sensor. The constant current generates a temperature-dependent voltage at the temperature sensor. The sensor voltage is connected to terminal *TS*, and the terminal voltage is compared to the threshold $V_{TS,th}$. The integrated comparator includes a noise filter of duration $t_{TS,filter}$ to safely detect the sensor signal that can be complemented by an external RC filter. The external capacitor must be below the maximum value of $C_{TS,ext}$.

The triggering of the overtemperature protection feature leads to the latched turn-off of the power switch and requires a reset on the input side.

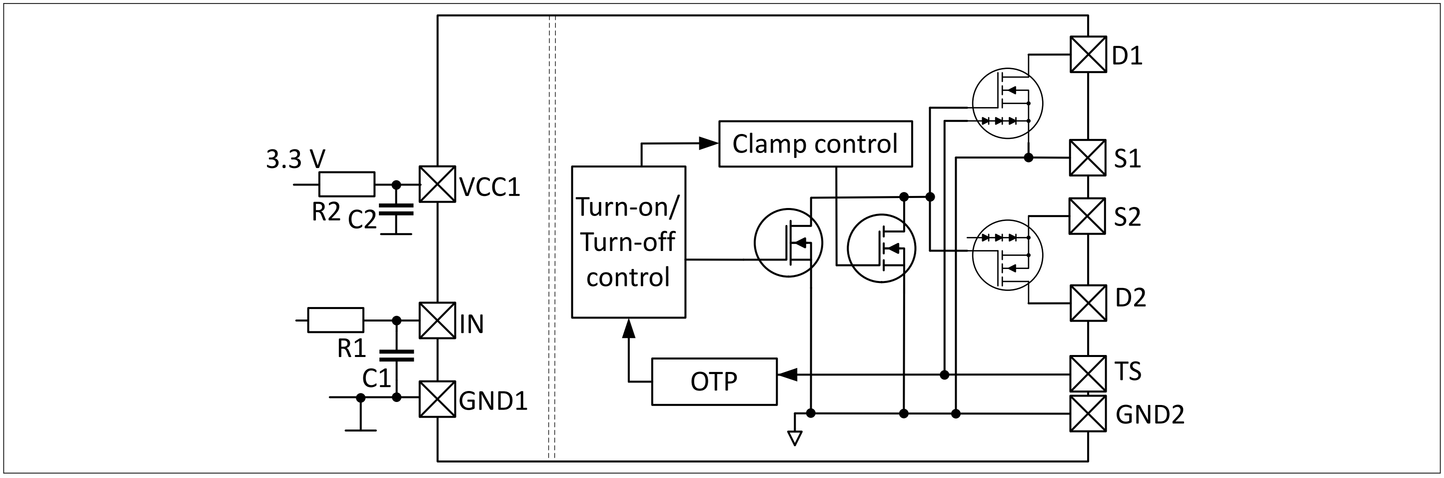


Figure 25 **Schematic of the overtemperature protection circuit**

7.2.7 Switching transistors

The switching transistors are realized in CoolMOS™ S7 technology and specified in the absolute maximum ratings and the electrical characteristics. Exceeding the absolute maximum ratings in one or even more parameters can cause irreversible damage to the MOSFETs. The two MOSFETs can be connected in series or in parallel.

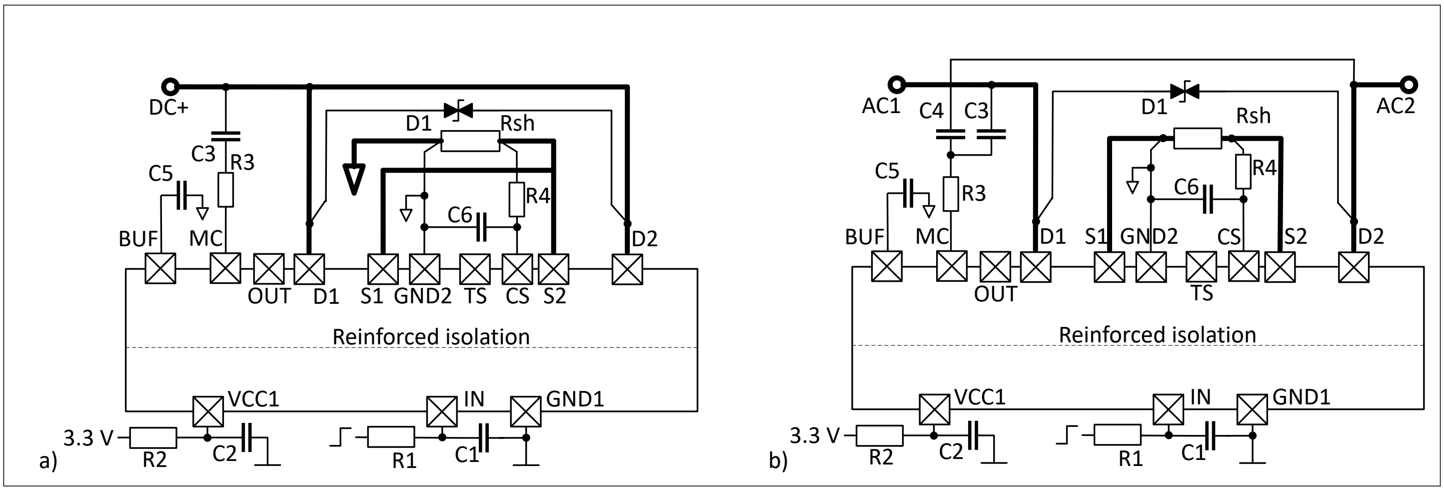


Figure 26 **MOSFETs in parallel (a) for DC applications and series (b) connection for AC applications**

8 Application section

Infineon is providing this information as a courtesy only and without acknowledging any legal obligation. Information in the following application chapters is not part of the Infineon component specification, and Infineon does not warrant its accuracy or completeness. Infineon's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Adaptation of the supply voltage

The Infineon SSR family iSSR60VxAxR1H is best operated from a voltage source of 3.3 V, such as directly from a microcontroller's supply. Please note that normally, the pull-down device of general-purpose I/O terminals or high-current terminals is stronger than the pull-up device. Thus, it is better to use the pull-down device to control the voltage supply of the Infineon SSI as shown below.

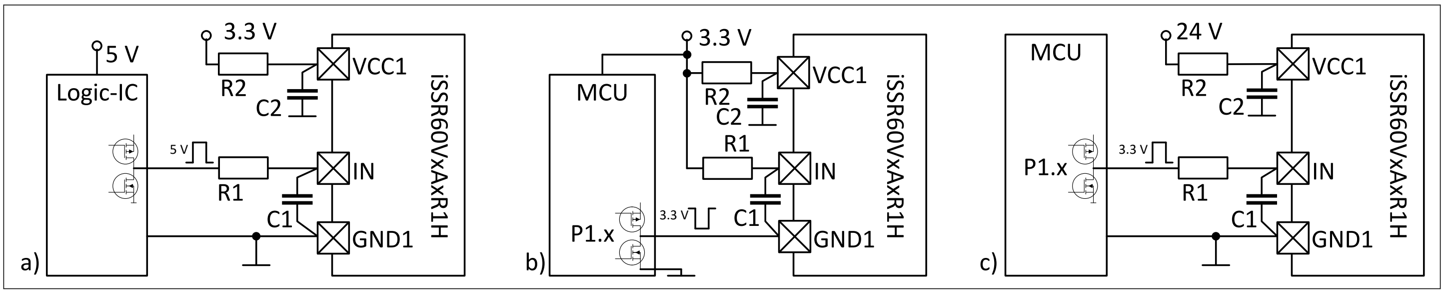


Figure 27 **Examples of application relevant control options**

The left part in the figure (option a) shows a logic IC supplied with 5 V, which provides a 5 V control signal, while the Infineon SSI is supplied with 3.3 V. This simplifies the interfacing as no downward level shifters are required.

Option b shows a simple option for the supply scheme. Terminal *IN* is connected to 3.3 V and terminal *GND1* is connected to the driving port of the microcontroller. The Infineon SSR's output is inverted to the control signal at *IN*. This option requires ports that are able to sink at least the maximum value of I_{IN}. If not, the effective supply voltage V_{IN} - V_{GND1} may not reach 3.3 V and the IC can stay in the undervoltage lockout (UVLO) mode or is not supplied correctly.

Option c) connects the supply terminal *VCC1* to a voltage higher than 3.3 V (for example, 24 V). In these cases, resistor R2 acts as a current-limiting resistor. The value for the current limit is the typical value of I_{VCC1}. This results in a limiting resistor value of

$$R2 = \frac{V_{\mathrm{supply}} - V_{\mathrm{VCC1,\,op,\,max}}}{I_{\mathrm{VCC1,\,typ}}} = \frac{24\ \mathrm{V} - 3.5\ \mathrm{V}}{16\ \mathrm{mA}} = 1281\ \Omega \tag{1}$$

A selection of R2 = 1.3 kΩ is sufficient. Of course, worst-case conditions and tolerances of the supply voltage V_{supply} also need to be considered. Even though inexpensive, the solution of using a current-limiting resistor may not be particularly efficient, depending on the resistor's power dissipation. Dimensioning R2 according to the maximum supply current $I_{\mathrm{VCC1,max}}$ results in higher losses inside the iSSR. Particularly when operating several Infineon SSR products, it is often more efficient to place a DC-DC-converter with a low-tolerance output voltage of 3.3 V instead of using a current-limiting resistor for each Infineon SSR.

Usually, simple microcontrollers do not have high-current I/O terminals. In such cases, use an interface transistor for driving with a single control signal. This means that terminals *VCC1* and *IN* are connected together. Such options using small-signal FETs are shown below.

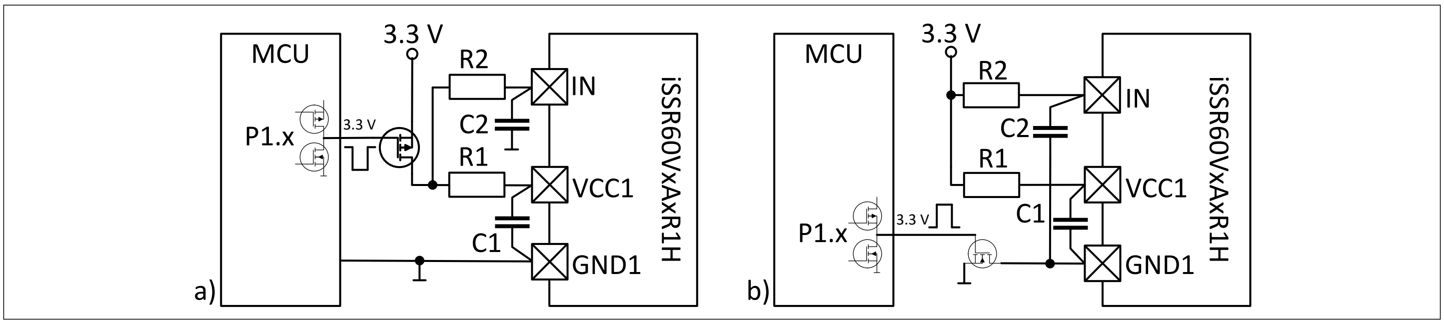


Figure 28 **Interfacing with an inverter circuit**

8.2 Grounding reference of current and temperature sensor signals

The two sensor signals of the current sensor (shunt) and the temperature sensor must refer to a single ground reference. It is good engineering to refer the overall ground to one of the sensors.

The left part shows an AC switch configuration. The iSSR family uses the integrated temperature sensor of one of the MOSFETs. The current measurement at terminal *CS* is more time-critical compared to the temperature sensing as it needs to react within a few hundreds of nanoseconds. Therefore, one of the shunt terminals is taken as the reference of the sensor signals. The example in the figure below utilizes the upper terminal of the shunt resistor R_{Sh} as the reference GND2. Direct connection of PCB traces from terminal *GND2* to the shunt and parallel routing of the current sense signal and its reference GND2 is mandatory to achieve the smallest signal distortion and filtering effort.

It is recommended to place the shunt in closest proximity to the source terminals *S1* and *S2* in order to keep the stray inductance L_σ as small as possible. Any stray inductance of the layout negatively affects the signal quality of the temperature sense voltage V_{TS}. However, temperature sensing can be easily filtered because the thermal capacitance of the switch allows the temperature to increase very slowly.

Please note that in AC configurations, the gate-source voltage of T1 $V_{GS,T1}$ is directly referenced to GND2 while the gate voltage of T2 $V_{GS,T2}$ is lowered by means of the shunt voltage V_{Sh} without a noticeable effect with respect to performance.

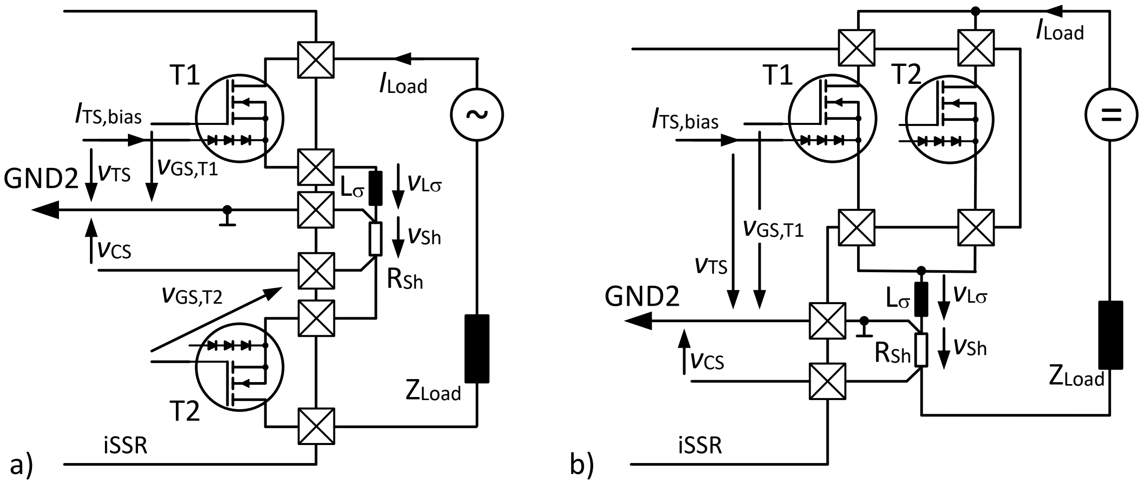


Figure 29 **Grounding scheme for AC switch with integrated temperature sensor (a) and with PTC temperature sensor (b)**

In DC switch configurations such as in the right part of the figure, follow the same guidelines for placing and routing the current sensor and the temperature sensor signals in the same way as for AC switch configurations. The shunt is placed symmetrically between the two source terminals to enable symmetrical switching of the two integrated MOSFETs.

8.3 Buffer capacitor dimensioning for fast turn-on

The fast turn-on feature enables high-current and high-voltage solid-state relays because it allows a high turn-on gate current that charges the gate capacitance very fast beyond the Miller voltage level. Leaving terminal *BUF* unconnected may lead to device malfunction or to the damage of the power switches due to an unsuitable turn on. See the "Fast turn-on" section in the "Functional description" chapter for more information.

The calculation of the buffer capacitor is simple, but yet essential to ensure a proper dimensioning of the fast turn-on. The gate voltage after the fast turn-on procedure should be in the range of 7.5 V to 8 V.

Because there is only one MOSFET of an AC configuration in blocking mode while the other MOSFET is in zero-voltage mode, the gate charge is derived as shown in the figure below.

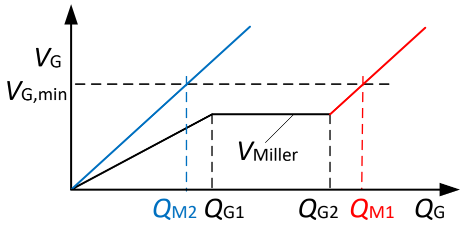


Figure 30 **Gate charge construction for AC switch configuration (common source)**

In an AC configuration of the switching transistor, there is always one switch that is in blocking mode. The other switching transistor is in freewheeling mode because its body diode or freewheeling diode is in forward bias. Therefore, only one transistor passes the Miller effect. The black/red graph shows a typical curve of the gate voltage V_G as a function of the gate charge Q_G for a MOSFET that is switched at a voltage lower than (for example, 2/3) of the breakdown voltage. The blue curve is the gate charge of a MOSFET under zero-voltage condition (V_{DS} = 0). The blue curve has usually the same slope as the red branch.

The minimum capacitance $C_{BUF,min}$ to be connected to terminal *BUF* is

$$C_{\mathrm{BUF,\,min}} = 1.2 \cdot \frac{Q_{\mathrm{M1}} + Q_{\mathrm{M2}}}{V_{\mathrm{BUF,\,th,\,min}} - V_{\mathrm{G,\,min}}} \tag{2}$$

When Q_{M1} and Q_{M2} are the related gate charges at the end of the fast turn-on when reaching $V_{G,min}$

$V_{BUF,th,min}$ is the minimum fast turn-on comparator threshold voltage

$V_{G,min}$ is the minimum gate-source voltage $V_{GS,min}$ of the switching transistors.

A safety factor of 1.2 covers the gate charge tolerance of the switching transistors.

For using iSSR60V4A0R1H as an AC switch, a drain-source voltage of 300 V, and a minimum gate-source voltage $V_{G,min}$ = 8 V, the minimum buffer capacitance $C_{BUF,min}$ is:

$$C_{\mathrm{BUF,\,min}} = 1.2 \cdot \frac{58\ \mathrm{nC} + 42\ \mathrm{nC}}{10\ \mathrm{V} - 7.5\ \mathrm{V}} = 48\ \mathrm{nF} \tag{3}$$

For using iSSR60V4A0R1H as an AC switch, both transistors have the characteristic of MOSFET M1 as per the above figure.

The table below shows the minimum buffer capacitors to be used with iSSR60V4A0R1H and iSSR60V2A5R1H in AC and DC configurations. The next higher value of the E12 series of capacitors is used.

Table 15 **Minimum buffer capacitors**

Configuration	iSSR60V4A0R1H	iSSR60V2A5R1H
AC	56 nF	33 nF
DC	56 nF	39 nF

8.4 Using the overcurrent protection feature

The overcurrent protection feature is designed to react fast when excessive current is detected using a shunt. This chapter explains how to use this feature in the example of a relay that operates AC-15 loads.

The AC-15 test is a generic test for electromechanical relays and for solid-state relays. Its test scheme is shown in the figure below. It brings demanding requirements for the dimensioning of the overcurrent protection feature. The protection should not trigger during the first interval of the AC-15 test when a load current of 10x of the nominal current is applied to the device under test followed by the interval t_2 - t_1 with nominal load current.

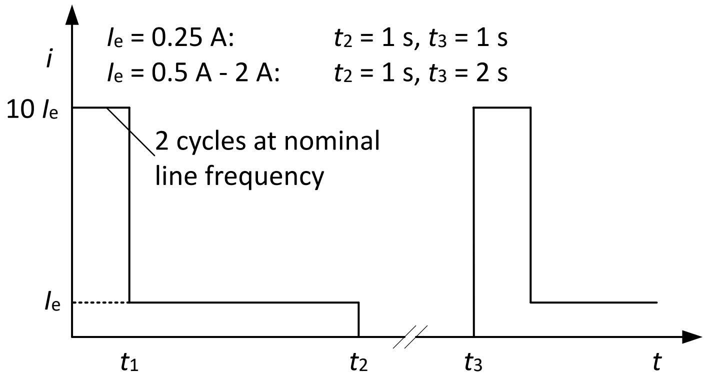


Figure 31 **AC-15 test (source: IEC 60947-1:2021)**

In addition, there are test requirements for the power factor at make and break events for various conditions and tests. The power factor itself does not influence the current amplitude and is therefore not considered. The following is an example for the shunt calculation for use in a solid-state relay with a current rating of 2 A supporting AC-15 tests.

The maximum load current in the AC-15 test is 10x the nominal and might appear at the maximum tolerated grid voltage which is 10% above nominal.

$$I_{\mathrm{pk,\,max}} = 1.1 \cdot \sqrt{2} \cdot 2\ \mathrm{A} \cdot 10 = 31.1\ \mathrm{A\ peak} \tag{4}$$

The worst-case analysis needs a margin of the target protection trigger current with respect to the calculated value $I_{\mathrm{pk,max}}$. The target protection trigger current is selected for $I_{\mathrm{pk,trig}}$ = 32 A peak. The overcurrent protection comparator is tolerated with +/-15 mV around the typical value of $V_{\mathrm{CS,th}}$ and an offset of 10 mV according to the figure below. Together with the assumed comparator overdrive of 20 mV, the minimum and maximum trigger currents are

$$\begin{aligned} I_{\mathrm{pk,\,trig,\,min}} &= I_{\mathrm{pk,\,trig}} \frac{v_{\mathrm{CS,\,th,\,min}} + 10\ \mathrm{mV} + 20\ \mathrm{mV}}{v_{\mathrm{CS,\,th,\,typ}} + 20\ \mathrm{mV}} = 31.27\ \mathrm{A\ peak} \\ I_{\mathrm{pk,\,trig,\,max}} &= I_{\mathrm{pk,\,trig}} \frac{v_{\mathrm{CS,\,th,\,max}} + 10\ \mathrm{mV} + 20\ \mathrm{mV}}{v_{\mathrm{CS,\,th,\,typ}} + 20\ \mathrm{mV}} = 35.64\ \mathrm{A\ peak} \end{aligned} \tag{5}$$

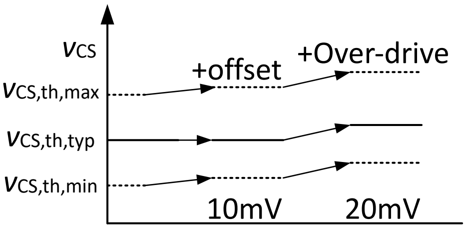


Figure 32 **Worst-case current sense trigger thresholds**

The dimensioning of the minimum shunt resistance follows this equation using the lowest trigger threshold including offset and overdrive and the maximum peak trigger current $I_{pk,trig,max}$.

$$R_{\mathrm{Sh,\,max}} = \frac{v_{\mathrm{CS,\,th,\,min}} + 10\ \mathrm{mV} + 20\ \mathrm{mV}}{I_{\mathrm{pk,\,trig,\,max}}} = \frac{215\ \mathrm{mV}}{35.64\ \mathrm{A}} = 6.033\ \mathrm{m\Omega} \tag{6}$$

The above equation results in a selected resistance of R_{Sh} = 6 mΩ.

8.5 Using the dynamic Miller clamping feature

Connecting a capacitor between the input terminal *MC* and the drain terminals of the switching transistors activates the dynamic Miller clamping feature that is available in the Infineon iSSR family. Leave terminal *MC* to float to deactivate the feature. The dynamic Miller clamp reinforces the strong, yet limited pull-down capability of Infineon SSR in case that high dV_{DS}/dt events occur at the switched transistors. This is in particular important during the off state if fast electric transients (bursts) occur. Even though there is usually no dedicated gate resistor in use, transients might lead to a parasitic turn-on of the switched transistor by pulling the gate higher than its gate-source threshold voltage.

The dimensioning of the coupling capacitors considers the fastest occurring dV_{DS}/dt rates that appear in the application. In AC applications, bursts according to IEC 61000-4-4 can be a reference that specifies very steep pulses. However, the resulting pulses that stress the device under test have a lower amplitude and slope due to the cabling inductance and capacitance. An assumption for dV_{DS}/dt can be, for example, 10 V/ns and the coupling capacitance may be 1 pF. Please note that one of the two capacitors is shorted bypassed to GND2 by the related switched transistor in parallel. Thus, the only one capacitor is coupling the dV_{DS}/dt signal.

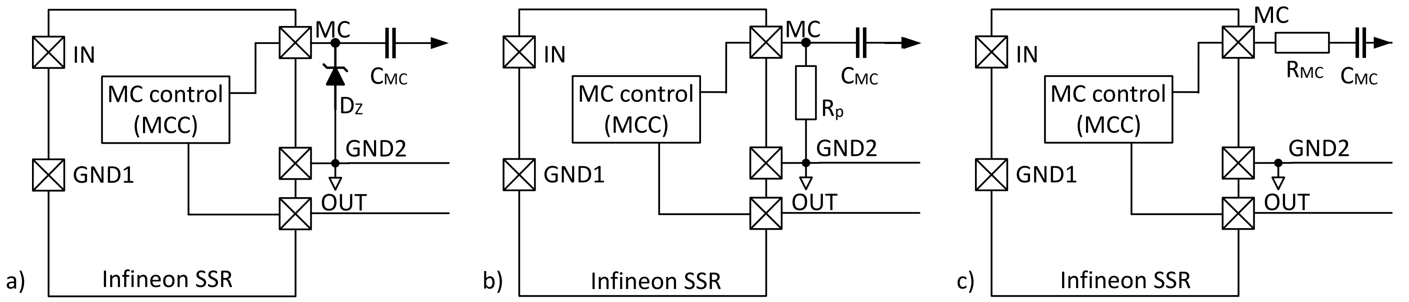


Figure 33 **Dynamic Miller clamp options with Zener diode (a), parallel resistor (b) and series resistor (c)**

In the above-mentioned example, the coupled capacitive current into terminal *MC* is 10 V/ns * 1 pF = 10 mA. This would generate a voltage at terminal *MC* of 10 mA * R_{MC} = 5 V. Even though the static absolute maximum voltage rating at *MC* is v_{MC} = 3.6 V, the dynamic current $I_{MC,dyn}$ for sporadic events (duty cycle < 1%, pulse duration < 1 µs) that is injected into this terminal can be applied for pulsed stress. Therefore, clamping elements, such a 3.3 V clamping Zener diode at terminal *MC* to reduce voltages above the Zener voltage might not be needed. However, special care needs to be taken at the evaluation of the highest dV/dt in systems. Other clamping options are a resistor between terminal *MC* and *GND2* that would take a portion of the coupled capacitive current, or applying a series resistor that generates enough voltage to keep the limits according to the figure above.

8.6 Inductive energy clamping methods

Solid-state relays are often used in combination with loads that have an inductive portion. The inductive portion generates an overvoltage condition if the isolator's output is turned off. The amplitude of the overvoltage can exceed the switching transistor's breakdown voltage. Therefore, a clamping element is needed to limit the drain-source voltage and the drain-source voltage slew-rate at turn-off of the switching transistor. Various options are possible:

- TVS (transient voltage suppressor) diodes
- Varistors
- Free-wheeling diodes (only in DC operation)
- Snubbers and others

Special care is required for the dimensioning and selection of the related components depending on the application's operating range. For example, two or even more TVS diodes may be required to fulfill the datasheet specifications of the clamping element. Combinations of the above-mentioned options may be considered to create an optimized clamping solution.

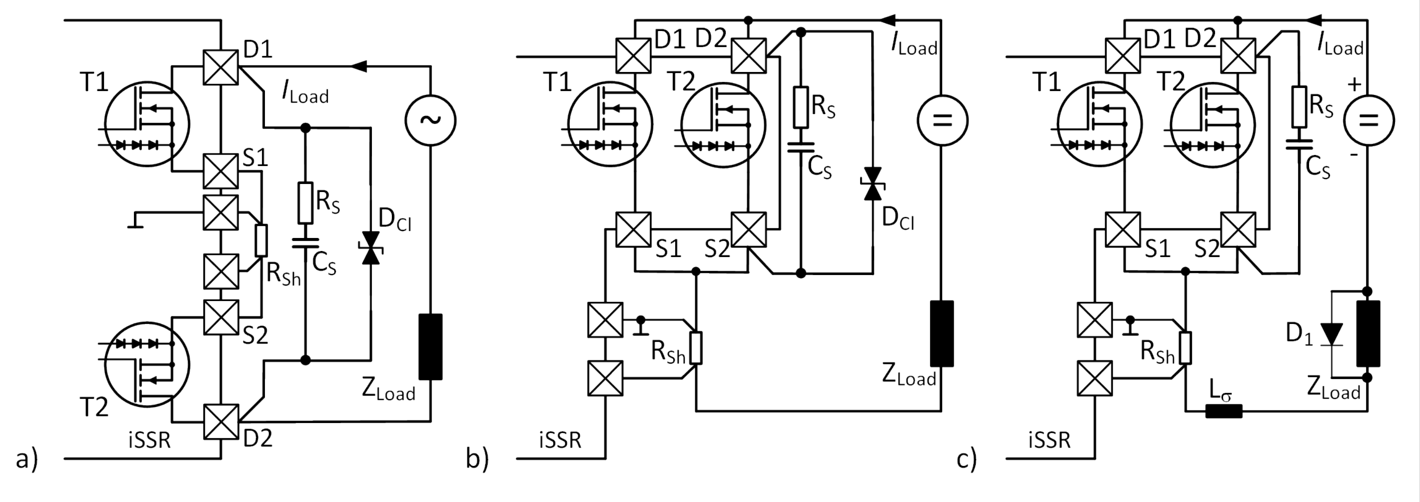


Figure 34 **Example of a drain-to-drain TVS diode D_{Cl} as a clamping element in an AC switch configuration (a) and drain-source clamping in DC switch configuration without inductive load freewheeling (b) and with load freewheeling (c)**

The clamping elements must be placed in closest proximity of the Infineon SSR to minimize the stray inductance between the drain terminals and the clamping element. As dV_{DS}/dt is limited for power transistors, a snubber enables lower dV/dt values. The capacitive portion of an RC snubber is related to the dV/dt at turn off. For example, a target dV/dt = 20 V/ns requires a snubber capacitance of

$$C_{\text{snubber}} = \frac{I_{pk}}{\frac{dv}{dt}} = \frac{40\text{A}}{20\frac{\text{V}}{\text{ns}}} = 2\text{ nF} \tag{7}$$

The resistive part of the RC snubber is required to not trigger the overcurrent protection feature at turn on. Please note that the instantaneous, single-pulse power loss of the snubber's resistive part must endure the charging energy and power of the capacitor that is

$$P_{R,\,\mathrm{snubber}} = I^2 R_{\mathrm{snubber}} \quad ; \quad E_{R,\,\mathrm{snubber}} = I^2 R_{\mathrm{snubber}} \cdot \Delta t \tag{8}$$

In DC systems with an inductive load, such as brake magnets of motor brakes, the clamping is often placed at the load. However, stray inductances can occur due to wiring, etc. that are not clamped. To mitigate detrimental effects of the unclamped stray inductance, still clamping elements may be necessary to be placed from the drain to the source of the switching transistors.

8.7 Operation with pulse-width modulation (PWM)

The operation under the PWM scheme is possible with the iSSR family. Care needs to be taken for the startup of the PWM as the fast turn-on feature increases the turn-on propagation delay. Therefore, the PWM on time needs to be longer than the turn-on propagation delay for a guaranteed turn-on. This is shown in part a) of the figure below. After the turn-on, both the buffer capacitor and the output is further charged. After turn-off, the buffer capacitor discharges according to its leakage current characteristic which is usually very low. In a PWM regime of several hertz, the voltage at terminal *BUF* may still be above the fast turn-on threshold $V_{\mathrm{BUF,th}}$ for the next rising edge of the control signal. This results in an instantaneous turn on with respect to IN.

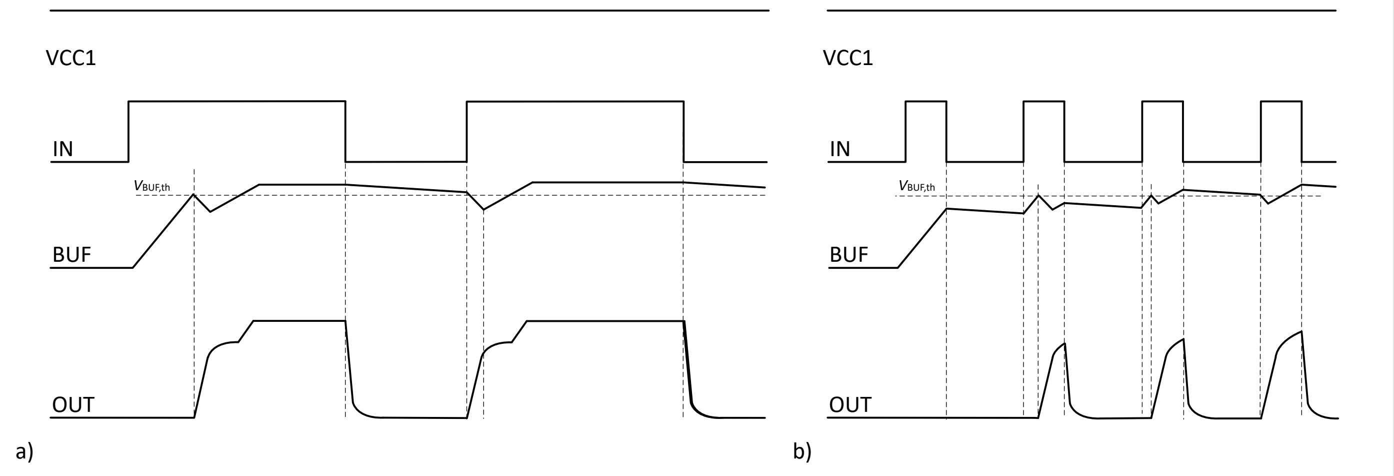


Figure 35 **PWM operation with long and short on-time**

If the PWM on-time is shorter than the time that is required to reach the fast turn-on threshold $V_{\mathrm{BUF,th}}$, turn-on does not occur in this particular cycle shown in part b) of the above figure. The fast turn-on threshold $V_{\mathrm{BUF,th}}$ is reached only in a later cycle, causing a delay for energizing the load. Note that in part b), the typical static output voltage V_{OUT} may never be reached with low on-times of the PWM. In such cases, special care needs to be taken for the power loss calculation of the integrated MOSFETs.

8.8 Layout recommendations and electromagnetic interference

As mentioned earlier, a few terminals, (*VCC1*, *IN*, *CS*, etc.) may require either blocking capacitors or RC filters for signal conditioning. The related capacitors must be placed as close to the IC as possible to get the best filtering effect. Small-footprint components help to minimize distances.

It is a good layout practice to have shielding planes connected to either GND1 or GND2. All signal and supply tracks should consider enough distance to the copper planes' borders to have effective shielding for the tracks as shown in the figure below. More detailed layout techniques are explained in [1]. Particularly, signal and supply tracks are best routed in the inner layers of the PCB for best shielding effects with the top and bottom layers.

Suitable components to mitigate radiated emissions can be Y-capacitors that provide a high-frequency path for noise. Such capacitors are conductive for high-frequency, but isolating for DC. Furthermore, conducted emissions can lead to radiated noise as well if tracks act as antennas. LC or pi filters can attenuate strongly conducted emissions and help reduce radiated emissions. Please refer to related application notes for more information.

8.9 Calculation of losses and junction temperature

The calculation of losses are essential for iSSR60V4A0R1H and iSSR60V2A5R1H for avoiding excessive junction temperatures. As the operating switching frequency is usually very low (<<1 Hz), the switching losses can be neglected. The power dissipation inside each of the MOSFETs is

$P_{D,MOS}(T_J) = I_D^2 \cdot R_{ds(on)}(T_J)$

$P_{D,Input} = I_{VCC1} \cdot V_{VCC1}$ and

$P_{D,Output} = I_{VCC1} \cdot V_{VCC1}$

The power dissipation of the MOSFETs causes a self-heating of the MOSFETs that requires a two-step approach. The calculation steps are:

1. Calculate the MOSFET's losses based on the ambient temperature condition
2. Calculate the self-heating relative to the ambient temperature using the thermal resistance junction to ambient using

   $\Delta T_J = P_{D,MOS} \cdot R_{th,j-a}$
3. Re-calculate the losses based on the ambient temperature and the self-heating using $T_J = T_A + \Delta T_J$
4. Re-calculate the resulting self heating
5. Calculate the junction temperature (like Step 3)

For example, the losses at an ambient temperature of T_A = 60°C (→ $R_{ds(on)}$(60°C) = 60 mΩ) and a drain current of I_D = 2 A DC can be calculated with

$$P_{D,MOS}(60°C) = I_D^2 \cdot R_{ds(on)}(60°C) = (2\text{A})^2 \cdot 60\text{m}\Omega = 240\text{mW}$$

The self heating is therefore

$$\Delta T_J = P_{D,MOS} \cdot R_{th,j-a} = 0.24\text{W} \quad \cdot 34\frac{\text{K}}{\text{W}} = 8.16\text{K}$$

Stepping through items 3, 4, and 5 of the above list results in a junction temperature of 68.7°C

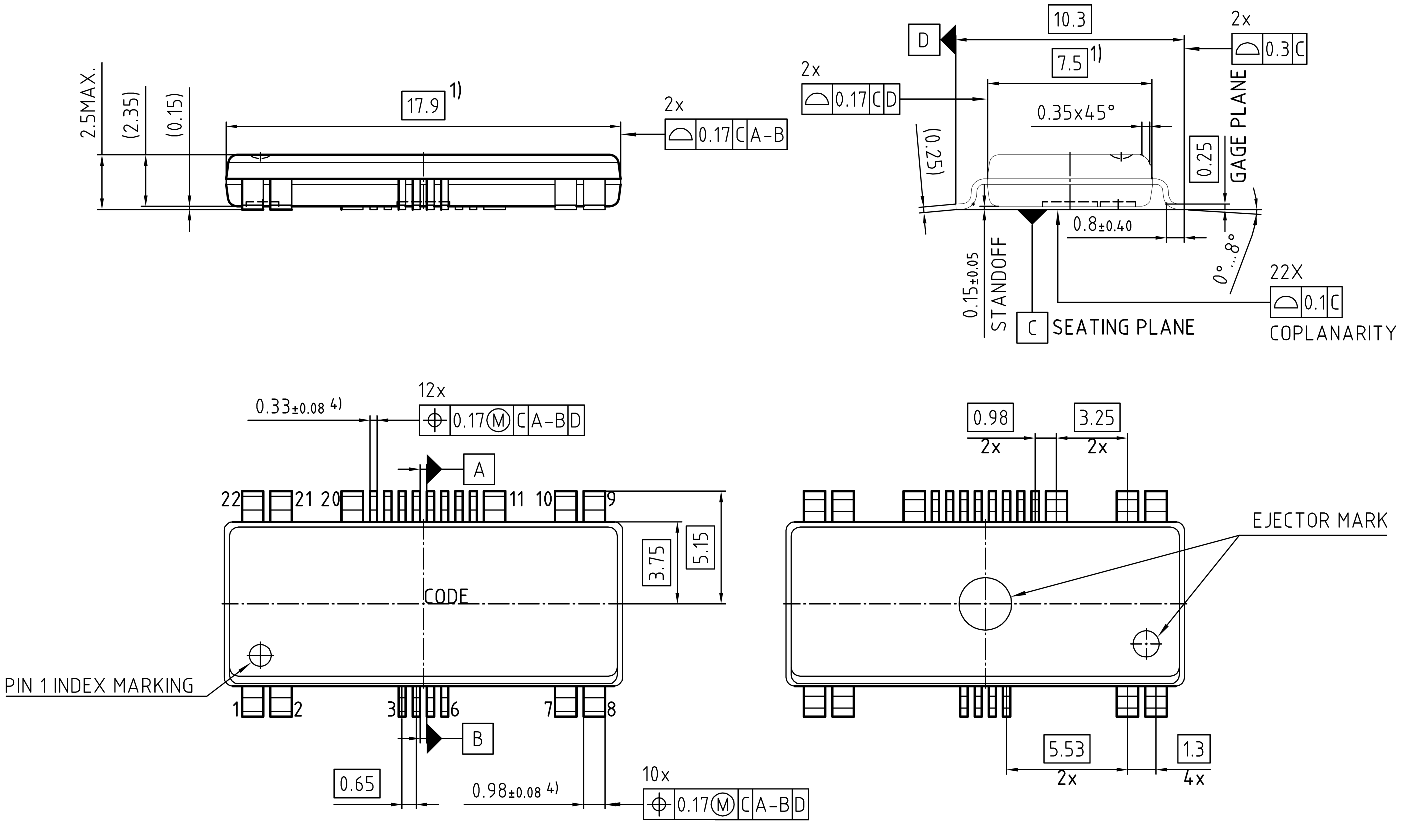
A further iteration is possible; however, the precision improvements become extremely small.

The characterization parameter Ψ_{Jtop} helps to calculate the steady-state junction temperature for a specific operating condition in the application. It is for estimation purposes under natural convection cooling. This thermal measurement can be compared with a calculated value from equipment such as an infrared camera. The related equation to use is

$T_J = P_{D,MOS} \cdot \Psi_{Jtop} + T_{top}$

with T_{top} being the surface temperature above the MOSFET.

9 Package dimensions



1) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OF 0.15 MAX PER SIDE
2) DOES NOT INCLUDE DAMBAR PROTRUSION OF 0.10 TOTAL IN EXCESS OF THE LEAD WIDTH AT MAXIMUM MATERIAL CONDITION
3) ALL DIMENSIONS IN MM
⚠ CHANGE MARKER WITH REVISION

Figure 36 PG-DSO-22-3 (Plastic (green) dual small outline package, 300 mil)

10 Revision history

Document version	Date of release	Description of changes
v0.10	2024-10-24	Initial official release
v0.20	2025-05-04	Updated parameters
v0.30	2026-02-25	Updated document, preliminary datasheet

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