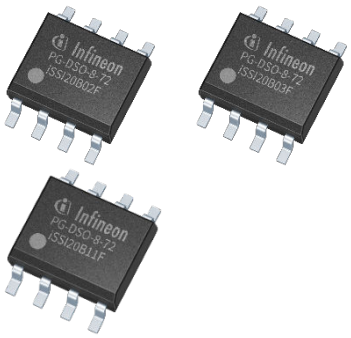
iSSI20B02F, iSSI20B03F and iSSI20B11
Infineon's coreless-transformer advanced solid-state isolators

Features

- Solid-state isolators using Infineon's coreless-transformer technology
- No isolated gate bias supply required for gate driving
- Perfect match for CoolMOS™, OptiMOS™, and TRENCHSTOP™ IGBT
- Input side supply from 2.85 V up to 24 V using current limiting resistor for V_{VCC1} > 3.5V
- High-impedance, CMOS input (buffered variants)
- High output voltage up to 18 V - no series or parallel configuration required for powerful gate driving
- High output peak current of 175 µA (direct drive variants) or 400 mA (buffered variants)
- Fast turn-off for safe switches' SOA operation
- Temperature sensor and current sensor protection inputs
- Latch-off in case of a failure event (overcurrent or over-temperature)
- Dynamic Miller clamping protection
- DSO-8 package with 4 mm creepage and clearance for UL 1577 (3 kV (rms), planned)

Potential applications

- Solid-state relay AC and DC applications
- Electro-mechanical relay replacements
- Programmable logic control, industrial automation, and controls
- Smart building and home automation systems (thermostat, lighting, heating control)
- Instrumentation equipment



PG-DSO-8-72

Product validation

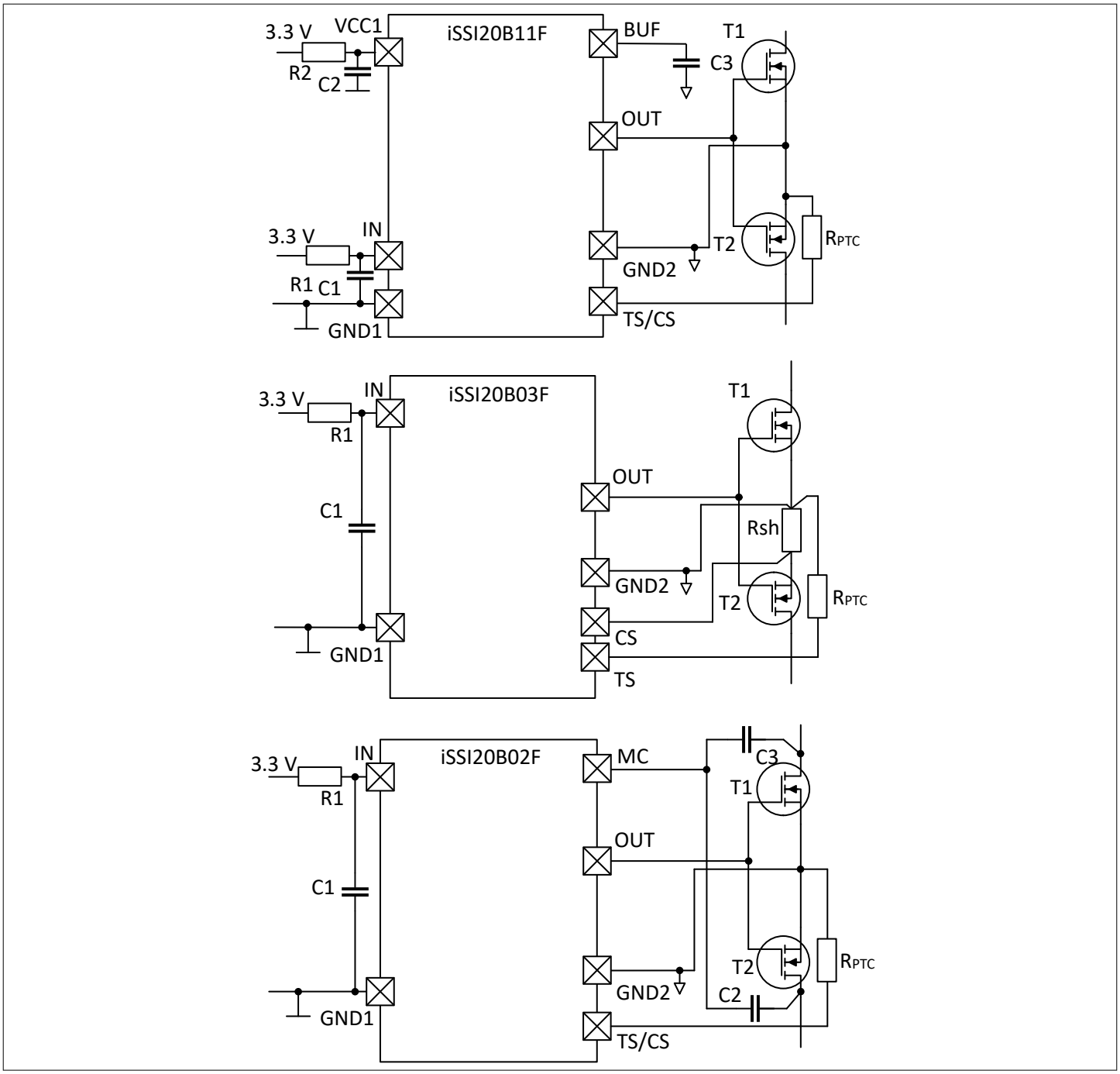
Qualified for industrial applications according to relevant tests of JEDEC47/20/22.

Description

The Infineon SSI solid-state isolator family provides powerful energy transmission over a galvanic isolation barrier to drive the gates of MOS-controlled power transistors, such as CoolMOS™, OptiMOS™, or TRENCHSTOP™ IGBT. The output side of the Infineon SSI solid-state isolator family does not require a dedicated voltage supply to drive the power transistor's gate. The output side offers advanced control functions such as fast turn-on, fast turn-off, overcurrent protection and over-temperature protection to easily and safely build up solid-state relays for various applications. The over-temperature protection can be used in combination with external PTC resistors. The Infineon SSI family offers precise protection functions for building cost effective systems. The input side of the isolator is 3.3 V compatible and operates with a supply current of typically 16 mA. The supply voltage range can be easily extended up to 24 V or higher by using a current limiting resistor.

The iSSI20B02F, iSSI20B03F, and iSSI20B11F come in a DSO-8-72 150-mil package.

The isolation is UL 1577 compliant (planned).



Product type	Protection features	Fast turn-on	Certification	Marking	Package
iSSI20B02F	OCP or OTP (PTC), DMC	No	UL1577	I20B02	PG-DSO-8-72
iSSI20B03F	OCP, OTP (PTC)	No	UL1577	I20B03	PG-DSO-8-72
iSSI20B11F	OCP or OTP (PTC)	Yes	UL1577	I20B11	PG-DSO-8-72

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1 Block diagrams

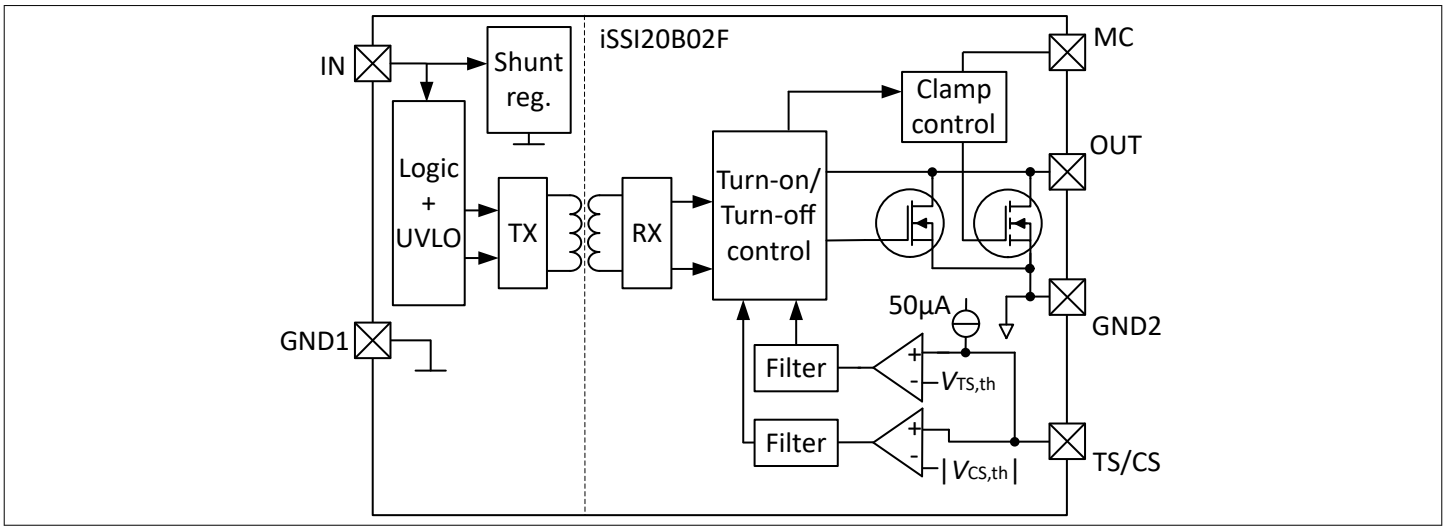


Figure 1 Block diagram of iSSI20B02F

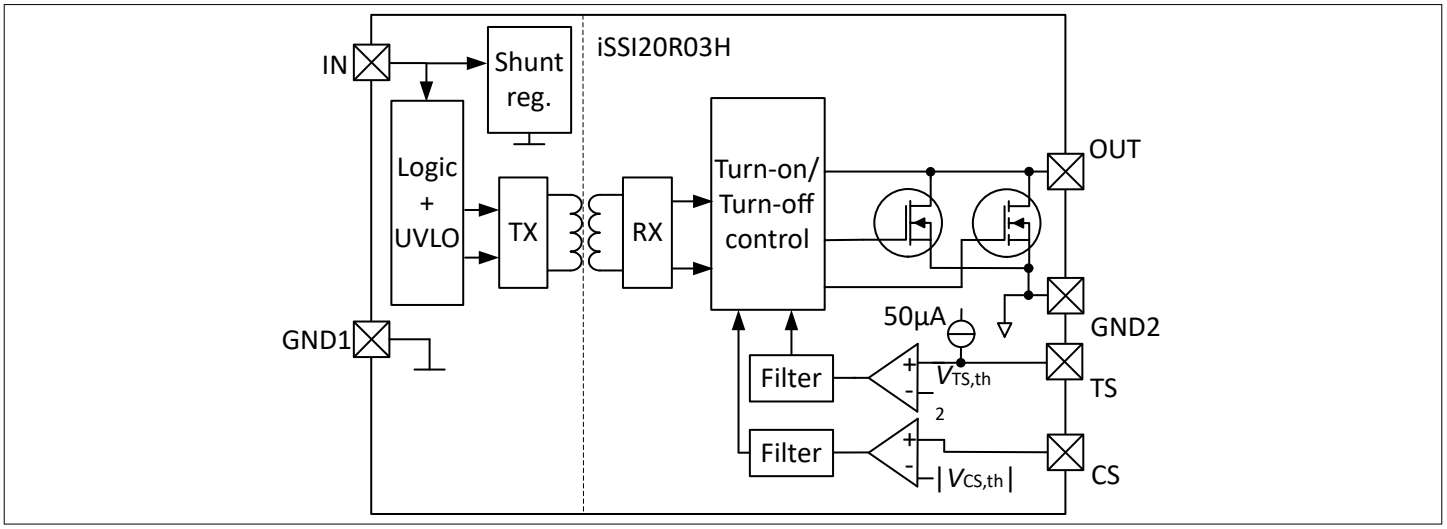


Figure 2 Block diagram of iSSI20B03F

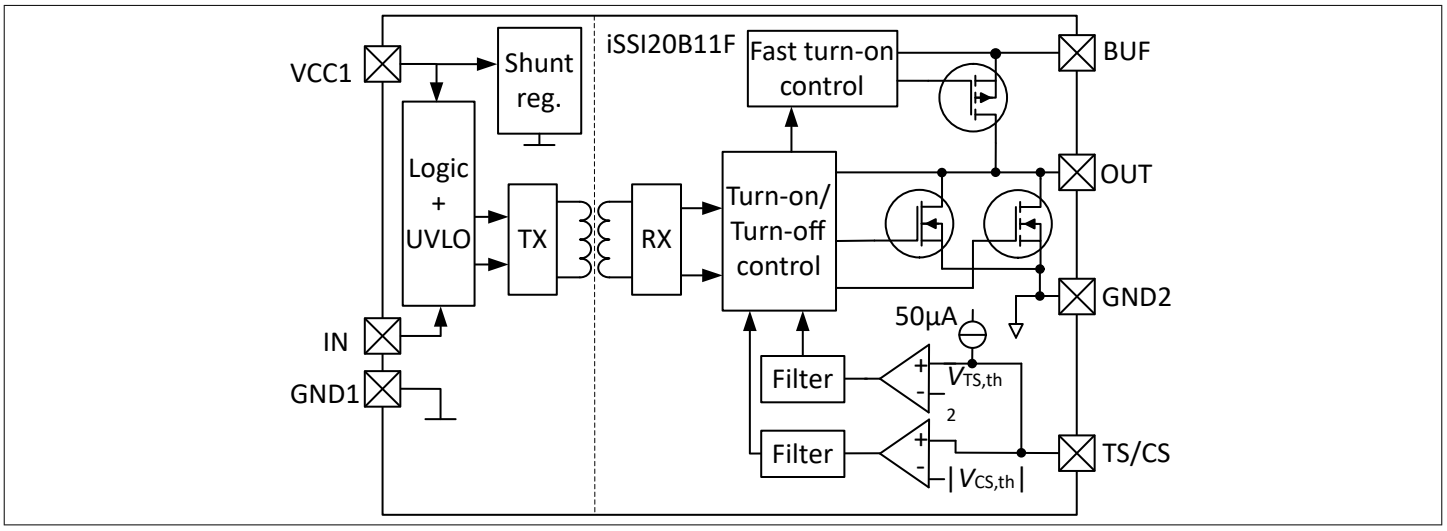


Figure 3 Block diagram of iSSI20B11F

2 Pin configuration

2.1 Pin configuration

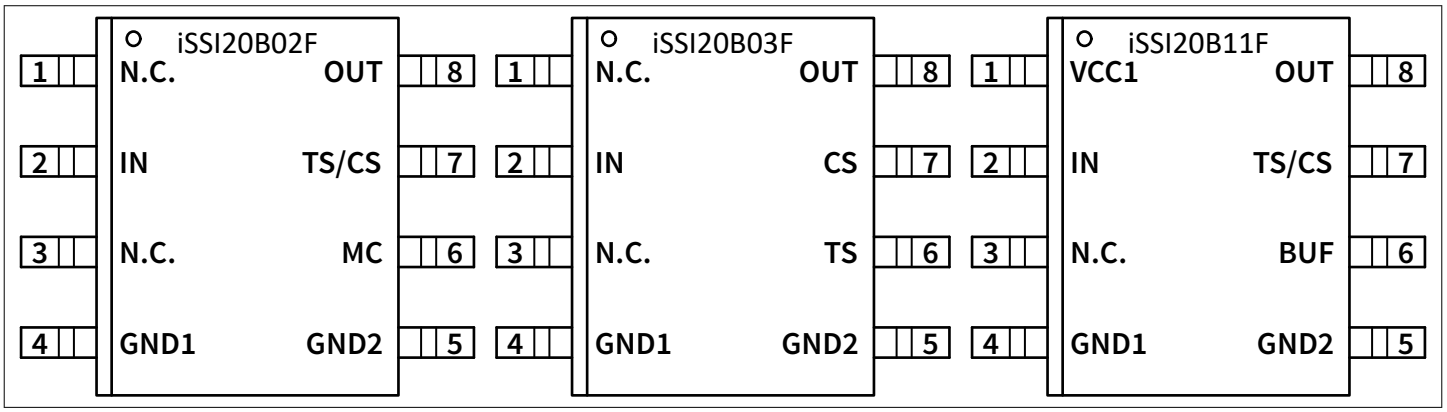


Figure 4 Pin configuration of Infineon SSI family

Table 1 Pin configuration for iSSI20B02F

Pin no.	Pin name	Pin type	Function
1	*N.C.*	-	Not connected
2	*IN*	PWR	Supply and non-inverting control input
3	*N.C.*	-	Not connected
4	*GND1*	PWR	Reference of control side
5	*GND2*	PWR	Reference of output side
6	*MC*	I	Miller clamp input
7	*TS/CS*	I/O	Output for temperature sensor bias current and input for sensed signal
8	*OUT*	O	Gate drive output

Table 2 Pin configuration for iSSI20B03F

Pin no.	Pin name	Pin type	Function
1	*N.C.*	-	Not connected
2	*IN*	PWR	Supply and non-inverting control input
3	*N.C.*	-	Not connected
4	*GND1*	PWR	Reference of control side
5	*GND2*	PWR	Reference of output side
6	*TS*	I/o	Output for temperature sensor bias current and input for temperature signal
7	*CS*	I	Input for current-sense signal
8	*OUT*	O	Gate drive output

Table 3 Pin configuration for iSSI20B11F

Pin no.	Pin name	Pin type	Function
1	*VCC1*	PWR	Supply input
2	*IN*	I	Non-inverting control input
3	*N.C.*	-	Not connected
4	*GND1*	PWR	Reference of control side
5	*GND2*	PWR	Reference of output side
6	*BUF*	I/O	Output for buffer charges and input for fast turn-on
7	*TS/CS*	I/O	Output for temperature sensor bias current and input for sensed signal
8	*OUT*	O	Gate drive output

2.2 Pin description

- *VCC1*: iSSI20B11F only, supply of input side; best operated with 3.3 V; can be shorted to terminal *IN*; referenced to GND1.
- *IN*: Logic input for iSSI20B11F, can be shorted to *VCC1*. It is the input supply pin for variants iSSI20B02F and iSSI20B03F. Pin is referenced to *GND1*
- *GND1:* Reference pin for *VCC1* and *IN*.
- *GND2*: Reference pin for *MC*, *CS*, *TS*, *TS/CS*, *OUT* and *BUF*.
- *MC*: Input pin for dynamic Miller clamp. Keep this pin unconnected to deactivate the dynamic Miller clamp function. Referenced to *GND2*.
- *CS*: Current sense input. When unused, it is recommended to connect to *GND2*. Referenced to *GND2*.
- *TS*: Temperature sense input. When unused, it is recommended to connect to *GND2*. Referenced to *GND2*.
- *TS/CS*: Pin can be used either as temperature sense input or as current sense input. When unused, it is recommended to connect to *GND2*. Referenced to *GND2*.
- *OUT*: Gate drive output. Referenced to *GND2*.
- *BUF*: Gate drive buffer. Typically, a capacitor is connected to implement the fast turn-on feature. Referenced to *GND2*.

3 Electrical characteristics and parameters

3.1 Absolute maximum ratings

Table 4 Absolute maximum ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only. Operating the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Device reliability may be affected by exposure to absolute-maximum-rated conditions for extended periods of time.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input to output offset voltage	V_{OFFSET}	-1200		1200	V	$V_{offset} = \lvert V_{GND1} - V_{GND2} \rvert$ [1]
Input supply voltage	V_{IN} V_{VCC1}	-10		4.25	V	
Input logic voltage (terminal IN)	$V_{IN,logic}$	-10		15	V	Reference to GND1
Output voltage at terminal OUT	V_{OUT}	-0.3		20	V	[2]
Voltage at terminal MC	V_{MC}	-0.3		3.6	V	[2]
Voltage at terminals TS, CS or TS/CS (static)	V_{TS}, V_{CS} $V_{TS/CS}$	-1.2		4	V	[2]
Voltage at terminals CS, TS and TS/CS (positive signals, dynamic)	$V_{pin,dyn}$	0		6	V	[2] $0 < I_{pin,dyn} < 10$ mA, $t_p < 2$ µs, $d < 0.001$
Voltage at terminals CS, TS and TS/CS (negative signals, dynamic)	$V_{pin,dyn}$	-2		0	V	[2] $0 > I_{pin,dyn} > -10$ mA, $t_p < 2$ µs, $d < 0.001$
Voltage at terminal BUF	V_{BUF}	-0.3		20	V	[2]
Input supply current	I_{IN} I_{VCC1}	0		120	mA	iSSI20B02F, iSSI20B03F iSSI20B11F
Current at terminal OUT (static)	I_{OUT}	-10		10	mA	$V_{IN} = 0$ V
Current at terminal OUT (dynamic)	$I_{OUT,dyn}$	-100		100	mA	$V_{IN} = 0$ V; $t_p < 10$ µs for negative current pulses; $t_p < 1$ µs for positive current pulses
Current at terminal MC (static)	I_{MC}	-6		6	mA	[2]
Current at terminal MC (dynamic)	$I_{MC,dyn}$	-100		100	mA	$t_p < 1$ µs; $d < 1\%$
Current at terminal TS	I_{TS}	-1		1	mA	[2]
Current at terminal CS or TS/CS	I_{CS}, $I_{TS/CS}$	-1		1	mA	[2]
Current at terminal BUF (static)	I_{BUF}	-10		10	mA	
Current at terminal BUF (dynamic)	$I_{BUF,dyn}$	-1		1	A	$t_p < 1$ µs
Power dissipation input part	P_{DIN}			200	mW	$T_A = 85$°C [3]
Power dissipation output part	P_{DOUT}			4.5	mW	$T_A = 85$°C [4]
Thermal resistance junction-to-ambient	R_{THJA}			145	K/W	$T_A = 85$°C, PG DSO-8-72, 2s2p footprint only

(table continues...)

Table 4 (continued) Absolute maximum ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only. Operating the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Device reliability may be affected by exposure to absolute-maximum-rated conditions for extended periods of time.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Characterization parameter junction-to-package top	Ψ_{Jtop}			34	K/W	T_A = 85°C, PG-DSO-8-72, 2s2p footprint only
ESD robustness - human body model	$\lvert V_{ESD,HBM} \rvert$	2			kV	5)
ESD robustness - charged device model	*ESD,CDM*			TC 1000	–	6)
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_{ST}	-55		150	°C	
Maximum switching frequency	f_{SW}			2	kHz	C_{Load} = 100 pF, V_{IN} = 3.3 V, V_{VCC1} = 3.3 V (where appropriate)

1) For functional operation only
2) Reference to GND2.
3) PG-DSO-8-72: derating of power above T_j = 121°C with 6.90 mW/°C, layout 2s2p (JESD 51-5 / JESD 51-7).
4) PG-DSO-8-72: derating of power above T_j = 149.3°C with 6.90 mW/°C, layout 2s2p (JESD 51-5 / JESD 51-7).
5) According to ANSI/ESDA/JEDEC-JS-001-2017 (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).
6) According to ANSI/ESDA/JEDEC-JS-002-2014 (TC = highest test condition passed according to AEC-Q100-011 Rev D).

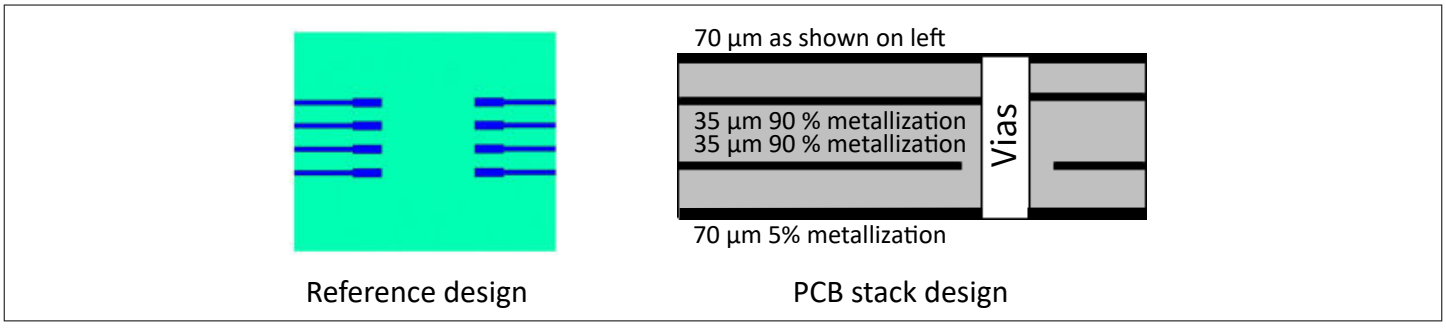


Figure 5 Thermal reference design

3.2 Recommended operating conditions

Table 5 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input supply voltage (terminal VCC1 (or IN if VCC1 is absent))	V_{VCC1}	2.85	3.3	3.5	V	
Voltage at terminals TS, CS, or TS/CS (static)	V_{TS}, V_{CS} $V_{TS/CS}$	-0.5		2.7	V	V_{CS} - V_{GND2}, V_{TS} - V_{GND2}, $V_{CS/TS}$ - V_{GND2}

(table continues...)

Table 5 (continued) Recommended operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External input supply capacitance including tolerances of the capacitor	$C_{VCC1,ext}$			4.7	nF	
Ambient temperature	T_A	-40		125	°C	
Junction temperature	T_J	-40		125	°C	
Common-mode transient immunity	$\|dv_{CM}/dt\|$			200	V/ns	V_{CM} = 1500 V

3.3 Electrical characteristics

The minimum and maximum electrical characteristics include the spread of values over supply voltages and temperatures within the recommended operating conditions. Electrical characteristics are tested in production at T_A = 25°C and the default load at terminal OUT is 100 pF. Typical values represent the median values measured at supply voltage V_{IN} = 3.3 V (or V_{VCC1} = 3.3 V where applicable) and T_A = 25°C. Minimum and maximum characteristics are verified by characterization/design. All voltages are referenced to their respective GND (GND1 for input side pins and GND2 for output side pins). This is valid for all electrical characteristics unless specified otherwise.

3.3.1 IC Supply

Table 6 IC Supply

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
UVLO threshold input side (power up)	V_{UVLOH1}	2.7	2.775	2.85	V	V_{IN} - V_{GND1}, V_{VCC1} - V_{GND1}
UVLO threshold input side (power down)	V_{UVLOL1}	2.6	2.68	2.75	V	V_{IN} - V_{GND1}, V_{VCC1} - V_{GND1}
UVLO hysteresis input side	V_{HYS1}	70			mV	[1] V_{UVLOH1}- V_{UVLOL1}
Supply current input side at terminal IN (or VCC1 where available)	I_{IN}	14	16	19	mA	V_{IN} = 3.3 V, I_{OUT} = 0
Standby input supply current at terminal VCC1	$I_{IN,STBY}$		1.4	2.5	mA	V_{VCC1} = 3.3 V, V_{IN} = 0
Integrated supply bias resistance	$R_{VCC1,bias}$	2.45		7.14	Ω	
Off-time before turn-on	$t_{OFF,IN}$ $t_{OFF,VCC1}$	25			µs	[1] V_{IN} < V_{UVLOL1} (or V_{VCC1} < V_{UVLOL1} where applicable)

1) Parameter is not subject to production test - verified by design/characterization.

3.3.2 Logic input (iSSI20B11F)

Table 7 Logic input (iSSI20B11F)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
IN logic low input threshold voltage	V_{IL}	1.0	1.2		V	V_{IN} - V_{GND1}
IN logic high input threshold voltage	V_{IH}		2.1	2.3	V	V_{IN} - V_{GND1}
IN logic low/high hysteresis	$V_{IN,HYS}$	0.7			V	V_{IN} - V_{GND1}
IN logic pull down resistor	$R_{IN,PD}$	200			kΩ	V_{IN} = 2.5 V
Off-time before turn-on	$t_{OFF,IN}$	25			µs	1) V_{VCC1} = 3.3 V, V_{IN} < $V_{IL,min}$

1) Parameter is not subject to production test - verified by design/characterization.

3.3.3 Gate drive

Table 8 Gate drive

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output voltage	V_{OUT}	15.5	17.1	18.5	V	V_{OUT} - V_{GND2}, V_{IN} = V_{VCC1} = 3.3 V, I_{OUT} = 0 mA, T_J = 25°C
Output voltage	V_{OUT}	10	15	20	V	V_{OUT} - V_{GND2}, V_{IN} = 3.3 V, I_{OUT} = 0
Output voltage	V_{OUT}	10	13	16	V	V_{OUT} - V_{GND2}, V_{IN} = 2.6 V, I_{OUT} = 0
Short circuit output current (iSSI20B02F, iSSI20B03F)	I_{OUT}	100	175	-	µA	V_{IN} = 3.3 V, V_{OUT} = 0
Short circuit output current (iSSI20B11F)	I_{OUT}	150	325	550	µA	V_{IN} = 3.3 V, V_{OUT} = 0
Turn-off current	$I_{off,sat}$	50	160	270	mA	1) V_{IN} = 0 V, V_{OUT} = 5 V
Fast turn-off transistor saturation current	$I_{off,fast,sat}$	488			mA	1) V_{IN} = 3.3 V, V_{CS} = 0.3 V, V_{OUT} = 5 V
High-level output resistance	R_{OH}	60	110	155	kΩ	V_{IN} = 3.3 V, ΔV_{OUT} = 1 V, iSSI20B02F, iSSI20B03F
High-level output resistance	R_{OH}	48	95	135	kΩ	V_{IN} = 3.3 V, ΔV_{OUT} = 1 V, iSSI20B11F
Low-level output resistance	R_{OL}	5	8.5	12	Ω	V_{VCC1} = 0, V_{OUT} < 0.5 V
Turn-on propagation delay terminal IN and VCC1 (where applicable) to terminal OUT or BUF (where applicable)	t_{PDON}			20	µs	V_{IN} = 3.3 V, V_{VCC1} = 3.3 V (where applicable), no load
Turn-off propagation delay	t_{PDOFF}	0.3	3	6	µs	V_{IN} = 0, no load, V_{VCC1} = 3.3 V (where applicable)

(table continues...)

Table 8 (continued) Gate drive

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Rise time	t_r, $t_{r,BUF}$		8	15	µs	V_{VCC1} = 3.3 V (where appropriate), V_{IN} = 3.3 V, no load
Fall time	t_f		1.9	4	µs	Supply at VCC1: V_{VCC1} = 3.3 V, V_{IN} ≤ 1 V, C_{BUF} = 3 nF, no load Supply at IN: V_{IN} ≤ 2.6 V
Fall time	t_f	1	3.2	6.5	µs	Supply at VCC1: V_{VCC1} = 3.3 V, V_{IN} ≤ 1 V, C_L = 10 nF Supply at IN: V_{IN} ≤ 2.6 V, C_L = 10 nF

1) Parameter is not subject to production test - verified by design/characterization.

3.3.4 Fast turn-on (iSSI20B11F)

Table 9 Fast turn-on (iSSI20B11F)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fast turn-on threshold (power up)	$V_{BUF,th}$	10.0	10.4	10.8	V	V_{BUF} - V_{GND2}
Fast turn-on saturation current	$I_{on,fast,sat}$	232	400		mA	*1)* V_{OUT} = 5 V, V_{BUF} = 10.4 V
Resistance between terminal BUF and OUT after fast turn-on	$R_{BUF-OUT}$	300	500		kΩ	*1)*
Fast turn-on propagation delay input-to-output	$t_{PDON,fast}$		5		ms	*1)* C_{BUF} = 33 nF, C_{OUT} = 5.6 nF, V_{OUT} = 1 V
Fast turn-on rise time	$t_{r,fast}$		530	1000	ns	*1)* C_{BUF} = 48 nF, C_{OUT} = 10 nF

1) Parameter is not subject to production test - verified by design/characterization.

3.3.5 Dynamic Miller clamping

Table 10 Dynamic Miller clamping

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Dynamic Miller clamp saturation current	I_{CLAMP}	500	1700		mA	*1)* V_{MC} = 2.5 V; V_{OUT} = 3 V
Low-level output resistance during dynamic Miller clamping	$R_{OL,MC}$	0.7	1.5	3.5	Ω	V_{MC} = 2.5 V, I_{OUT} = 10 mA
Input resistance terminal MC	R_{MC}	400	500	600	Ω	V_{VCC1} = 0, V_{MC} = 0.5 V

1) Parameter is not subject to production test - verified by design/characterization.

3.3.6 Over-temperature protection

Table 11 Over-temperature protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Temperature sense comparator threshold	$V_{TS,th}$	190	200	210	mV	V_{TS} - V_{GND2}, V_{IN} = 3.3 V
Temperature sense bias current (terminals TS and TS/CS)	$I_{TS,bias}$ $I_{TS/CS,bias}$	40	50	60	µA	V_{IN} = V_{VCC1} = 3.3 V
Temperature sense protection propagation delay	$t_{PD,TS}$			5	µs	V_{IN} = 3.3 V, C_{Load} ≤ 100 pF, V_{TS} = $V_{TS,th1}$ +20 mV
Temperature sense filter time	$t_{TS,filter}$	0.12	0.15	0.175	µs	V_{IN} = V_{VCC1} = 3.3 V, V_{TS} = $V_{TS,th1}$ +20 mV
Fast turn-off fall time after OTP trigger	$t_{f,TS}$			725	ns	[1] C_{OUT} = 28 nF, V_{OUT} = 12 V

1) Parameter is not subject to production test - verified by design/characterization.

3.3.7 Overcurrent protection

Table 12 Overcurrent protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overcurrent comparator shut down threshold	$\|V_{CS,th}\|$	185	200	215	mV	V_{CS} - V_{GND2}, V_{VCC1} = V_{IN} = 3.3 V
Overcurrent shut-down delay	$t_{CS,off}$		0.6	1	µs	V_{CS} = 300 mV, V_{OUT} = 2.5 V
Overcurrent filter time	$t_{CS,filter}$	120	150	175	ns	[1] $\|v_{CS}\|$ = 0.3 V
Fast turn-off fall time after OCP trigger	$t_{f,CS}$			725	ns	[1] C_{OUT} = 28 nF, V_{OUT} = 12 V, $\|dv_{CS}/dt\|$ > 480 mV/µs

1) Parameter is not subject to production test - verified by design/characterization.

4 Insulation characteristics (iSSI20BxxF)

This coupler is suitable for rated insulation only within the given safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 13 Insulation specification

Description	Symbol	Characteristic	Unit
Safety limiting values			
Maximum ambient safety temperature	T_S	150	°C
Maximum input-side power dissipation at T_A = 25°C[1)]	P_{SI}	200	mW
Maximum input-side supply current at T_A = 25°C[2)]	I_{SI}	120	mA
Maximum output-side power dissipation at T_A = 25°C[3)]	P_{SO}	4.5	mW
General			
External clearance	*CLR*	> 4	mm
External creepage	*CPG*	> 4	mm
Comparative tracking index	*CTI*	> 600	–
Recognized under UL 1577 (planned)			
Insulation withstand voltage (60 s)	V_{ISO}	3000	V (rms)
Insulation test voltage (1 s)	$V_{ISO,TEST}$	3600	V (rms)

1) IC input-side power dissipation is derated linearly at 6.90 mW/°C above 122.0 °C
2) IC input-side power dissipation is derated linearly at 4.2 mA/°C above 122.0 °C
3) IC output-side power dissipation is derated linearly at 6.9 mW/°C above 149.3 °C

5 Timing diagrams

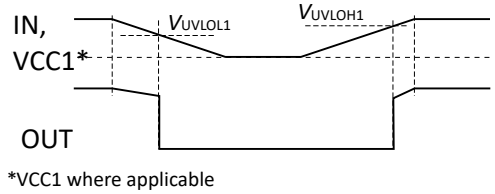


Figure 6 UVLO behavior

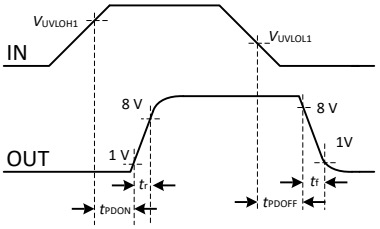


Figure 7 Direct gate drive turn-on and turn-off propagation delay, rise and fall time

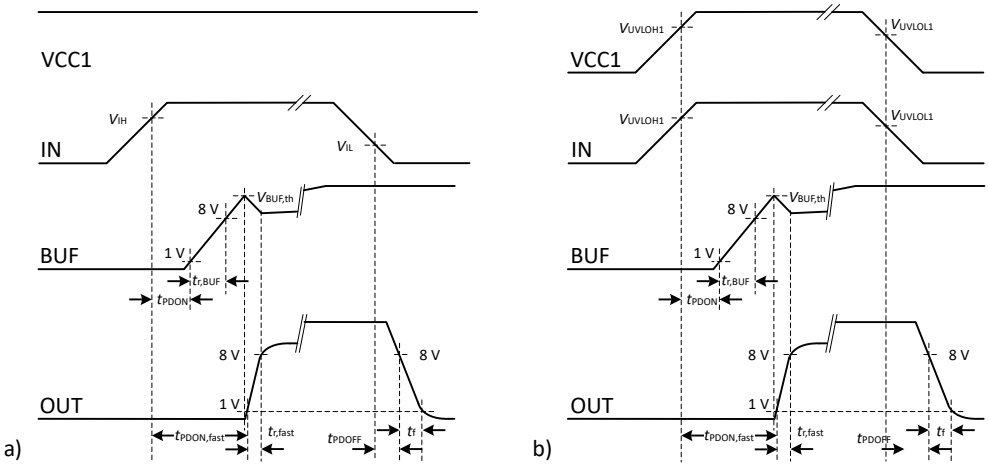


Figure 8 Fast turn-on timing using a buffer capacitor: a) separate *VCC1* and *IN*, b) *VCC1* and *IN* shorted

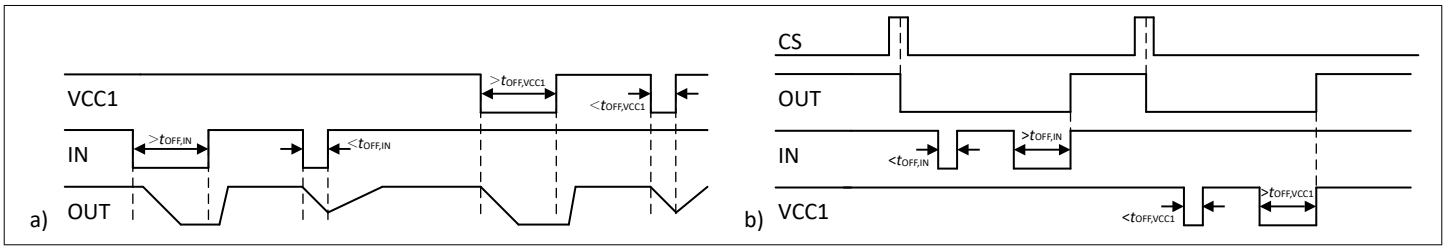


Figure 9 a) Off-time before turn-on, b) off-time after protection (example of overcurrent protection)

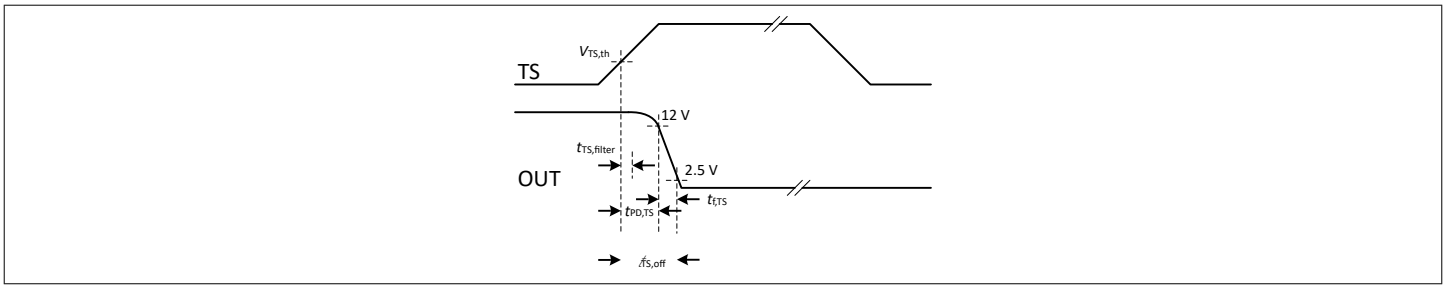


Figure 10 Over-temperature protection timing

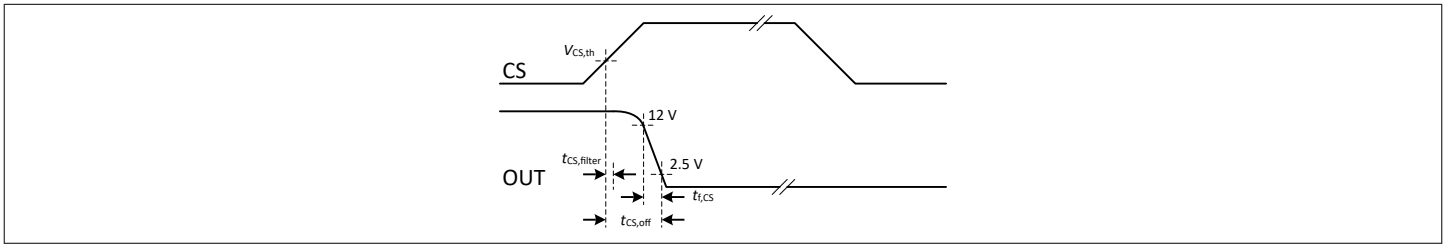


Figure 11 Overcurrent protection timing

6 Functional description

6.1 Input side

6.1.1 Input side supply

The input side of the Infineon SSI family is 3.3 V compatible and operates best with an input voltage tolerance of 5%. The power-up under-voltage threshold voltage is V_{UVLOH1}. It ensures sufficient output voltage for operating the output. The power-down under-voltage threshold is V_{UVLOL1}. The integrated supply is based on a shunt regulator that emulates a diode structure to simplify designs. The device can then be supplied even by any voltage rail that exceeds the operating range by using a current limiting resistor placed in series to the supply terminal *IN* or *VCC1* (where applicable). If no suitable resistor in series to terminal *VCC1* is used for current limitation, then staying within the operating parameters is recommended to avoid unnecessary power dissipation in the IC.

The input side of the IC contains an integrated power supply buffer capacitor. External buffer capacitors for the supply voltage are not necessary, but possible. Such external buffer capacitors should not exceed $C_{VCC1,ext}$.

In addition, the Infineon SSI family provides a strong reverse bias capability for the supply terminals *IN* or *VCC1* (where applicable). This enables all variants to operate in differential operation with respect to their terminals *IN* and *GND1*.

A minimum off-time $t_{OFF,IN}$ or $t_{OFF,VCC1}$ is required between the turn-off and turn-on signals to establish a defined "off"-state on the output side of the isolator.

Variants iSSI20B02F and iSSI20B03F use the supply terminal *IN* to perform the reset procedure after the output side latch-off procedure of the protection functions. Variant iSSI20B11F can perform this reset at either at terminal *VCC1* or at terminal *IN*. In any case of reset of any variant, ensure that the reset time is larger than $t_{OFF,IN}$or $t_{OFF,VCC1}$ before turning on again after a protection event.

6.1.2 Logic input

Variant iSSI20B11F offers separate supply and control terminals. The control logic thresholds V_{IL} and V_{IH} at terminal *IN* are 3.3 V CMOS compliant and can be controlled directly from standard CMOS logic outputs. Please note that the signal level at terminal *IN* can be substantially higher than the supply voltage at terminal *VCC1*. For example, it is possible to apply signals on 5 V level while V_{VCC1} = 3.3 V. The output acts in phase with the input control signal at terminal *IN*. Before turning on, a minimum off-time $t_{OFF,IN}$ has to be considered for resetting the output side. If the equivalent MOSFET's input capacitance is larger than 100 pF longer off-times than $t_{OFF,IN}$ might be needed.

A new reset procedure has to be performed after a protection triggered turn-off. Variant iSSI20B11F can perform this reset at either at terminal *VCC1* or at terminal *IN*. In any case of reset of any variant, ensure that the reset time is larger than $t_{OFF,IN}$ before turning on again after a protection event.

Application can use variant iSSI20B11F with externally shorted terminals *VCC1* and *IN*. In this case, all operating guidelines of variants iSSI20B02F and iSSI20B03F apply.

6.2 Output side

6.2.1 Direct gate drive

Terminal *OUT* is the gate drive output. The output voltage V_{OUT} is sufficient to drive CoolMOS™, OptiMOS™, or TRENCHSTOP™ IGBT without additional, external buffers. Variants iSSI20B02F and iSSI20B03F are designed for direct gate drive and provide the short circuit output current I_{OUT} directly to the gate. This enables a quick turn-on of MOS-controlled power transistor.

6.2.2 Fast turn-on feature

Variant iSSI20B11F is designed for fast turn-on that further enforces the turn-on current by accumulating charge in an external buffer capacitor at terminal *BUF*. The accumulated charge is released to terminal *OUT*, if the voltage at terminal *BUF* equal or higher than the buffer threshold voltage $V_{BUF,th}$ and a turn-on condition is given on the control side.

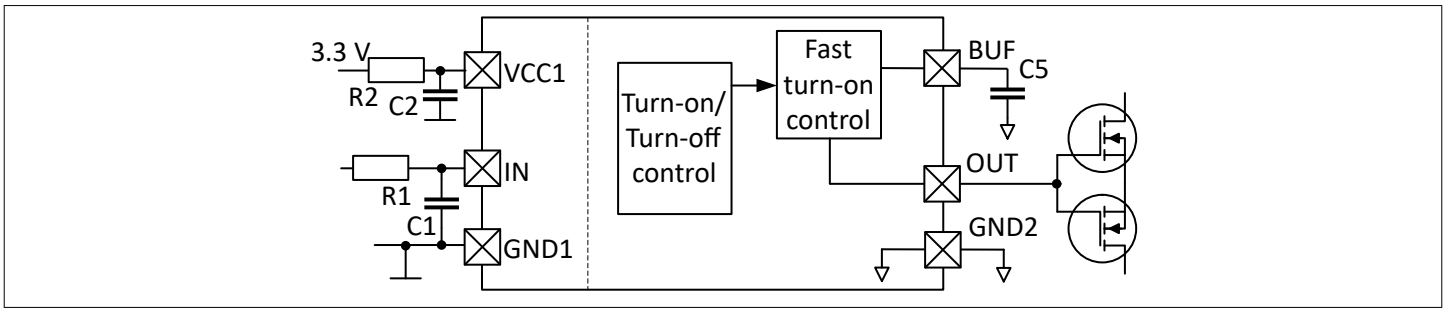


Figure 12 Fast turn-on feature of iSSI20B11F

6.2.3 Normal turn-off

The normal turn-off feature is implemented in all variants. A turn-off signal from the input side activates the integrated depletion FET. The depletion FET discharges the gate node of the operated power transistor. The Infineon SSI family's sink saturation current $I_{off,sat}$ is dimensioned to discharge CoolMOS™ S7 transistors within a few microseconds.

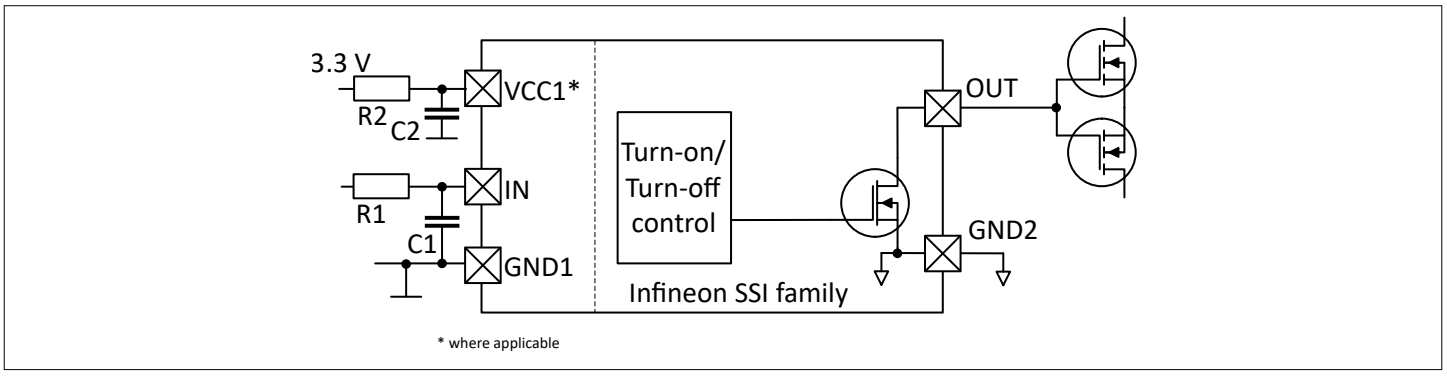


Figure 13 Normal turn-off

6.2.4 Fast turn-off

Overcurrent or over-temperature events trigger the fast turn-off feature of the Infineon SSI family. The fast turn-off enables the Infineon SSI family to shut down the power transistors inside their safe operating area particularly under high load operations. The Infineon SSI family's fast turn-off sink saturation current $I_{off,fast,sat}$ is dimensioned to discharge CoolMOS™ S7 transistors faster than a normal turn-off.

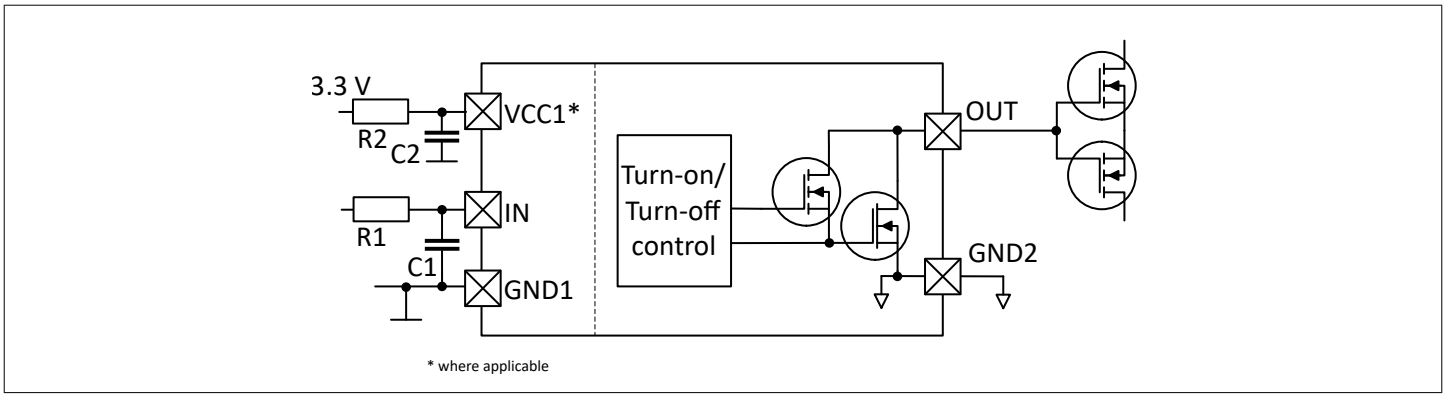


Figure 14 Fast turn-off

6.2.5 Dynamic Miller clamping (DMC)

The dv/dt applied by the connected AC voltage creates capacitive displacement currents through the parasitic capacitances of a power transistor. This can lead to parasitic turn-on of the power switch by increasing the voltage at the gate node of the power switch during its "off"-state. Three major effects can cause dv/dt to occur in installations:

- surge voltages
- fast electric transients (burst)
- dv/dt of line voltage

  The dv/dt of line voltage results in a relatively slow dv/dt of 320 V * 2*π * 50 Hz ~ 100 V/ms in 230 V a.c. grids. Many power transistors are robust, by default, against parasitic turn-on under this condition. Surge voltages and fast electric transients result in a much faster dv/dt and power transistors benefit from the dynamic Miller clamping feature.

The dynamic Miller clamping feature ensures that the power switch stays in the “off” state. It is activated by connecting the power switch's drain to terminal *MC* with a suitable capacitor. The dv/dt appearing at the drain also injects a current into terminal MC and activates of the dynamic Miller clamp FET.

Voltage clamping elements at the Miller clamping terminals may be needed to stay within the absolute maximum ratings.

6.2.6 Overcurrent protection

Overcurrent protection detects excessive, positive and negative current through the power transistor and uses the voltage drop at an external shunt resistor to trigger a comparator with a fixed threshold $|V_{CS,th}|$ at terminal *CS* or *TS/CS*. Please note that $V_{CS,th}$ can be positive or negative. Once triggered, the protection reacts quickly and is able to turn off, for example, CoolMOS™ IPT60R022S7 in very short time. Thus, it is able to support the AC-15 system tests according to IEC 60947-5-1 under appropriate operating conditions. The integrated noise filter has a filter time of $t_{CS,filter}$ and can be backed up by an external RC-filter. However, it is recommended to have as little external filtering as possible to get a quick reaction time in case of overcurrent.

The triggering of the overcurrent protection leads to the latched turn-off of the power switch with a sinking current of $I_{off,\,fast,sat}$.

Terminal *TS/CS* sources a bias current for temperature sensing in iSSI20B02F and iSSI20B11F. As the current sensing shunt is usually very low-resistive, the effect of the biasing current $I_{TS/CS,bias}$ with respect to the shunt signal can be neglected.

The dimensioning of the shunt follows this equation: $R_{sh} = \frac{|V_{CS,\,th}|}{I_{pk,\,max}}$

6.2.7 Over-temperature protection

The over-temperature protection of the Infineon SSI family offers protection against excessive temperatures of the driven power transistor by reading a PTC resistor. The Infineon SSI family products provide a constant bias current $I_{TS,bias}$ or $I_{TS/CS,bias}$, respectively, for the two types of temperature sensors listed above. The constant current generates a temperature dependent voltage at the temperature sensor. The sensor voltage is connected to terminal *TS* or TS/CS, and the terminal voltage is compared to the threshold $V_{TS,th}$. The integrated comparator includes a noise filter of duration $t_{TS,filter}$ for safe detection of the sensor signal that can be complemented by an external RC-filter. The resistive portion of the RC-filter influences the trigger temperature of the sensor, because the resistor adds a positive offset voltage to the temperature dependent voltage of the sensor. This influence can also be used to actively tune the protection feature for individual requirements. When using the over-temperature protection together with the over-current protection for example with iSSI20B03F, both sensing signals need to reference to GND2.

The triggering of the over-temperature protection leads to the latched turn-off of the power switch with a sinking current of $I_{off, fast,sat}$.

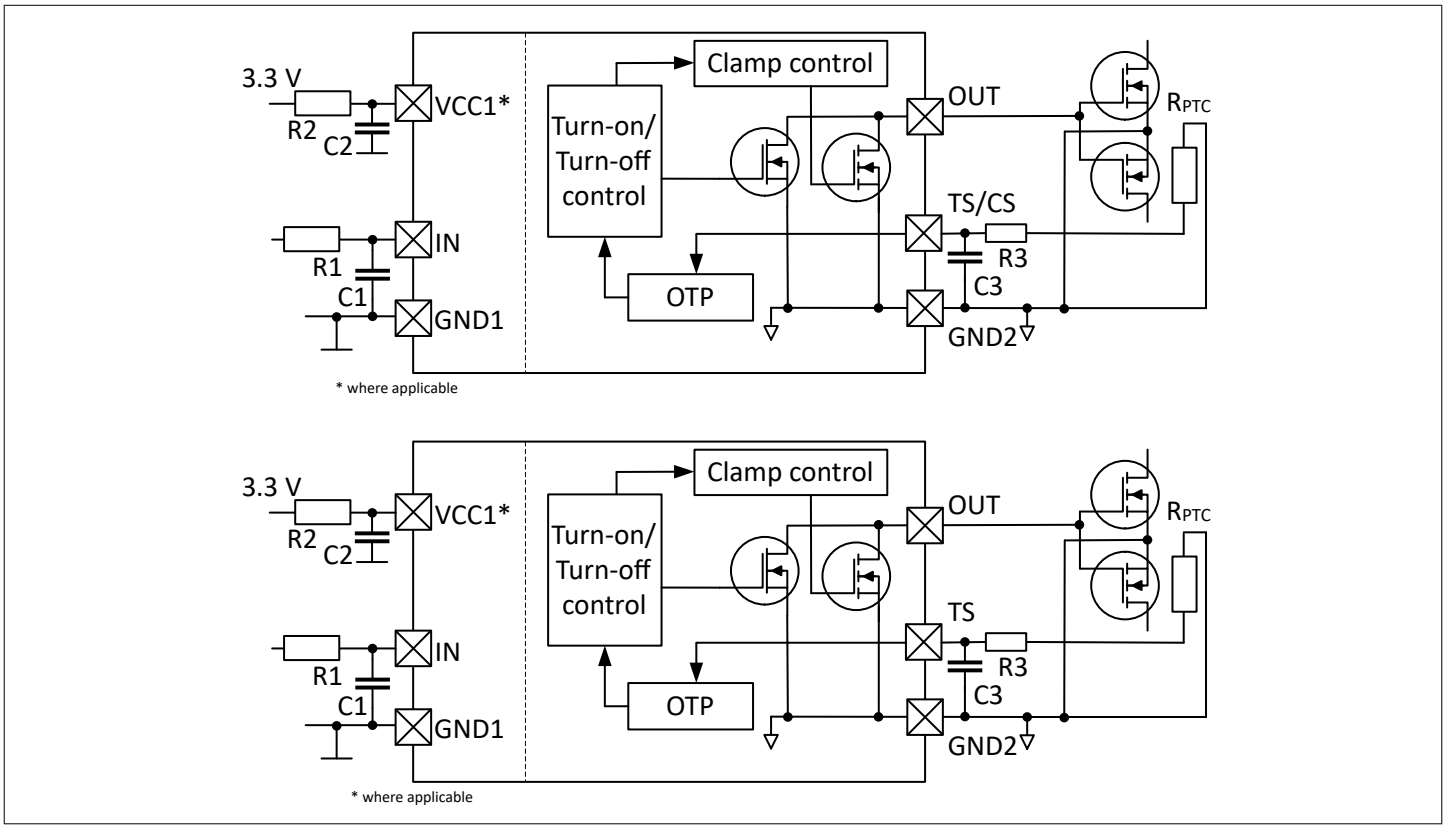


Figure 15 Schematic examples of the over-temperature protection circuit

7 Application information

Infineon is providing this information as a courtesy only and without acknowledging any legal obligation. Information in the following application chapters is not part of the Infineon component specification, and Infineon does not warrant its accuracy or completeness. Infineon's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Adaptation of the supply voltage

The Infineon SSI-family is best operated from a voltage source of 3.3 V. This allows a direct supply from a microcontroller. Please note that normally the pull-down device of general purpose I/O-terminals or high current terminals is stronger than the pull-up device. Thus, it is better to use the pull-down device to control the voltage supply of the Infineon SSI as it is displayed in the figure below.

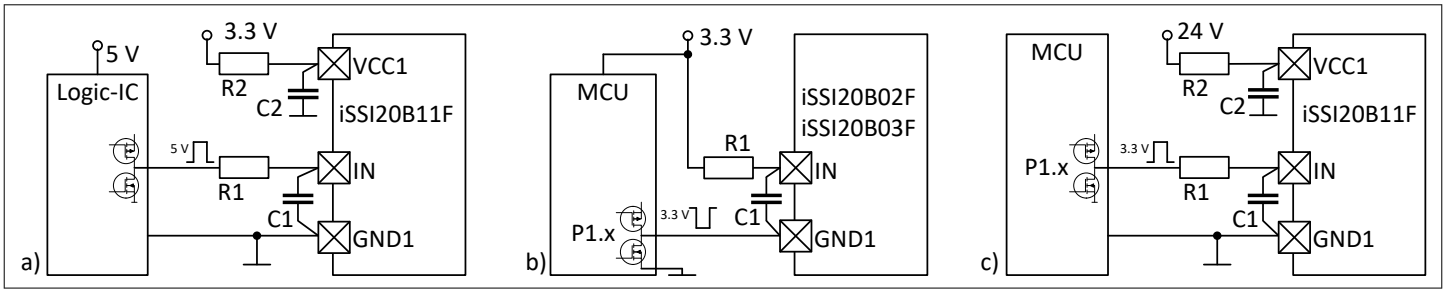


Figure 16 Examples of application relevant control options

The left part in the figure shows the option of using a logic -IC that is supplied with 5 V. Therefore, the logic-IC provides a control signal with 5 V, too, while Infineon SSI is supplied with 3.3 V. This simplifies the interfacing as no downward-level-shifters are required.

The middle part depicts a simple option for the supply scheme for iSSI20B02F and iSSI20B03F. Terminal *IN* is connected to 3.3V and terminal GND1 is connected to the driving port of the microcontroller. The Infineon SSI's output is inverted to the control signal at *IN*. This option requires ports that are able to sink at least the maximum value of I_{IN}, otherwise the effective supply voltage V_{IN} - V_{GND1} may not reach 3.3 V and the IC can stay in the under-voltage lockout mode.

Option c) connects the supply terminal *VCC1* to a higher voltage than 3.3 V, for example 24 V. In these cases, resistor R2 acts as a current limiting resistor. The value for the current limit is the typical value of I_{VCC1}. This results in a limiting resistor value of

$$R2 = \frac{V_{\text{supply}} - V_{\text{VCC1, op, max}}}{I_{\text{VCC1, typ}}} = \frac{24\ \text{V} - 3.5\ \text{V}}{16\ \text{mA}} = 1281\ \Omega \quad (1)$$

A selection of R2 = 1.3 kΩ is sufficient. Of course, worst-case conditions and tolerances of the supply voltage V_{supply} need to be considered, too. It is easy to understand that the solution using a current limiting resistor is not efficient as the resistor might dissipate noticeable power . Dimensioning R2 according to the maximum supply current $I_{VCC1,max}$ yields in higher losses inside the IC. Particularly when operating several Infineon SSI isolators, it is often more efficient to place a DC/DC-converter with a low-tolerance output voltage of 3.3 V instead of using a current limiting resistor for each Infineon SSI.

Very simple microcontroller have often no high current I/O-terminals. In such cases, an interface inverter is a solution for driving iSSI20B02F and iSSI20B03F. Such options using small-signal FETs are given in this figure.

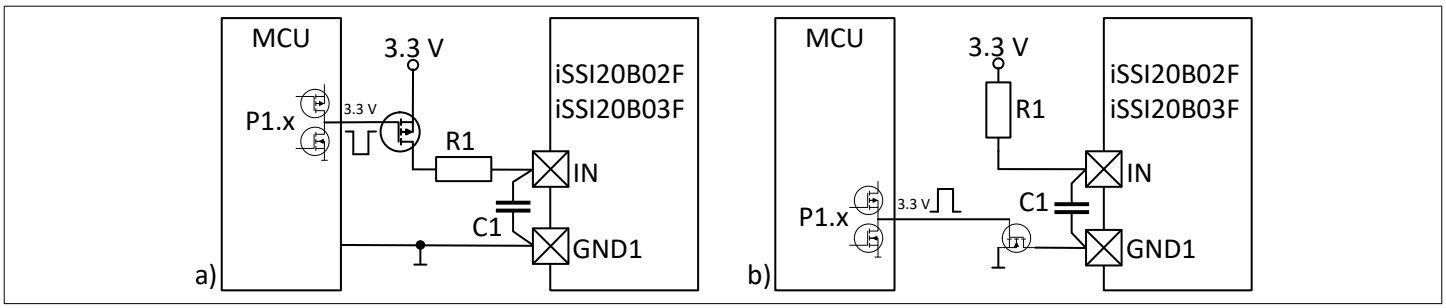


Figure 17 Interfacing with an inverter circuit

7.2 Grounding reference of current and temperature sensor signals

The two sensor signals of the current sensor (shunt) and the temperature sensor have to refer to a single ground reference. It is good engineering to refer the overall ground to one of the sensors.

It is recommended to place the shunt in closest proximity to T1 in order to keep the stray inductance L_σ as small as possible. Any stray inductance of the layout is of course detrimental for the temperature sense voltage v_{TS} signal quality. However, the temperature sensing can be filtered easier because the thermal capacity of the switch allows temperature increases only in the range of hundreds of microseconds or even more.

Please note that the gate voltage of T1 $v_{G,T1}$ is directly referenced to GND2 while the gate voltage of T2 $v_{G,T2}$ is lowered by means of the shunt voltage v_{Sh}.

The PTC resistor requires a good thermal coupling to the source pad of T1. The stray inductance L_σ is still active, but the good thermal coupling is a superior target to achieve than the minimization of the stray inductance.

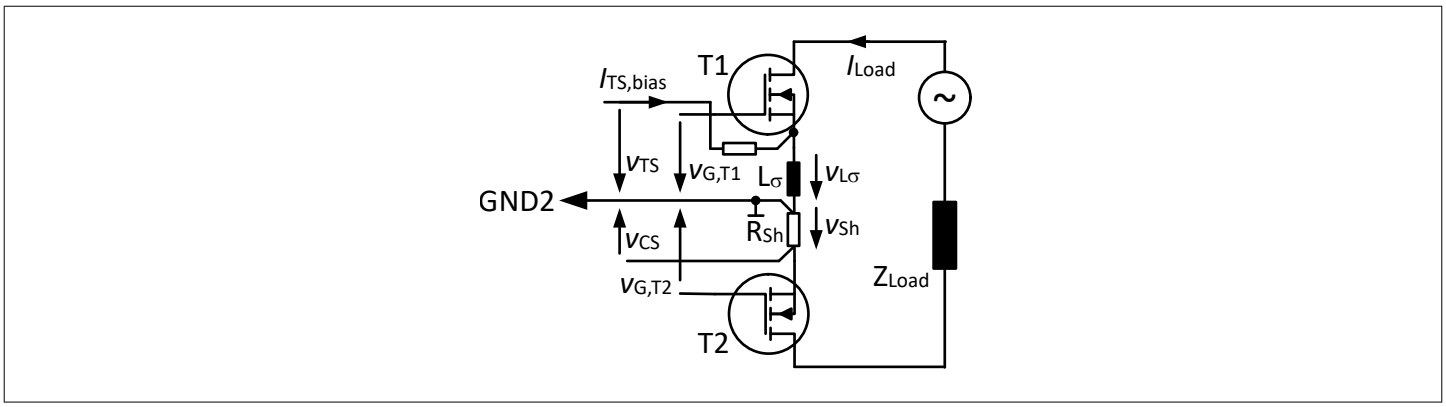


Figure 18 Grounding scheme for AC-switch with PTC temperature sensor

In DC-switch configurations, all aspects for placing and routing the current sensor and the temperature sensor signals apply in the same way as for AC-switch configurations.

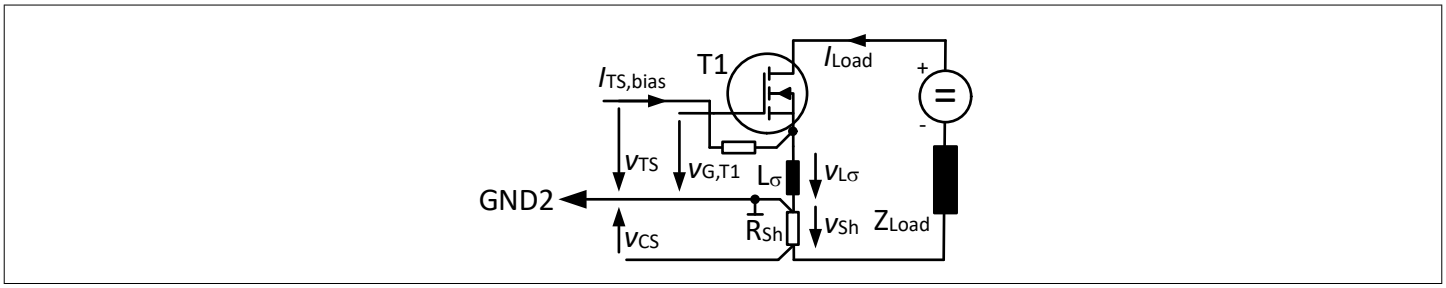


Figure 19 Grounding scheme for DC-switch with PTC temperature sensor

7.3 Fast turn-on using iSSI20B11F

The fast turn-on feature enables high-current high-voltage solid-state relays because it allows an amplified turn-on gate current that charges the gate capacitance much faster beyond the Miller voltage level. The fast turn-on saturation current $I_{on,fast,sat}$ of the integrated driving FETs is more than 1000 times higher compared to the direct drive output current I_{OUT} , when keeping terminal BUF unconnected. Please see also the chapter "Fast turn-on" in "Functional description" for more information. The fast turn-on feature should be used in particular in systems where high inrush currents require extremely short turn-on times.

The calculation of the buffer capacitor is simple, but yet essential to ensure a proper dimensioning of the fast turn-on. Take the example of a solid-state relay using two 22 mΩ CoolMOS™ in an a.c.-switch configuration (common-source). The gate voltage after the fast turn-on procedure is proposed to be in the range of 7 V to 8 V. The minimum fast turn-on comparator threshold $V_{BUF,th,min}$.

As there is only one MOSFET of an a.c. configuration in blocking mode while the other MOSFET is in zero-voltage mode, the gate charge is derived graphically in the way as explained in figure below.

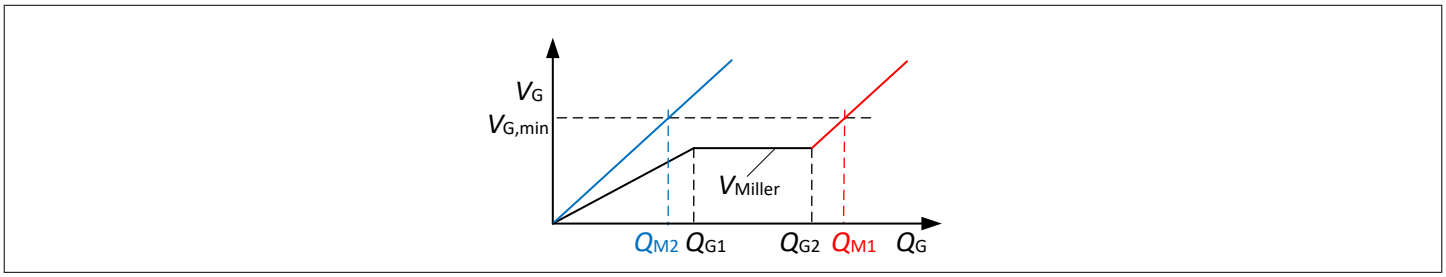


Figure 20 Gate charge construction for a.c. switch configuration (common source)

In an a.c. configuration of the switching transistor, there is always one switch that is in blocking mode. The other switching transistor is in freewheeling mode as its body diode or freewheeling diode is in forward bias. Therefore, only one transistor passes the Miller effect. The black/red graph shows a typical curve of the gate voltage V_G as a function of the gate charge Q_G for a MOSFET that is switched under voltage of - for example - 2/3 of the breakdown voltage. The blue curve is the gate charge of a MOSFET under zero-voltage condition (V_{DS} = 0). The blue curve has usually the same slope as the red branch.

The minimum capacitance $C_{BUF,min}$ to be connected to terminal *BUF* is

$$C_{\mathrm{BUF,\,min}} = 1.2 \cdot \frac{Q_{\mathrm{M1}} + Q_{\mathrm{M2}}}{V_{\mathrm{BUF,\,th,\,min}} - V_{\mathrm{G,\,min}}} \tag{2}$$

with Q_{M1} and Q_{M2} being the related gate charges at the end of the fast turn-on when reaching $V_{G,min}$, $V_{BUF,th,min}$ being the minimum fast turn-on comparator threshold voltage and $V_{G,min}$ being the minimum gate-source voltage $V_{GS,min}$ of the switching transistors. A safety factor of 1.2 covers the gate charge tolerance of the switching transistors.

For a.c. switch using two CoolMOS™ IPT60R022S7, a drain-source voltage of 300 V, and a minimum gate-source voltage $V_{G,min}$ = 7 V, the minimum buffer capacitance $C_{BUF,min}$ yields in:

$$C_{\mathrm{BUF,\,min}} = 1.2 \cdot \frac{100\ \mathrm{nC} + 70\ \mathrm{nC}}{10\ \mathrm{V} - 7\ \mathrm{V}} = 68\ \mathrm{nF} \tag{3}$$

7.4 Using the overcurrent protection feature

The overcurrent protection is a shunt voltage controlled feature that acts within a few 100 nanoseconds. The calculation of the shunt value considers the tolerances of the supply voltage, peak values in case of AC current, and the tolerances of the IC.

The calculation for covering protection at $I_{load,\,rms}$ = 5 A follows this flow:

First, the peak load current including a tolerance of 10% is calculated:

$$I_{\mathrm{pk,\,max}} = 1.1 \cdot \sqrt{2} \cdot 5\,\mathrm{A} = 7.78\ \mathrm{A\ peak} \tag{4}$$

Then the worst-case currents are calculated by considering the IC's tolerances:

$$\begin{aligned} I_{\mathrm{pk,\,trig,\,min}} &= I_{\mathrm{pk,\,trig}} \frac{v_{\mathrm{CS,\,th,\,min}} + 10\,\mathrm{mV} + 20\,\mathrm{mV}}{v_{\mathrm{CS,\,th,\,typ}} + 20\ \mathrm{mV}} = 9.77\ \mathrm{A\ peak} \\ I_{\mathrm{pk,\,trig,\,max}} &= I_{\mathrm{pk,\,trig}} \frac{v_{\mathrm{CS,\,th,\,max}} + 10\,\mathrm{mV} + 20\,\mathrm{mV}}{v_{\mathrm{CS,\,th,\,typ}} + 20\ \mathrm{mV}} = 11.34\ \mathrm{A\ peak} \end{aligned} \tag{5}$$

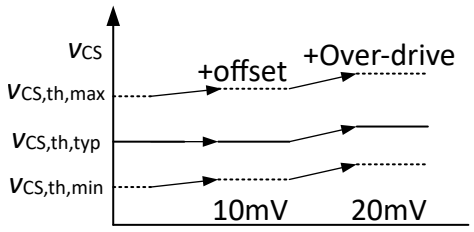


Figure 21 Worst-case current sense trigger thresholds

As the protection should not trigger for the minimum overcurrent comparator threshold, the shunt resistor value is:

$$R_{\mathrm{Sh,\,max}} = \frac{v_{\mathrm{CS,\,th,\,min}} + 10\,\mathrm{mV} + 20\,\mathrm{mV}}{I_{\mathrm{pk,\,trig,\,max}}} = 19.0\ \mathrm{m\Omega} \tag{6}$$

The above equation results in a selected resistance of R_{Sh} = 18 mΩ.

7.5 Using the dynamic Miller clamping

Connecting a capacitor between the input terminal *MC* and the drain terminals of the switching transistor activates the dynamic Miller clamping feature that is available in variant iSSI20B02F. Let terminals *MC* float to deactivate the feature. The dynamic Miller clamp reinforces the strong, yet limited pull-down capability of Infineon SSI in case that high dv_{DS}/dt events occur at the switched transistors. This is in particular important during off-state, if fast electric transients (bursts) occur. Even though there is usually no dedicated gate resistor in use, transients might lead to a parasitic turn-on of the switched transistor by pulling the gate higher than its gate-source threshold voltage.

The dimensioning of the coupling capacitors considers the fastest occurring dv_{DS}/dt-rates that appear in the application. In a.c. applications, bursts according to IEC 61000-4-4 can be a reference that specifies very steep pulses. However, the resulting pulses that stress the device-under-test have a lower amplitude and slope due to the cabling inductance and capacitance. An assumption for dv_{DS}/dt can be, for example, 10 V/ns and the coupling capacitance may be 1 pF. Please note that one of the two capacitors is shorted bypassed to GND2 by the related switched transistor in parallel. Thus, the only one capacitor is coupling the dv_{DS}/dt signal.

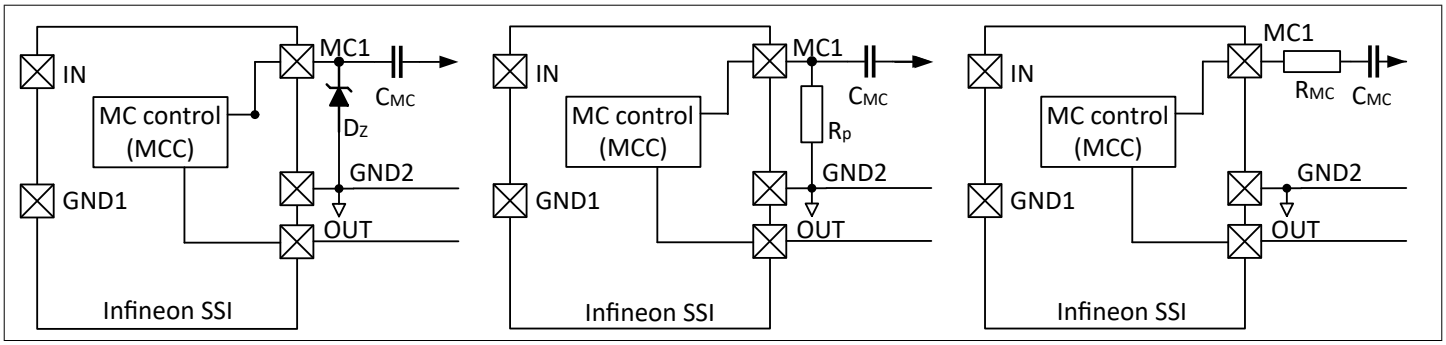


Figure 22 Dynamic Miller clamp options with zener diode (left), parallel resistor (middle) and series resistor (right)

In the above mentioned example, the coupled capacitive current into terminal *MC* is 10 V/ns * 1 pF = 10 mA. This would generate a voltage at terminal *MC* of 10 mA * R_{MC} = 5 V. Even though the static absolute maximum voltage rating at *MC* is v_{MC} = 3.6 V, the dynamic current $I_{MC,dyn}$ for sporadic events (duty cycle < 1%, pulse duration < 1 µs) that is injected into this terminal can be applied for pulsed stress. Therefore, clamping elements, such a 3.3 V clamping zener diode at terminal *MC* to reduce voltages above the zener voltage might not be needed. However, special needs to be taken at the evaluation of the highest dv/dt in systems. Other clampings options are a resistor between terminal *MC* and *GND2* that would take a portion of the coupled capacitive current or applying a series resistor that generates enough voltage to keep the limits according to the figure above.

7.6 Inductive energy clamping methods

Solid-state relays are often used in combination with loads that have an inductive portion. The inductive portion generates an over-voltage, if the isolator's output is turned off. The amplitude of the over-voltage can exceed the switching transistor's maximum breakdown voltage. Therefore, a clamping element is needed to limit the drain-source voltage of the switching transistor. Various options are possible:

- TVS (transient voltage suppressor) diodes,
- varistors,
- snubbers and
- others

Special care is required for the dimensioning and selection of the related components depending on the application's operating range. For example, two or even more TVS diodes can be required to fulfill the datasheet of the clamping element. Also combinations of the above mentioned options can help for a optimized clamping solution.

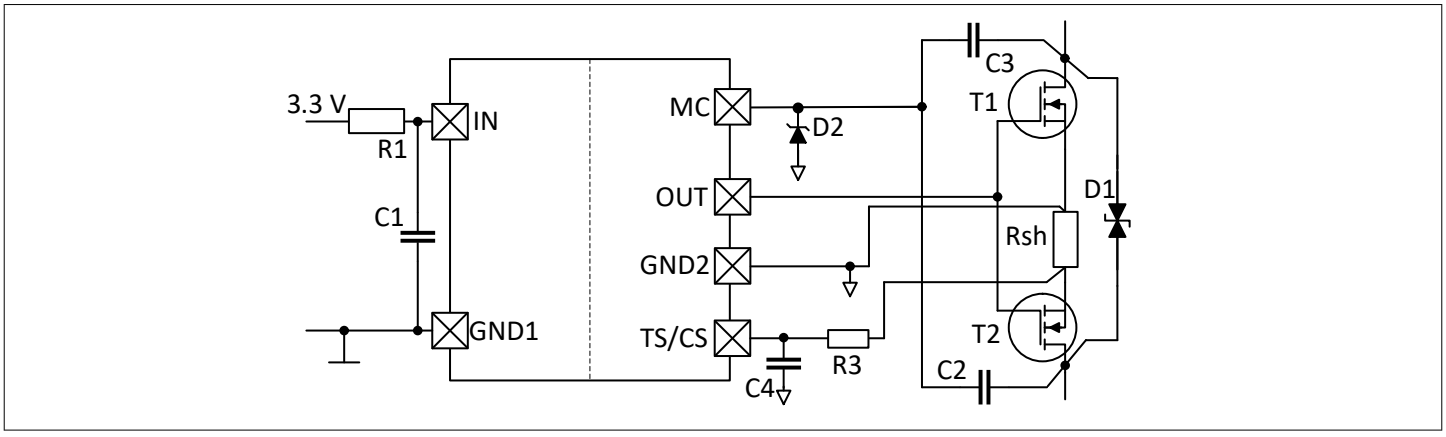


Figure 23 Example of a drain-to-drain TVS-diode D1 as a clamping element in an AC-switch configuration using iSSI20B02F

7.7 Electro Magnetic Interference (EMI) mitigation methods

Infineon's iSSI family of solid-state isolators have built-in spread spectrum techniques that reduce the noise power level at one frequency. Depending on the end equipment, additional components and PCB layout considerations are needed to meet the EMI performance. The system designer can select which of the measures work to minimize EMI depending on the overall system constraints and end equipment regulation standards (Class A or Class B).

The measures listed below reduce emissions by providing a capacitive return path from the secondary side to the primary side or by increasing the common mode loop impedance with an inductive component on the primary side.

- **Capacitive Return Paths:** Use a discrete Y capacitor between the primary ground and secondary ground. Sometimes the system design requires a Y capacitor for safety purposes and if this Y capacitance is located on the same board as the iSSI solid-state isolator, this will act as a capacitive return path. For functional isolation a normal capacitor with sufficient voltage rating can be used.
- **Inductive Components:** A pair of ferrite beads or a common mode choke with a high frequency impedance in the range of 600 Ω to 10 kΩ may be placed in series with the system supply or VCC pin and GND1 pin supply on the primary side. A similar arrangement can be placed on the control signal input or IN pin and GND1 pin if a separate control signal is used.
- **Input RC:** By placing a resistor in series with the input bias supply and a capacitor in parallel, the circuit prevents high-frequency components from entering the DC supply line, reducing electromagnetic interference (EMI), and improving stability.

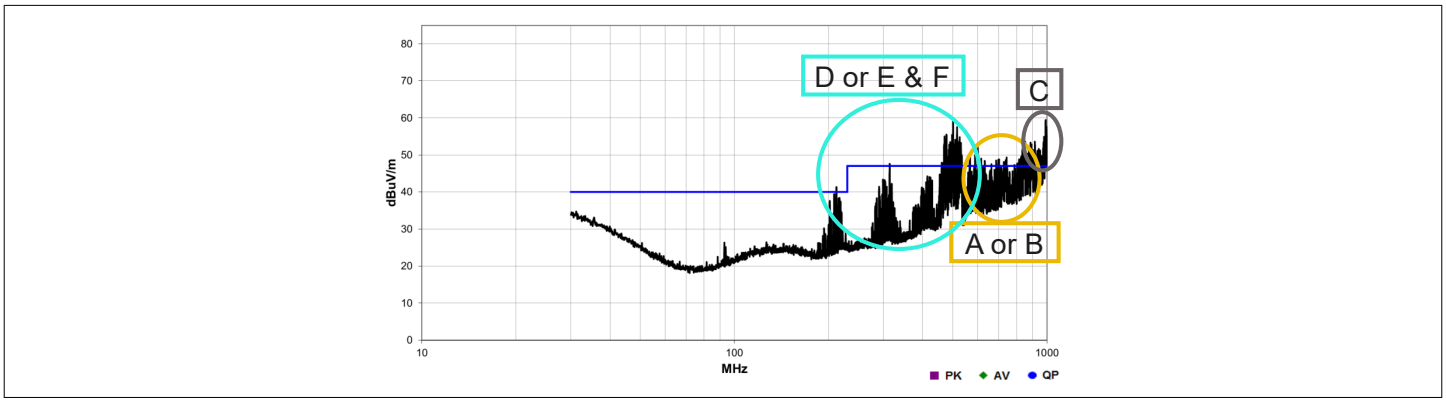


Figure 24 Example EMI Mitigation – Common mode choke CM1/CM2, pi-filter with ferrite bead FB1/FB2, Y1/Y2 capacitors

As shown in the figures below, different EMI mitigation schemes can be applied to the iSSI20BxxF family of solid-state isolators to meet the EMC standards under test. Standalone or a combination of the mitigation techiques usually work together to meet EMI. Eg: Y capacitors + Ferrite Bead or Ferrite beads only or Y-capacitors +common mode choke.

(A) or (B) Common mode chokes (2.2 kΩ @ >100 MHz) or Ferrite Beads (2.2 kΩ @ > 100 MHz) for reducing noise peaks greater than 100 MHz

(C) R1 / C1 higher R1 (75 Ω to 150 Ω) based on input voltage limits > 800 MHz high frequency peaks

R1 sizing guidelines as per equation 1 in the earlier section 7.1 of the datasheet should be considered. VCC1 / IN of the IC must not go below UVLO (2.85 V) under all operating conditions.

Y2 capacitors (in series below the IC) – for solving noise peaks at fundamental frequencies (100MHz, 200 MHz, 300 MHz ....upto 800 MHz)

(E) & (F) Y2 capacitors (in parallel on the two sides of the IC) – for solving noise peaks at fundamental frequencies (100MHz, 200 MHz, 300 MHz....upto 800 MHz)

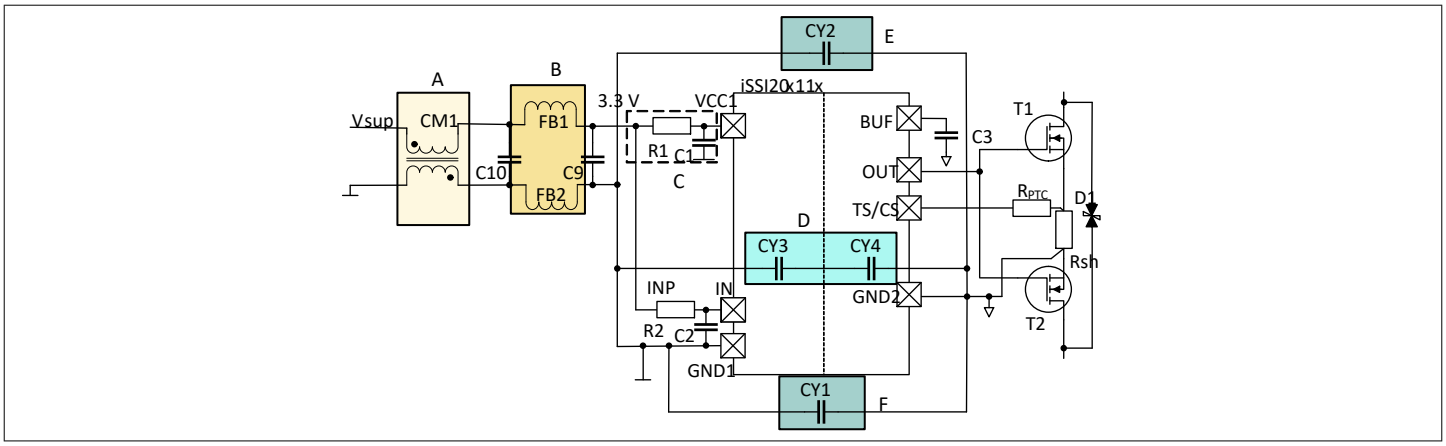


Figure 25 Example EMI Mitigation – Common mode choke CM1/CM2, pi-filter with ferrite bead FB1/FB2, Y1/Y2 capacitors

Different layout techniques depending on both the system EMI requirements and the system dielectric withstand testing (HiPot) parameters are possible. An optimal layout is shown in the figure below with these considerations:

- Seperating the input ground and connecting via common mode choke or ferrite bead
- Stiched vias for low impedance ground planes

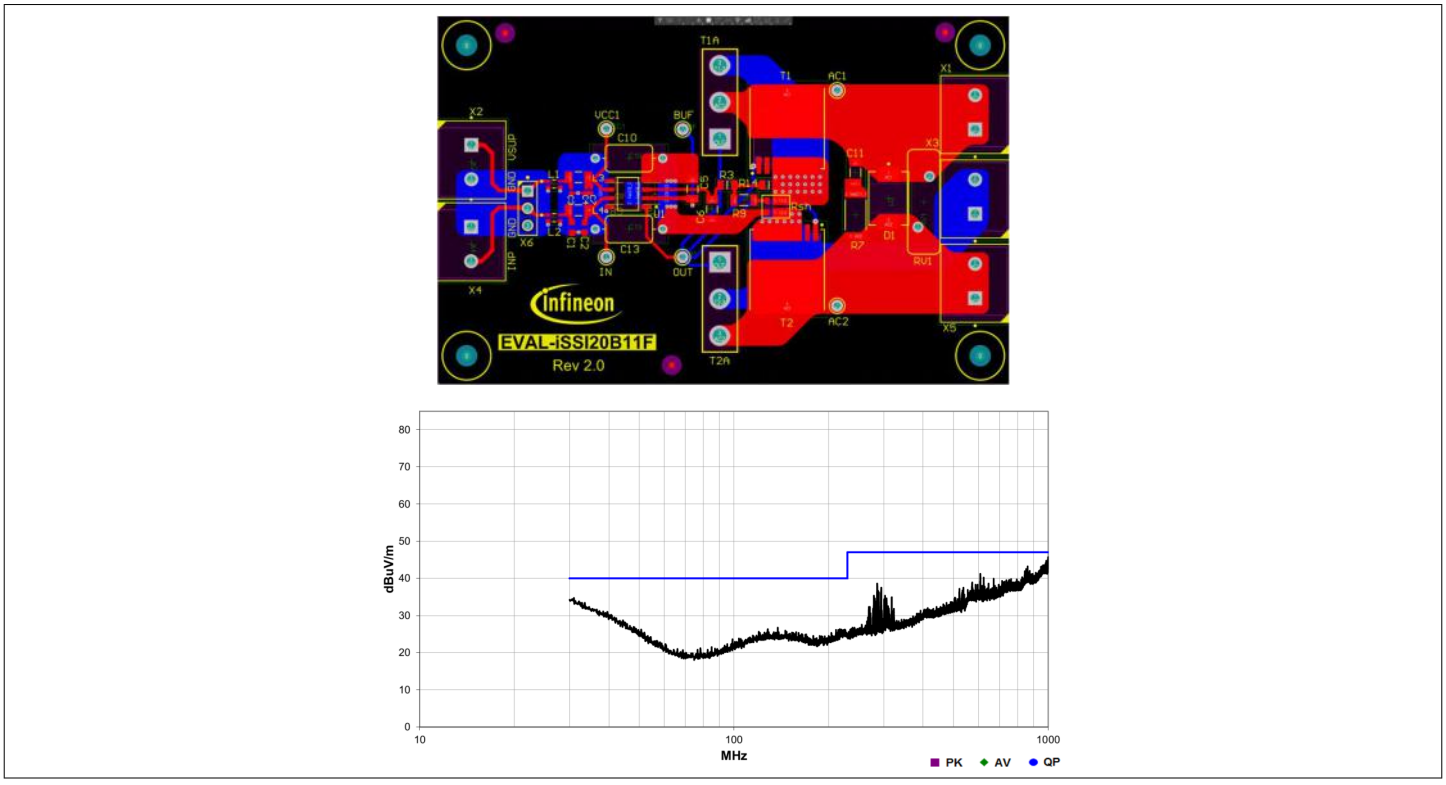


Figure 26 Evaluation board of iSSI20B11F meeting EN55032 / CISPR32 Class B Standard for 3 m radiated emission scan

Using the Y capacitors and ferrite beads, EVAL-iSSI20B11F evaluation boards meet the CISPR32 / EN55032 Class B Radiated EMI standards as required for light industrial, commercial, and residential application. Here two ferrite beads reduce the flow of CM current into the interfacing ground plane of the control circuitry. The iSSI20BxxF family reduces costs by meeting CISPR 32/EN 55032 Class B with significant margin on a 2-layer PCB without the need for any expensive radiate emission mitigation techniques.

Further EMI mitigation details can be found in the EMI mitigation application note on our solid-state isolators webpage (www.infineon.com/issi).

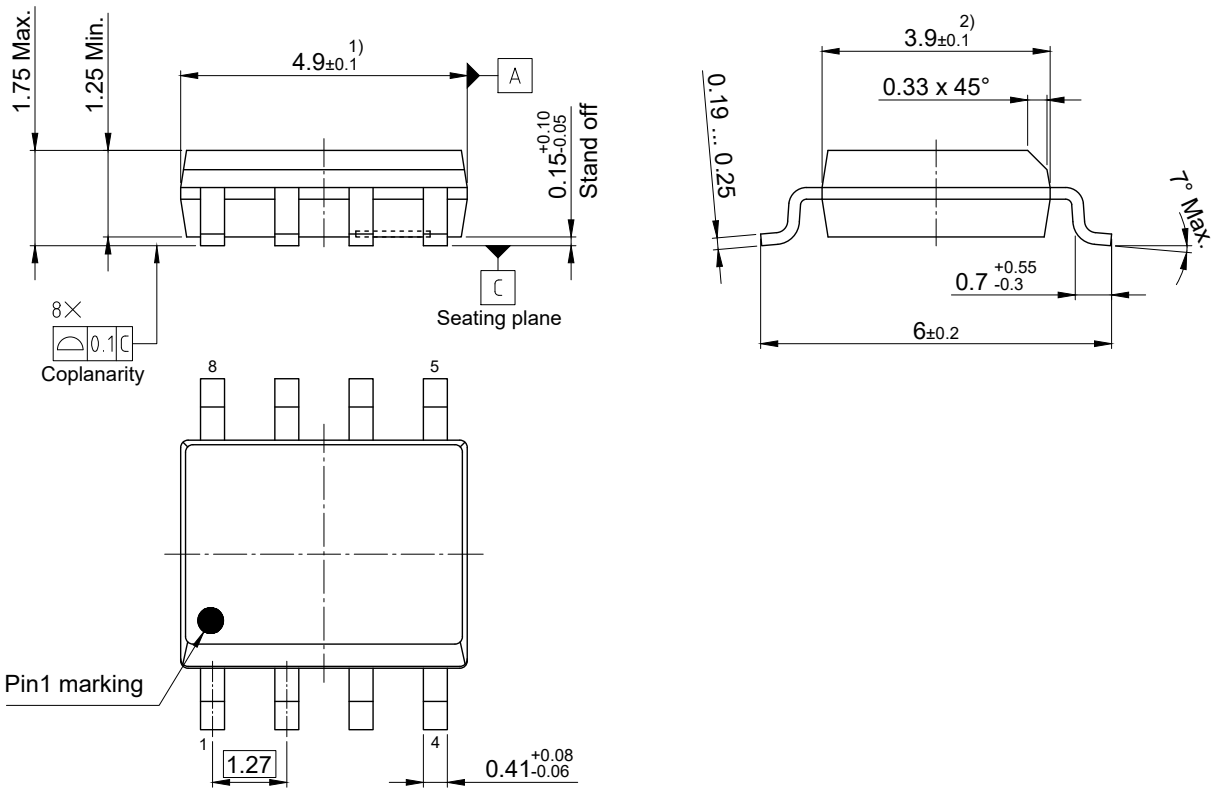
8 Related products

Infineon is providing this information as a courtesy only and without acknowledging any legal obligation. Information in the this chapter is not part of the Infineon component specification, and Infineon does not warrant its accuracy or completeness. Infineon's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Product group	Product name	Description
Infineon SSI solid-state isolators	Eval-iSSI20B11F	solid-state relay featuring overcurrent protection and fast turn-on and 600 V, 65 mΩ CoolMOS™ S7
Infineon SSI solid-state isolators	Eval-iSSI20B03F	Solid-state relay featuring over-temperature protection (PTC), overcurrent protection, and standard turn-on with 100 V, 3.5 mΩ MOSFETs in source-to-source configuration
Infineon SSI solid-state isolators	Eval-iSSI20B02FCS	Solid-state relay featuring overcurrent protection, dynamic miller clamping and standard turn-on with 60 V, 1.5 mΩ MOSFETs in source-to-source configuration
Infineon SSI solid-state isolators	Eval-iSSI20B02FTS	Solid-state relay featuring over-temperature protection (PTC), dynamic miller clamping and standard turn-on with 100 V, 3.5 mΩ MOSFETs in source-to-source configuration
CoolMOS™ S7 discrete MOSFETs with and without integrated temperature sensor	IPT60R065S7 / IPT60T065S7	600 V, 65 mΩ MOSFET in TO-leadless (HSOF-8) / incl. integrated temperature sensor
	IPT60R040S7 / IPT60T040S7	600 V, 40 mΩ MOSFET in TO-leadless (HSOF-8) / incl. integrated temperature sensor
	IPT60R022S7 / IPT60T022S7	600 V, 22 mΩ MOSFET in TO-leadless (HSOF-8) / incl. integrated temperature sensor
	IPQC60R022S7 / IPQC60T022S7	600 V, 22 mΩ MOSFET in QDPAK bottom-side cooled package (HDSOP) / incl. integrated temperature sensor
	IPDQ60R022S7 / IPDQ60T022S7	600 V, 22 mΩ MOSFET in QDPAK top-side cooled package (HDSOP) / incl. integrated temperature sensor
	IPDQ60R040S7	600 V, 40 mΩ MOSFET in QDPAK top-side cooled package (HDSOP)
	IPDQ60R065S7	600 V, 65 mΩ MOSFET in QDPAK top-side cooled package (HDSOP)
OptiMOS™ Linear FET, discrete MOSFETs	IPT008N06NM5LF	60 V, 0.8 mΩ MOSFET in TO-leadless (HSOF-8)
	IPT013N08NM5LF	80 V, 1.3 mΩ MOSFET in TO-leadless (HSOF-8)
	IPB017N10N5LF	100 V, 1.7 mΩ MOSFET in D2PAK 7pin (TO-263 7pin)
	IPB020N10N5LF	100 V, 2.0 mΩ MOSFET in D2PAK 7pin (TO-263 7pin)
	IPB033N10N5LF	100 V, 3.3 mΩ MOSFET in D2PAK (PG-TO263-3)
	IPB048N15N5LF	150 V, 4.8 mΩ MOSFET in D2PAK (PG-TO263-3)
	IPB083N15N5LF	150 V, 8.3 mΩ MOSFET in D2PAK (PG-TO263-3)
	IPB110N20N3LF	200 V, 11 mΩ MOSFET in D2PAK (PG-TO263-3)

9 Package dimensions

9.1 Package outline



1) Does not include plastic or metal protrusion of 0.15 mm max. per side
2) Does not include plastic protrusion of 0.25 mm max. per side.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]
Drawing according to ISO 8015, general tolerances ISO 2768-mK

Figure 27 PG-DSO-8-72

Revision history

Document version	Date of release	Description of changes
0.8	2025-06-25	Target Datasheet
1.0	2025-12-04	Preliminary Datasheet
1.1	2026-01-07	Preliminary datasheet with minor language changes and removal of redundant diagrams
1.2	2026-01-12	Modified diagrams
1.3	2026-02-26	Revised marking info on page 2
1.4	2026-03-16	Final Datasheet. Revised final product picture on page 1, added EMI Mitigation in section 7.7
1.41	2026-06-02	Changed layout

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