

Isolated digital input IC for industrial automation

Features

- Digital inputs for industrial sensors in sink configuration:
 - 8 input channels for 24 V sensors, Type 1 or 3 (compliant to IEC61131-2)
 - With two channels in parallel: 4 inputs for 48-V sensors, Type 1 or 3, 2.3 mA (compliant to IEC61131-2)
- -60 V to +60V sensor input voltage range
- High precision sensor current regulation: 2.1 mA to 2.5 mA
- Configurable sampling frequency: 20 kHz, 200 kHz or 500 kHz
- Configurable deglitching filter times: 50 μ s to 20 ms
- Configurable 3.3 V microcontroller interface for 8/16/24bit SPI modes, parallel mode or optocoupler emulation mode
- Input synchronization with data freeze pin
- Advanced SPI features: CRC checks and daisy chain
- Control for the channel-status LED indicators
- Interrupt pin signaling any change on input status
- Diagnostic feedback:
 - channel resolved sensor wire-break detection
 - V_{BB} missing voltage warning
 - Loss of V_{BB} (V_{BB} undervoltage shutdown)
 - V_{BB} overvoltage warning
 - Overtemperature alarm
- ± 150 V/ns (min) common-mode transient immunity (CMTI)
- 200 A/m (min) magnetic field immunity (MFI)
- -40°C to +125°C junction temperature



Potential applications

- Programmable logic controllers (PLC)
- Robotics
- Industrial PCs
- Commercial and agricultural vehicles (CAVs)
- Industrial IO systems
- Manufacturing machinery

Product validation

Qualified for industrial applications according to JEDEC.

Isolation

2500 Vrms galvanic isolation according to UL1577 (pending).

Description

ISOFACE™ ISO2I828V is an eight channel digital input IC for sink configuration. In an 8 mm × 8 mm 40-pin VQFN-40-24 package, the ISO2I828V offers 2500 Vrms integrated galvanic insulation, according to UL1577 (pending certification). The integrated high precision current sink regulators are designed to minimize the power dissipation of the application. The ISO2I828V is designed for eight 24 V sink inputs or alternatively four 48 V sink inputs, each according EN61131-2, Type 1 and Type 3. The ISO2I828V diagnostics can support preventive system-level maintenance. A 3.3 V CMOS-level microcontroller interface is available. It can be operated in SPI serial mode or parallel mode to setup the system and to read sensor information, the system status and diagnostic feedback.

Description

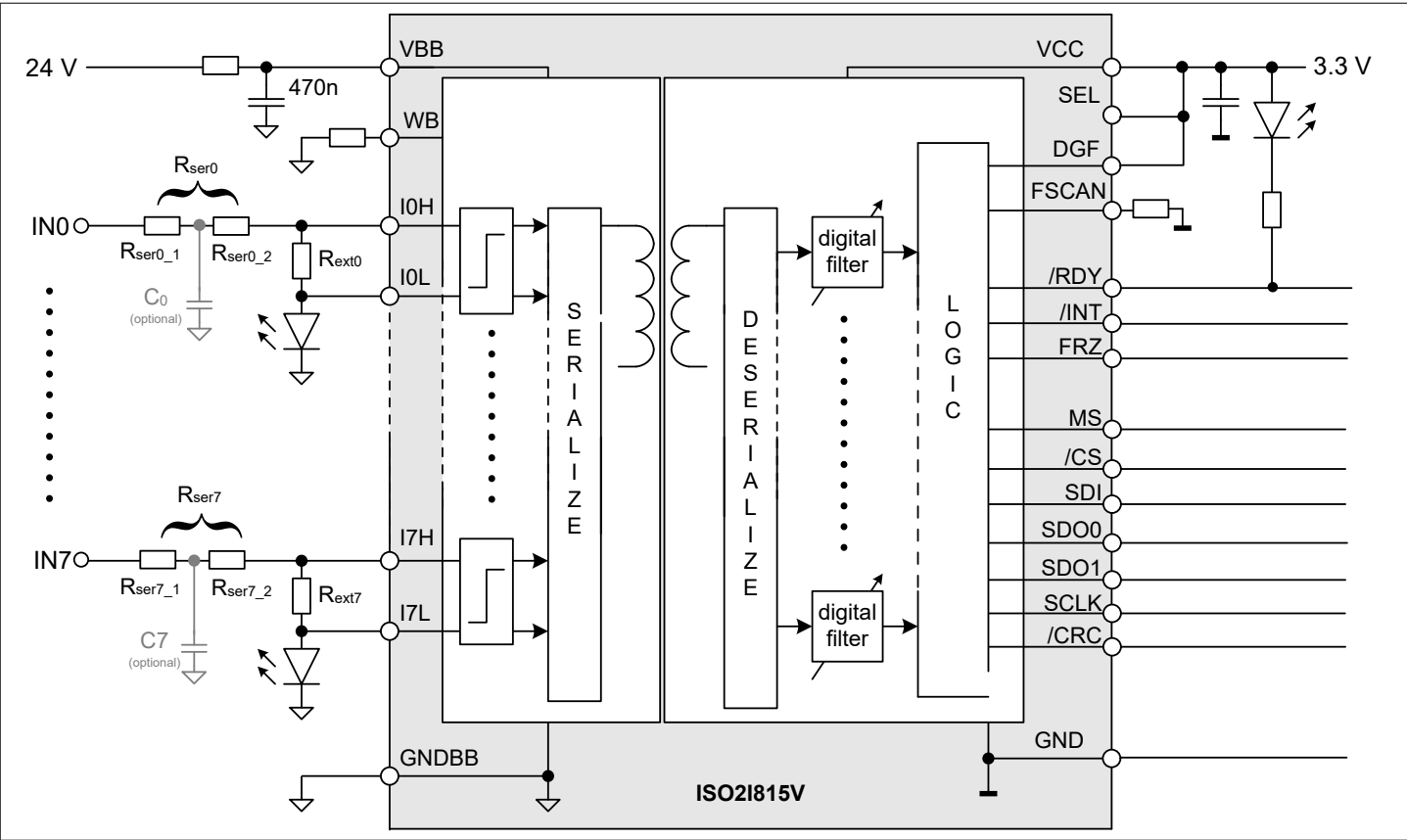


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1 Typical application circuits with and without channel LEDs

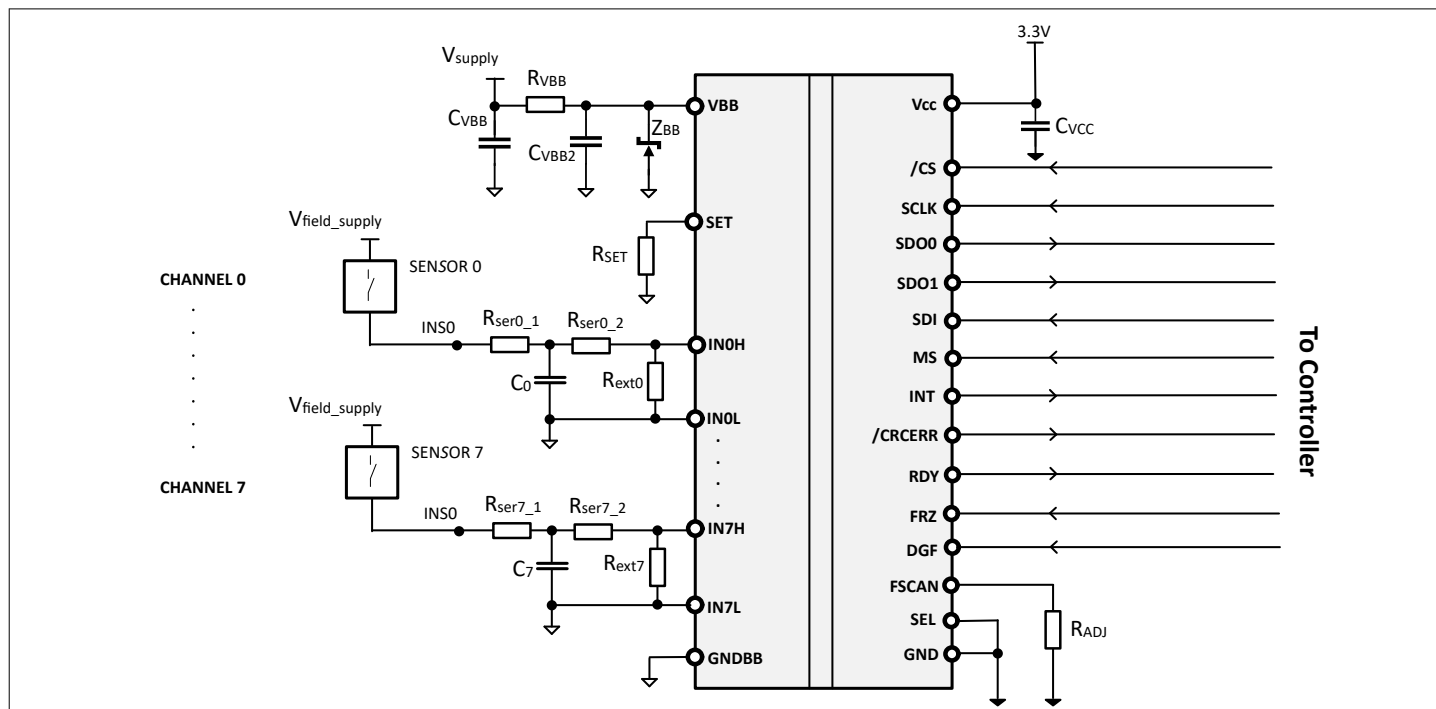


Figure 1 Typical application using SPI interface with eight 24 V sensors in sink configuration (2.3 mA per channel) without status LEDs

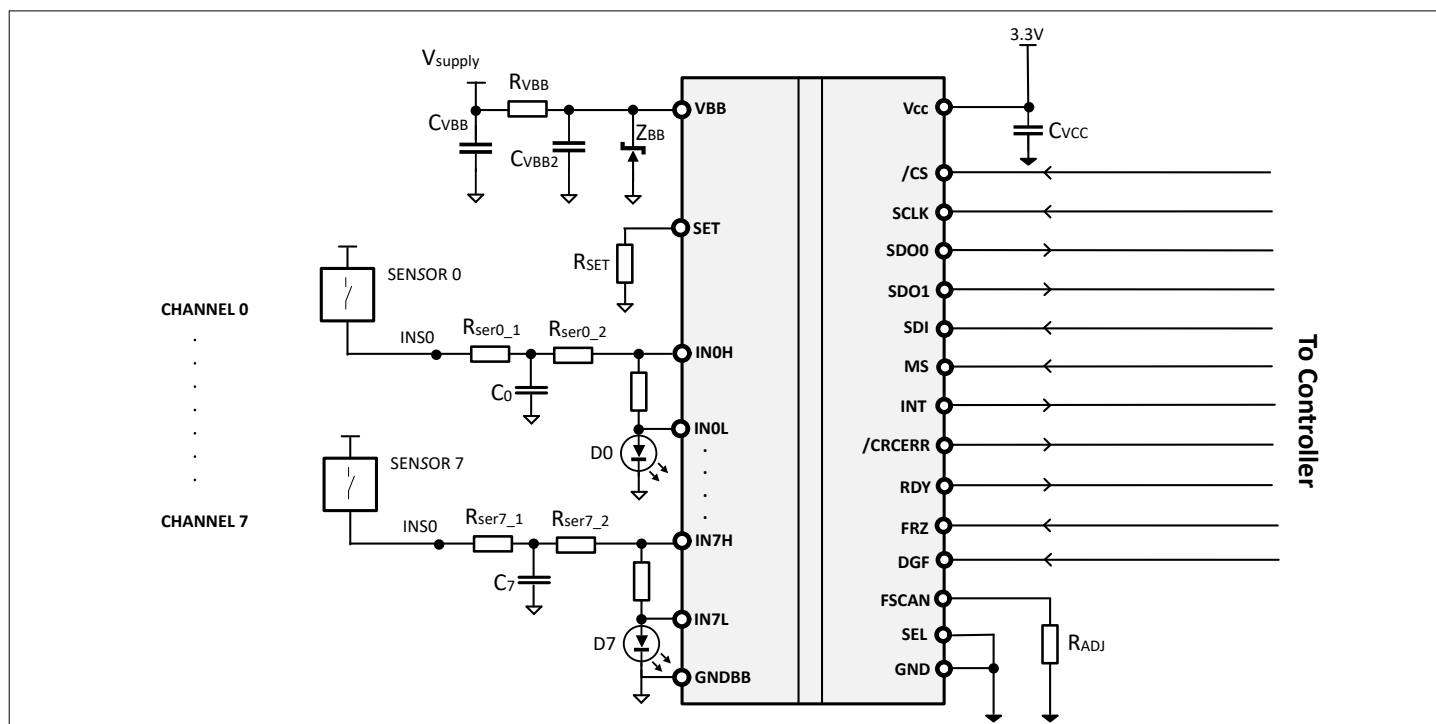


Figure 2 Typical application using SPI interface with eight 24 V sensors in sink configuration (2.3 mA per channel) in combination with loss-free status LEDs

1 Typical application circuits with and without channel LEDs

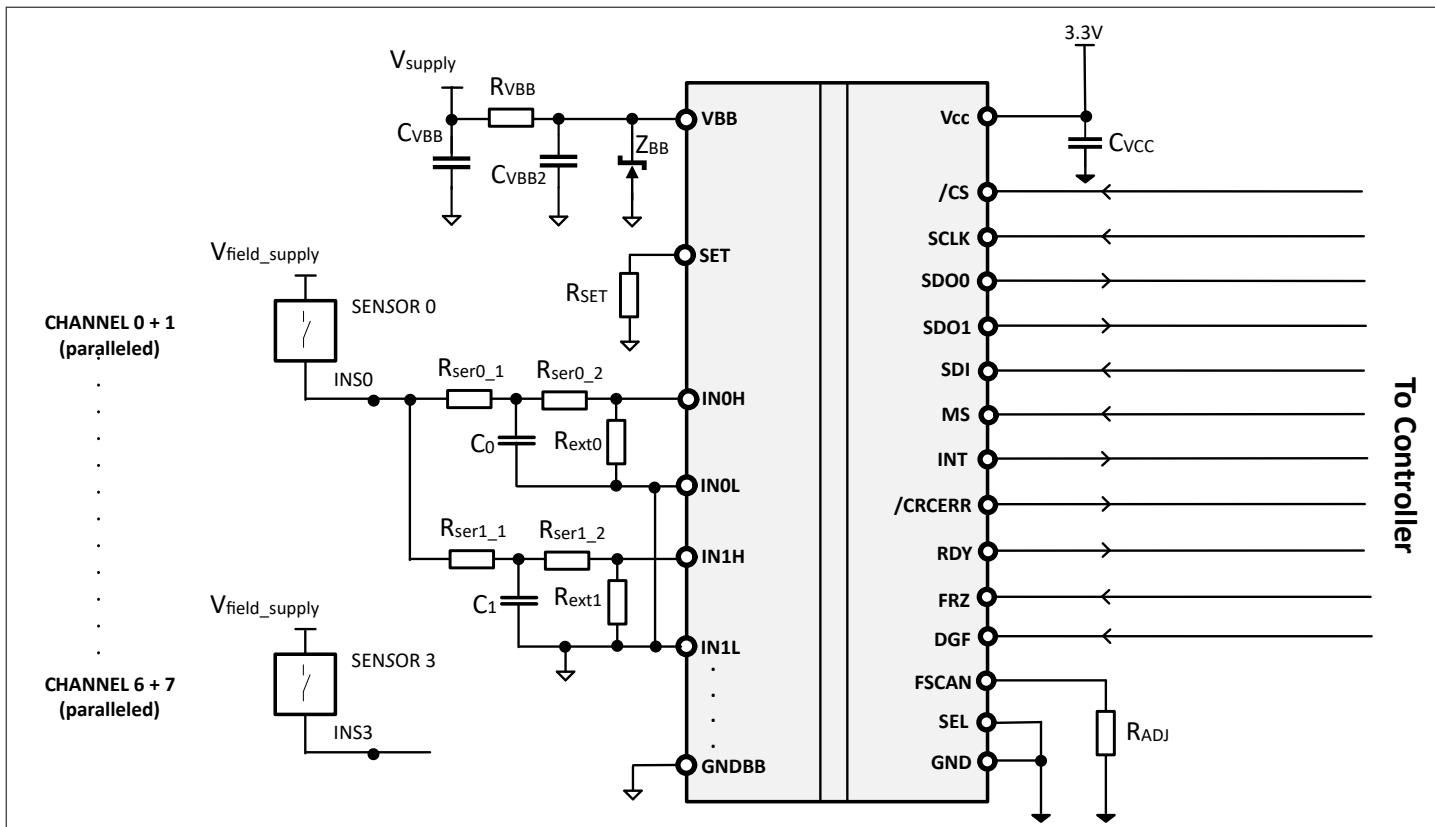


Figure 3 Typical application using SPI interface with four 48 V sensors in sink configuration (2.3 mA per channel) without status LEDs

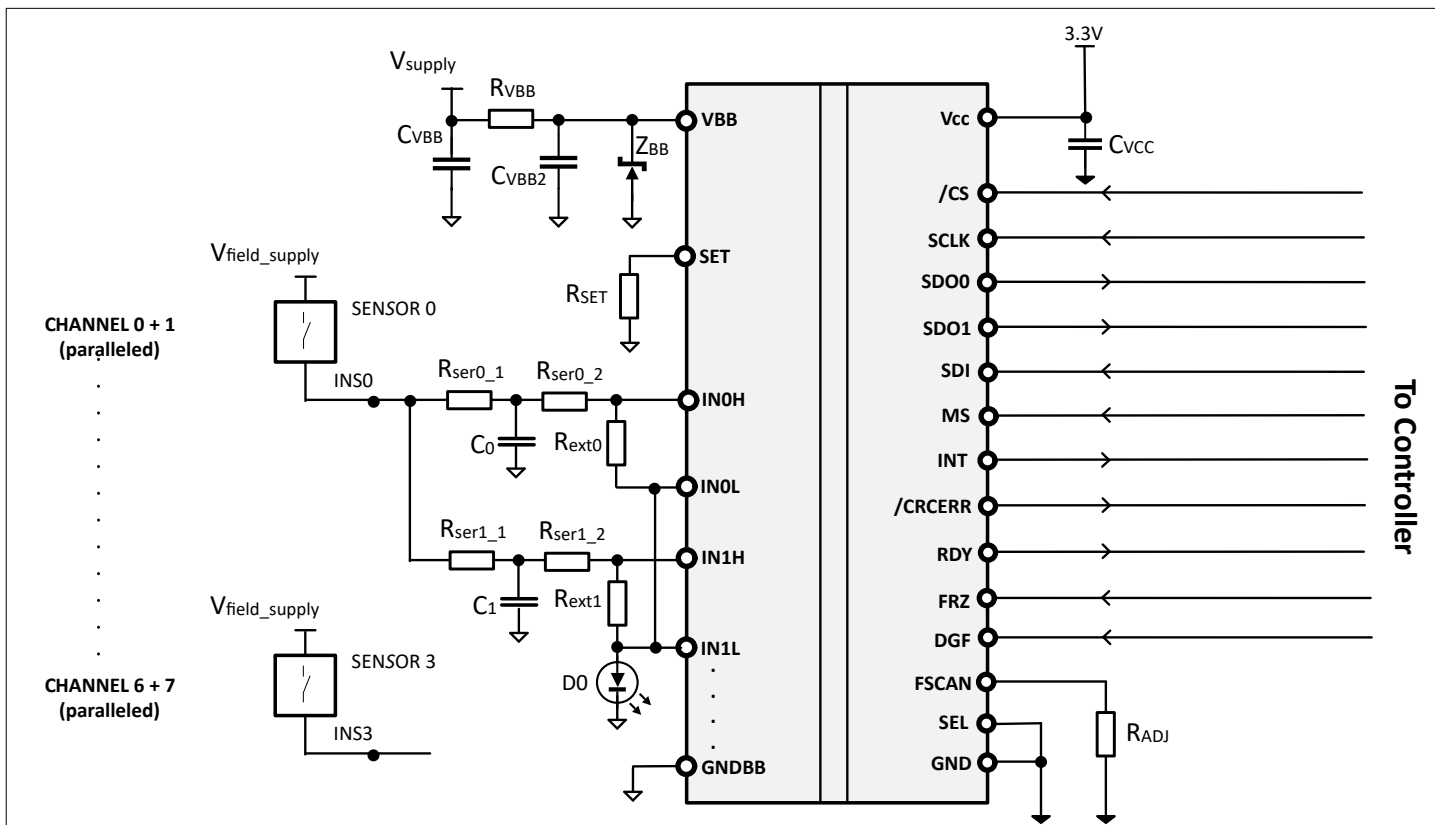


Figure 4 Typical application using SPI interface with four 48 V sensors in sink configuration (2.3 mA per channel) in combination with loss-free status LEDs

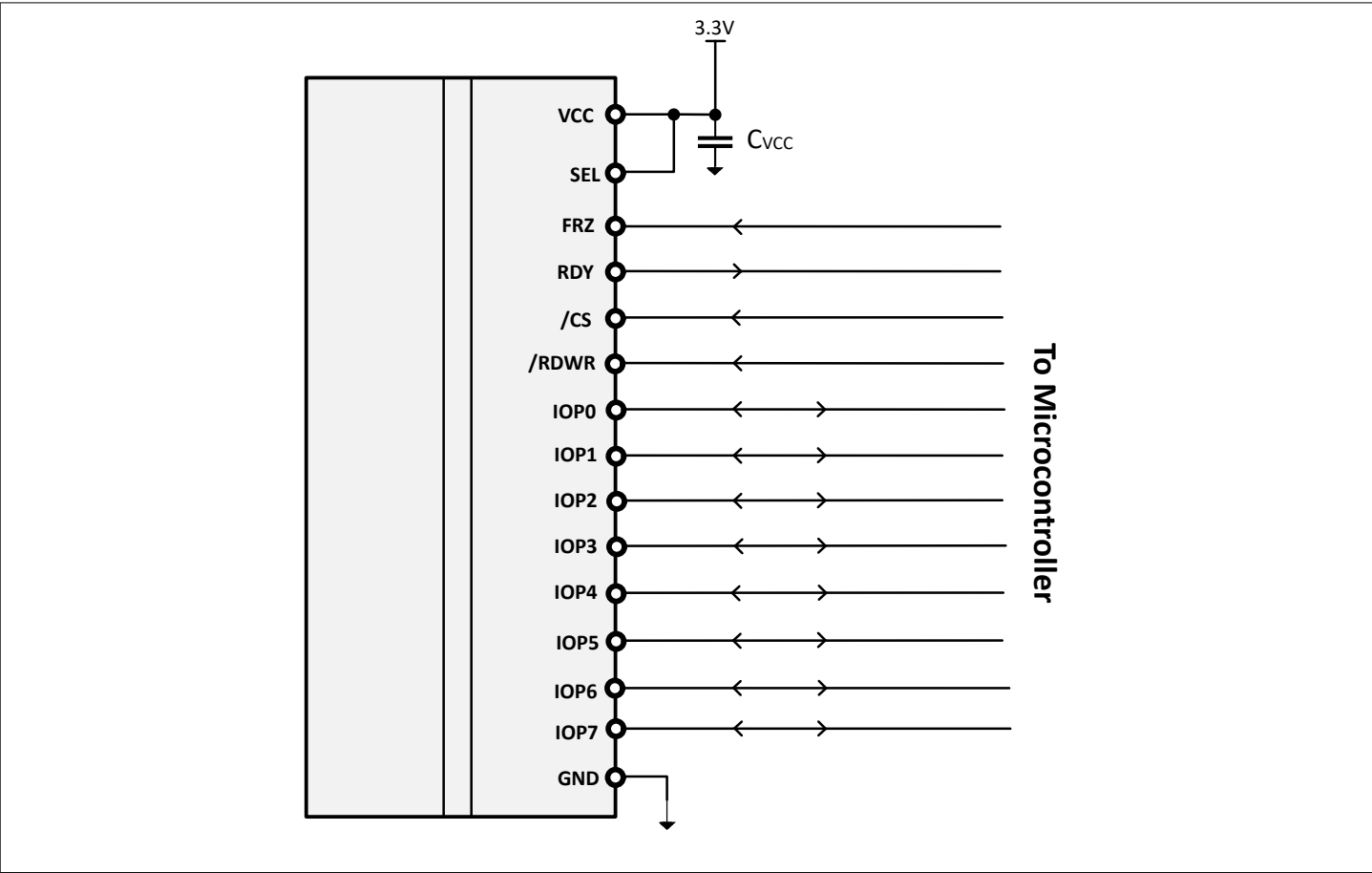


Figure 5 Parallel interface suitable for each of the previous input configurations with 24 V and 48 V sensors

2.1 Pin configuration

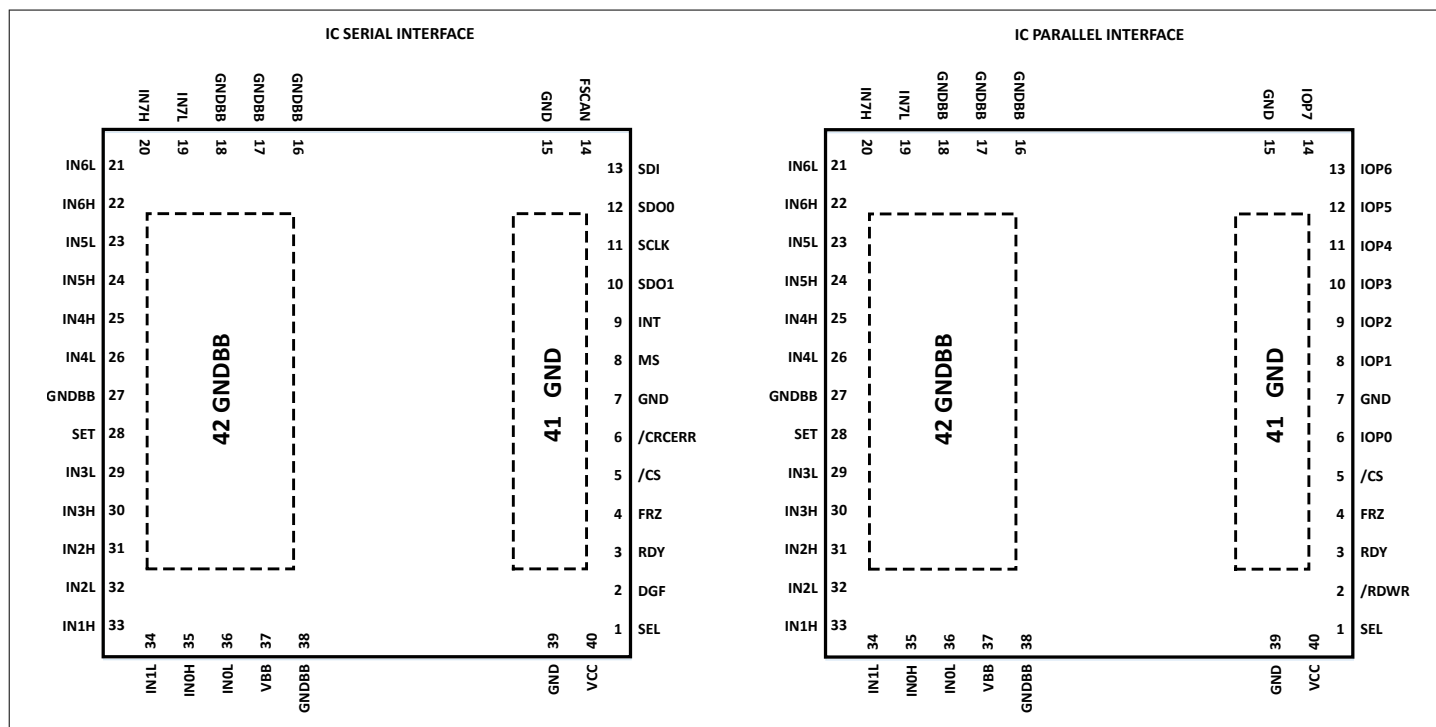


Figure 6 Pins configuration in serial and parallel modes

2.2 Pin functionality

Table 1 **Sensors input side pins**

Symbol	Pin Number	IC I/O	Type	Function	Configuration in the application
IC Power supply pins					
GNDBB	16, 17, 18, 27, 38, 42			Input side ground voltage reference for all signals on input side	Connect all GNDBB pin to the GNDBB thermal pad
VBB	37			supply pin for input side	Connect capacitor with a minimum of 330nF. Not protected against reverse voltage
Input pins					
INxH	20, 22, 24, 25, 30, 31, 33, 35	I	A	connections to sensors	resistor network as shown in Chapter 1
INxL	19, 21, 23, 26, 29, 32, 34, 36	I	A	this pin controls the LED status according to the detected sensor status	LED connections as shown in Chapter 1

(table continues...)

2 Pin configuration and functionality

Table 1 (continued) Sensors input side pins

SET	28	I	A	the value of the resistor connected at this pin sets the threshold for the selected sensor type	Connect a resistor to GNDBB. Resistor values are shown in Chapter 5
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A = analog, I=input pin

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Table 2 Controller interface pins

Symbol	Pin Number	IC I/O	Type	Function	Configuration in the application
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IC Power Supply pins

GND	7, 15, 39, 41			Ground voltage reference for all signals on controller side	Connect all the GND pins to to the GND thermal pad
VCC	40			supply pin for microcontroller side	Connect capacitors for filtering noise and voltage fluctuations, typically between 100 and 470 nF.

General interface pins

SEL	1	I	PD	Interface Selection: low = SPI serial interface, high = parallel interface.	Connect this pin to GND for Serial mode or V _{CC} to parallel mode
RDY	3	O	OD, PU	IC ready: high = no active alarms, low=one or more alarms are present	Connect to a high impedance microcontroller input pin. Leave floating if not used
FRZ	4	I	PU	Freeze: high = continuous scanning mode, low=freeze registers for new incoming input data and new incoming diagnostic data	Connect to a controller output pin. Connect to Vcc if not used
/CS	5	I	PU	Chip Select, when low enables the communication through SPI serial interface	Connect to a controller output pin directly or through a resistor

pins used in SPI serial interface pins

DGF	2	I	PU	deglitching filter: low = channel filter time programmed in register, high = 3.2ms filter applied to all the channels.	Connect to a controller output pin directly or through a resistor
/CRCERR	6	O	OD, PU	CRC error: high = no errors, low = a CRC error is present in CRC in the last received communication	Connect to a high impedance controller input pin. If not used can be left floating
MS	8	I	PD	selection of one of the two different SPI serial modes. The mode can be changed during operation	Connect to a controller output or hardwire the pin to either GND or Vcc depending on desired selection

(table continues...)

2 Pin configuration and functionality

Table 2 (continued) Controller interface pins

INT	9	O	OD, PU	Interrupt on change: low = input change after last SPI access.	Connect to a high impedance microcontroller input pin. Leave it floating if not used
SCLK	11	I	PD	SPI serial interface clock is fed to this pin.	Connect to a controller output pin directly or through a resistor
SDO1	10	O	PPZ	Output of input status and diagnostics information	Connect to high impedance microcontroller input pins
SDO0	12	O	PPZ		
SDI	13	I	PD	IC data input for SPI communication	Connect to controller output pin.
FSCAN	14	I	A	Configuration pin for input scan frequency	connect FSCAN pin with corresponding resistor to GND: • 82kΩ resistor for 20kHz • 33kΩ for 200kHz • 0.5kΩ short to GND for 500kHz

pins used in parallel interface

/RDWR	2	I	PU	Read/Write trigger: control the acquisition of addresses and data in both direction	Connect to a controller output pin
IOPx	6, 8, 9, 10, 11, 12, 13, 14	I/O	PPZ	Input or output the address or data bit of a specific register	Connect to controller GPIO output pins

I: IC input pin, O: IC output pin, A: analog pin, OD: Open-Drain, PU: internal Pull-Up resistor, PD: internal Pull-Down resistor, PPZ: Push-Pull pin with High-Impedance functionality,

3 Specifications

3.1 Electrical parameters

3.1.1 Absolute maximum ratings

Stresses beyond the values listed in the table 4 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Positive values indicates current flowing into the IC pin, negative value current flowing out of the IC pin.

Table 3 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VBB max range	V _{BB_Abs}	-0.3	–	62	V	Referenced to GNDBB
VCC max range	V _{CC_Abs}	-0.3	3.3	3.9	V	Referenced to GND
Junction temperature range	T _{J_Abs}	-40	–	150	°C	
Storage temperature	T _{Storage}	-50		150	°C	
SET pin voltage range	V _{SET_Abs}	-0.3	3.3	3.9	V	Referenced to GNDBB
INxH pin Voltage Range	V _{INxH_Abs}	-62		60.5	V	Referenced to GNDBB
INxH current on reverse Polarization	I _{INxH_rev}	-0.1			mA	V _{INxH} = -60 V referenced to GNDBB
Signal Slope	V _{inSlope}			2	V/μs	
INxL pin voltage range	V _{INxL_Abs}	-0.3		4	V	Referenced to GNDBB
LED Voltage	V _{F_LED}			2.2	V	Value at 25°C and typical currents between 2mA ...3mA
Logic output pin sink current	I _{Log_Out}			5	mA	Applicable to all output pins. Absolute current value. V _{pin} < 0.25·VCC
Logic output pin source current	I _{log_source}			5	mA	Applicable to all output pins. Absolute current value. V _{pin} > 0.75 · VCC
Logic pin max range	V _{log_Abs}	-0.3		0.3 + Vcc	V	
Overtemperature alarm threshold	T _{OT}	105		125	°C	
Overtemperature hysteresis	T _{OT_Hys}		10		°C	

3.1.2 Power supply

Table 4 Operating range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
For correct functionality the IC has to be applied inside the allowed operating range						
VBB operating range 24 V sensors	V _{BB_Op24V}	9.6	24	30	V	SET resistor R _{set} according mode labels M_24V_T3 and M24V_T1 according Table 25 . Referenced to GNDBB
VBB operating range 48 V sensors	V _{BB_Op48}	9.6	48	60	V	SET resistor R _{set} according mode labels M_48V_T3 and M48V_T1 according Table 25 . Referenced to GNDBB
VCC operating range	V _{CC_Op}	2.7	3.3	3.6	V	referenced to GND
Junction Operating Temperature	T _{J_Op}	−40		125	°C	

The parameters in the following tables apply over the full operating range unless noted differently

Table 5 Power supply general parameters

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VBB UVLO Startup threshold	V _{BB_UVLO_ON}			9.6	V	Values Referenced to GNDBB
VBB UVLO Shutdown threshold	V _{BB_UVLO_OFF}	8			V	Values Referenced to GNDBB
VBB UVLO Hysteresis	V _{BB_UVLO_Hys}			1	V	
VBB Quiescent current 20kHz	I _{Q_VBB_30V_20kHz}			4.6	mA	VBB = 30 V, INxH = 0 V, INxL = 0 V referenced to GNDBB, VCC = 3.3 V referenced to GND, R _{adJ} = 82 kΩ,
VBB Quiescent current 200kHz	I _{Q_VBB_30V_200kHz}			5.5	mA	VBB = 30 V, INxH = 0 V, INxL = 0 V referenced to GNDBB, VCC = 3.3 V referenced to GND, R _{adJ} = 33kΩ,
VBB Quiescent current 500kHz	I _{Q_VBB_30V_500kHz}			7	mA	VBB = 30 V, INxH = 0 V, INxL = 0 V referenced to GNDBB, VCC = 3.3 V referenced to GND, RadJ = 0 Ω,
VBB Quiescent current 39 V 200 kHz	I _{Q_VBB_39V}			5.5	mA	VBB = 39 V, INxH = 0 V, INxL = 0 V refernced to GNDBB, VCC=3.3 V referenced to GND, R _{adJ} =33kΩ,

(table continues...)

Table 5 (continued) Power supply general parameters

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VBB Quiescent current 60 V 200 kHz	$I_{Q_VBB_60V}$			5.5	mA	VBB = 60 V, INxH = 0 V, INxL = 0 V referenced to GNDBB, VCC = 3.3 V referenced to GND, R_{adJ} = 33 kΩ
VBB related Startup Delay	t_{start_VBB}		50		μs	Time interval from VBB _{on} to first data output at 500kHz sampling frequency. Digital filter bypassed. Parameter not subject to production test - verified by design
VCC UVLO Startup threshold	$V_{CC_UVLO_ON}$			2.7	V	Measured at VCC pin, value referenced to GND
VCC UVLO Shutdown threshold	$V_{CC_UVLO_OFF}$	2.3			V	Measured at VCC pin, Value Referred to GND
VCC UVLO threshold hysteresis	$V_{CC_UVLO_Hys}$		0.1		V	
VCC quiescent Current 3.3 V	$I_{Q_VCC_3.3V}$	–	2	–	mA	VBB = 0 V referenced to GNDBB, VCC = 3.3 V referenced to GND, 500 kHz scan frequency
VCC related Startup Delay	t_{start_VCC}		100		μs	Time interval from VCC _{on} to first data output at 500kHz sampling frequency. Digital filter bypassed. Parameter not subject to production test - verified by design

Table 6 Voltage alarms

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VBB MV and OV Hysteresis	$V_{BB_MVOV_Hys}$			1	V	Applies to all the different sensor types
VBB MV and OV blanking time	$V_{BB_MVOV_BT}$		6		scan cycle s	Applies to all the different sensor types. Scan cycle = 1 / scan frequency

(table continues...)

Table 6 (continued) Voltage alarms

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltage alarm parameters for 24 V sensors type 1 or type 3 selected via R _{set}						
VBB MV Alarm-On-threshold type 1, 24 V	V _{BB_MV_ON_T1_24}	15			V	SET resistor R _{set} according mode label M24V_T1 according Table 25 . Referenced to GNDBB
VBB MV Alarm-Off-threshold type 1, 24 V	V _{BB_MV_OFF_T1_24}			17	V	SET resistor R _{set} according mode label M24V_T1 according Table 25 . Referenced to GNDBB
VBB MV Alarm-On-threshold type 3, 24 V	V _{BB_MV_ON_T3_24}	12.1			V	SET resistor R _{set} according mode label M24V_T3 according Table 25 . Referenced to GNDBB
VBB MV Alarm-Off-threshold type 3, 24 V	V _{BB_MV_OFF_T3_24}			13.9	V	SET resistor R _{set} according mode label M24V_T3 according Table 25 . Referenced to GNDBB
VBB OV Alarm Turn-On-threshold 24 V sensors	V _{BB_OV_ON_24}			31	V	SET resistor R _{set} according mode labels M24V_T3 or M24V_T1 according Table 25 . Values measured at VBB, referenced to GNDBB
VBB OV Alarm Turn-Off-threshold 24 V sensors	V _{BB_OV_OFF_24}	28.8			V	SET resistor R _{set} according mode labels M24V_T3 or M24V_T1 according Table 25 . Values measured at VBB, referenced to GNDBB
Voltage alarm parameters for 48-V sensors type 1 or type 3 selected via R _{set}						
VBB MV Alarm-On-threshold type1, 48 V	V _{BB_MV_ON_T1_48}	34			V	SET resistor R _{set} according mode label M48V_T1 according Table 25 . Values measured at VBB, referenced to GNDBB
VBB MV Alarm-Off-threshold type1, 48 V	V _{BB_MV_OFF_T1_48}			37	V	SET resistor R _{set} according mode label M48V_T1 according Table 25 . Values measured at VBB, referenced to GNDBB

(table continues...)

Table 6 (continued) Voltage alarms

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VBB MV Alarm-On-threshold type 3, 48 V	$V_{BB_MV_ON_T3_48}$	30			V	SET resistor R_{set} according mode label M48V_T3 according Table 25 . Values measured at VBB, referenced to GNDBB
VBB MV Alarm-Off-threshold type 3, 48 V	$V_{BB_MV_OFF_T3_48}$			33	V	SET resistor R_{set} according mode label M48V_T3 according Table 25 . Values measured at VBB, referenced to GNDBB
VBB OV Alarm Turn-On threshold 48 V sensors	$V_{BB_OV_ON_48}$			60	V	SET resistor R_{set} according mode label M48V_T3 or M48V_T1 according Table 25 . Values measured at VBB, referenced to GNDBB
VBB OV Alarm Turn-Off threshold 48 V sensors	$V_{BB_OV_OFF_48}$	57			V	SET resistor R_{set} according mode label M48V_T3 or M48V_T1 according Table 25 . Values measured at VBB, referenced to GNDBB

3.1.3 Sensor input parameters

3.1.3.1 Sensor detection parameters

The parameters in the following table apply over the full operating range unless noted differently. Sensor current and voltage thresholds for Type 1 and Type 3 refer to EN61131-2

Table 7 Sensor current regulation and status detection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Sensor input parameters with R _{set} selected 24 V sensors Type 1 or Type 3						
L-H threshold type 3, 24 V	V _{TH_H_T3_24}	–	–	5.6	V	SET resistor R _{set} according mode label M24V_T3 in Table 25 . INxL shorted to GNDBB, Values measured at INxH, referenced to GNDBB
H-L threshold type 3, 24 V	V _{TH_L_T3_24}	3.5	–	–	V	SET resistor R _{set} according mode label M24V_T3 in Table 25 . INxL shorted to GNDBB, Values measured at INxH, referenced to GNDBB
L-H threshold type 1, 24 V	V _{TH_H_T1_24}	–	–	9.5	V	SET resistor R _{set} according mode label M24V_T1 in Table 25 . INxL shorted to GNDBB, Values measured at INxH, referenced to GNDBB
H-L threshold type 1, 24 V	V _{TH_L_T1_24}	6.0	–	–	V	SET resistor R _{set} according mode label M24V_T1 in Table 25 . INxL shorted to GNDBB, Values measured at INxH, referenced to GNDBB
Hysteresis voltage threshold, 24 V	V _{TH_HYS_24}	–	0.75	–	V	SET resistor R _{set} according mode label M24V_T3 or M24V_T1 in Table 25 .
INxH regulated current at the minimum input voltage	I _{INxH_5.5V}	1.685		2.33	mA	INxH voltage = 5.5 V, INxL shorted to GNDBB. SET resistor R _{set} according mode label M24V_T3 or M24V_T1 in Table 25 . Referenced to GNDBB
INxH regulated current at the maximum input voltage	I _{INxH_28V}	0.1		0.28	mA	INxH voltage = 28 V, INxL shorted to GNDBB. SET resistor R _{set} according mode label M24V_T3 or M24V_T1 in Table 25 . Referenced to GNDBB

(table continues...)

Table 7 (continued) **Sensor current regulation and status detection**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Sensor input parameters with Rset selected 48-V sensors type 1 or type 3						
L-H threshold type 3, 48 V	V _{TH_H_T3_48}	–	–	22.0	V	SET resistor R _{set} according mode label M48V_T3 in Table 25 . INxL shorted to GNDBB. Values measured at INxH, referenced to GNDBB
H-L threshold type 3, 48 V	V _{TH_L_T3_48}	15.0	–	–	V	SET resistor R _{set} according mode label M48V_T3 in Table 25 . INxL shorted to GNDBB. Values measured at INxH, referenced to GNDBB
L-H threshold type 1, 48 V	V _{TH_H_T1_48}	–	–	22.0	V	SET resistor R _{set} according mode label M48V_T1 in Table 25 . INxL shorted to GNDBB. Values measured at INxH, referenced to GNDBB
H-L threshold type 1, 48 V	V _{TH_L_T1_48}	15.0	–	–	V	SET resistor R _{set} according mode label M48V_T1 in Table 25 . INxL shorted to GNDBB. Values measured at INxH, referenced to GNDBB
Hysteresis voltage threshold 48 V sensors	V _{TH_HYS_48}	–	1.8	–	V	SET resistor R _{set} according mode label M48V_T3 or M48V_T1 in Table 25 .
INxH regulated current min input voltage 48 V sensors	I _{INxH_24V}	0.63	–	0.97	mA	INxH voltage = 24 V, INxL shorted to GNDBB. SET resistor R _{set} according mode label M48V_T3 or M48V_T1 in Table 25 . Referenced to GNDBB
INxH regulated current max input voltage 48 V sensors	I _{INxH_59V}	0.1	–	0.4	mA	INxH voltage = 59 V, INxL shorted to GNDBB. SET resistor R _{set} according mode label M48V_T3 or M48V_T1 in Table 25 . Referenced to GNDBB

3.1.3.2 Wire-break detection

Table 8 Wire-break detection parameters

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Wire break current threshold 24 V sensors	WB _{THpin_24V}		75		μA	SET resistor R _{set} according mode label M24V_T3 or M24V_T1 in Table 25 . Measured at INxH pin.
Wire break current threshold 48 V sensors	WB _{THpin_48V}		25		μA	SET resistor R _{set} according mode label M48V_T3 or M48V_T1 in Table 25 . Measured at INxH pin. As for 48 V configuration two channels are used in parallel the resulting current threshold at the sensor has to be calculated by adding both channels.
WB Blanking Time	t _{WB_Blank}		38		μs	Parameter not subject to production test - verified by design

3.1.4 Controller interface

The parameters in the following table apply over the full operating range unless noted differently.

Table 9 Output side characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Scan frequency range 20 kHz	$f_{sc_rg_20kHz}$	18		22	kHz	82 kΩ 1% Resistor connected to FSCAN pin
Scan frequency range 200 kHz	$f_{sc_rg_200kHz}$	180		220	kHz	33 kΩ 1% Resistor connected to FSCAN pin
Scan frequency range 500 kHz	$f_{sc_rg_500kHz}$	450		550	kHz	FSCAN pin shorted to GND
Logic level High threshold MCU side input	V_{LogInp_High}	$0.7 \cdot V_{CC}$		V_{CC}	V	Value referenced to GND
Logic level Low threshold MCU side input	V_{LogInp_Low}	-0.3	-	$0.3 \cdot V_{CC}$	V	Value referenced to GND
Logic level High threshold MCU side Output	V_{LogOut_High}	$0.8 \cdot V_{CC}$		V_{CC}	V	Value referenced to GND. Pin current 2 mA
Logic level Low threshold MCU side Output	V_{LogOut_Low}	0		$0.2 \cdot V_{CC}$	V	Value referenced to GND. Pin current 2 mA
Internal Pull-up current at Controller-side input pins	I_{PU}			180	μA	Applicable to DGF, RDY, /RDWR, FRZ, /CS, /CRCERR, INT. Conditions $V_{CC} = 3.6V$, output inactive, 0V applied to the pin
Internal Pull-down current at Controller-side input pins	I_{PD}			180	μA	$V_{CC} = 3.6 V$. $V_{pin} = V_{CC}$. Applicable to MS, SCLK, SDI, SEL

3.1.5 Timing parameters

The parameters in the following tables are defined over the full operating range otherwise differently specified.

Table 10 Signal input timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Channel Jitter	t_{ch_jitt}			1	scan cycle	Timing variation on input/output delay. Scan cycle = 1 / scan frequency

(table continues...)

Table 10 (continued) Signal input timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Propagation Delay	t_{prop_delay}	2		3	scan cycle s	Time from new data present at input to point in time where new data is accessible in register. The time for read access to uC (e.g. via SPI) has to be added. Digital filter bypassed. Scan cycle = 1 / scan frequency. Parameter not subject to production test - verified by design.
DGF setting filter value SINK	t_{DGF}		1600		scan cycle s	DGF pin connected to VCC. Applied to all the 8 channels (value corresponds to 3.2 ms filter time @ 500 kHz scan frequency)
Register programmable filter times	t_{COEFIL}	0		20	ms	values for 500kHz scan frequency. This time is incremental to the propagation delay. See COEFIL register description for details
Digital filter register settings 00 on channel x SINK	t_{FILx00}		25		scan cycle s	COEFIL register setting = _0h (value corresponds to 50 us filter time @ 500 kHz scan frequency)
Digital filter register settings 01 on channel x SINK	t_{FILx01}		50		scan cycle s	COEFIL register setting = _1h (value corresponds to 100 us filter time @ 500 kHz scan frequency)
Digital filter register settings 02 on channel x SINK	t_{FILx02}		200		scan cycle s	COEFIL register setting = _2h (value corresponds to 400 us filter time @ 500 kHz scan frequency)
Digital filter register settings 03 on channel x SINK	t_{FILx03}		400		scan cycle	COEFIL register setting = _3h (value corresponds to 800 us filter time @ 500 kHz scan frequency)
Digital filter register settings 04 on channel x SINK	t_{FILx04}		800		scan cycle s	COEFIL register setting = _4h (value corresponds to 1.6 ms filter time @ 500 kHz scan frequency)

(table continues...)

Table 10 (continued) Signal input timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Digital filter register settings 05 on channel x SINK	t_{FILx05}		1600		scan cycle s	COEFIL register setting = _5h (value corresponds to 3.2 ms filter time @ 500 kHz scan frequency)
Digital filter register settings 06 on channel x SINK	t_{FILx06}		5000		scan cycle s	COEFIL register setting = _6h (value corresponds to 10 ms filter time @ 500 kHz scan frequency)
Digital filter register settings 07 on channel x SINK	t_{FILx07}		10000		scan cycle s	COEFIL register setting = _7h (value corresponds to 20 ms filter time @ 500 kHz scan frequency)
Digital filter register settings 08 on channel x SINK	t_{FILx08}		4		scan cycle s	COEFIL register setting = _8h to _Fh digital filter bypassed

Table 11 MCU communication timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		

Serial communication timing parameters

/CS disable time	t_{CSD}	100			ns	/CS high time between two read or write accesses to different registers
/CS Hold time	t_{CSH}	40			ns	last falling edge of SCLK of frame to rising edge of /CS
SCLK pin serial clock frequency	f_{SCLK}			20	MHz	
Serial Clock Period (1/ f_{SCLK})	t_{SCLK}	50			ns	Equivalent to 1/ f_{SCLK}
SCLK Setup time	t_{SCLK_su}	80			ns	/CS falling edge to SCLK rising edge
SCLK valid time	t_{SCLK_valid}			30	ns	SCLK falling edge to data available at outputs SDO0 and SDO1
Output Valid time	t_{CS_valid}			50	ns	/CS falling edge to available data at outputs SDO0 SDO1
Input data Hold time	t_{HD}	15			ns	SCLK rising edge to deactivation data at SDI
Output float time	t_{float}			65	ns	/CS rising edge to output disabled

(table continues...)

Table 11 (continued) MCU communication timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Parallel communication timing parameters						
/CS disable time parallel	t _{CSD}	100			ns	/CS in high state between two IC accesses
/RDWR setup time	t _{RDWRsu}	20			ns	Time between the /CS falling front and the /RDWR falling front
/RDWR low time	t _{RDWRlow}	100			ns	/ RDWR to stay low during data exchange
/RDWR high time	t _{RDWRhigh}	100			ns	/RDWR High time between address and data communication
/RDWR hold time	t _{RDWRHD}	10			ns	/RDWR rising edge to /CS rising edge
IOPx setup time	t _{su}	20			ns	
IOPx hold time	t _{hold}	20			ns	
register latency time parallel	t _{lat}	600			ns	/RDWR rising edge to the register written and ready
tvalid1 - parallel direct mode	t _{valid1_direct}			100	ns	output ports update time, to be filtered by the external MCU
Tdirect for direct mode	t _{direct}	4			μs	/CS /RDWR low time to enter parallel direct mode

3.1.6 ESD

The parameters in the following table apply over the full operating range unless noted differently.

Table 12 ESD

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ESD HBM	$V_{\text{ESD_HBM}}$	2			kV	According to JEDEC JESD22-A114-B
ESD CDM	$V_{\text{ESD_CDM}}$	0.5			kV	According to JEDEC JSD22 C101

3.1.7 Insulation

Table 13 Insulation parameters

Parameter	Symbol	Value	Unit	Note or condition
External clearance	CLR	>3.5	mm	Shortest distance in air from any input pin to any output pin according to IEC60664-1 ¹⁾
External creepage	CRP	>3.5	mm	Shortest distance over package surface from any input pin to any output pin according IEC60664-1
Distance through insulation	DTI	>16.1	μm	
Comparative tracking index	CTI	>400	V	According to IEC 60112
Material group		II		According to IEC 60112
Common mode transient immunity	CMTI	>150	V/ns	
Magnetic field immunity	MFI	>200	A/m	According to EN61000-4-8, EN61000-4-9
Input-to-output insulation according to UL1577 Ed. 5				
Input-to-output insulation voltage	V _{ISO}	2500	V _{rms}	V _{TEST} = V _{ISO} for t = 60 s (qualification); V _{TEST} = 1.2 × V _{ISO} for t = 1 s (100% productive tests)

1) Creepage and clearance requirements depend on the application and related end-equipment insulation standards. Ensure that the printed circuit board meets the required creepage and clearance values.

3.2 Thermal characteristics

Table 14 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance junction to case top	R _{thJC_top}			35	K/W	Top Side of Package fixed to T _{AMB} . Calculated at 85°C
Thermal resistance junction to case bottom	R _{thJC_BOT}			8	K/W	Bottom Side of Package fixed to T _{AMB} . Calculated at 85°C
Thermal resistance junction to ambient	R _{thJA}			38	K/W	Metallization according to JEDEC 2s2p (JESD 51-5, JED51-7), Inner Layers split. Calculated at 85°C

4 IC functionality description

4.1 IC supply voltages

The IC needs two separate voltage supplies at VCC pin and VBB pin. The two supply voltages have separate ground references: GND for VCC voltage and GNDBB for VBB voltage with the supported operating voltage range according to Table 4. The pins are not protected against reverse voltage. Provide an external protection diode if needed. Depending on the EMC pulse capability requested, the supply pin VBB may need external protection components. For details see Chapter 5.1.

The voltage at VBB is monitored as part of the system diagnostics. When the voltage drops to a level that potentially cannot ensure correct sensor status detection or indicates a functional problem in inside the application corresponding alarms are triggered by the IC as described in Chapter 4.3.2.

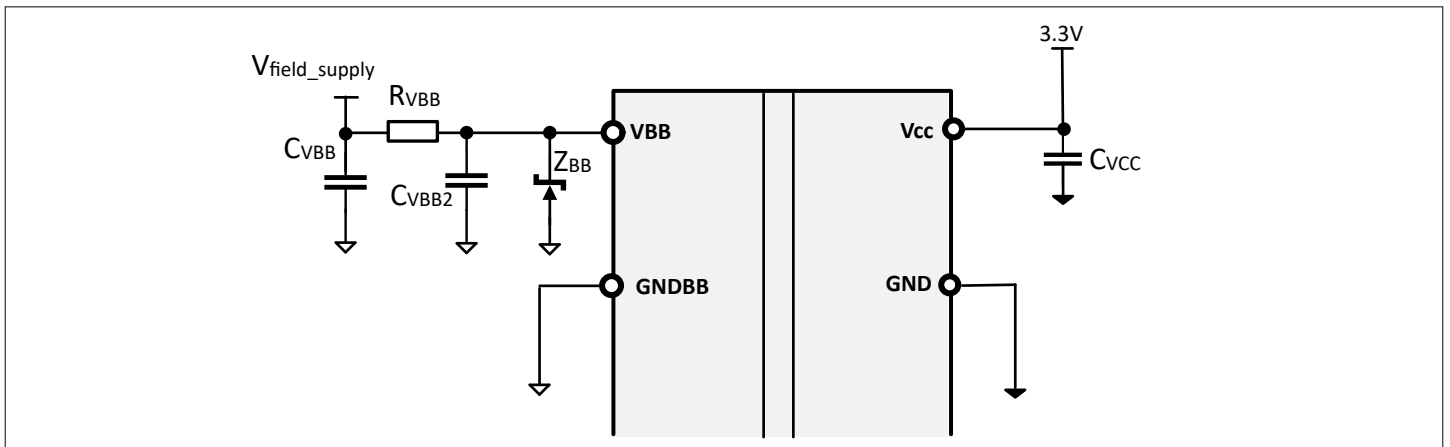


Figure 7 Power supply network

4.2 Sensor input

Figure 8 shows the external circuit configuration for channel 0. Equivalent circuits are connected to all other channels (1 to 7) as well. The sensor is connected to the IC pin IN0H through the resistor R_{ser0} . The resistor R_{ext0} connects IN0H to the corresponding IN0L pin. If an analogue filter capacitor C_0 is intended to be used for channel 0 the serial resistor R_{ser0} has to be split symmetrically to R_{ser0_1} and R_{ser0_2} and the capacitor C_0 placed in-between the two. In order to ensure the full immunity of the input channel against surge pulses the analog filter capacitor C_0 must not be placed directly at INx0 but between R_{ser0_1} and R_{ser0_2} like illustrated in Figure 8.

The INxH pins of all eight channels can sustain continuous voltages of up to 60 V and continuous negative voltages down to -60 V without damage.

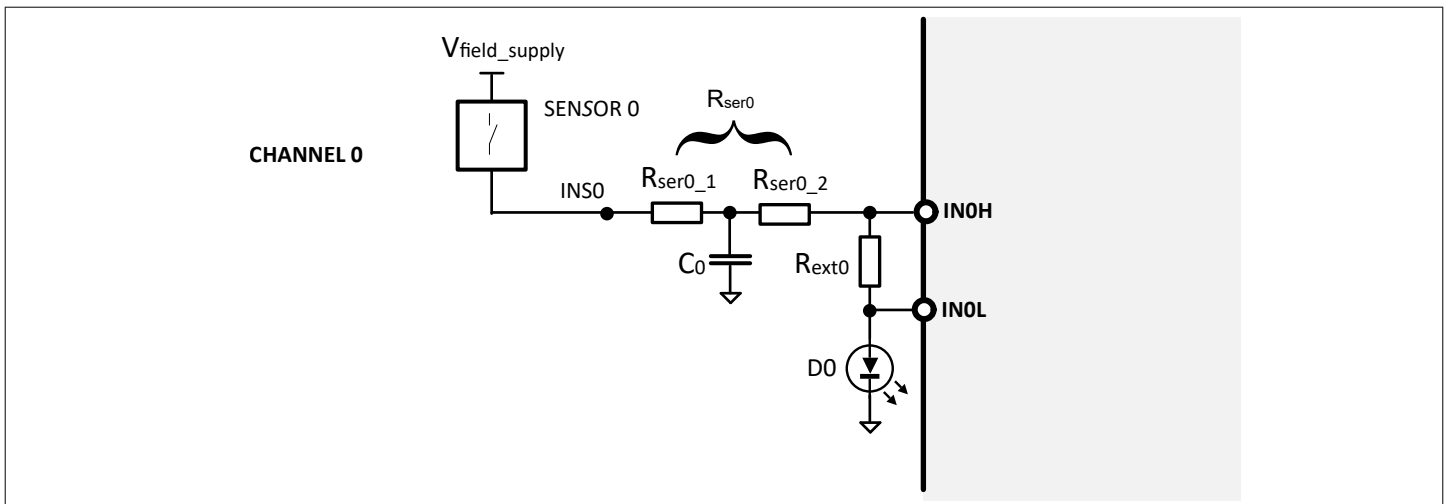


Figure 8 24 V sensor input schematics exemplary for channel 0

The ISO2I828V can also support 48 V sensors (Type 1 or Type 3). For 48 V sensors, the power dissipation inside the IC for each connected sensor is typically twice as high as for 24 V sensors because of the doubled sensor voltage. For this reason - when configured for 48 V applications - the sink current per channel reduced to half of the 24 V value. In order to achieve the channel characteristics acc. EN61131-2 for 48 V configuration two channels have to be paralleled for one sensor. In this case the total amount of sensors per IC is limited to 4 as shown in the [Figure 3](#)

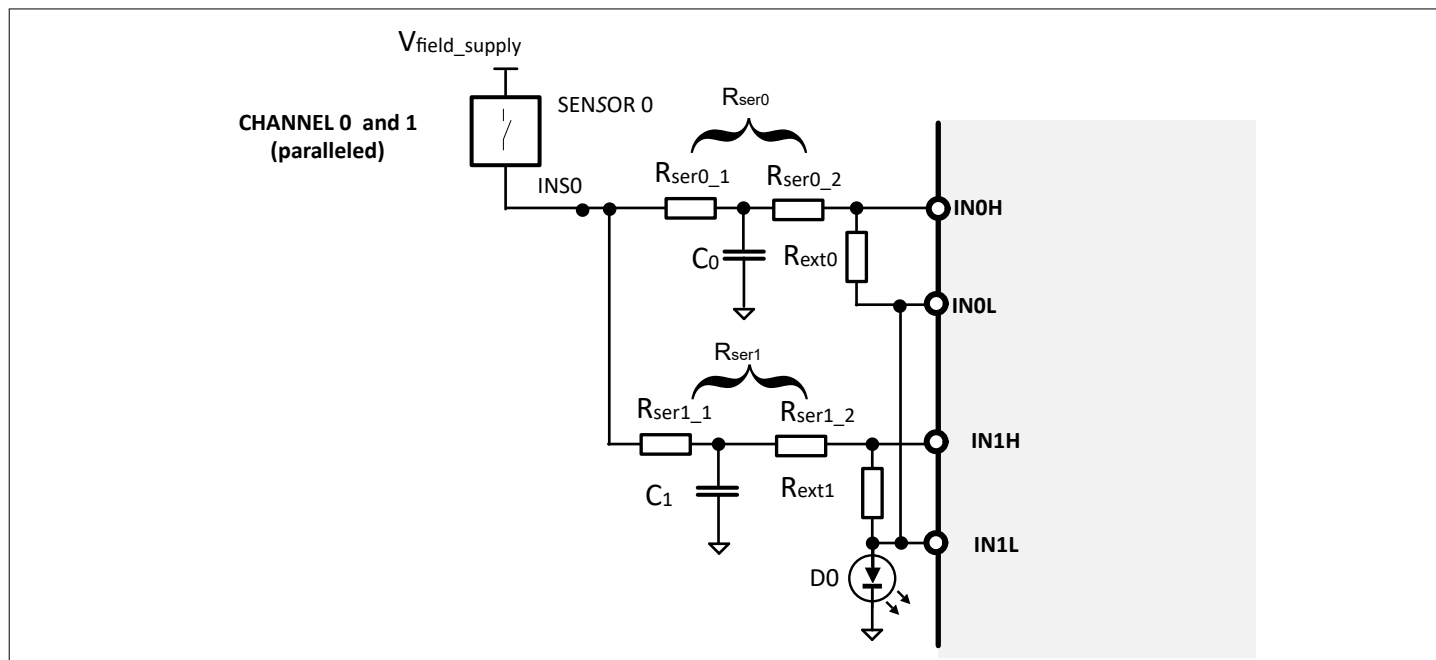


Figure 9 48 V sensor input schematics using two paralleled channels (exemplary shown for ch0 and ch1)

The input channel circuit has the following functionalities implemented:

- detecting the sensor's on-off status (described in [Chapter 4.2.1](#))
- regulating the sensor current to limit the system power consumption (described in [Chapter 4.2.2](#))
- system diagnostics detecting sensor wire breaks (described in [Chapter 4.3.3](#))

4.2.1 Sensor status detection

The voltage at pin IN0H is measured with reference to GNDBB and compared with the thresholds defined in standard EN61131-2 as shown in [Figure 10](#) to evaluate the sensor status (on = logic "high" or off = logic "low").

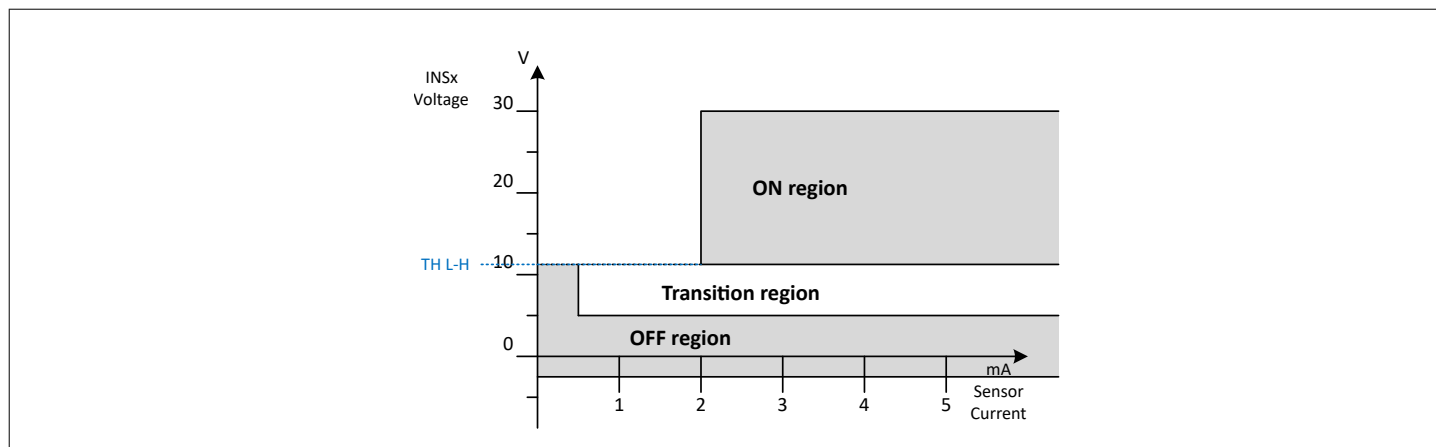


Figure 10 On region, Off region and transition region EN61131-2

The status of 48 V sensors is detected in the same way as for 24 V sensors by comparing the voltage inputs at the pins $INxH$ and $IN(x+1)H$, with the threshold for the configured sensor, Type 1 or Type 3, as described in the standard EN61131-2.

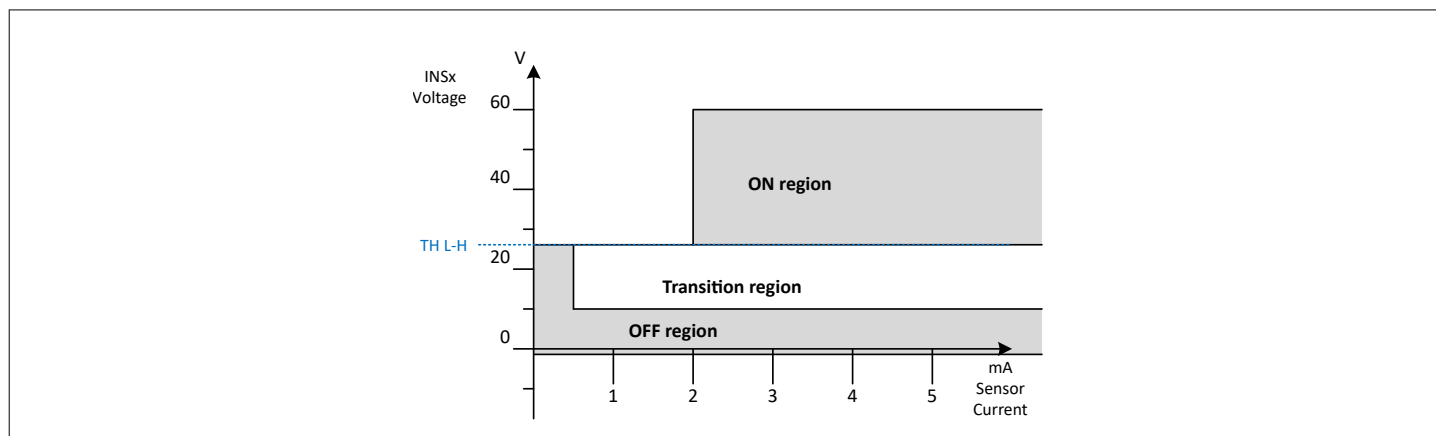


Figure 11 ON region, OFF region and transition region EN61131-2

According to IEC61131-2, the necessary conditions for detecting the sensor "on" status are: $V_{INSx} > L-H$ threshold and Sensor current > 2.1 mA.

The necessary conditions for the sensor to be detected "off" status are sensor current < 1.5 mA or $V_{INSx} < H-L$ threshold. In the transition region between L-H and H-L thresholds, the IC applies a hysteresis to the status detection to avoid output instabilities. The detection of the input status of all channels is continuously performed based on the configured scan frequency. The acquired input status information is communicated across the isolation, subsequently filtered digitally and stored in the register INPDATA. The controller interface allows a continuous readout of the register content.

To set the IC parameters for the selected sensors, connect R_{set} resistor between SET pin and GNDBB with the values described in [Chapter 5.2](#).

The sensor selection is detected when the IC starts up and cannot be changed while IC is active.

4.2.2 Sensor current regulation

The sensor current is regulated by the IC in order to limit the system power consumption within the sensor specification limits defined in EN61131-2. The IC measures the voltage drop across R_{ext} by measuring the voltage difference between $INxH$ and $INxL$. Based on this value the IC sinks via $INxH$ the appropriate amount of current to keep the sensor current above the limit requested by the standard (> 2.1 mA). At higher input voltages, when more current is sunk by the R_{ext} resistor, the IC gradually reduces its internal channel current to keep the total sensor current flat at the intended target value. [Figure 12](#) shows the sensor current profile composed of the current flowing in the R_{ext} resistor proportional to the input voltage and the current in the IC with its variable internal impedance being a function of the input voltage.

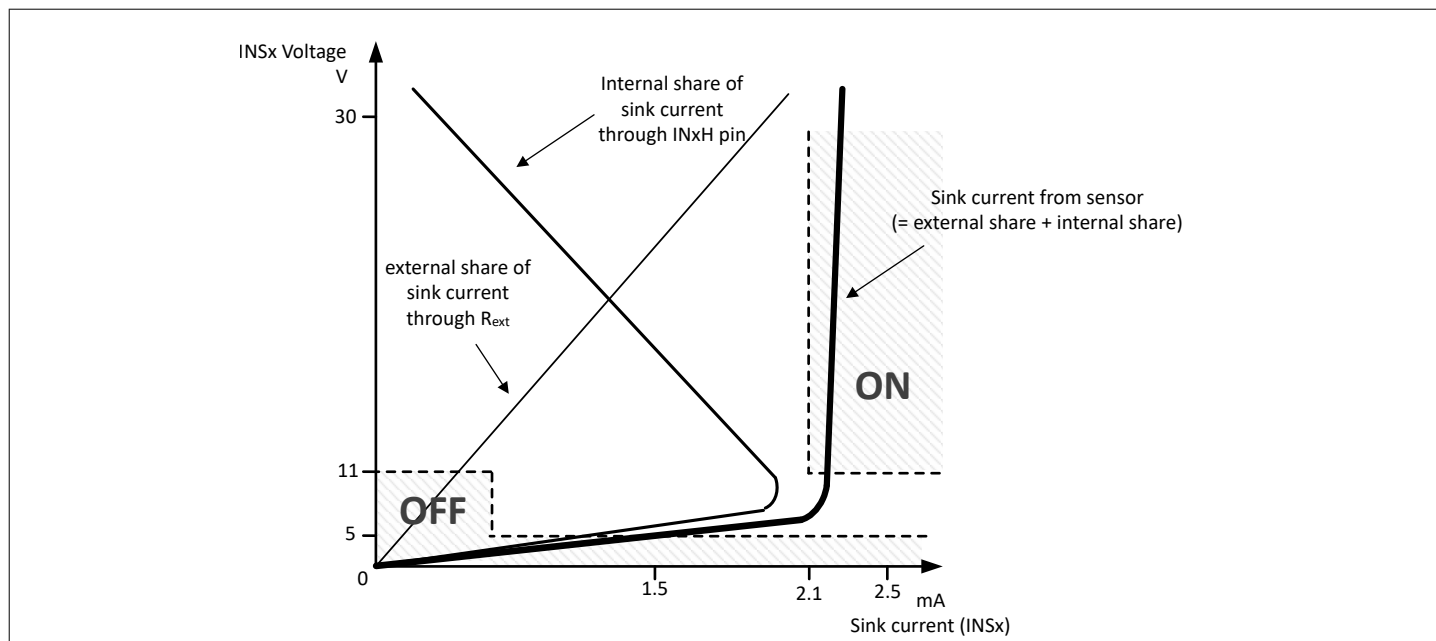


Figure 12 External share (through R_{ext}) and internal share (through IC) of sink current vs sensor voltage (exemplary drawing for 24 V Type 3 sensors)

For 48 V sensors the target sensor current according to EN61131-2 is the same as for 24 V sensors (typ. 2.3 mA). Each parallelized channel contributes with half of the sensor current (typ. 1.15 mA).

For the individual channel, the principle of current sharing between the external resistor network (R_{ext}) and the internal current through INxH is the same as for 24 V applications. Figure 13 illustrates the dependencies of the currents through R_{ext} and the INxH pins of the IC as a function of the applied sensor voltage.

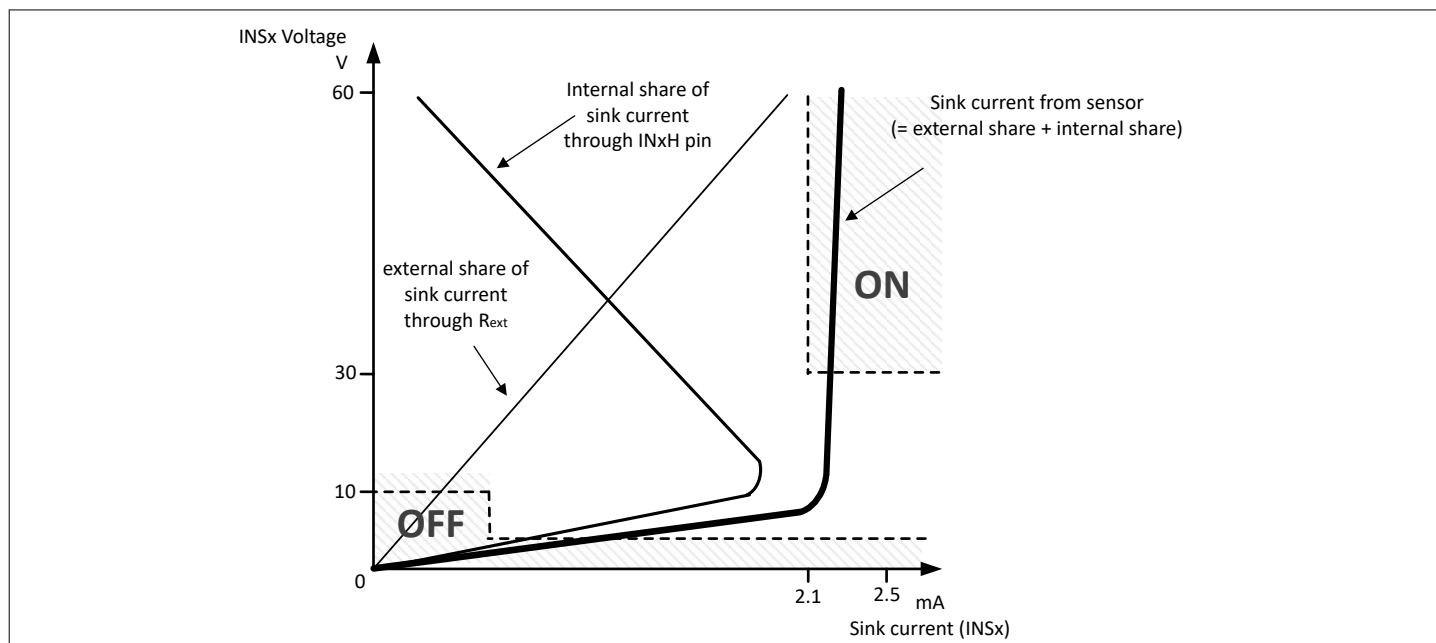


Figure 13 External share (through R_{ext}) and internal share (through IC) of sink current vs sensor voltage (exemplary drawing for 48 V Type 1 sensors)

4.2.3 Sensor status LEDs

For each of the eight channels, a status LED can be connected between INxL and GNDBB as described in the typical application schematics in chapter [Chapter 1](#). The sensor current flows in the channel LED when the sensor is detected as being on. The IC short-circuits the corresponding INxL pin to GNDBB to turn the LED off when sensor is detected as being off. A capacitor between INxL and GNDBB improves the noise immunity of the IC. If the status LED is not required, the pin INxL has to be shorted to GNDBB.

When channels are parallelized, one LED is used for pair of channels (see figure [Figure 9](#) for an example). The sink current coming from one sensor that was divided between the two channels is joined back again to flow in the LED when the sensor is detected as being on.

4.2.4 IC digital filtering of input data

A digital filter is available to eliminate the effect of disturbances and noise on the input signal. The digital filter cuts every signal, positive or negative, shorter than a defined time. The programmed filter time applies both – to data and to diagnostics. The digital filter can be chosen between 50 μ s and 20 ms in steps as indicated in [Chapter 4.4.3.3](#) when being programmed via SPI. In this case the COEFIL register for each channel can be programmed individually with the desired filter time. Alternatively, there is a common filter time of 3.2ms available that can be set with the control pin DGF. The common filter of 3.2 ms via DGF pin is applied to all channels if the DGF pin is held at high level – no matter what is programmed in the COEFIL registers. If the DGL pin is set to low level, the programmed filter values of the COEFIL registers are applied to the channels. The digital filter can be disabled by setting DGF to GND and writing the filter value 0 μ s to the COEFIL register. Note: When the DGF pin is high, the COEFILx registers can be still accessed and written but they do not configure the filters. The programmed filter times set in the COEFILx registers are activated only once the DGF pin is set to low. The following figure shows how the digital filter changes its output according to the averaging length that is selected with the filter value. The change of the detected sensor input is delayed by the averaging length. Sensor spikes that are shorter than the averaging length are suppressed.

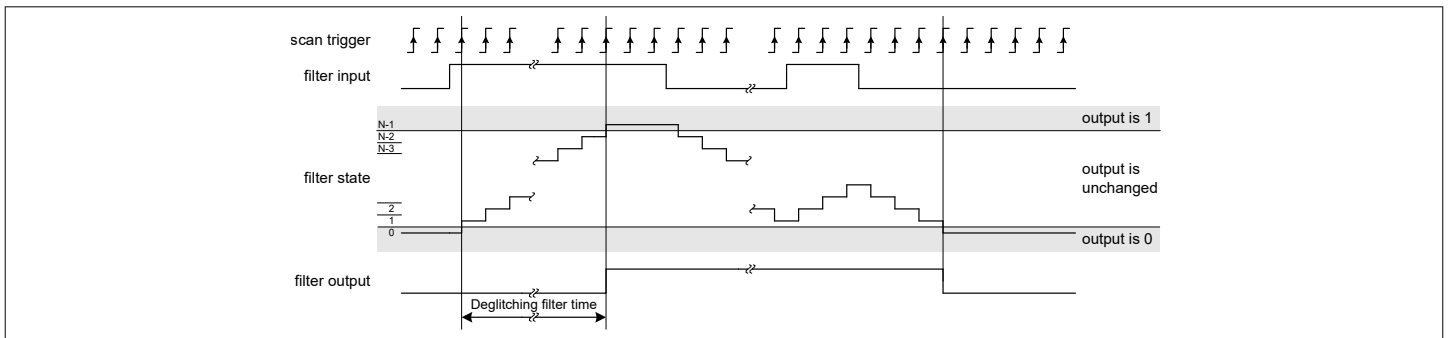


Figure 14 Deglitching filter functionality

4.2.5 Register update freeze for input synchronization

The freeze functionality (FRZ pin set to logic low state) allows to synchronize data data acquisitions from input channels of different ICs on a module or as well from different modules inside a system. As long as the FRZ pin is in logic high state, the IC operates in a continuous scanning mode. This means that the data registers are updated with actual data for each scan cycle. When the FRZ pin is set to low state and freeze mode is entered, the data and diagnostic registers are updated for the last time (data and diagnostic information) with the falling edge of the FRZ pin. For the time where the FRZ pin is kept low the registers are not updated anymore with new incoming data of following scan cycles. But even though during freeze mode no new input data or new information about new upcoming diagnostic events are written to the corresponding registers the existing diagnostic bits in the diagnostic registers can still be reset also during freeze mode. This is the case if the diagnostic events have vanished and if the diagnostic information has been read by the controller after they have vanished. With other words, the sticky bits of diagnostic events can be reset according to the same rules as outside of freeze mode but no new occurring diagnostic events during freeze mode will be written to the registers. During freeze mode write operations to the COEFIL-registers to change the filter values are still possible. The new filters values will only be applied after exiting freeze mode.

4.2.6 Interrupt on change output

To reduce the microcontroller communication effort over the SPI serial interface, the IC has an interrupt-on-change output. The IC pulls the INT output pin low, when one or more of the eight input changes status. The pin remains low until the next SPI access, then it is reset to high until the next change in the inputs. The INT functionality together with the RDY functionality avoids the need to continuously access the SPI interface for new data. Status changes on the RDY pin indicate a diagnostic event, while changes on INT indicate an data change on the input pins. The INT pin does not indicate input changes when the device is in FRZ mode.

4.3 Diagnostic features

4.3.1 RDY pin output

The IC includes several diagnostic functions to monitor and signal abnormal IC status. Any single or multiple of the following diagnostic events are signaled by pulling the RDY pin to low status if the IC is operated in serial or parallel mode:

- V_{BB} OV: overvoltage at VBB has been detected. The IC is still functional and communicates the input status of the channels. The occurrence of any overvoltage event is stored by setting the OV bit of the GLERR register.
- V_{BB} MV: "missing voltage" at VBB. The IC is still working but the VBB supply voltage potentially can be too low to detect the sensor status correctly under all circumstances. The occurrence of any "missing voltage" event is stored by setting the MV bit of the GLERR register.
- V_{BB} UVLO: VBB undervoltage lock-out of the sensor side. Insufficient VBB voltage to maintain a stable operation of the IC leading to an undervoltage shutdown. The occurrence of any UVLO event is stored by setting the W4S bit of the INTERR register.
- TE: transmission error over galvanic isolation. This occurrence is stored by setting the TE bit of the INTERR register.

After detecting the generic RDY pin alarm, the controller can read the details of the diagnostic event accessing the registers GLERR and INTERR.

Even when the fault conditions are no longer present, the status of the RDY pin remain in alarm status and the corresponding diagnostic bits in the registers remain set to indicate the event. They are reset only once the relevant registers are read by the external controller after the fault has gone.

If the IC is operated in direct parallel mode, in addition to the above listed diagnostic bits also a wire-break occurrence of one or multiple channels is signaled as well by pulling RDY to low state. The occurrence of the "or-ed" wire-break event is stored by setting the channel fault bit CF of the GLERR register. Also take note that in parallel direct mode the alarm on the RDY-pin is in general not "sticky" and the RDY-flag is immediately reset when the diagnostic events are no more present.

The following table lists the diagnostics cases and how to reset the indicators:

Table 15 **Fault status description**

Description	RDY	Register bit change	Alarm reset by reading	IC behavior
Status Normal, no fault	High	GLERR = 00h INTERR = 00h	–	IC is functional, normal operation
W4S: V_{BB} UVLO	Low	INTERR bit 2 set (W4S)	INTERR	sensor side of IC is disabled because of missing VBB supply voltage; no input data evaluation possible

(table continues...)

Table 15 (continued) **Fault status description**

Description	RDY	Register bit change	Alarm reset by reading	IC behavior
OV: V_{BB} overvoltage alarm	Low	GLERR bit 2 set (OV)	GLERR	IC remains functional, but unexpected high supply voltage is detected
MV: V_{BB} "missing voltage" alarm	Low	GLERR bit 1 set (MV)	GLERR	IC remains functional, but input data integrity cannot be ensured
WB: wire-break detected	High (except for direct parallel mode: Low)	DIAG register bits of affected channels (DIAGx) and GLERR bit 0 (CF) are set	DIAG	IC continues normal operation for non-affected channels. Affected channels cannot provide correct sensor data (always low)
OT: IC overtemperature alarm	High	INTERR bit 0 set (OT)	INTERR	IC remains functional, but unexpected IC temperature is detected and data integrity cannot be ensured
TE: IC transmission error	Low	INTERR bit 1 set (TE)	INTERR	IC sensor side communication is disturbed and data integrity cannot be ensured
V_{CC} UVLO	Low	not registered	–	no communication

IMPORTANT: The overtemperature alarm is not a protection of the IC or any system parts by itself – it only signals an abnormal condition inside the IC and allows the system to react.

4.3.2 Power supply monitoring

The IC monitors the voltage supply level at V_{BB} pin to verify the reliability of the acquired sensor signal status. Alarm voltage thresholds are described in [Table 6](#):

UVLO Undervoltage lock-out: When V_{BB} supply voltage drops below UVLO threshold:

- Sensor side IC turns off - $I_{N \times H}$ and $I_{N \times L}$ current drop to zero (note that the the sensor current is still different from zero due to R_{ext} resistors)
- Microcontroller Side IC remains active and can communicate
- RDY pin is pulled to low
- INTERR register's W4S and TE bits are set to high

After voltage returns to its normal working range the IC is back to normal operation. RDY and INTERR bit are reset only when the register is accessed with a read command

MV "missing voltage" alarm: When supply voltage V_{BB} drops below the "missing voltage" level:

- The IC continues to operate, but – especially in case of further dropping V_{BB} – the correct detection of the sensor status cannot be ensured.
- RDY pin is pulled to low
- GLERR register's MV bit is set to high

After the voltage returns to its normal working range, the RDY and GLERR bit are reset only after the register is accessed and content read

OV Overvoltage alarm: When V_{BB} supply voltage exceeds overvoltage threshold:

- The IC continues to operate but it indicates that the field supply voltage is outside the nominal range and potentially may have unwanted effects on the application itself.
- RDY pin is pulled to low
- GLERR register's OV bit is set to high

After the voltage returns to its normal working range, the RDY flag and the OV bit are reset only after the GLERR register has been read (Read access to GLERR register)

IC General startup procedure: At start-up and every time V_{BB} voltage is below UVLO, the GLERR register bits OV and MV and INTERR register bits W4S and TE have value 1 with diagnostic alarm active. Therefore the RDY pin is low at startup, signaling an error condition. RDY and the states of register status are sticky and can be reset to normal by reading GLERR nad INTERR registers. .

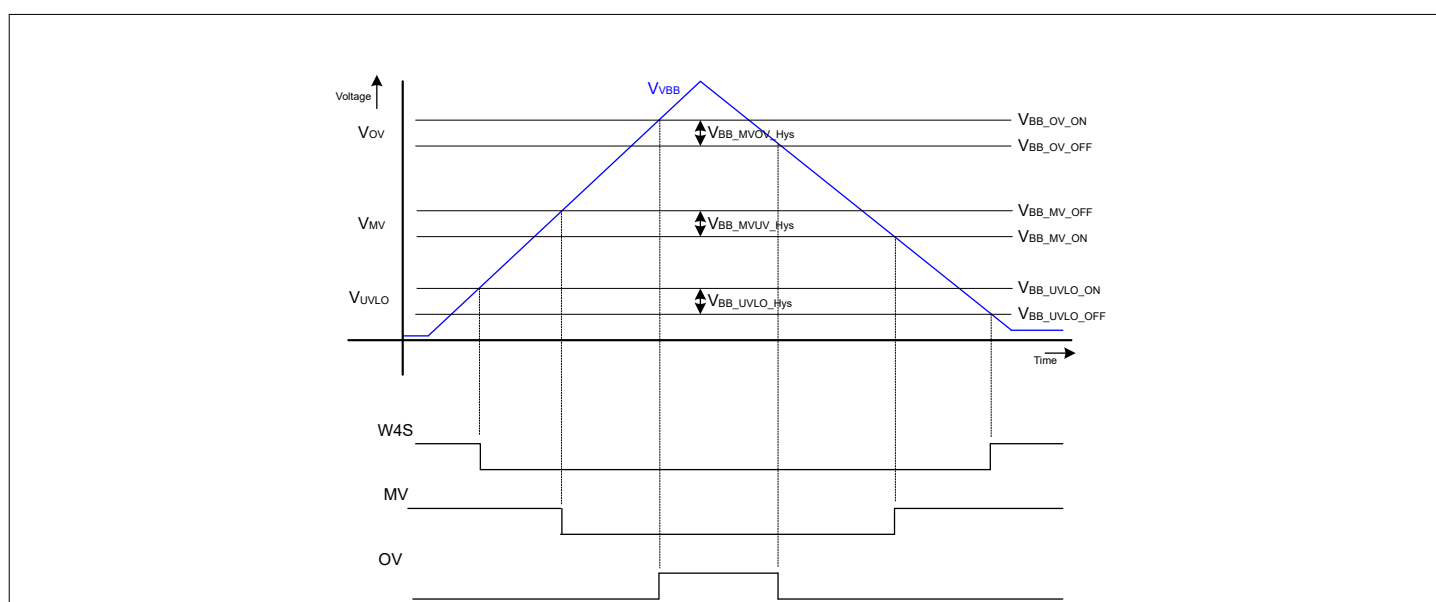


Figure 15 Voltage supply diagnostics sequence when applying a voltage ramp at VBB pin

4.3.3 Sensor input wire-break detection

The IC can verify the integrity of IC to sensor connection and detect any wire breaks, measuring the leakage current when the sensor is off. A wire break is indicated when the sensor current is below the wire break threshold.

The 8 channels wire-break diagnostic status is detected with the same input scan frequency rate, sent across isolation, and stored in the corresponding of the 8 bit of DIAG register. The GLERR register CF bit is set to 1 if one of the DIAG register bit is set to 1.

DIAG bits are not reset to 0 when the channel connection is recovered, but only when DIAG register is read trough the controller interface and no WB is present on the channel. CF bit on GLERR register is reset only when DIAG bits are all reset to zero after a DIAG register read.

When a sensor has no leakage current, it is possible in some cases to add a high ohmic resistor in parallel that allows wire break detection. If sensor leakage current is too low and no parallel resistor can be added, wire-break cannot be detected.

If necessary, the channel wire-break detection can be disabled by setting the bit 4 (MWB) in the channel's COEFIL register to zero.

RDY pin changes status in case of WB event only when parallel direct interface is selected, in SPI serial mode and parallel mode RDY doesn't signal the WB event.

4.3.4 Overtemperature alarm

The IC monitors the junction temperature. The IC activates the overtemperature alarm when IC temperature exceeds the overtemperature threshold T_{OT} .

When overtemperature alarm is on:

- The IC continues to operate, but for further rising temperature outside the temperature operating range the data integrity cannot be ensured.
- INTERR register's OT bit is set to value 1

After the temperature returns to the working operating range, the OT bit of the INTERR register remains set until the INTERR register has been read (Read access to INTERR register). The overtemperature alarm is not mapped to the RDY signal. In order to receive overtemperature warnings the system has to read the INTERR register.

IMPORTANT: The overtemperature alarm by itself is not a protection of any system part. It only signals to the system that there is an abnormal temperature condition inside the IC.

4.4 Controller interface

The IC can be accessed through an SPI serial interface or parallel interface. The IC's input pin SEL selects between these two options. Several pins on the output side change their functions based on this pin selection.

The available options are described in the table below:

Table 16 SEL communication interface options

Communication type	SEL pin condition
SPI serial communication	shorted to GND
Parallel communication	shorted to VCC

This selection cannot be changed while IC is active.

4.4.1 SPI Serial interface

SPI serial interface is available for reading the registers containing information about sensor input status and diagnostics. Some registers can also be written to setup the application.

IC pins used in SPI interface:

- /CS: to open the communication with the IC when this IC input pin is pulled to low
- SCLK: SPI clock for in and out data synchronization, provided by the controller
- SDI: port for IC data input
- SDO0: port for IC data output
- SDO1: additional port for IC data output for simultaneous diagnostics data communication

The following figure shows the connections and signal directions:

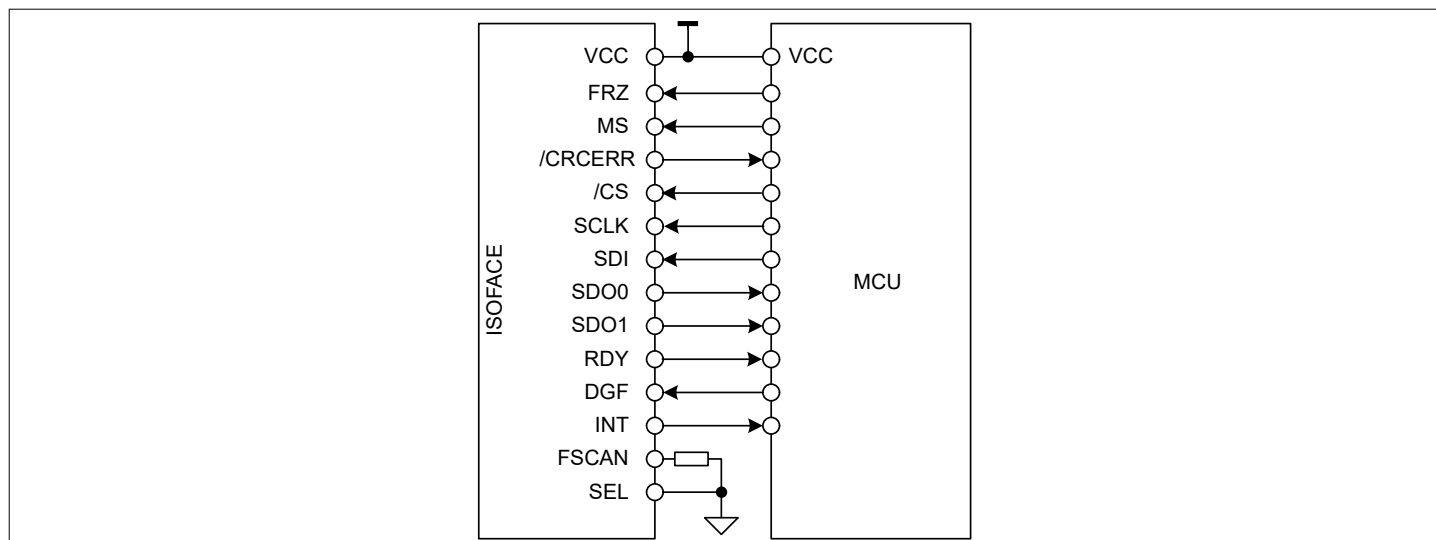


Figure 16 SPI Serial communication interface

Two different SPI modes are available allowing to select 16bit or 24 bit communication.

The SPI serial mode is set through the MS pin as in the following table and can be changed while the IC is active:

Table 17 SPI Serial modes detail

Mode	MS pin Status	Commands available	Bits	Ports used	CRC check	Daisy chain
0	Low	Register Read and Write	16	SDI, SDO0, SDO1	no	yes
1	High	Register Read and Write	24	SDI, SDO0, SDO1	yes	yes

SPI serial mode 0 (16-bit): read command

When /CS pin is low the IC interface is activated and ready for data exchange. The content of the registers are frozen at /CS falling edge and remain frozen as long as /CS is low. Data received is stored and analyzed only at the /CS rising edge at the end of the communication frame.

If, at the /CS rising edge, the clock number count is not a multiple of 8, a module 8 error is triggered and /CRCERR pin changes status.

In Mode 0, clock pulses over the 16th are shifted out at SDO0 for daisy chain communication. When daisy-chaining is active data has to be transmitted in multiple of 16 bit or it is discarded.

The data pattern is described in [Figure 17](#), first byte received from the IC is the register address to READ or WRITE. A register address is 7 bit long, so the MSB is used to indicate a READ (MSB = 0) or WRITE (MSB = 1) command. Second Byte received by the IC at SDI is not relevant in READ command and consists of eight zeros.

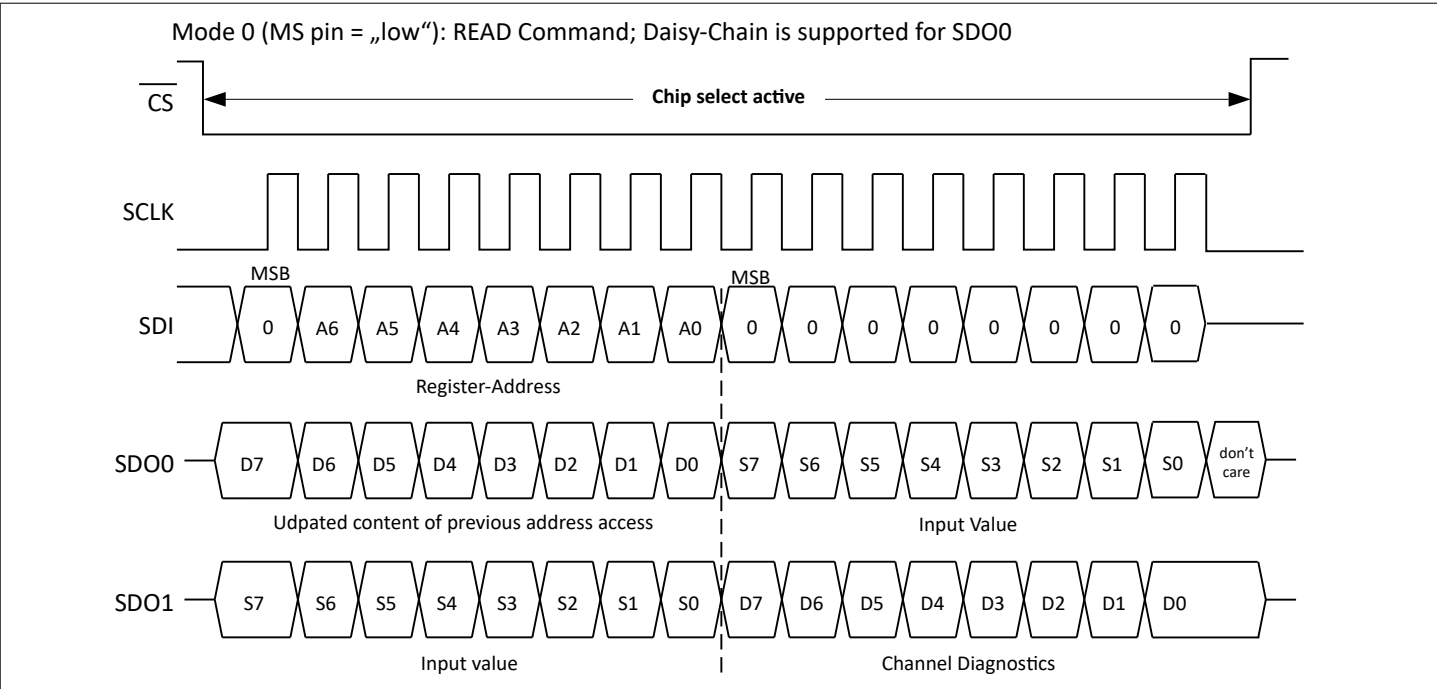


Figure 17 SPI mode 0: Read pattern

While the IC is receiving the bit stream from the controller, it sends information at the serial outputs SDO0 SDO1 as shown above in the figure. When at least one register read access has been requested, the first byte contains the data of the last register addressed. The second byte output over SDO0 is always sensor input status. For SDO1, the first byte output is always the sensor input status, the second byte is always the sensor wire break diagnostics. Once the communication frame is completed, the IC is ready to answer with the updated content of the requested register at the next communication frame. SDO1 sends at the same time the usual content of sensor input status and sensor diagnostics for the wire break.

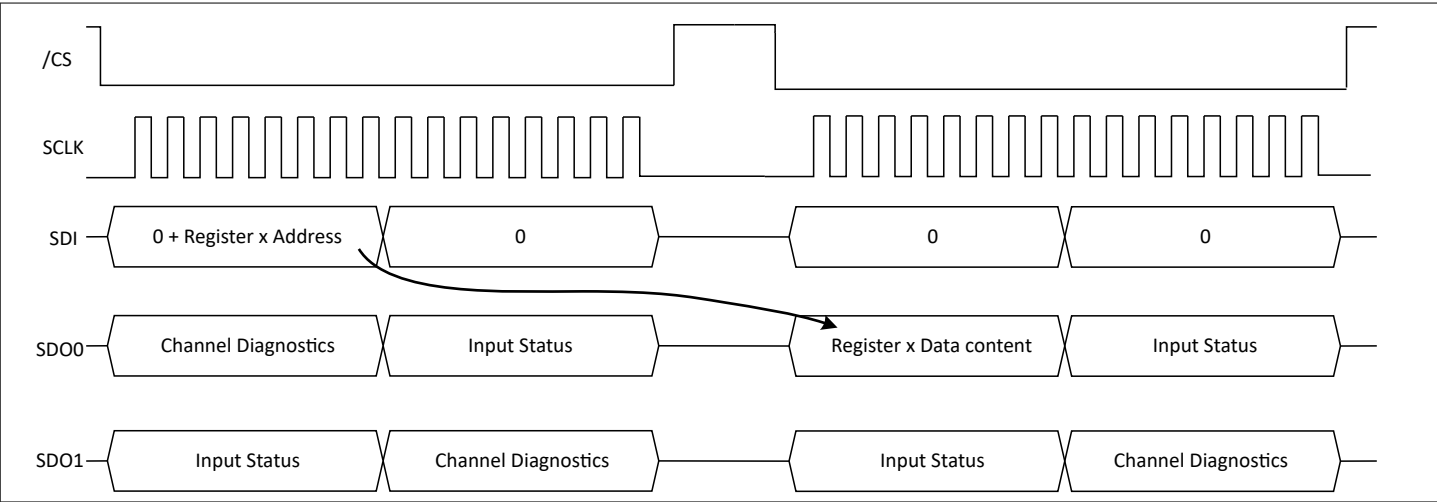


Figure 18 SPI Serial mode full read procedure

SPI Mode 0 Fast - read command:

When faster transmission is required, the frames can be stopped after eight clock pulses and the read procedure can be executed in half of the time. The following picture shows a Mode 0 fast read. Daisy chain is not available in SPI Mode 0 fast. And write commands are not allowed with SPI Mode 0 fast.

SPI Mode 0 Fast - read command:

When faster transmission is required, the frames can be stopped after eight clock pulses and the read procedure can be executed in half of the time. The following picture shows a Mode 0 fast read. Daisy chain is not available in SPI Mode 0 fast. And write commands are not allowed with SPI Mode 0 fast.

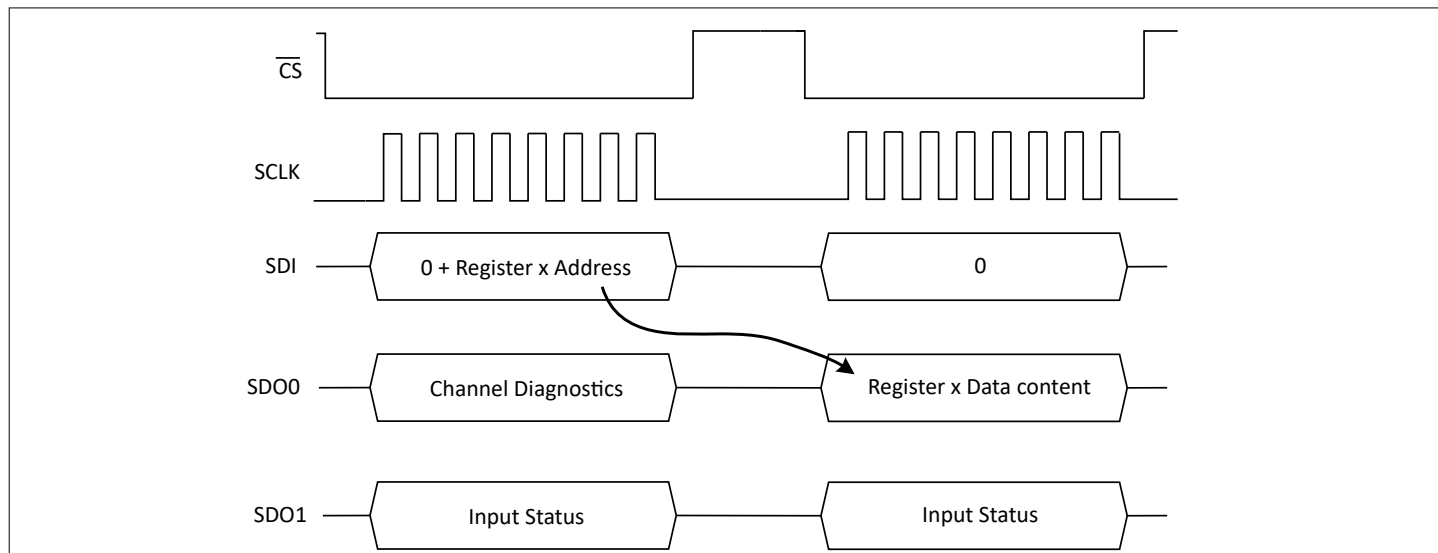


Figure 19 Mode 0 fast read command procedure

SPI Serial mode 0 (16bit): WRITE Command

To write to a register, it is necessary to send the address preceded by 1 as MSB value, followed by the byte content to be written to the register.

While receiving the write command frame the IC answers with same data content as described in read command for SDO0 and SDO1.

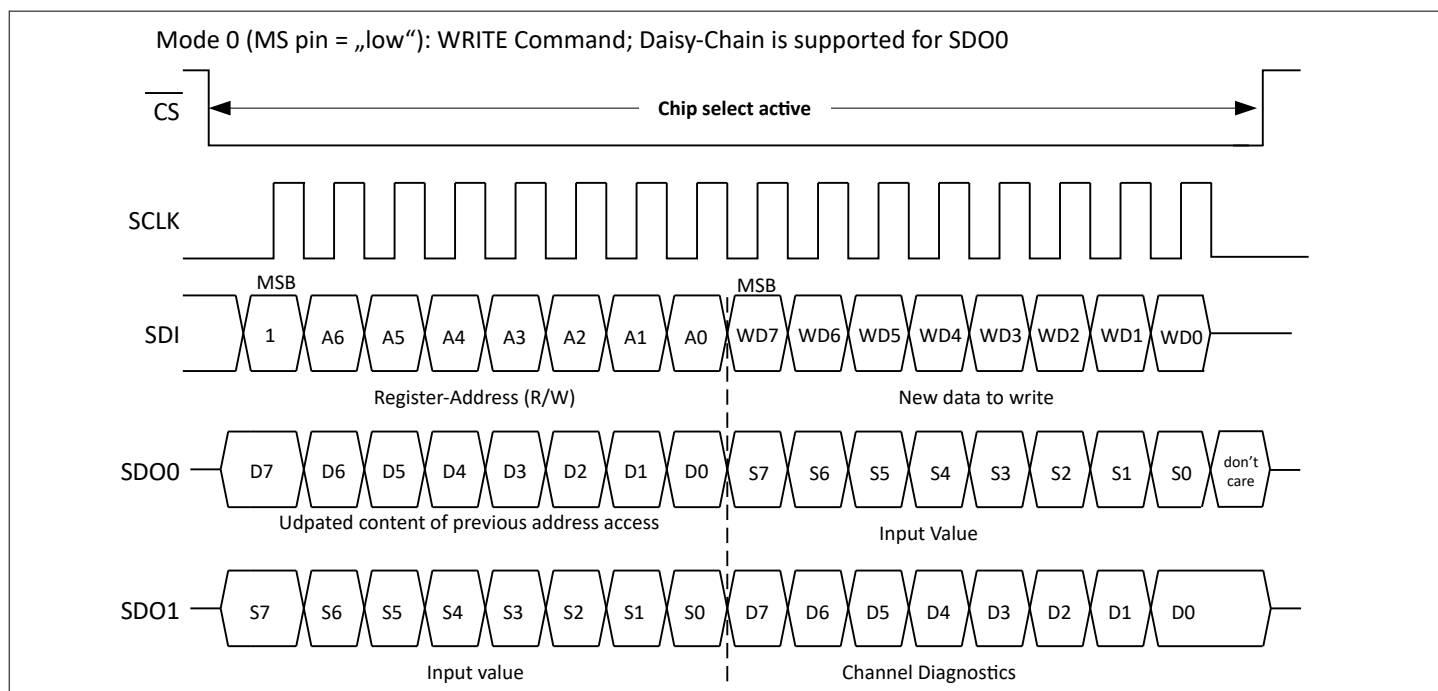


Figure 20 SPI mode 0: Write pattern

SPI serial Mode 1 (24bit):

Mode 1 is similar to Mode 0 but uses an additional byte for the 5bit CRC. The remaining three bits of the third byte are populated with the diagnostic information contained in GLERR and INTERR register.

SPI serial Mode 1 (24-bit): read command As shown in [Figure 21](#) Mode1 works like MODE 0 for first and second bytes. The read command is set by the MSB of the first byte received over the SDI pin with a value of 0 being followed by the 7 bits address of the register to be read. Third bit contains the CRC in the five LSB.

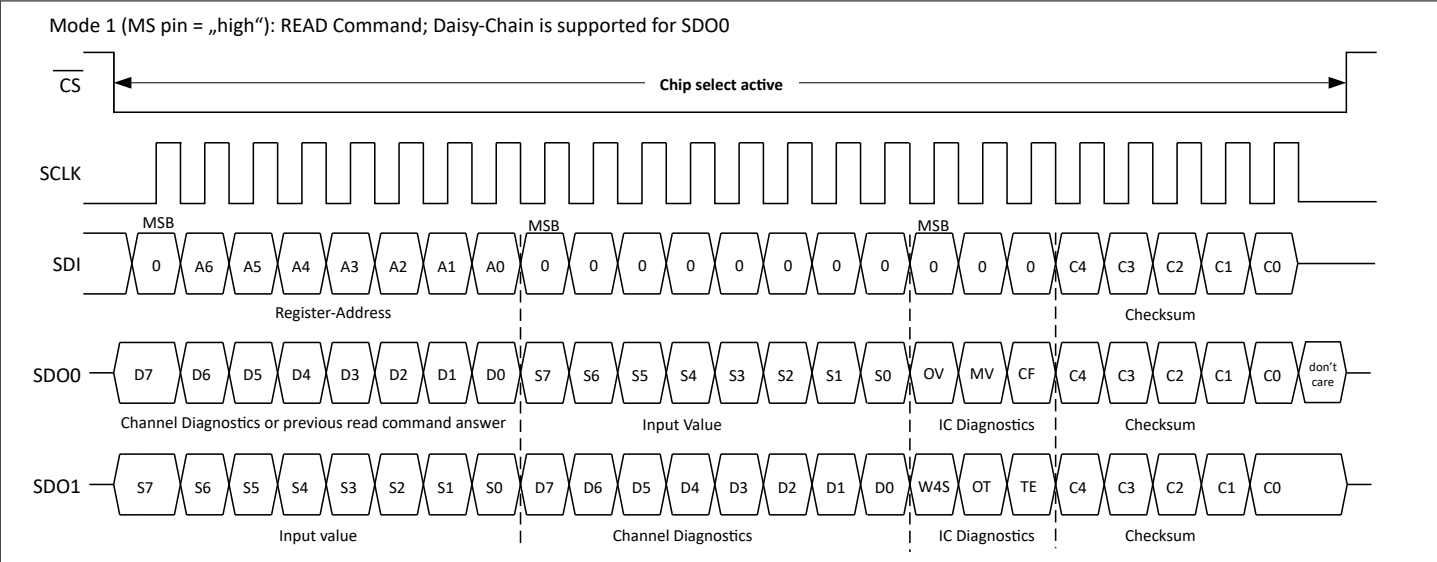


Figure 21 SPI mode 1 : Read pattern

SPI Serial Mode (24bit): WRITE Command

Register write commands follow the same principles as in MODE 0 with the addition of the CRC information in the third byte of data as shown in [Figure 22](#).

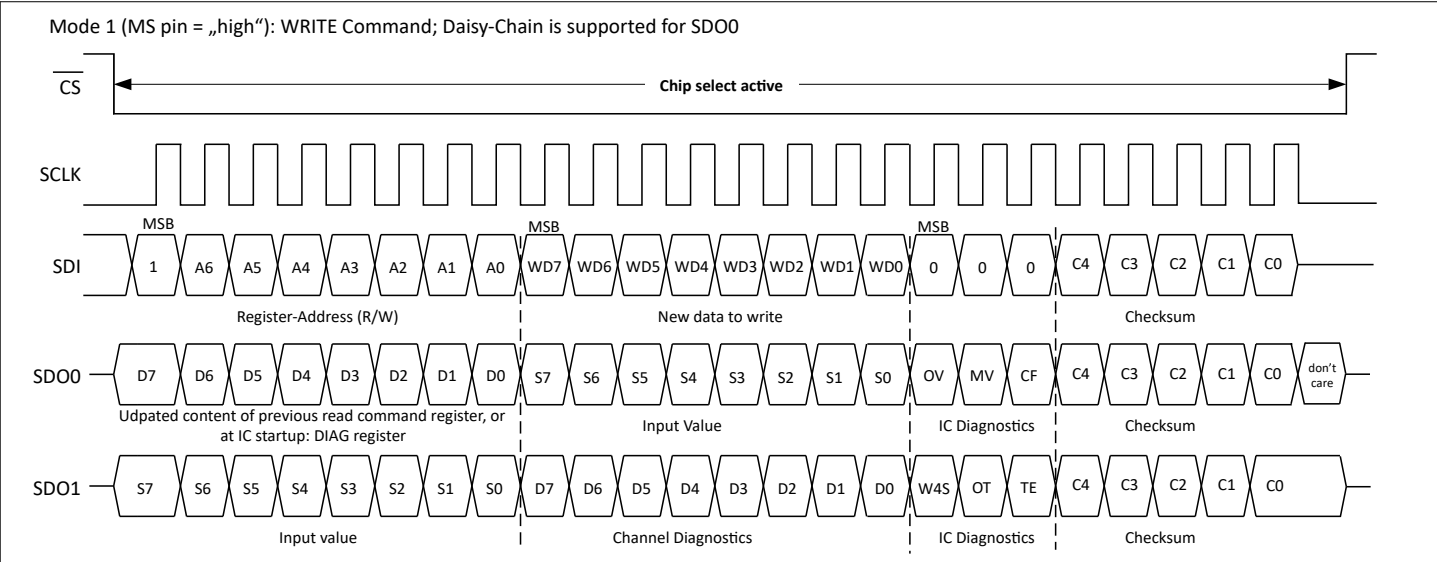


Figure 22 SPI mode 1: Write pattern

4.4.1.1 SPI serial communication timing

The clock signal supplied at this IC input synchronizes the acquisition of the data at SDI IC input pin and of data provided at the SDO0 and SDO1 outputs. Input data are sampled with the SCLK signal's rising edges while output data has to be sampled from the controller at the SCLK signal's falling edge. Following figure shows the timing and parameters of the signals involved in the SPI serial communication.

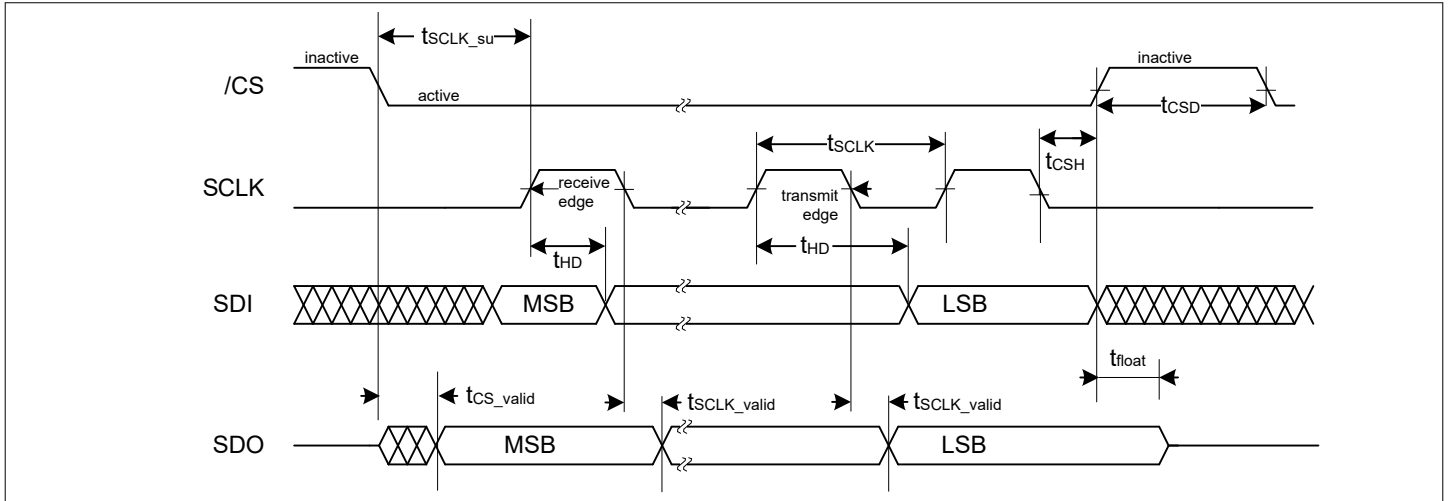


Figure 23 SPI protocol timing

The timing parameters in the figure above are (for details see table [Table 11](#)):

- t_{CS_valid} : time from /CS falling edge to data becoming available at SDO0 and SDO1 outputs
- t_{SCLK_su} : time from /CS falling edge to SCLK rising edge
- t_{HD} : time from SCLK rising edge to deactivation data at SDI
- t_{SCLK} SPI clock period
- t_{SCLK_valid} : time from SCLK falling edge to data available at SDO0 and SDO1 outputs
- t_{CSH} : time from last SCLK last rising edge to /CS signal rising edge
- t_{float} : time after the rise of /CS when the SDO0 and SDO1 data are reset
- t_{CSD} : /CS high time between two R/W accesses on different registers

4.4.1.2 CRC check

CRC check verifies the correctness of the SPI serial communication between controller and IC. The IC indicates the reception of an invalid CRC by setting the /CRCERR Pin to low. The /CRCERR pin is reset to high by the next communication with a valid CRC check.

CRC Calculation: In SPI serial communication, the CRC is a 5-bit-checksum calculated using the polynom $X^5 + X^2 + 1$ (binary: 100101b) from the entire three-byte content [23:0]. The CRC calculation starts by applying an XOR operation using the binary string 11111b to the five most significative bits. The following bits are then shifted-in and XOR with the CRC Polynom is performed until the end of the string. The calculated checksum is then substituted to bit [4:0].

To verify the CRC-check correctness the same procedure is applied to the 24-bit string received. The CRC calculation result has to be 00000b. If the result is different from binary 00000b the delivered CRC-signature is not consistent with the bit stream.

For communication from the IC to the controller, a 5 bit CRC-signature has to be calculated and delivered with the pure data bitstream (19 bits). The bitstream read from the IC has to be processed according to the CRC algorithm by the microcontroller to verify the integrity of the transmission.

In the following pictures an example of calculation and verification of the CRC checksum.

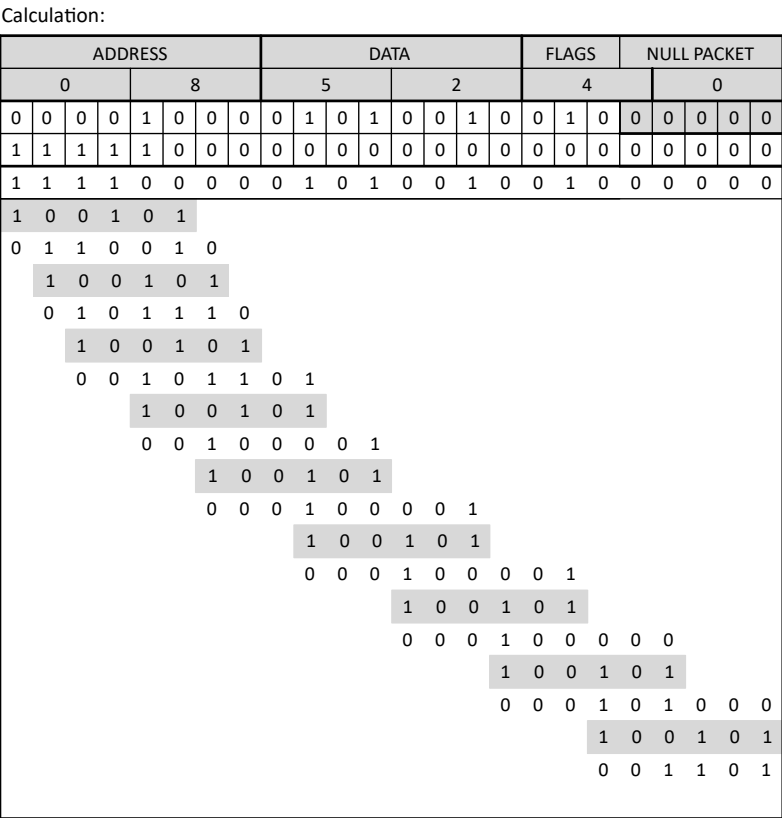


Figure 24 CRC Calculation

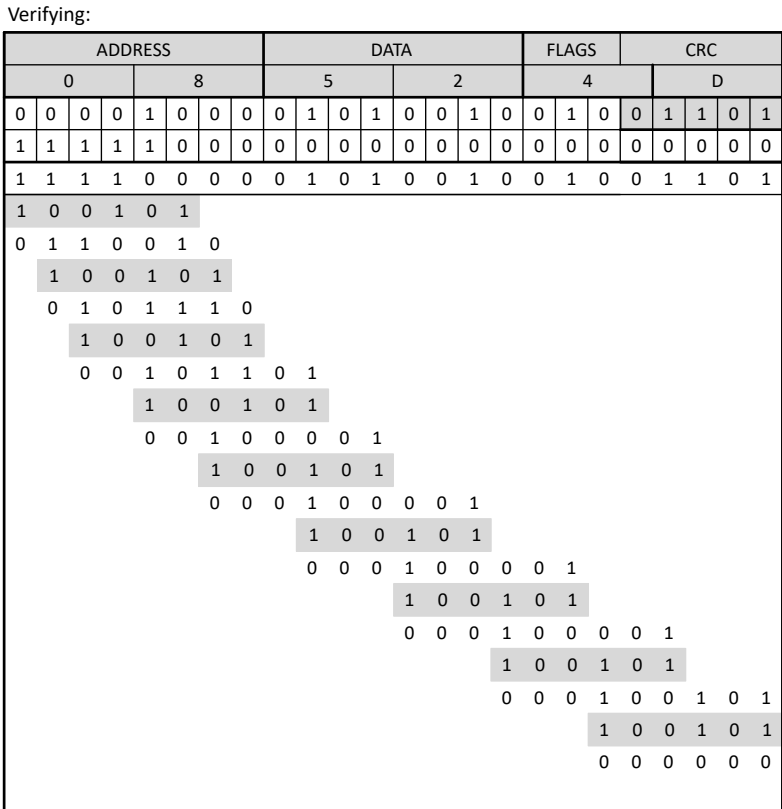


Figure 25 CRC Verification

SPI serial communication supports different SPI topologies: pure bus topology and daisy-chain, like in the examples shown in the following figure. In Daisy chain configuration, after all internally sampled bits have been transferred to SDO0, the buffered bits from the input SDI are provided to the SDO0 register to be sent to the next IC in the chain, or to the microcontroller for the last IC in the chain.

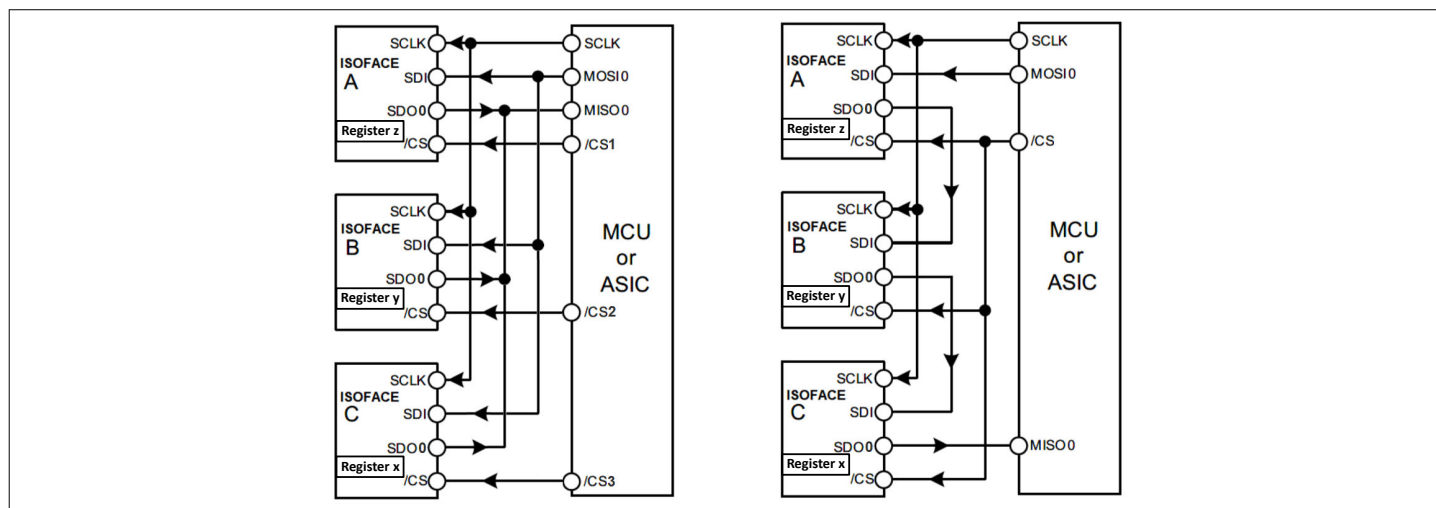


Figure 26 **Direct bus (left) and daisy chain (right) configuration**

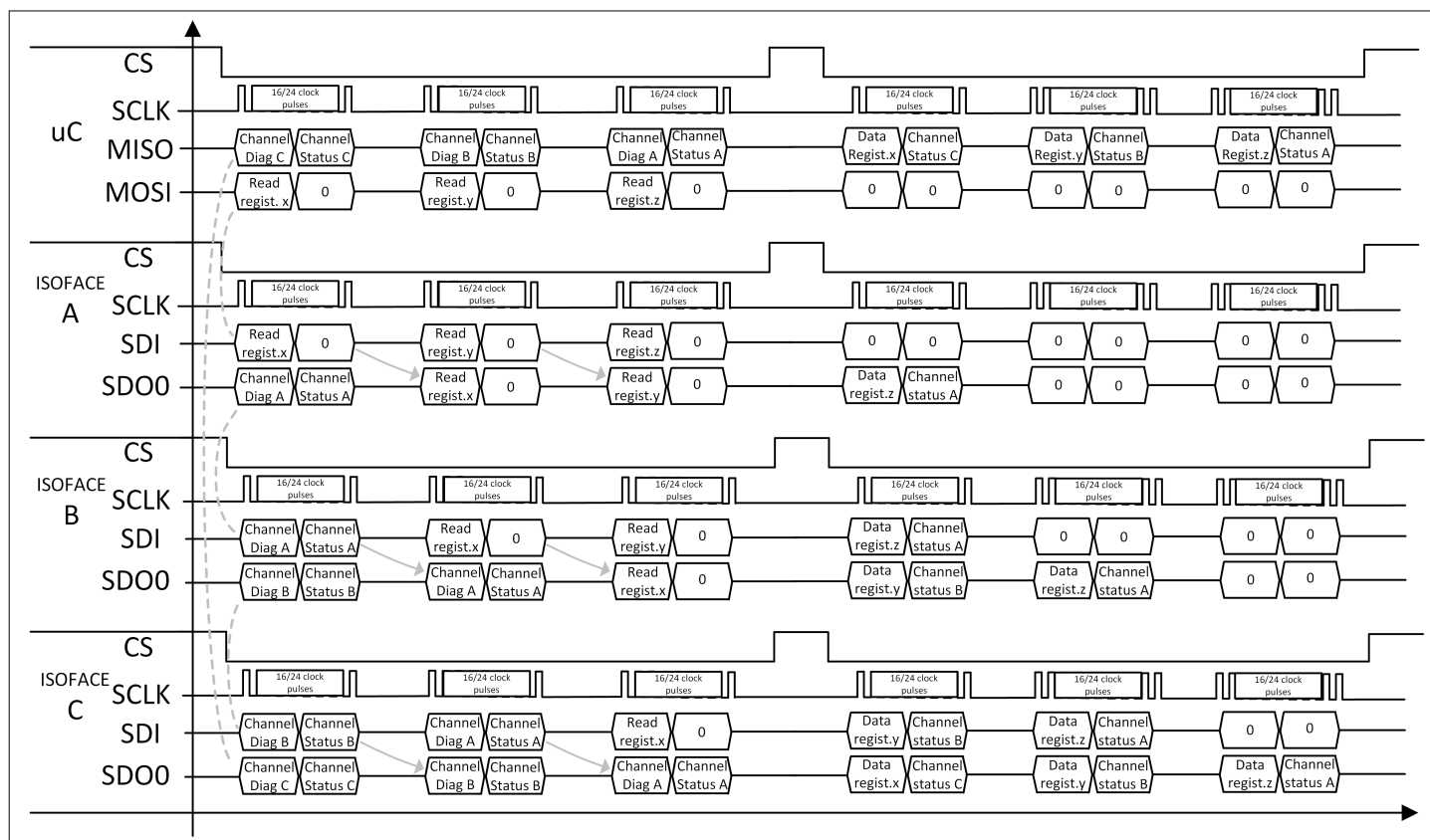


Figure 27 **Daisy chain pattern**

4.4.2 Parallel interface

In addition to the SPI serial interface, the IC has a parallel interface for simple and fast communication with the controller. eight pins are available to provide simultaneously 8 bits of information representing the address or content of the register.

The parallel interface setup is illustrated in the following figure.

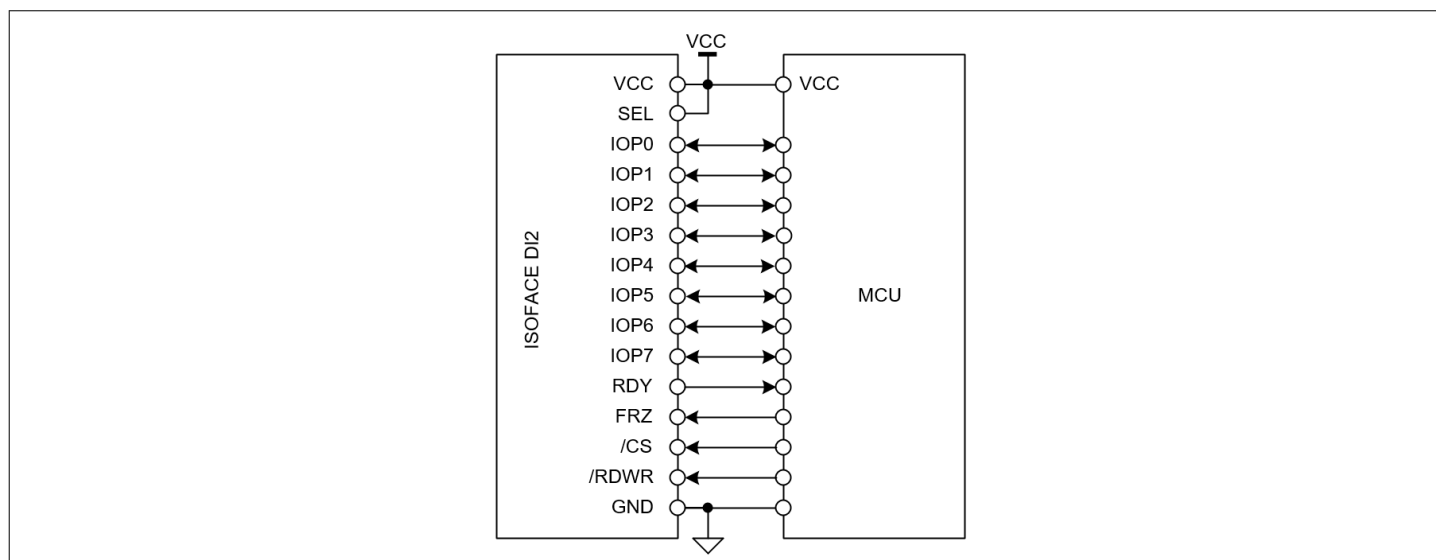


Figure 28 Parallel communication interface

To read or write a register, the controller must send the register's address and set the read or write bit as shown in following table:

Table 18 Table of parallel communication address bytes

IC Pin	IOP7	IOP6	IOP5	IOP4	IOP3	IOP2	IOP1	IOP0
Data	MSB							LSB
READ Command	0	Register address to Read						
WRITE Command	1	Register Address to Write						

4.4.2.1 Parallel interface timings

READ Command:

At the beginning of every communication procedure indicated by a falling edge of /CS signal, the IC sets IOP0 to IOP7 ports as inputs and waits for the register address data. If a read command is detected the IC sets the IOP0 to IOP7 ports as outputs after the /RDWR pin rising edge in order to send out the requested register data content.

The microcontroller closes the communication to the IC by setting /CS to high status after receiving the first data answer from the IC or it can keep the communication open sending multiple read requests for the same register applying a new cycle of /RDWR low-high as shown in [Figure 29](#)

The timing parameters in figure 31 are (for parameter values see [Table 11](#)):

- t_{RDWRsu} : time after the falling edge of /CS for the IC to start sampling the input
- $t_{RDWRlow}$: time for the signal /RDWR to be low
- $t_{RDWRhigh}$: time for the signal /RDWR to be high
- t_{RDWRHD} : time between last rising edge of /RDWR signal and rising edge of /CS signal

4 IC functionality description

- t_{su} : time for setup the data to be read
- t_{hold} : time for holding data to be read after $/RDWR$ rising edge

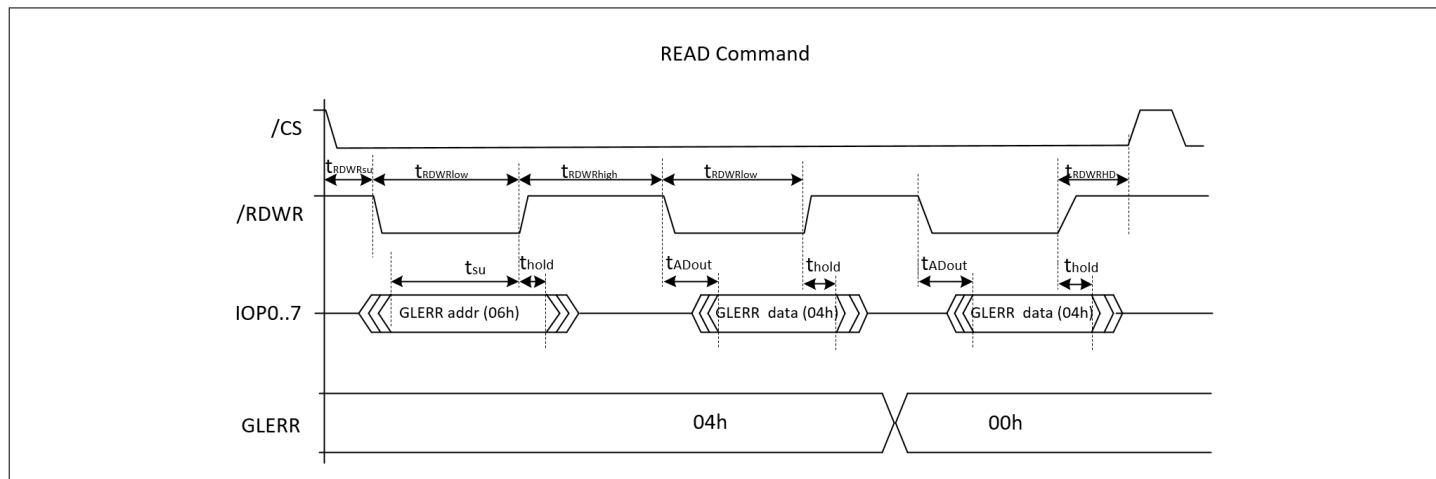


Figure 29 Parallel communication READ command timing

WRITE Command:

The WRITE command is identified by the MSB of the address byte sent from the microcontroller at value 1. The $IOP0$ to $IOP7$ ports are set by the IC as inputs at the beginning of every communication procedure, when receiving a WRITE command, the IC keeps the $IOP0$ to $IOP7$ ports as inputs after the acquisition of the address byte, in order to receive the new data to write to the register. Figure 30 shows the parallel write procedure, including the following parameters described in Table 11:

- t_{RDWRsu} : time after the falling edge of $/CS$ before the IC starts sampling the inputs
- $t_{RDWRlow}$: time for the signal $/RDWR$ to be low
- $t_{RDWRhigh}$: time for the signal $/RDWR$ to be high
- t_{RDWRHD} : time between last rising edge of $/RDWR$ signal and rising edge of $/CS$ signal
- t_{CSD} : $/CS$ high time between two R/W accesses on different registers
- t_{drdy} : time between $/RDWR$ rising edge and the data being ready and available in the register
- t_{su} : time before $/RDWR$ signal rising edge for setting data to be read
- t_{hold} : time after $/RDWR$ signal rising edge, to hold the data to be read

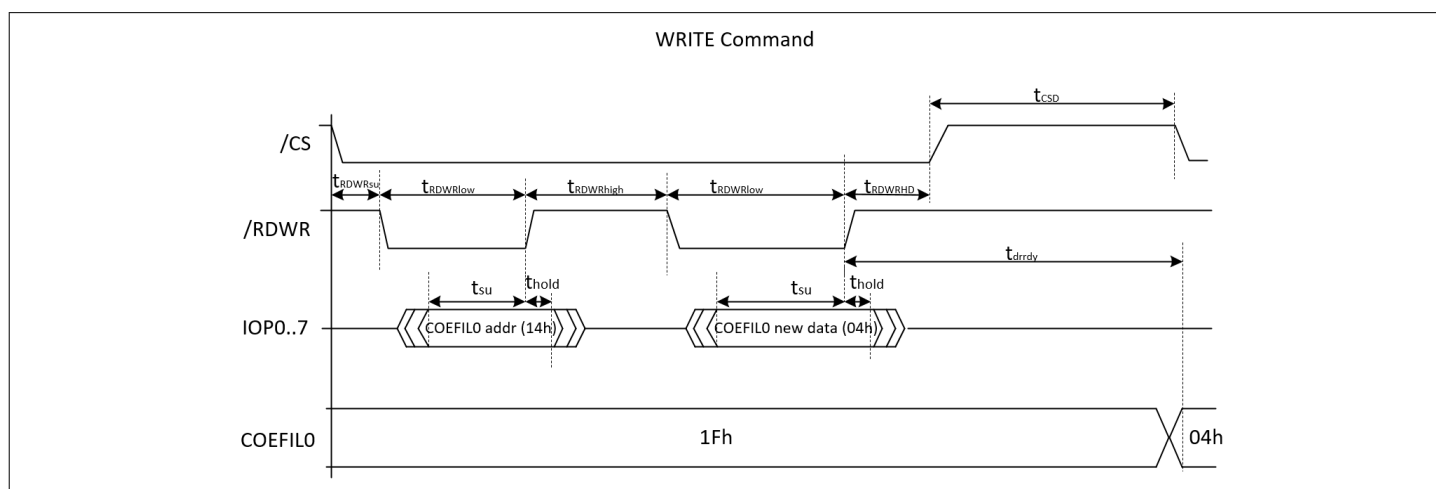


Figure 30 Parallel communication WRITE Command timing

4.4.2.2 Direct parallel interface

The IC enters parallel direct mode when both $/CS$ and $/RDWR$ are kept low for more than t_{direct} which value is indicated in Table 11. In direct mode the IC directly updates IOP0 to IOP7 output pins with the content of the INPDATA register when new data is available, no access request is needed. This mode can be considered an optocoupler emulation mode. The IC exits the parallel direct mode when $/CS$ or $/RDWR$ are pulled high.

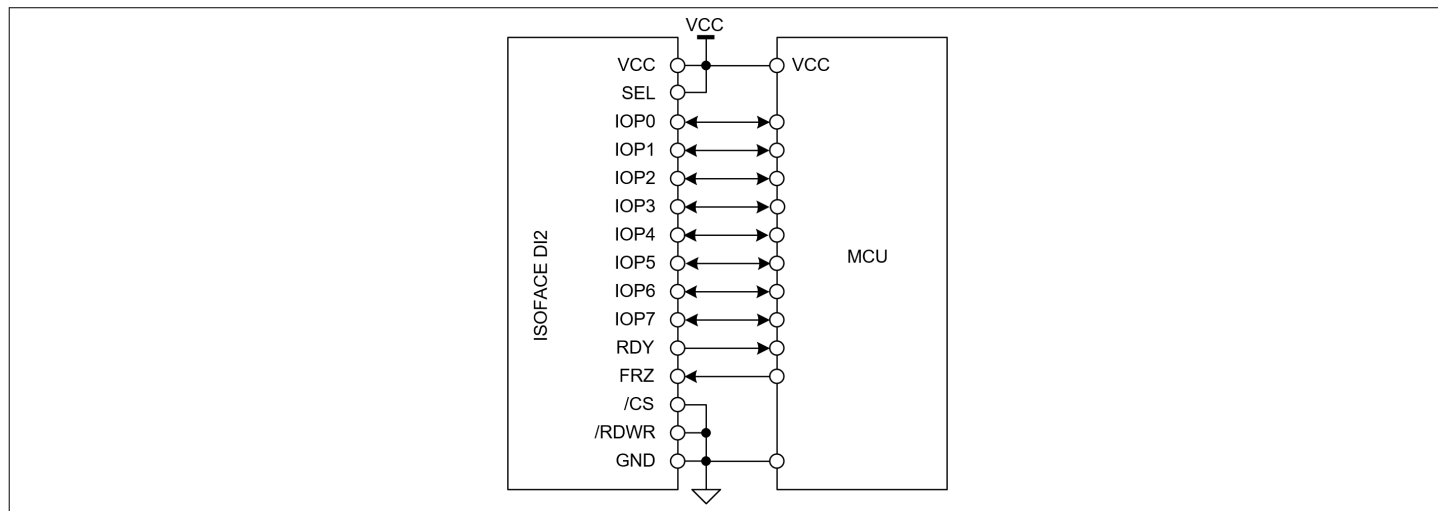


Figure 31 Parallel direct mode interface

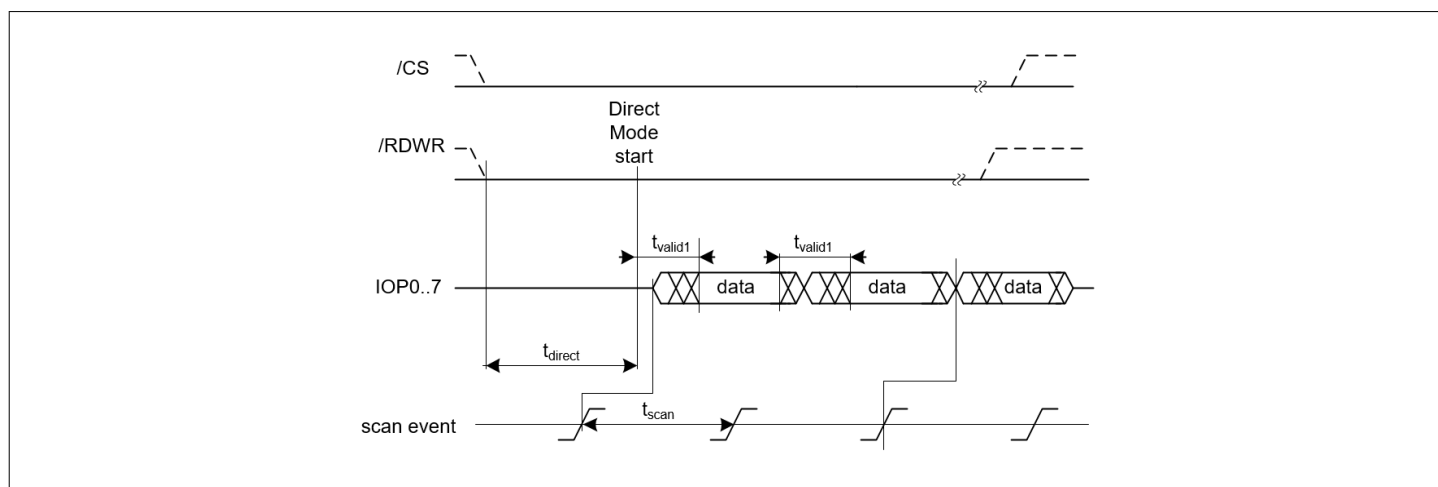


Figure 32 Parallel direct communication timing

Figure 32 shows the parallel direct mode timing pattern including the following parameters describe in Table 11:

- t_{valid1} : data validation time for output update
- t_{direct} : $/CS$ and $/RDWR$ low time to start direct mode
- t_{scan} : scan timing

Note 1: To avoid misreading during data update the MCU needs to implement in parallel direct mode a digital filter higher than t_{valid1} (data transition during update)

Note 2: In parallel direct mode the RDY pin follows directly the diagnostic status without sticky behavior

4.4.3 Registers

The microcontroller side chip provides several 8-bit registers which can be accessed by the microcontroller over the serial interface. The access is controlled by an internal arbiter processing the read / write requests as well as the synchronization requirements. Some timing requirements apply to ensure the consistency of the data provided to the controller.

Table 19 Register list

Short name	Description	Access	Read address	Write address
DIAG	Collective Diagnostics Register (Wire-Break Detection)	r, h	00 _H	
INPDATA	Input Data Register	r, h	02 _H	
GLERR	Global Error Register	r, h	04 _H	
COEFIL0	Filter Time and Diagnostics of Channel 0	r, w	06 _H	86 _H
COEFIL1	Filter Time and Diagnostics of Channel 1	r, w	08 _H	88 _H
COEFIL2	Filter Time and Diagnostics of Channel 2	r, w	0A _H	8A _H
COEFIL3	Filter Time and Diagnostics of Channel 3	r, w	0C _H	8C _H
COEFIL4	Filter Time and Diagnostics of Channel 4	r, w	0E _H	8E _H
COEFIL5	Filter Time and Diagnostics of Channel 5	r, w	10 _H	90 _H
COEFIL6	Filter Time and Diagnostics of Channel 6	r, w	12 _H	92 _H
COEFIL7	Filter Time and Diagnostics of Channel 7	r, w	14 _H	94 _H
INTERR	Internal Error Register	r, h	16 _H	

r - register can be read h - register is updated by the device itself w - register can be written

The diagnostic registers GLERR, INTERR and DIAG have a sticky behavior. They only can be cleared when an explicit read access to the corresponding register address is performed after the diagnostic event has disappeared.

4.4.3.1 **DIAG register**

DIAG register contains the filtered values of the Wire-Break detection for channels 0 to 7. This register can be read by the microcontroller. As soon as one of DIAG bits is set, the CF-bit of the GLERR register is set as well. The bits of the DIAG register are sticky, that is, once a wire-break condition has been detected (after the filter time), the respective bit remains set. A read access resets the sticky bits under the condition that no wire-break is detected anymore and no wire-break information is pending at the filter outputs.

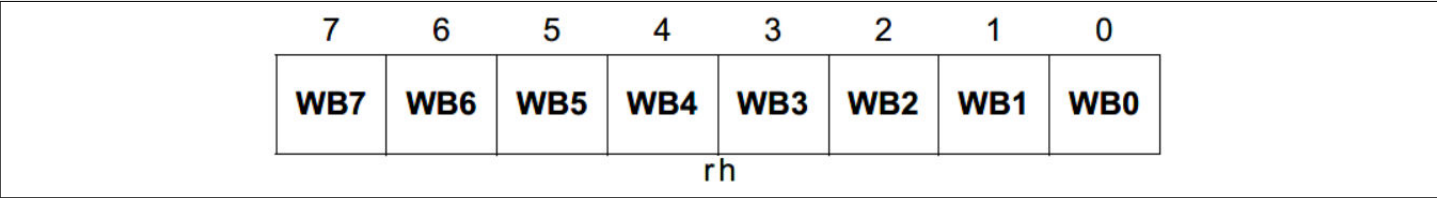


Figure 33 DIAG register bit configuration

Table 20 DIAG (Collective diagnostic register) - Address: 00h - Reset value 00h

Field	Bits	Type	Description
WB[x]	7:0	r, h	Channel wire-break detection 0 _b no wire-break signal detected at channel x 1 _b wire-break signal detected at channel x

4.4.3.2 INPDATA register

INPDATA register contains the filtered values of the input data detected at the channels 0 to 7. The microcontroller can only read this register.

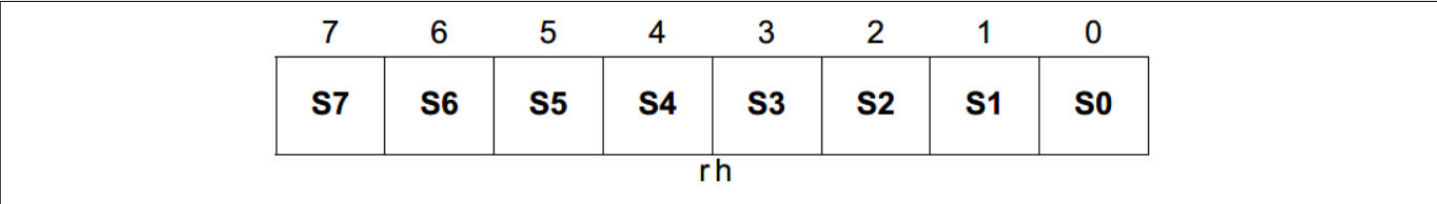


Figure 34 INPDATA register bit configuration

Table 21 INPDATA (Input Data Register) - Address: 02h - Reset value 00h

Field	Bits	Type	Description
S[x]	7:0	r h	Input channel data this bit represents the input data detected at the pin INxH of the channel x 0 _b input data below the input threshold for selected sensor 1 _b input data above the input threshold for selected sensor

4.4.3.3 COEFIL 0-7 Channel configuration registers

The COEFIL registers can be written and read by an external microcontroller. The COEFIL registers allow the channel resolved setting of the deglitching filter times but as well to activate or deactivate the wire-break detection. If wire-break detection is enabled the same filter settings as for input data are also used for filtering the detection of wire-break events. The programmed register values are applied to the input signals if the DGF pin is low. The listed timing values for the digital filters apply to 500 kHz scan frequency, for other scan frequencies they scale proportionally. Write access requires specific time for updating the internal registers, timing parameters section of this document defines the timing requirements to access the registers.

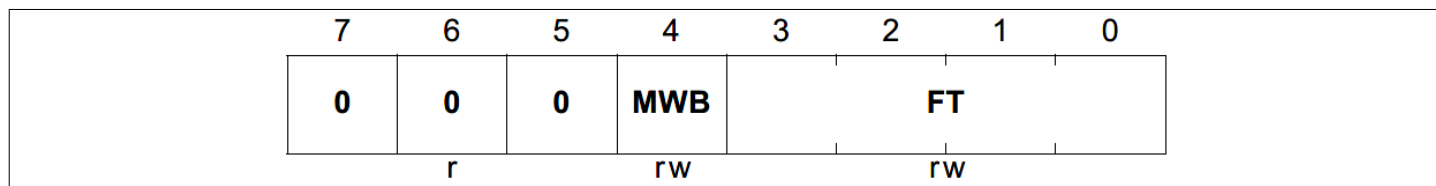


Figure 35 COEFIL register bit configuration

Table 22 COEFIL (Channel 0 to 7 filter setting registers) - Address: 06h to 14h for read access, 86h to 94h for write access - Reset value 1Fh - The deglitching filter time values apply to scan frequencies of for 500kHz scan frequency, and are scaled proportionally for other for different scan frequencies

Field	Bits	Type	Description
FT	3:0	r, w	Digital filter time this bit range configures the digital filter time for averaging the data and wire-break signals detected at channels 0 to 7 00 _h 25 scan cycles (50 μs @ 500 kHz) 01 _h 50 scan cycles (100 μs @ 500 kHz) 02 _h 200 scan cycles (400 μs @ 500 kHz) 03 _h 400 scan cycles (800 μs @ 500 kHz) 04 _h 800 scan cycles (1.6 ms @ 500 kHz) 05 _h 1600 scan cycles (3.2 ms @ 500 kHz) 06 _h 5000 scan cycles (10 ms @ 500 kHz) 07 _h 10000 scan cycles (20 ms @ 500kHz) 08 _h - 0F _h filter bypassed (default)
MWB	4	r, w	Monitor wire-break events this bit enables the detection of wire-break events 0 _b The wire-break detection is not enabled 1 _b The wire-break detection is enabled an the filtered result of detected wire-break events is written to the DIAG and GLERR registers. After start-up, the default setting is that wire-break detection is enabled.
0	5:7		Reserved

4.4.3.4 GLERR Global error register

The microcontroller has only read access to the GLERR register. The GLERR register contains the states of the IC parameters monitored during operation. The MV and UV bit are set if the supply voltage is dropping below the corresponding thresholds. The CF-bit is the OR-combination of all bits of the DIAG register indicating the wire-break status for each of the eight or-ed channels. The bits of the GLERR register are used for the evaluation of the error status indicated via the RDY pin. The bits of this register are sticky and remain set even if the root cause has vanished. They are only cleared once they are read by the microcontroller after the faults are not present anymore. The CF bit itself is not reset by reading the GLERR register itself as it acts as 'or-ed' summary of the content of the DIAG register. Consequently this bit is reset if all wire break events have vanished and the related DIAG register has been read afterwards.

For further details to the generation of error signal on the RDY pin see also [Chapter 4.3.1](#).

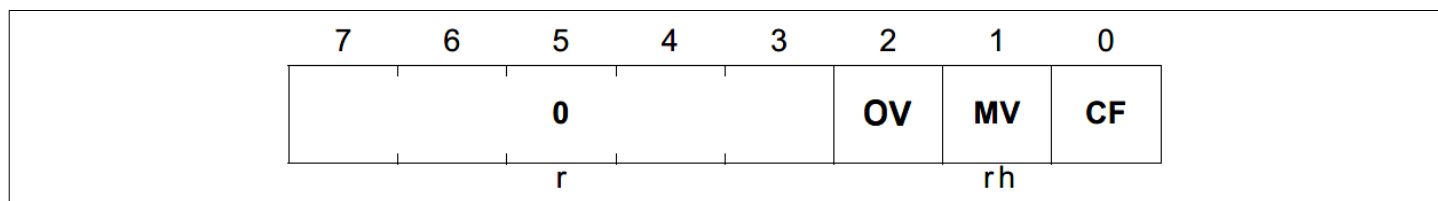


Figure 36 GLERR register bit configuration

Table 23 GLERR (Global Error Register) - Address: 04h - Reset value 06h

Field	Bits	Type	Description
CF	0	r, h	Channel fault 0 _b no wire-break condition has been detected at the channels 1 _b at least one channel shows wire-break condition
MV	1	r, h	VBB "missing voltage" 0 _b no "missing voltage" detected at VBB 1 _b a "missing voltage" condition has been detected at VBB
OV	2	r, h	VBB overvoltage 0 _b no overvoltage detected at VBB 1 _b a overvoltage condition has been detected at VBB
0	3:7		reserved

4.4.3.5 INTERR Internal error register

The INTERR register contains the states of the internal errors monitored for safe IC operation. The microcontroller has only read access to the INTERR register and the bits of the INTERR register are used for the evaluation of the error status which is indicated by the RDY output pin pulled to low. The bits of the INTERR register are sticky and remain set once a fault condition is detected until the bits are read after the diagnosed faults are resolved. On power up (UVLO), the bits W4S and TE bits are preset and have to be cleared by a read access during or after the startup phase.

For further details to the generation of error signal on the RDY pin see also [Chapter 4.3.1](#).

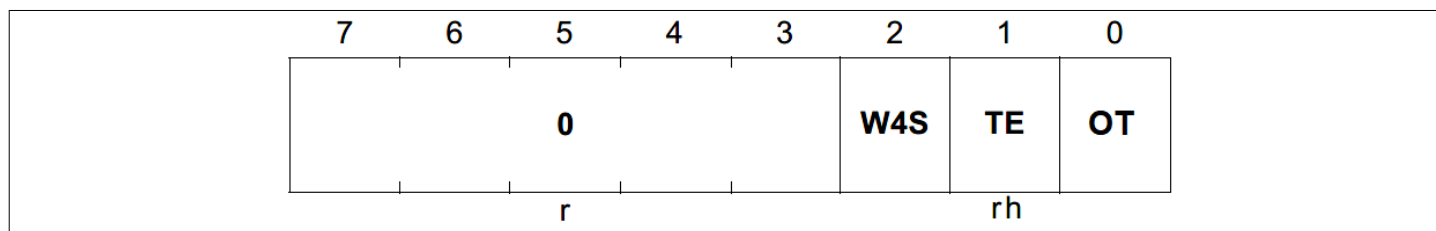


Figure 37 INTERR register bit configuration

Table 24 INTERR (IC Status Register) - Address: 16h - Reset value 06h

Field	Bits	Type	Description
OT	0	r, h	IC Overtemperature alarm 0 _b : no overtemperature detected 1 _b : overtemperature detected
TE	1	r, h	Transmission error 0 _b : no transmission error 1 _b : transmission error
W4S	2	r, h	Wait for sense chip/VBB UVLO 0 _b : sense side chip is powered and ready 1 _b : sense chip is not powered
0	3:7		reserved

5 Application information

Note: The following information is given just as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

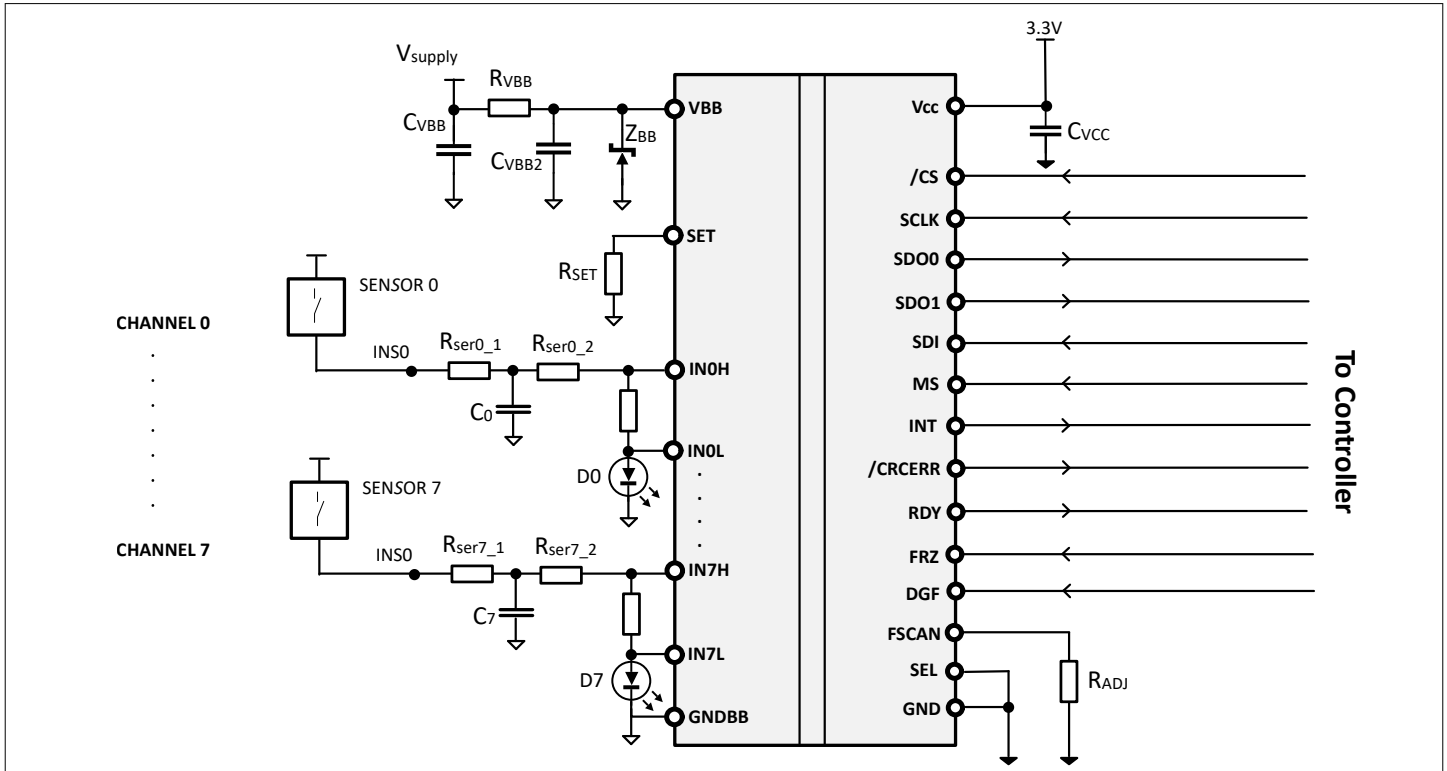


Figure 38 Typical application schematics (24V sensors)

5.1 IC supply

The IC is supplied via the VBB pin for the input side and the Vcc pin for the controller interface. Capacitors are needed between the Vcc pin and GND with typical values of 1µF and 10V and between VBB pin and GNDBB with typical values of 330nF to 4.7 µF and 100V. If enhanced EMC pulse withstanding capability is required at VBB pin, additional external protection or additional capacitance has to be added. [Figure 7](#) shows a standard configuration including 100 Ω series resistor for safety functionality and an external suppressor to meet surge and burst EMC requirements. The voltage alarm threshold at application level are shifted by the voltage drop on the resistor.

5.2 Input channels

To configure the IC parameters for the compatible sensor types, connect R_{set} resistor between SET pin and GNDBB with a value as indicated in the following table. The resistors $R_{ser(x)}$ and $R_{ext(x)}$ must have the values indicated in the table to ensure a correct sensor status detection and an optimized sensor current regulation. If a filter capacitor is applied for the input channel the resistor $R_{ser(x)}$ has to be split symmetrically to $R_{ser(x_1)}$ and $R_{ser(x_2)}$ and the capacitor has to be placed in-between the two of them. For further details refer to [chapter 4.2](#).

Table 25 Sensor selection settings

Mode label	R _{set} value	Sensor type	Nominal voltage	R _{ext(x)}	R _{ser(x)}	Sensor current at INxS	Sensor threshold at INxS L→H	Sensor threshold at INxS H→L	MV threshold	OV threshold
M_24V_T3	R _{set1} ≤ 0.5 kΩ (or GND)	Type 3	24 V	13 kΩ 1%	2 kΩ 1%	2.1-2.5 mA	11 V	5 V	12.1 V	30 V
M_24V_T1	R _{set2} = 10 kΩ 1%	Type 1	24 V	13 kΩ 1%	2 kΩ 1%	2.1-2.5 mA	15 V	5 V	15 V	30 V
M_48V_T1	R _{set3} = 24 kΩ 1%	Type 1	48 V	56 kΩ 1%	2 kΩ 1%	1.05-1.25 mA	30 V	16 V	34 V	57.5 V
M_48V_T3	R _{set4} = 56 kΩ 1%	Type 3	48 V	56 kΩ 1%	2 kΩ 1%	1.05-1.25 mA	34 V	16 V	30 V	57.5 V

Please note that the values for R_{ser(x)} given in table [Table 25](#) refer to the cumulative resistance of R_{ser}. In case R_{ser} is split because a filter capacitor is used at INxH, the values for the be split resistors R_{ser(x_1)} and R_{ser(x_2)} have to fulfill the equation

$$R_{ser(x_1)} = R_{ser(x_2)} = \frac{R_{ser(x)}}{2}$$

Equation 1

The sensor type selected via R_{set} cannot be changed during operation as the configuration takes place at power-up. For R_{set} outside the values and tolerances indicated in the table, the proper functionality of the IC cannot be ensured. Sensor Type 1 and Type 3 are included in the standard EN61131-2. The sink current is limited by the current regulator of the IC to values in the listed range which are complying to the standard.

A disconnection of the sensor wiring (wire-break) can be detected by measuring the remaining leakage current when the sensor is in off-state. The wire-break detection is using the leakage current that is flowing into the IC (INxH pin). The corresponding threshold for wire break detection is given in [Table 8](#), Please note that the resulting threshold current for wire break detection at the sensor is higher by the current share that is flowing through R_{ext} to GND. With the listed values for R_{ser} and R_{ext} the resulting wire break threshold at the sensor translates to typ. 125 µA.

5.3 Scan frequency settings

In SPI serial mode the scan frequency can be selected between 3 values: 500kHz for higher resolution, 200kHz or 20kHz to optimize power consumption. The selection is made based on the value of the R_{adj} resistor to connect between FSCAN and GND as shown in the following table:

Table 26 Resistor values for frequency settings

Resistor value	Scanning Frequency [kHz]
82 kΩ 1%	20 kHz
33 kΩ 1%	200 kHz
Shorted to GND	500 kHz

In parallel communication the scan frequency is fixed and set at 500 kHz.

5.4 Safety limits

Table 27 safety limit values

Parameter	Symbol	Value	Unit	Note or condition
Maximum ambient safety temperature	T_J	<150	°C	
Maximum T_{case_top}	T_{case_top}	<113	°C	no air flow
Safety power dissipation	P_S	3	W	$R_{thJA} = 41\text{ K/W}^{(1)}$, $T_A = 25^\circ\text{C}$, $T_J = 150^\circ\text{C}$
Safety supply current	$I_{S,tot}$	100	mA	$R_{thJA} = 41\text{ K/W}^{(1)}$, $T_A = 25^\circ\text{C}$, $T_J = 150^\circ\text{C}$, $V_{BB} = 30\text{ V}$

1) PCB with dimension and metallization as defined by JEDEC 2s2p (JESD 51-5, JED51-7), Inner Layers split

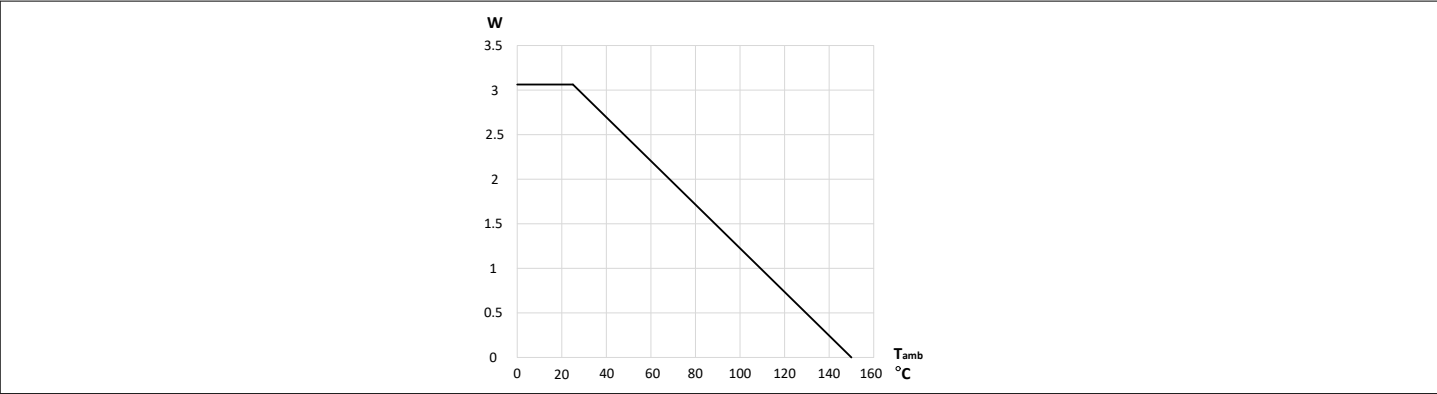


Figure 39 Safety limit graph

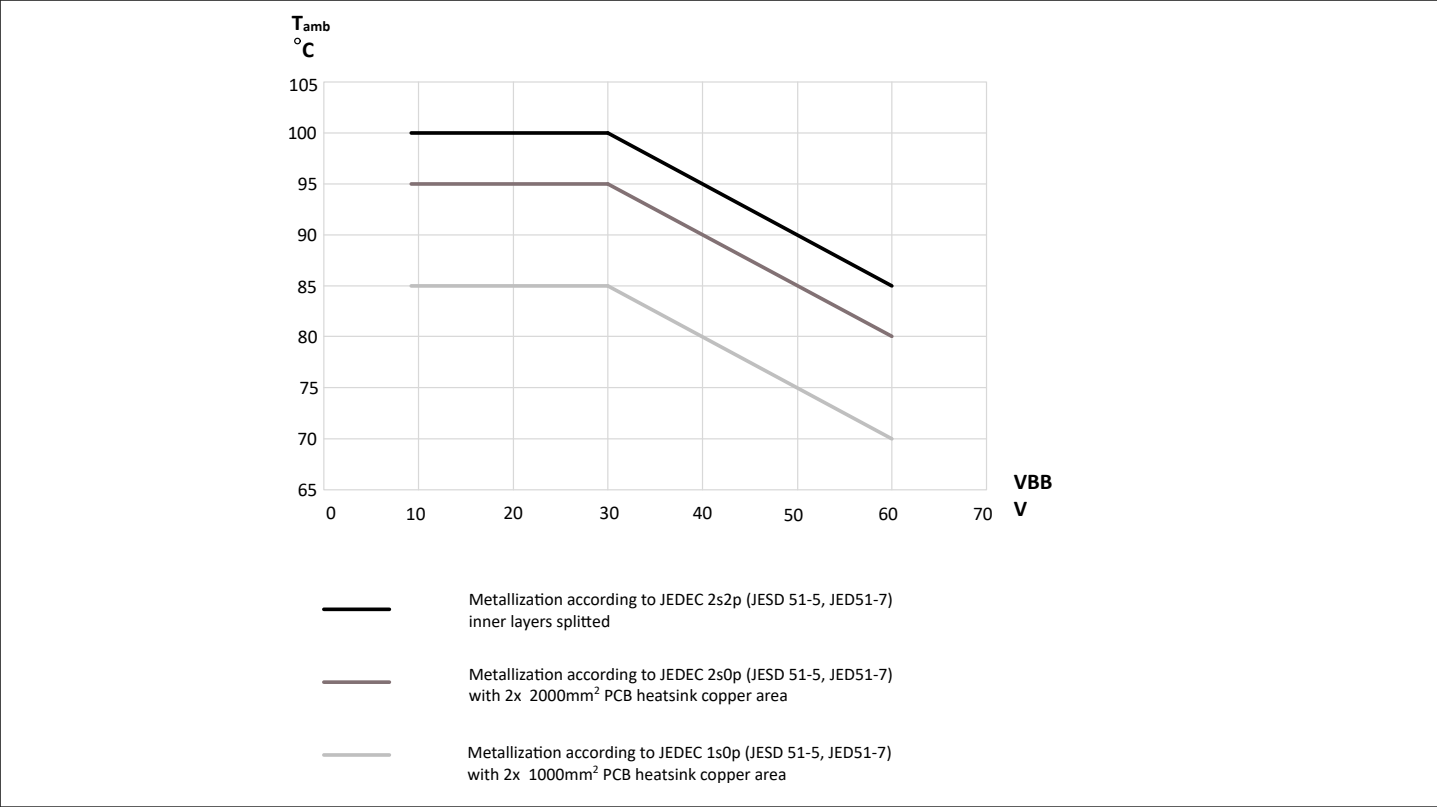


Figure 40 T_{amb} vs IC supply voltage

6 EMI compliance

The IC is designed to target applications that comply with the following EMI requirements standards, external components have to be dimensioned in order to comply with the standards.

EN61000-4-2 ESD immunity test

EN61000-4-4 Electrical fast transient/burst immunity test

EN61000-4-5 Surge immunity test

EN61000-4-6 Immunity to conducted disturbances induced by radio-frequency fields

EN61000-4-8 Power frequency magnetic field immunity

EN61000-4-9 Impulse magnetic field immunity

EN61000-6-4 conducted and radiated emissions

7 PCB layout recommendations

For a proper IC functionality the PCB layout has to be optimized following these guidelines:

- Ensure separation of the two domains isolated by the IC with a PCB creepage and clearance distance according to the isolation requirements. ISO2I828V has 3.5 mm creepage and clearance to target 2.5 kVac isolation.
- It is possible to implement the application on a two-layer board layout, with the top layer dedicated to the connections and the bottom layer to dissipation and expanded GND and GNDBB copper area, keep the two ground separated with proper creepage and clearance for the application target isolation.
- PCB vias connect the IC heatsink pads copper to the dissipating copper on bottom layer. The Heatsink pads have to be connected separately to the respective GNDBB or GND pin.
- For higher ambient temperatures, a four-layer PCB is suggested. In this case, top layer is used for connections and bottom layer for dissipation, internal layers can also add additional dissipation copper. All dissipation areas have to be connected through vias to the IC heatsink pads.
- Capacitors for immunity protection at the VBB pin have to be placed as close as possible to the VBB pin.
- If analog filter capacitors are used for the input channels it is important that the serial resistors $R_{\text{ser}(x)}$ of these channels are split by half into two individual resistors $R_{\text{ser}(x_1)}$ and $R_{\text{ser}(x_2)}$ placed in series and the filter capacitor to GNDBB has to be placed in the middle of the two. The effective serial resistance of the channel must not change due to this. See also [Chapter 4.2](#).
- At startup the IC detects the values of resistors connected to FSCAN pin and SET pins and GND and configures the application parameters. It is important that the tracks that connect pins and resistors are short and narrow, that no GND plane is present below these tracks, and that no capacitances are applied to SET and FSCAN pins.

8 Package information

8.1 Soldering

The soldering must follow the standard reflow J-STD-020. The part is qualified with 3 times soldering simulation (preconditioning).

8.2 IC package

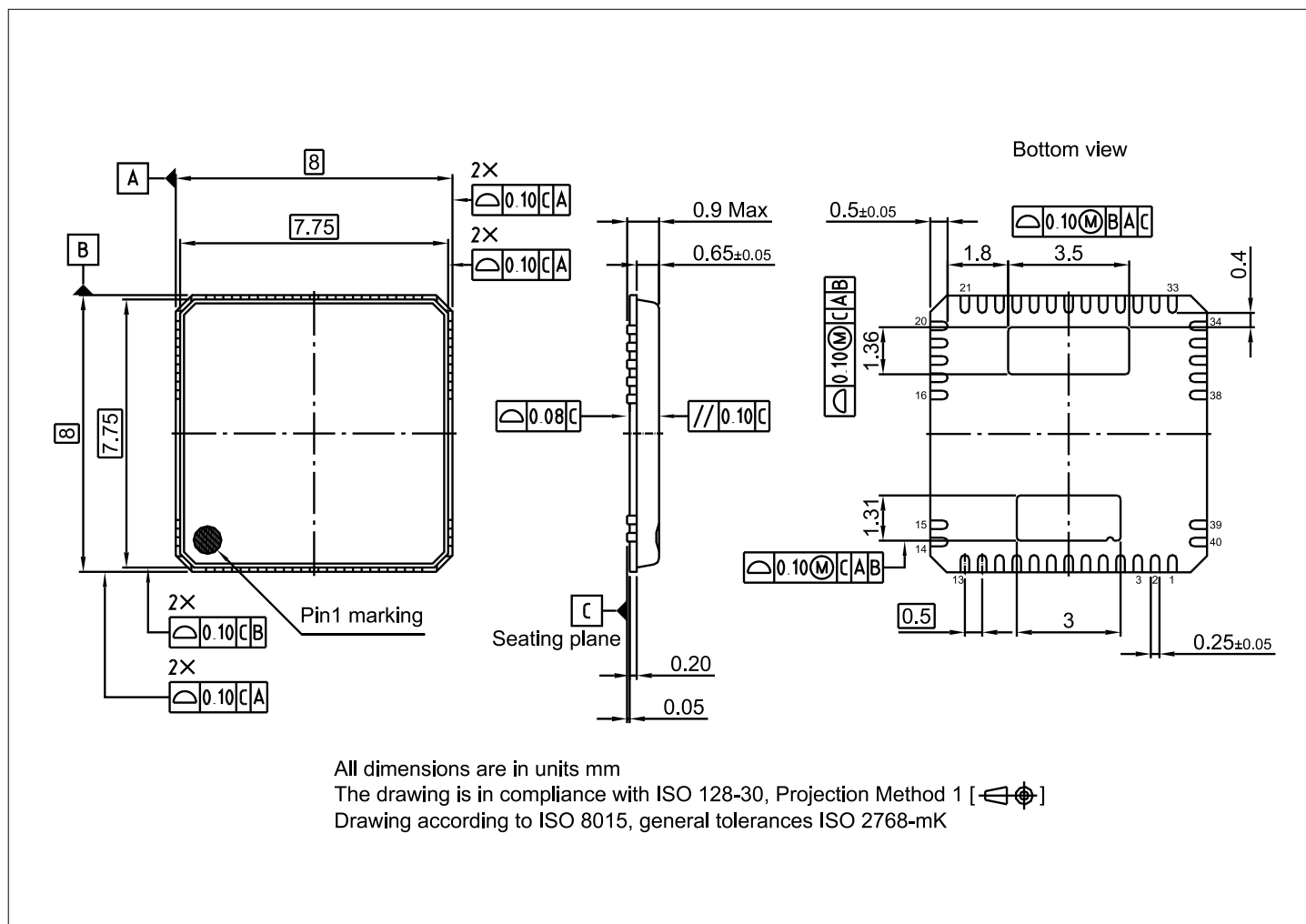


Figure 41 VQFN-40 (dimensions in mm)



8.3 Packaging information

The part is classified MSL level 1. The IC is delivered in standard tape and reel with 2500 pieces per reel and 1 reel per box. Reel diameter is 300mm. Dimensions of the reel in the following figure:

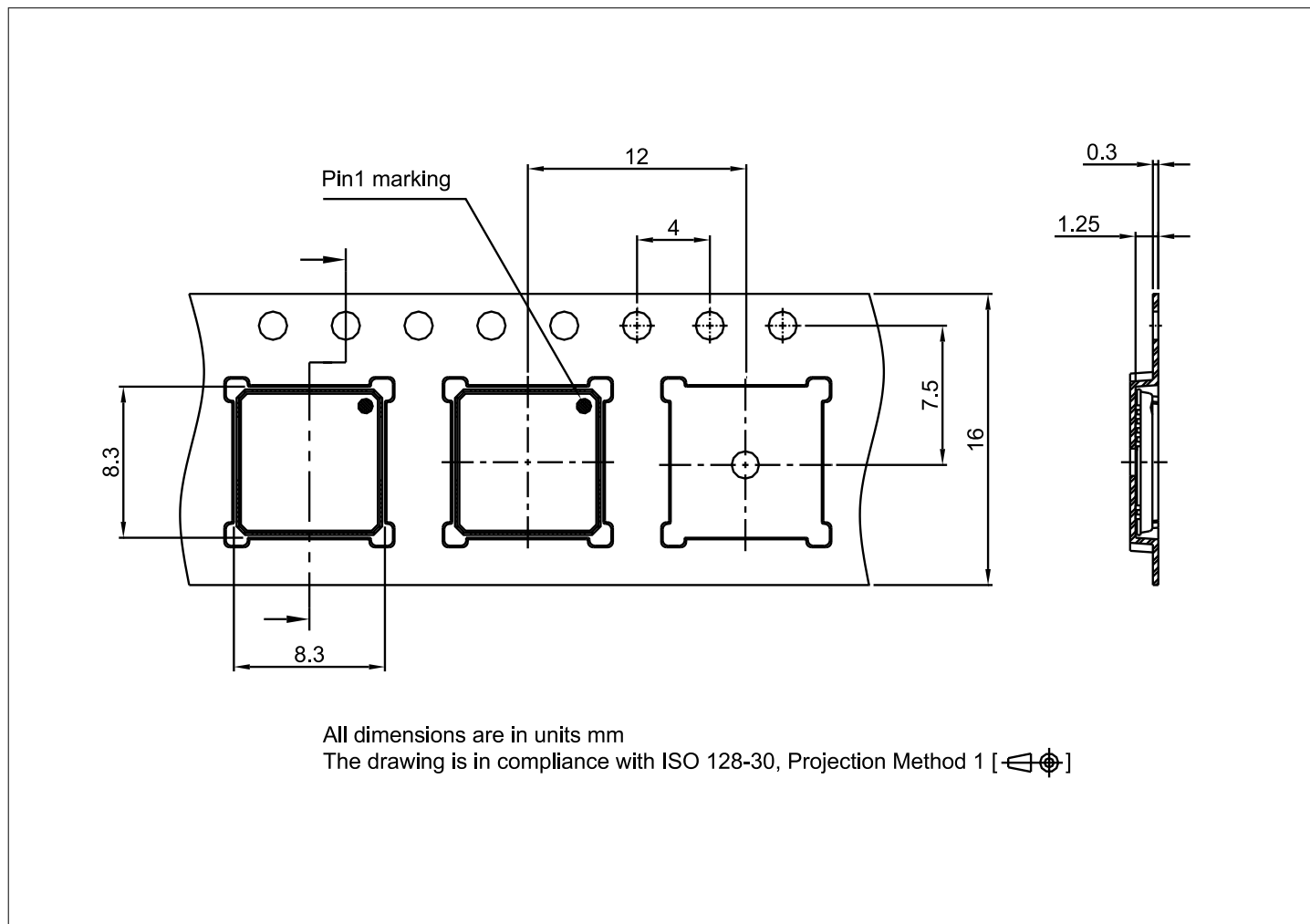


Figure 43 Dimensions of the tape in mm

Green Product (RoHS compliant)

To meet the worldwide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). Further information on packages: <https://www.infineon.com/packages>



Revision history

Document version	Date of release	Description of changes
Rev. 0.8	2026-08-10	Preliminary datasheet initial release

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