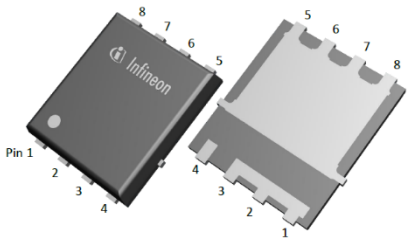
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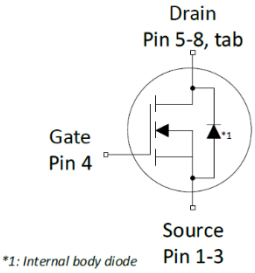
OptiMOS™ 7 功率晶体管，40 V

PG-TDSON-8



特性

- N沟道，标准电平
- 增强型SOA
- 驱动优化
- 卓越的热阻
- 100% 雪崩测试
- 无铅镀层；符合 RoHS 标准
- 符合 IEC61249-2-21 标准的无卤素



产品验证

符合 JEDEC JESD47, JESD22 和 J-STD-020 相关测试的工业应用要求。

表 1　　主要性能参数

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),max}$	0.69	mΩ
I_D	357	A
Q_{OSS}	107	nC
$Q_G(0V..10V)$	85	nC
$Q_{rr}(100A/\mu s)$	56	nC

Part number	Package	Marking	Related links
ISCH69N04NM7V	PG-TDSON-8	69N04NM7	-

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1 最大额定值

除非另有规定，T_A =25 °C

表 2 最大额定值

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	357	A	V_{GS}=10 V, T_C=25 °C
				252		V_{GS}=10 V, T_C=100 °C
				260		V_{GS}=15 V, T_C=100 °C
				48		V_{GS}=10 V, T_A=25 °C, R_{THJA}=50 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	1428	A	T_C=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	368	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	167	W	T_C=25 °C
				3.0		T_A=25 °C, R_{thJA}=50 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

1) 额定值指产品仅具有数据手册指定的绝对最大值，保持外壳温度符合规定要求。其他外壳温度请参见图 2。需要根据实际环境条件降低额定值。

2) 器件置于40 mm × 40 mm × 1.5 mm 环氧树脂 PCB FR4 上，配有6 cm^2（单层，70 µm厚）铜层面积用于漏极连接。PCB在静止空气中垂直放置。

3) 详细信息请参见图 3

4) 详细信息请参见图 13

2 热特性

表 3 热特性

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	0.9	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}			20		
Thermal resistance, junction - ambient, 6 cm^2 cooling area [5)]	R_{thJA}			50		

5) 器件置于40 mm × 40 mm × 1.5 mm 环氧树脂 PCB FR4 上，配有6 cm^2（单层，70 µm厚）铜层面积用于漏极连接。PCB在静止空气中垂直放置。

3 电气特性

除非另有规定，T_j = 25°C

表 4 静态特性

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.4	2.75	3.2	V	V_{DS}=V_{GS}, I_D=82 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C
			10	100		V_{DS}=40 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.56	0.65	mΩ	V_{GS}=15 V, I_D=50 A
			0.63	0.69		V_{GS}=10 V, I_D=50 A
Gate resistance	R_G	-	0.7	-	Ω	-
Transconductance	g_{fs}	-	140	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=50 A

表 5 动态特性

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [6]	C_{iss}	-	5600	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Output capacitance [6]	C_{oss}		2900			
Reverse transfer capacitance [6]	C_{rss}		64			
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r		5.3			
Turn-off delay time	$t_{d(off)}$		27			
Fall time	t_f		8.7			

[6] 由设计指定，未经过生产测试。

表 6 栅极电荷特性[7)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	26	-	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$		15	-	nC	
Gate to drain charge	Q_{gd}		18	-	nC	
Switching charge	Q_{sw}		29	-	nC	
Gate charge total [8)]	Q_g		85	106	nC	
Gate plateau voltage	$V_{plateau}$		4.7	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	77	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	107	142	nC	V_{DS}=20 V, V_{GS}=0 V

7) 参数定义请参数见“栅极电荷波形”

8) 由设计指定，未经过生产测试。

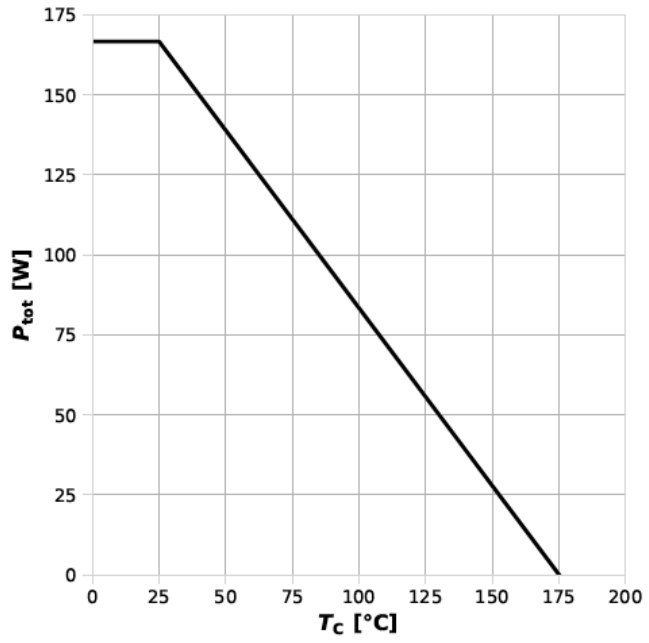
表 7 反向二极管

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	159	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			1428		
Diode forward voltage	V_{SD}	-	0.80	1.0	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time [9)]	t_{rr}	-	50	-	ns	V_R=20 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge [9)]	Q_{rr}		56		nC	

9) 由设计指定，未经过生产测试。

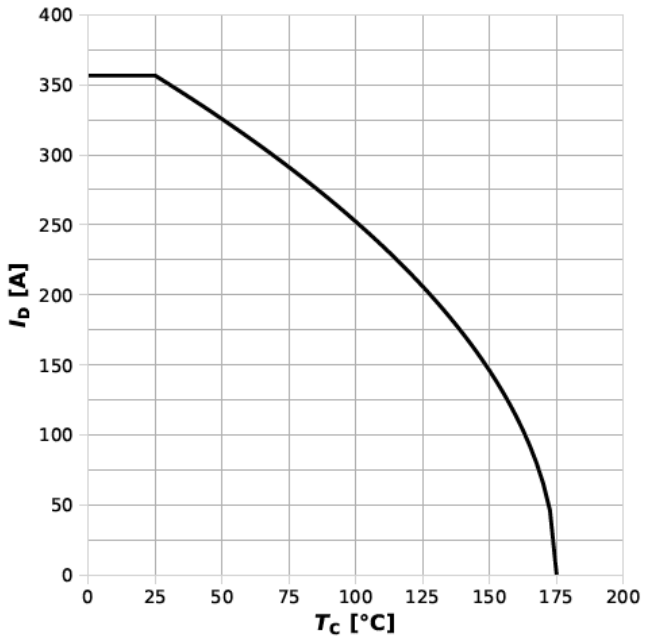
4 电气特性图

Diagram 1: Power dissipation



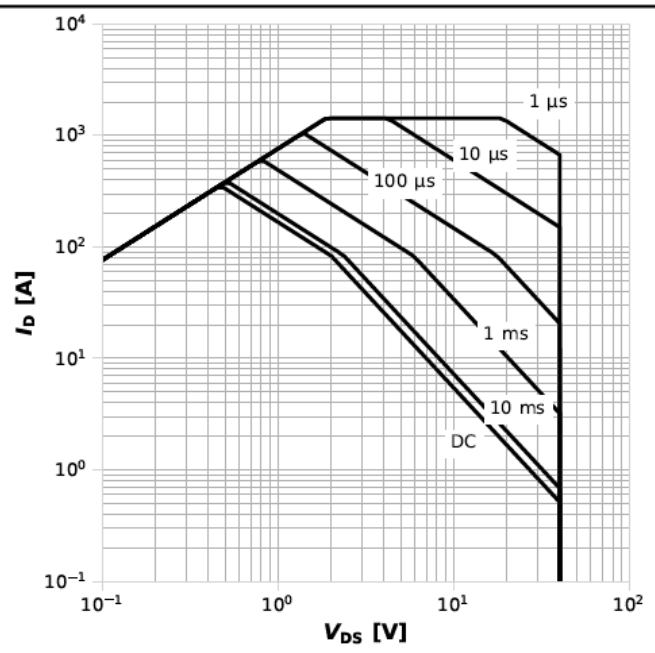
P_{tot}=f(T_C)

Diagram 2: Drain current



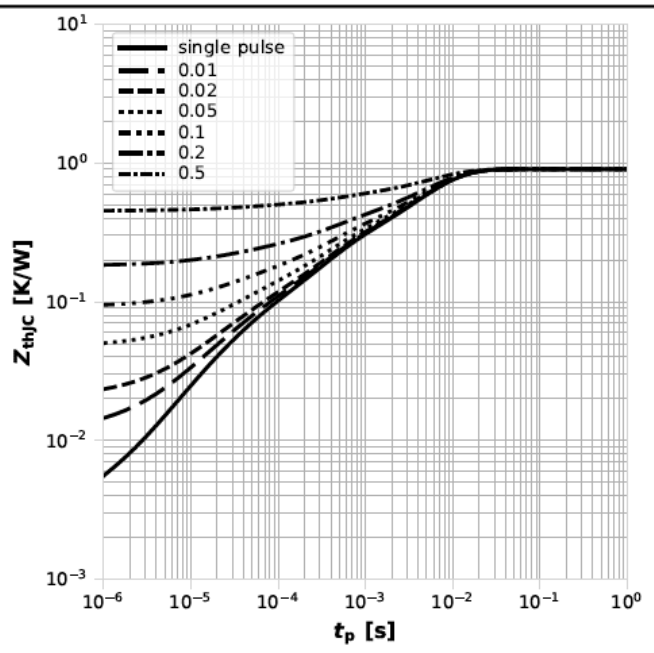
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



Z_{thJC}=f(t_p); parameter: D=t_p/T

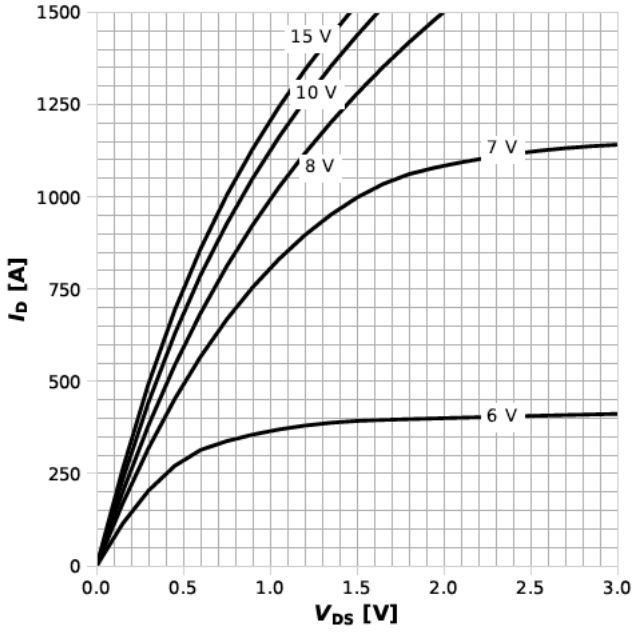
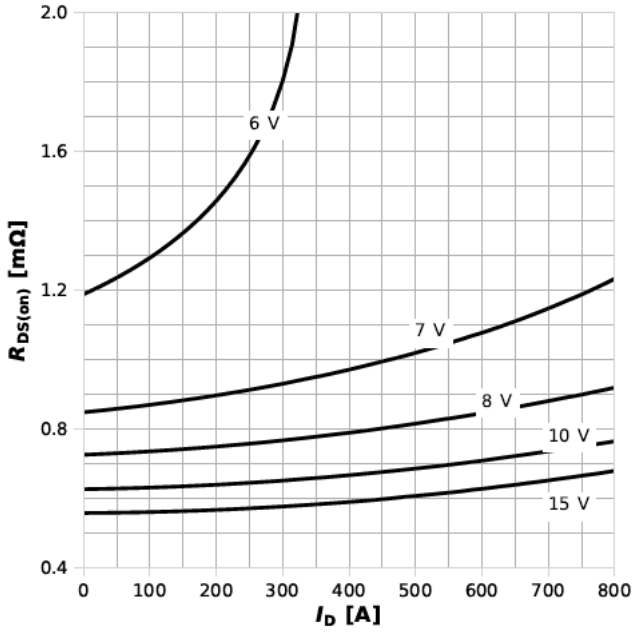
Diagram 5: Typ. output characteristics	Diagram 6: Typ. drain-source on resistance
	
$I_D=f(V_{DS})$, T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}=f(I_D)$, T_j=25 °C; parameter: V_{GS}

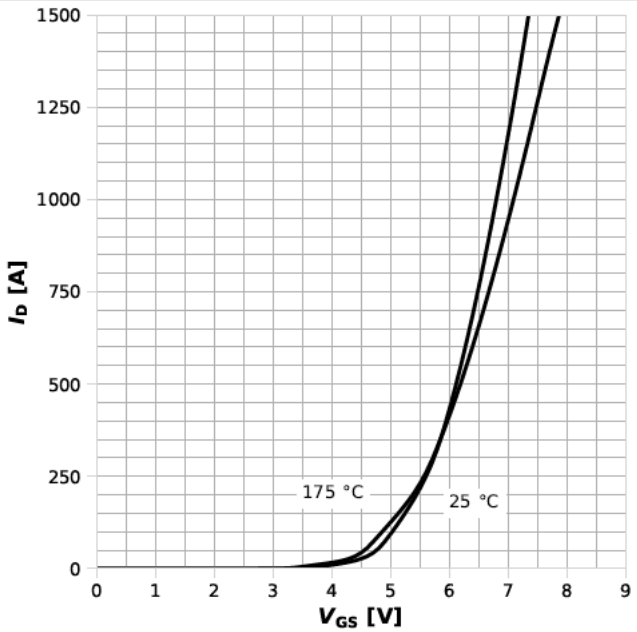
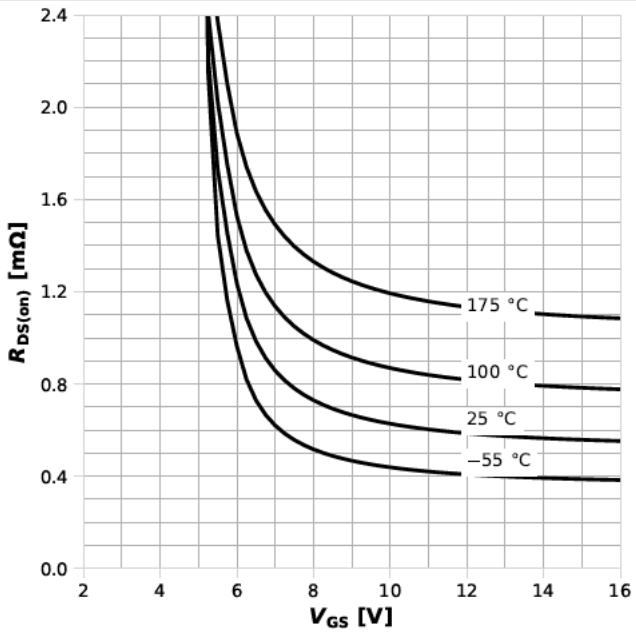
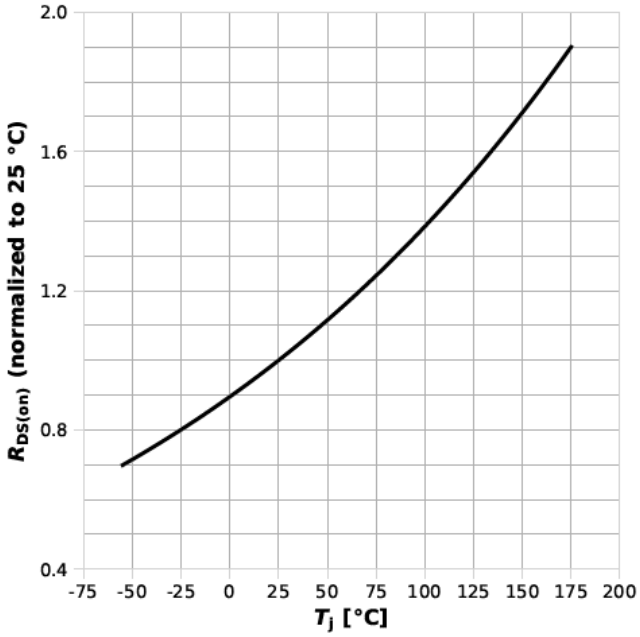
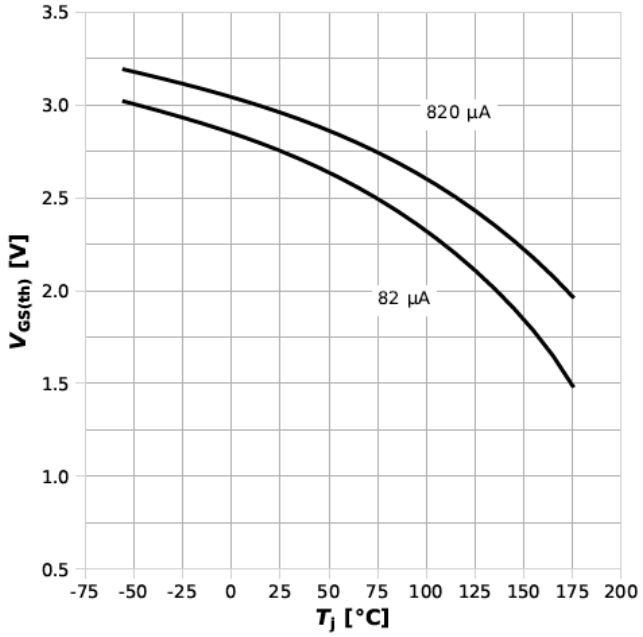
Diagram 7: Typ. transfer characteristics	Diagram 8: Typ. drain-source on resistance
	
$I_D=f(V_{GS})$, $\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$; parameter: T_j	$R_{DS(on)}=f(V_{GS})$, I_D=50 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



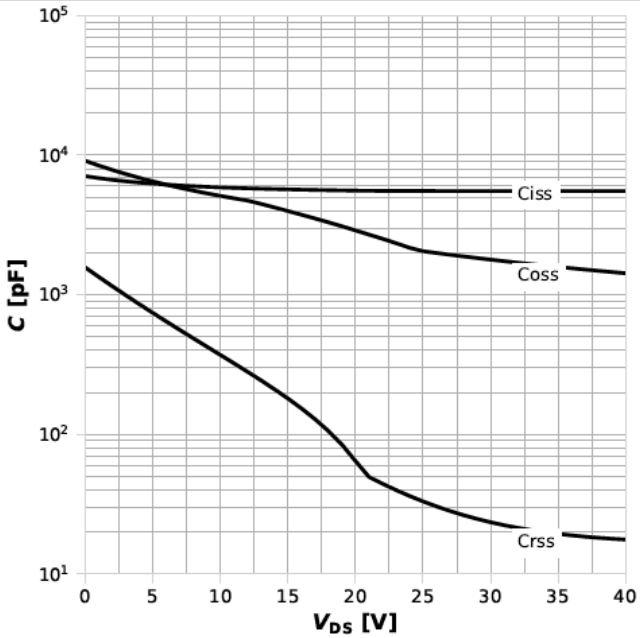
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



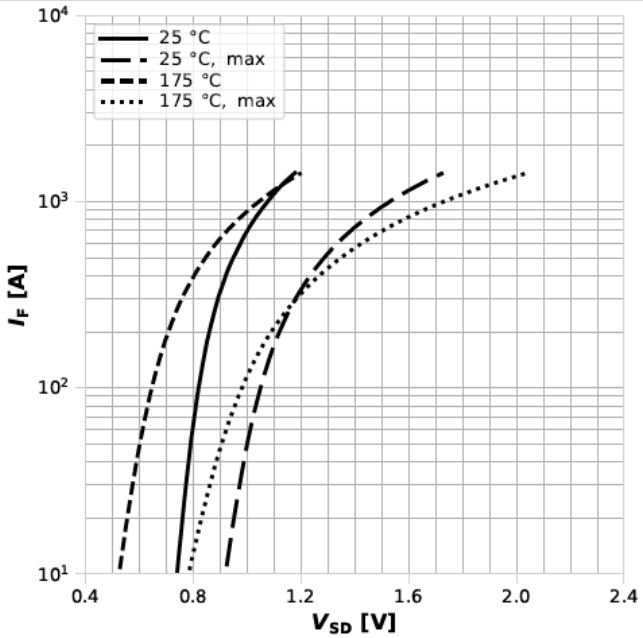
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

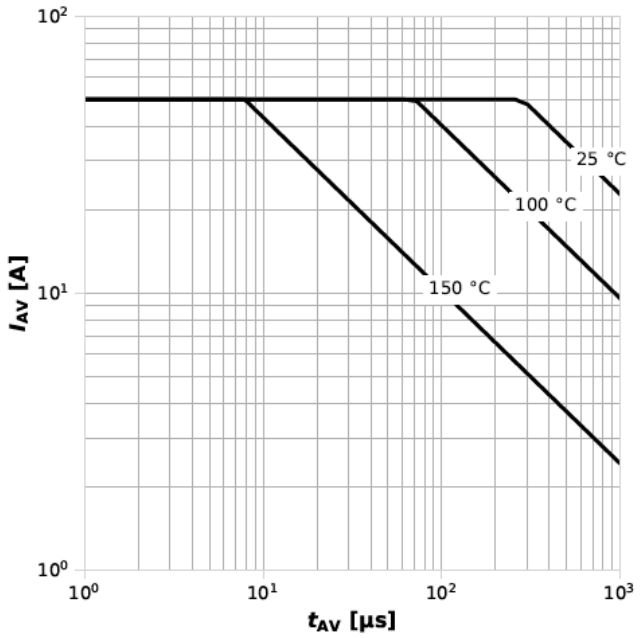
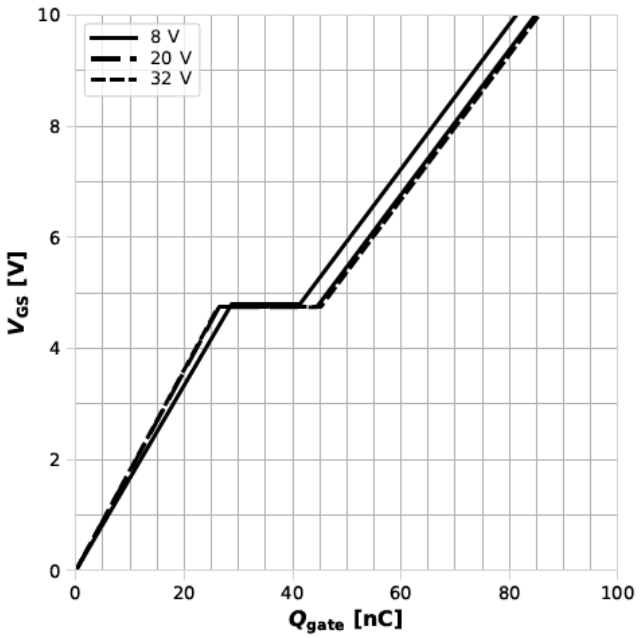
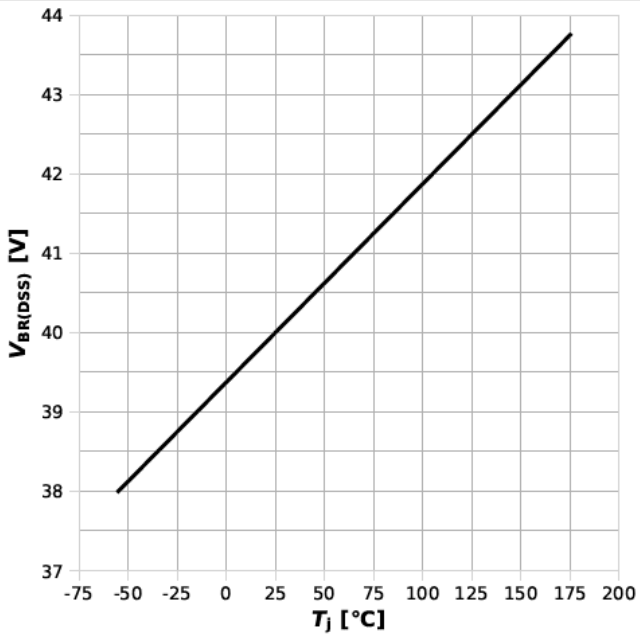
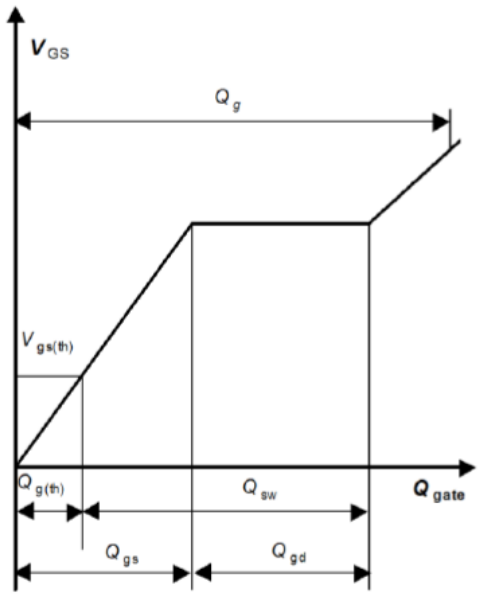
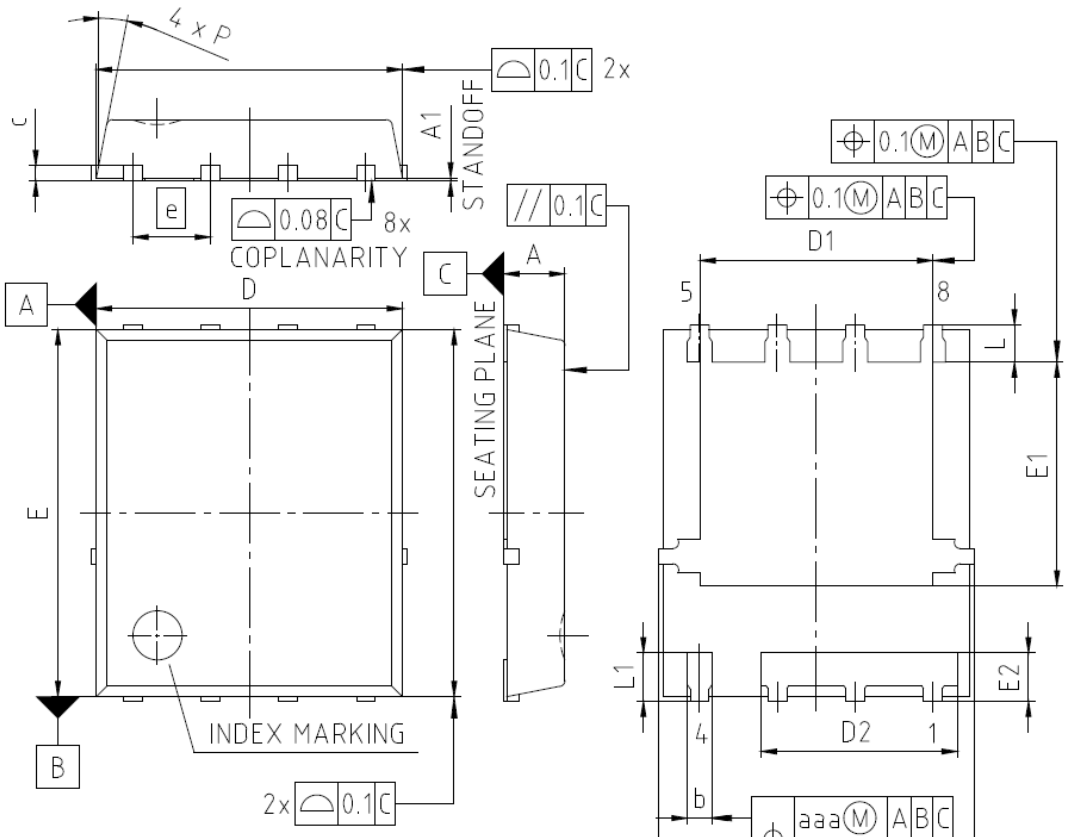
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$	$V_{GS}=f(Q_{gate})$, $I_D=50$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA	-

5 封装外形



PACKAGE - GROUP NUMBER:	PG-TDSON-8-U04	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0	0.05
b	0.26	0.54
c	0.15	0.35
D	4.80	5.35
D1	3.70	4.40
D2	2.94	3.25
D3	4.80	5.15
E	5.70	6.10
E1	3.40	3.76
E2	0.69	0.90
e	1.27	
L	0.45	0.72
L1	0.69	0.90
aaa	0.10	0.25
P	8°	12°

1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
   INTRUSION 0.1 MM
   PROTRUSION 0.1 MM
3) LEAD LENGTH UP TO ANTI FLASH LINE
4) ALL METAL SURFACES ARE PLATED,
   EXCEPT AREA OF CUT

图 1　　PG-TDSON-8 封装外形，尺寸单位为毫米

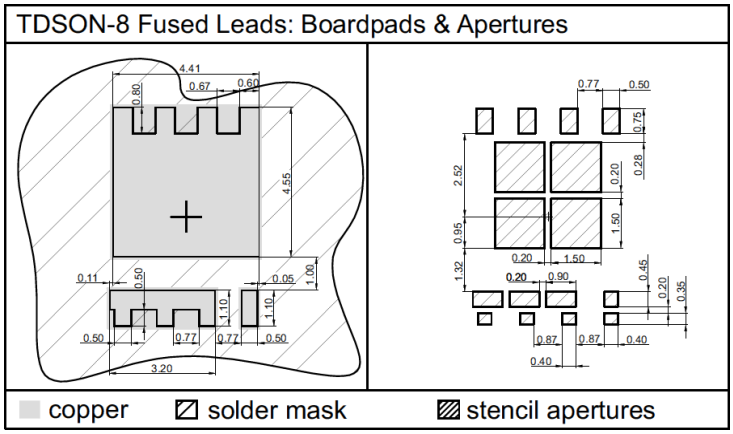


图 2　　PG-TDSON-8 封装图，尺寸单位为毫米

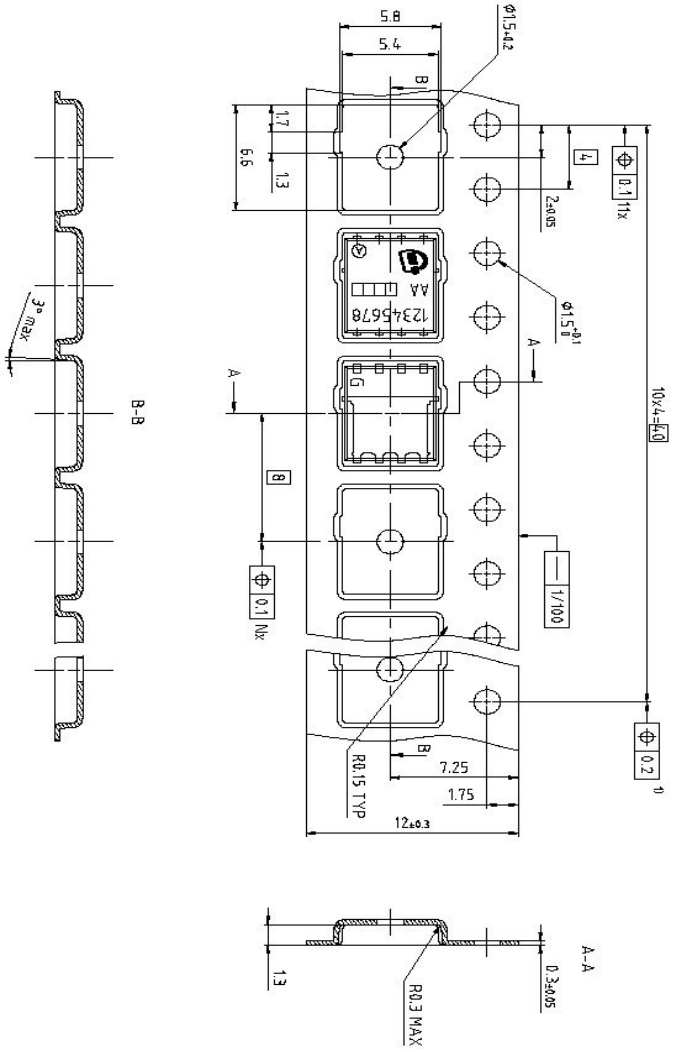


图 3　　PG-TDSON-8 封装变体，尺寸单位为毫米

修订记录

ISCH69N04NM7V

Revision 2025-05-05, Rev. 1. 1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-04-22	Release of final version
1.1	2025-05-05	Update threshold voltage range

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