

## MOSFET

### OptiMOS™ 8 Power-Transistor, 100 V

#### Features

- N-channel, normal level
- Very low on-resistance  $R_{DS(on)}$
- High  $I_D$  current rating
- Tight  $V_{GS(th)}$  spread
- Soft body diode recovery and low  $Q_{rr}$
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020

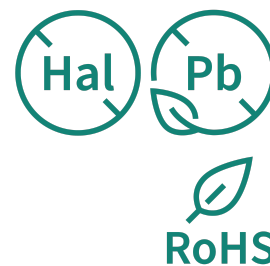
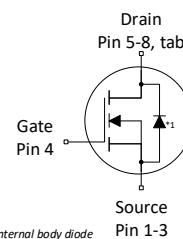
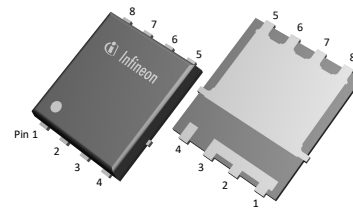
#### Product validation

Qualified according to relevant JEDEC tests.

**Table 1** Key performance parameters

Parameter	Value	Unit
$V_{DS}$	100	V
$R_{DS(on),max}$	3.33	mΩ
$I_D$	150	A
$Q_{oss}$	114	nC
$Q_G$ (0 V...10 V)	59	nC
$Q_{rr}$ (100 A/μs)	41	nC

PG-TDSON-8



Part number	Package	Marking	Related links
ISC033N10NM8	PG-TDSON-8	033N10N8	-



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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	150	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$
				106		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$
				108		$V_{GS}=15\text{ V}, T_C=100\text{ °C}$
				20		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{THJA}=50\text{ °C/W}^2)$
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	600	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	240	mJ	$I_D=25\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	179	W	$T_C=25\text{ °C}$
				3.0		$T_A=25\text{ °C}, R_{THJA}=50\text{ °C/W}^2)$
Operating and storage temperature	$T_j, T_{stg}$	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 14 for more detailed information

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$		0.56	0.84	°C/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	20		
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>5)</sup>	$R_{thJA}$		-	50		

<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.4	2.8	3.2	V	$V_{DS}=V_{GS}$ , $I_D=63\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1	1	$\mu\text{A}$	$V_{DS}=80\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$
Zero gate voltage drain current <sup>6)</sup>	$I_{DSS}$	-	10	100	$\mu\text{A}$	$V_{DS}=80\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.78	3.33	m $\Omega$	$V_{GS}=15\text{ V}$ , $I_D=25\text{ A}$
			2.97	3.43		$V_{GS}=10\text{ V}$ , $I_D=25\text{ A}$
			3.22	3.75		$V_{GS}=8\text{ V}$ , $I_D=12.5\text{ A}$
Gate resistance <sup>6)</sup>	$R_G$	-	0.8	1.6	$\Omega$	-
Transconductance <sup>6)</sup>	$g_{fs}$	40	80	-	S	$ V_{DS} \geq 2 I_D $ , $R_{DS(on)max}$ , $I_D=25\text{ A}$

<sup>6)</sup> Defined by design. Not subject to production test.

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance <sup>7)</sup>	$C_{iss}$	-	3800	4900	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>7)</sup>	$C_{oss}$		560	730		
Reverse transfer capacitance <sup>7)</sup>	$C_{rss}$		110	190		
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=12.5\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$		2.7			
Turn-off delay time	$t_{d(off)}$		29			
Fall time	$t_f$		13			

<sup>7)</sup> Defined by design. Not subject to production test.

**Table 6 Gate charge characteristics** <sup>8)</sup>

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	16	-	nC	$V_{DD}=50\text{ V}$ , $I_D=12.5\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	11	-	nC	
Gate to drain charge <sup>9)</sup>	$Q_{gd}$	-	15	23	nC	
Switching charge	$Q_{sw}$	-	20	-	nC	
Gate charge total <sup>9)</sup>	$Q_g$	-	59	74	nC	
Gate plateau voltage	$V_{plateau}$	-	4.2	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	49	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>9)</sup>	$Q_{oss}$	-	114	152	nC	$V_{DS}=50\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>8)</sup> See "Gate charge waveforms" for parameter definition

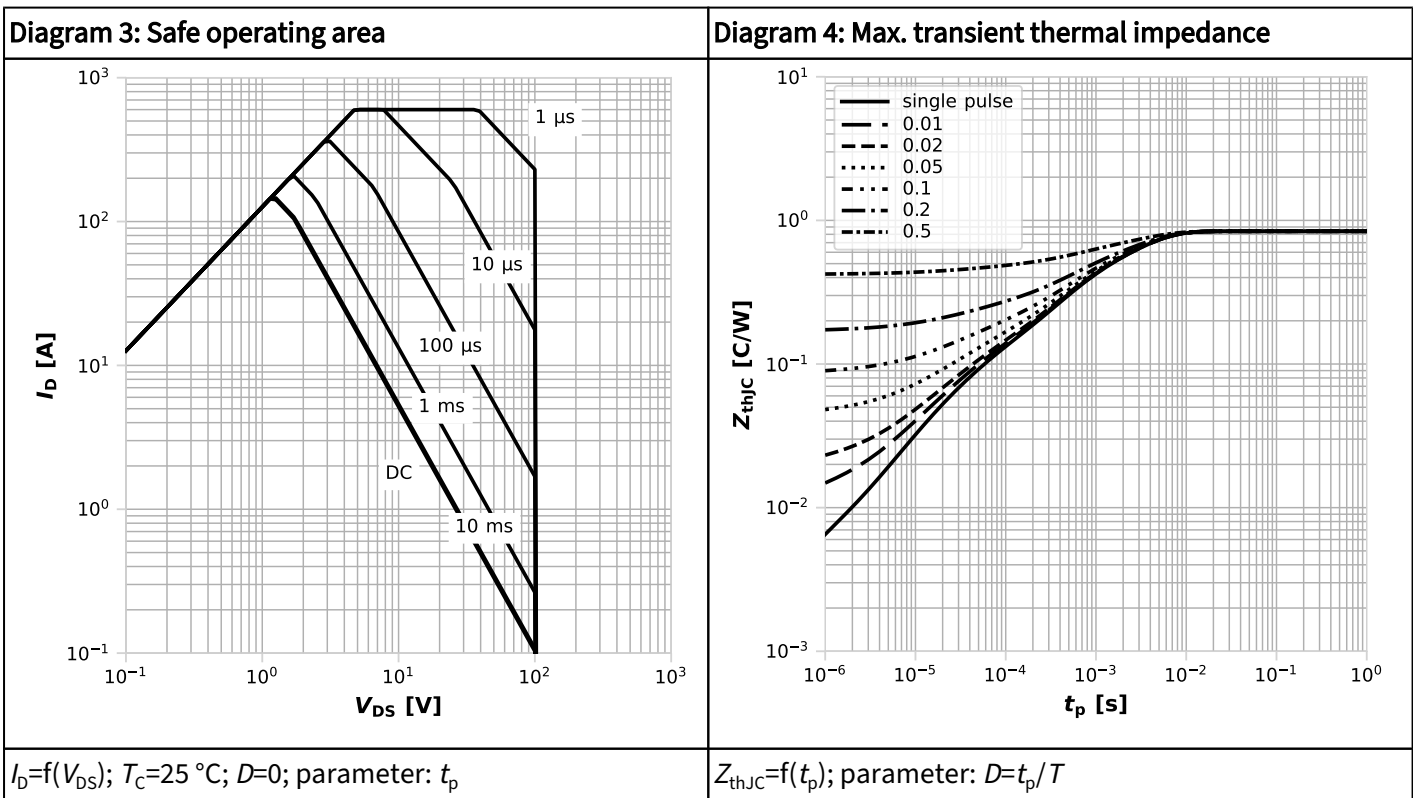
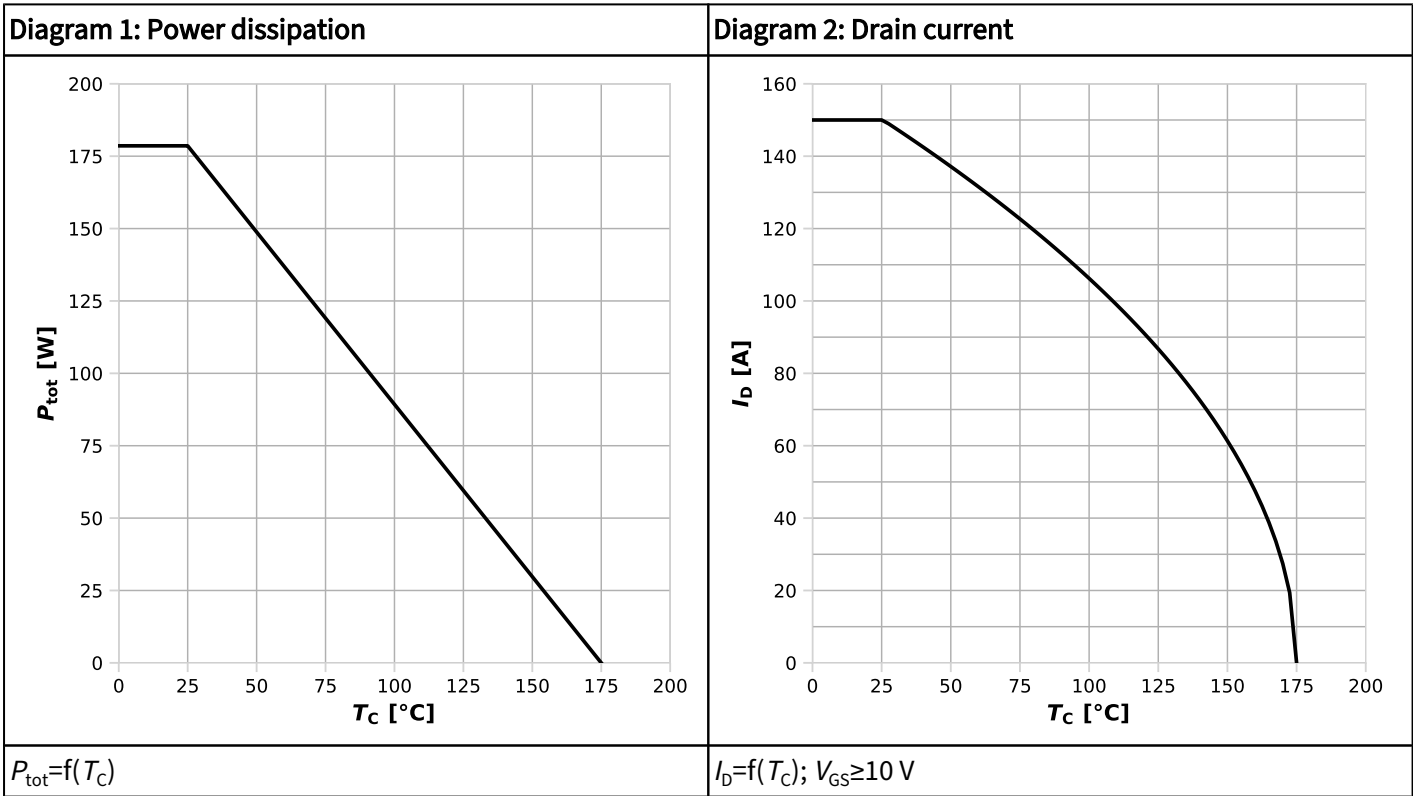
<sup>9)</sup> Defined by design. Not subject to production test.

**Table 7 Reverse diode**

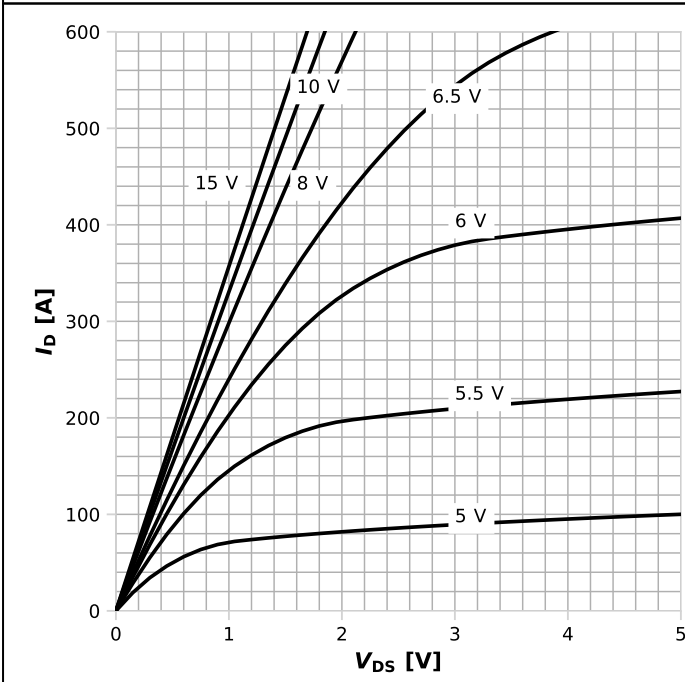
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	146	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	600		
Diode forward voltage	$V_{SD}$	-	0.82	1	V	$V_{GS}=0\text{ V}$ , $I_F=25\text{ A}$ , $T_j=25\text{ °C}$
Reverse recovery time <sup>10)</sup>	$t_{rr}$	-	31	63	ns	$V_R=50\text{ V}$ , $I_F=12.5\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>10)</sup>	$Q_{rr}$	-	41	81	nC	
Reverse recovery time <sup>10)</sup>	$t_{rr}$	-	26	52	ns	$V_R=50\text{ V}$ , $I_F=12.5\text{ A}$ , $di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>10)</sup>	$Q_{rr}$	-	256	511	nC	

<sup>10)</sup> Defined by design. Not subject to production test.

### 4 Electrical characteristics diagrams

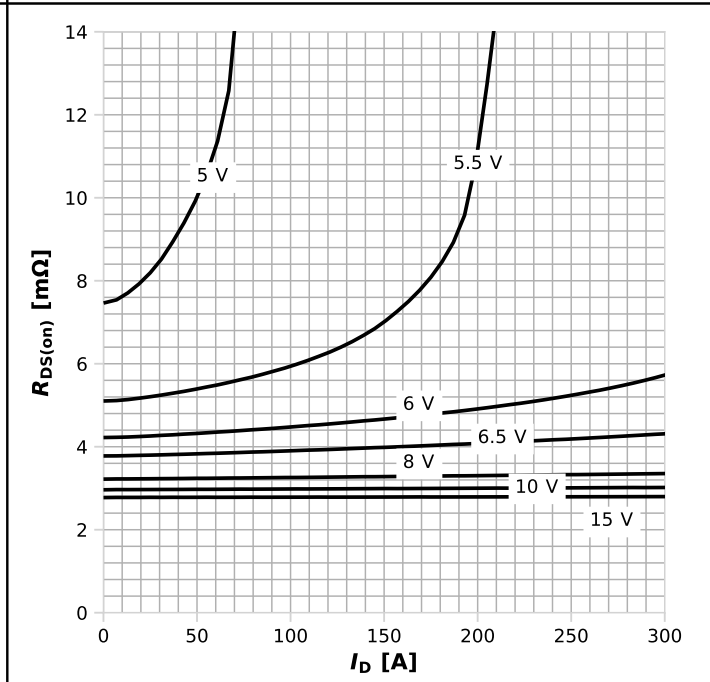


**Diagram 5: Typ. output characteristics**



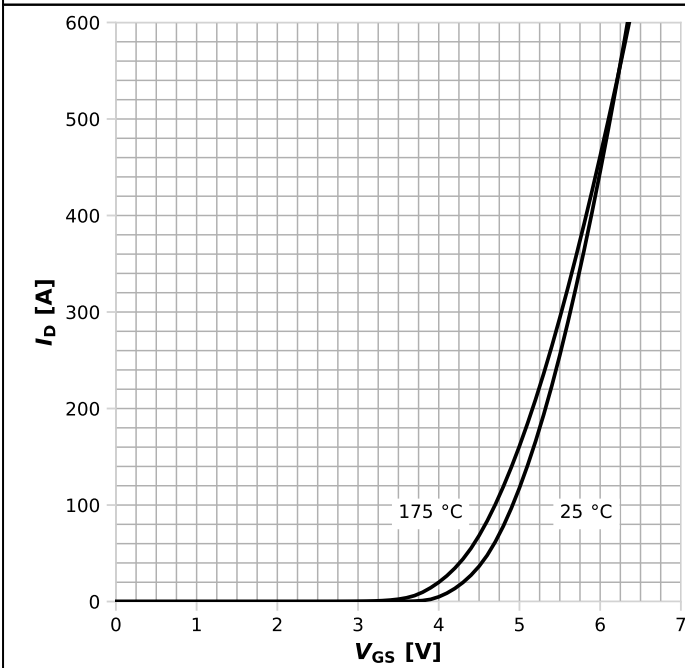
$I_D = f(V_{DS}), T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



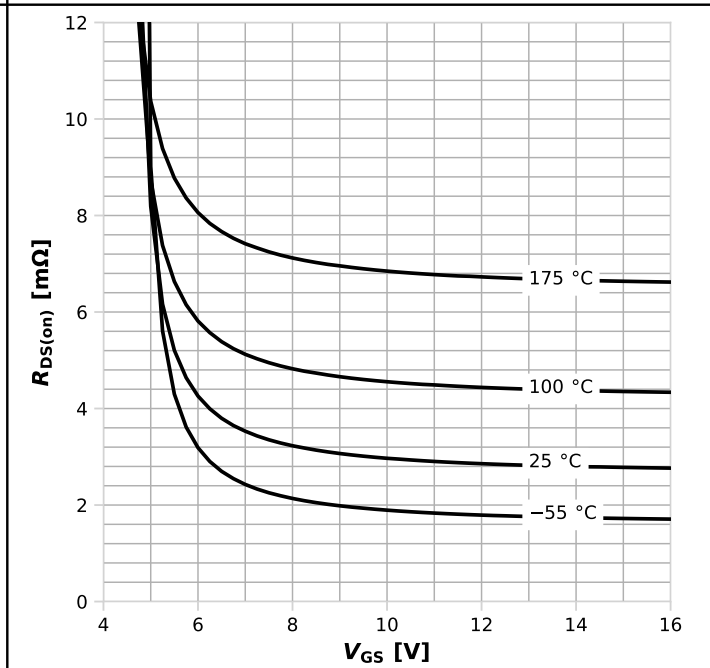
$R_{DS(on)} = f(I_D), T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



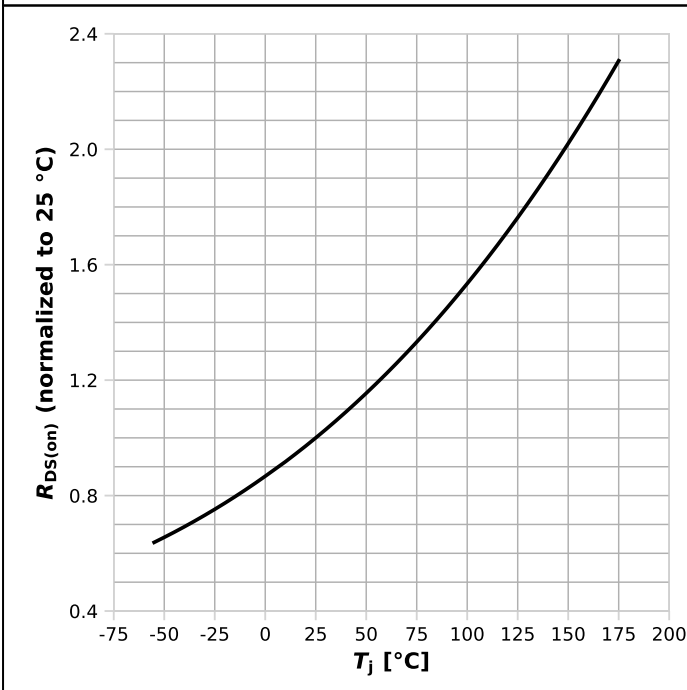
$I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)max};$  parameter:  $T_j$

**Diagram 8: Typ. drain-source on resistance**



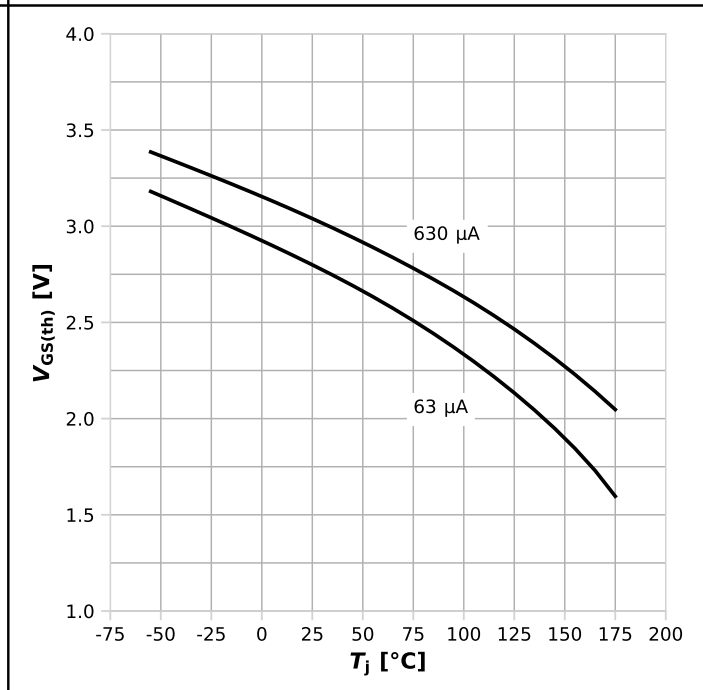
$R_{DS(on)} = f(V_{GS}), I_D = 25\text{ A};$  parameter:  $T_j$

**Diagram 9: Normalized drain-source on resistance**



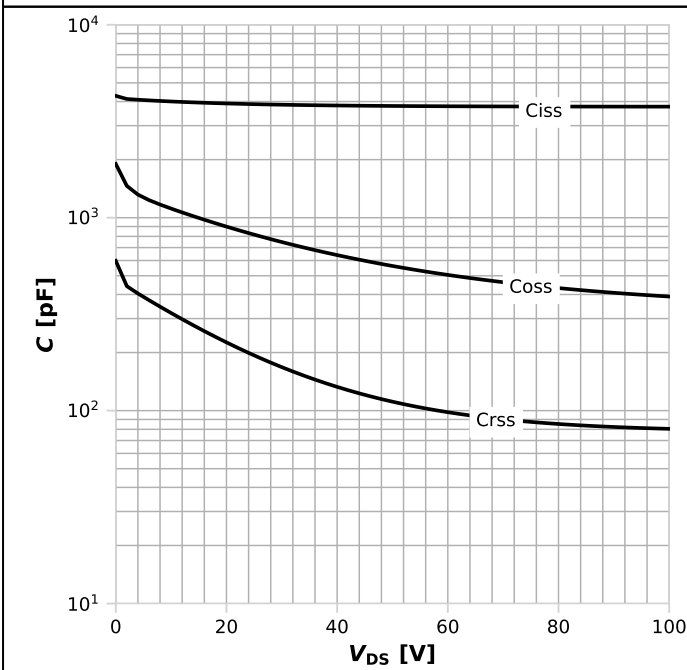
$R_{DS(on)}=f(T_j), I_D=25\text{ A}, V_{GS}=10\text{ V}$

**Diagram 10: Typ. gate threshold voltage**



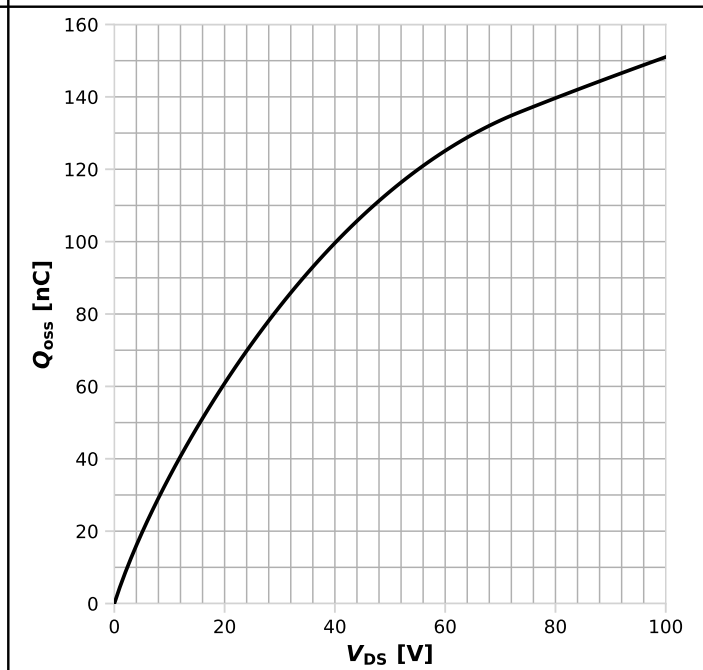
$V_{GS(th)}=f(T_j), V_{GS}=V_{DS}; \text{parameter: } I_D$

**Diagram 11: Typ. capacitances**



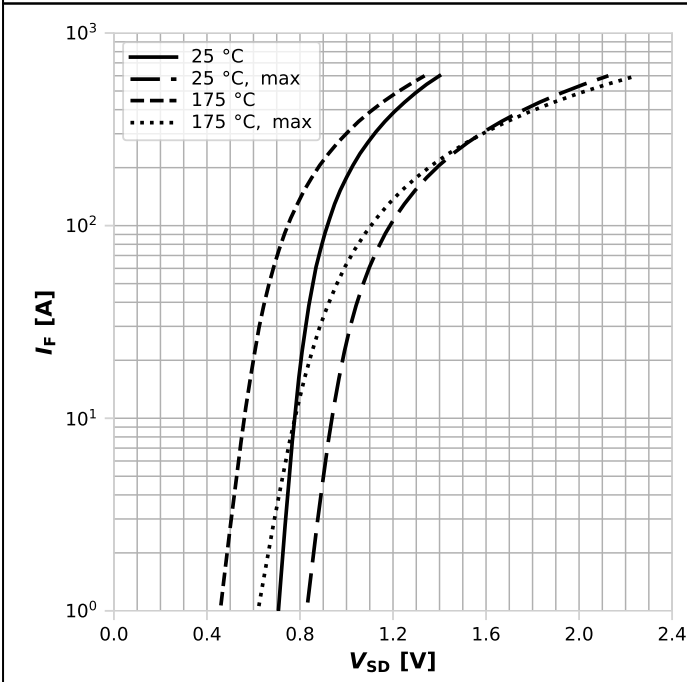
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

**Diagram 12: Typ. output charge**



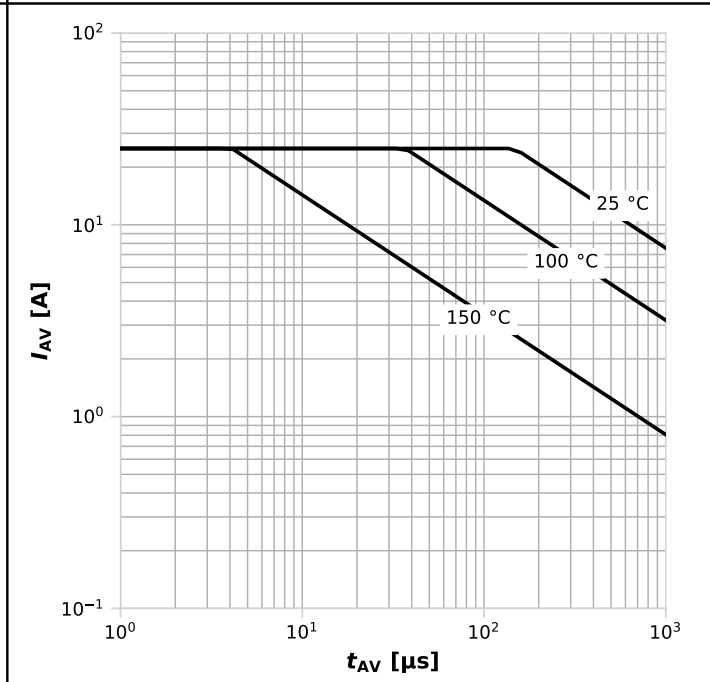
$Q_{oss}=f(V_{DS}), V_{GS}=0\text{ V}$

Diagram 13: Forward characteristics of reverse diode



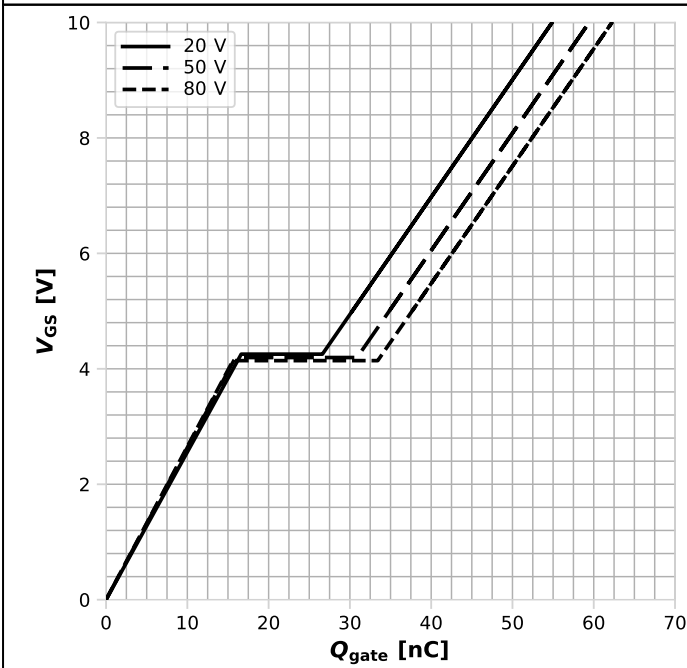
$I_F=f(V_{SD})$ ; parameter:  $T_j$

Diagram 14: Avalanche characteristics



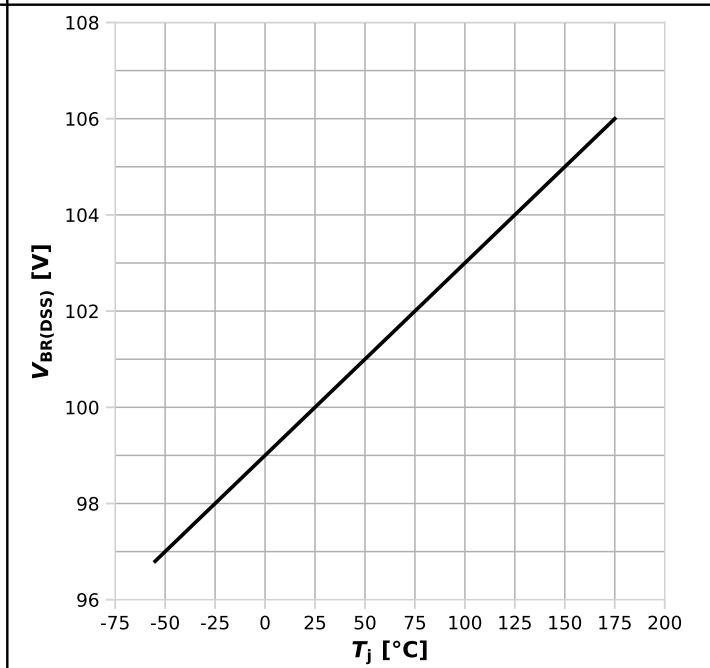
$I_{AS}=f(t_{AV})$ ;  $R_{GS}=25 \Omega$ ; parameter:  $T_{j,start}$

Diagram 15: Typ. gate charge

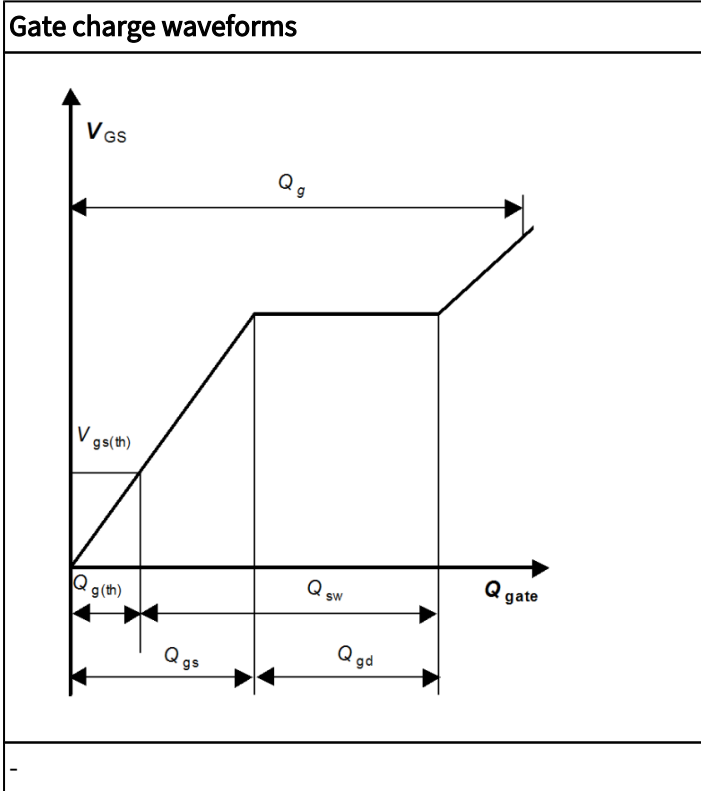


$V_{GS}=f(Q_{gate})$ ,  $I_D=12.5 \text{ A}$  pulsed,  $T_j=25 \text{ °C}$ ; parameter:  $V_{DD}$

Diagram 16: Min. drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$ ;  $I_D=1 \text{ mA}$



## 5 Package outlines

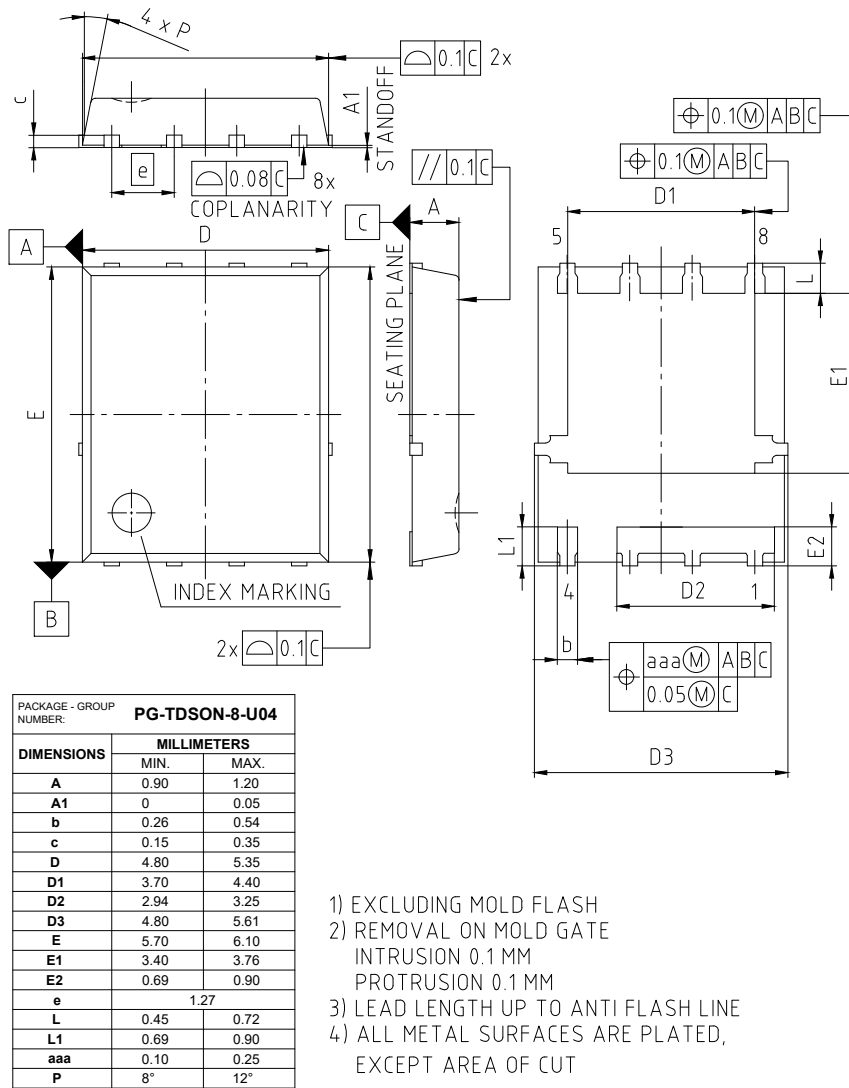


Figure 1 Outline PG-TDSON-8, dimensions in mm

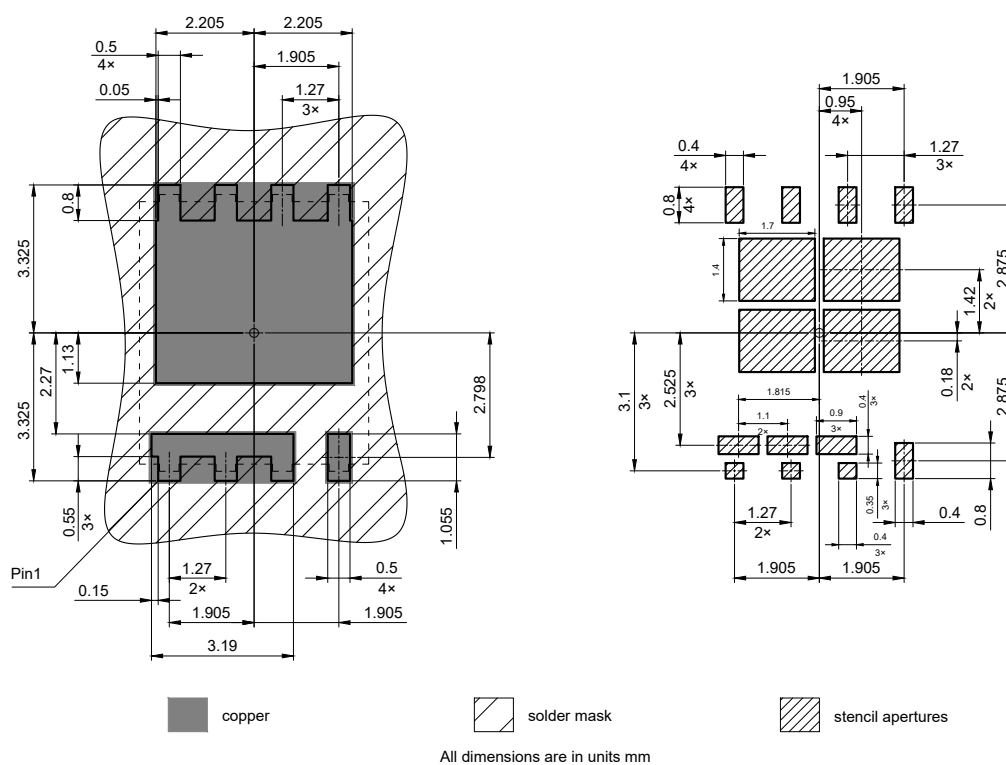


Figure 2 Footprint drawing PG-TDSON-8, dimensions in mm

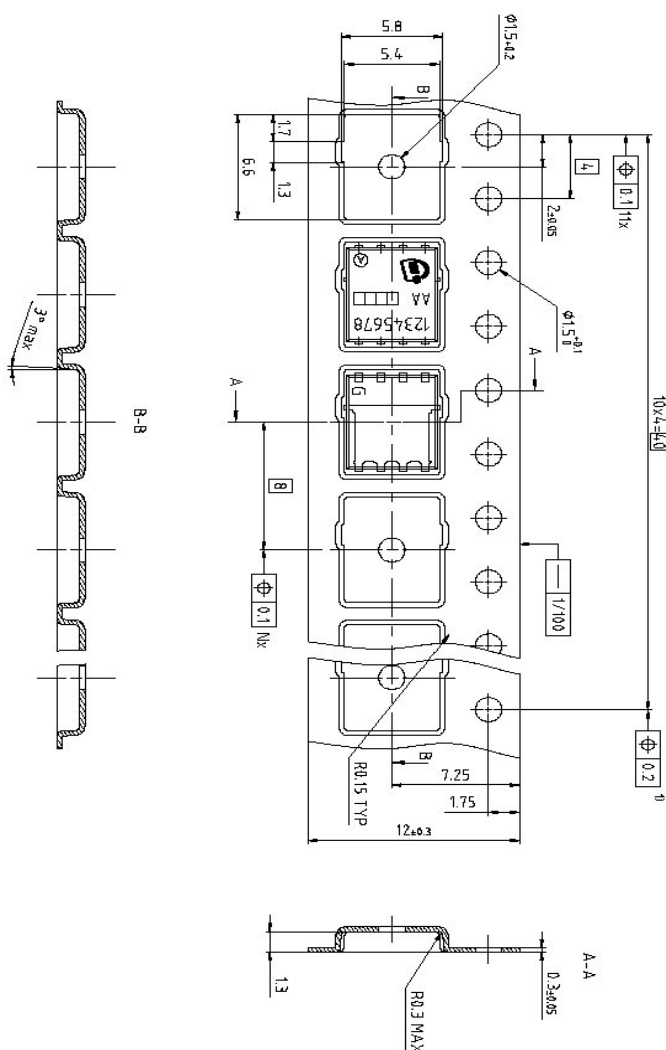


Figure 3 Packaging variant PG-TDSON-8, dimensions in mm



### Revision history

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ISC033N10NM8

#### Revision 2025-12-10, Rev. 1.1

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Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-11-24	Release of final version
1.1	2025-12-10	Added footnote to Gate resistance

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