

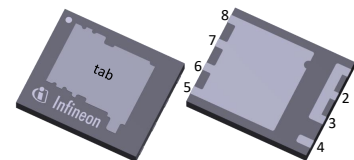
MOSFET

OptiMOS™ 6 Power-MOSFET, 80 V

Features

- Dual-side cooled package with lowest Junction-top thermal resistance
- N-channel, normal level
- Optimized for high performance SMPS
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- 100% avalanche tested
- 175°C operating temperature
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

PG-WSON-8

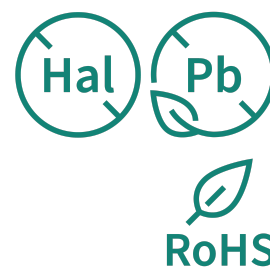
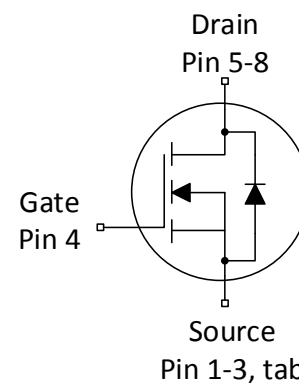


Product validation

Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on),max}$	2.5	mΩ
I_D	170	A
Q_{oss}	91	nC
Q_G (0V..10V)	46	nC
Q_{rr} (100A/μs)	72	nC



Part number	Package	Marking	Related links
ISC025N08NM6SC	PG-WSON-8	025N08SC	-



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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	170	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$
				120		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$
				108		$V_{GS}=8\text{ V}, T_C=100\text{ °C}$
				23		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{THJA}=50\text{ °C/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	680	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	219	mJ	$I_D=50\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	167	W	$T_C=25\text{ °C}$
				3.0		$T_A=25\text{ °C}, R_{THJA}=50\text{ °C/W}^2)$
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information.

⁴⁾ See Diagram 13 for more detailed information.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.45	0.90	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}		0.43	0.86		
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}		-	50		

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.4	3.0	3.5	V	$V_{DS}=V_{GS}$, $I_D=81\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1	1	μA	$V_{DS}=64\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
Zero gate voltage drain current ⁶⁾	I_{DSS}	-	10	100	μA	$V_{DS}=64\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.1	2.5	m Ω	$V_{GS}=10\text{ V}$, $I_D=50\text{ A}$
			2.6	3.15		$V_{GS}=8\text{ V}$, $I_D=25\text{ A}$
Gate resistance ⁶⁾	R_G	0.45	0.65	0.95	Ω	-
Transconductance ⁶⁾	g_{fs}	40	95	-	S	$ V_{DS} \geq 2 I_D $, $R_{DS(on)max}$, $I_D=50\text{ A}$

⁶⁾ Defined by design.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance ⁷⁾	C_{iss}	-	3300	4000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁷⁾	C_{oss}		1100	1380		
Reverse transfer capacitance ⁷⁾	C_{rss}		28	39		
Turn-on delay time	$t_{d(on)}$	-	15	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=25\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r		8.6			
Turn-off delay time	$t_{d(off)}$		22			
Fall time	t_f		5.3			

⁷⁾ Defined by design.

Table 6 Gate charge characteristics ⁸⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge ⁹⁾	Q_{gs}	-	16	19	nC	$V_{DD}=40\text{ V}$, $I_D=25\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold ⁹⁾	$Q_{g(th)}$	-	9.8	11.8	nC	
Gate to drain charge ⁹⁾	Q_{gd}	-	9.3	13	nC	
Switching charge	Q_{sw}	-	16	-	nC	
Gate charge total ⁹⁾	Q_g	-	46	55	nC	
Gate plateau voltage	$V_{plateau}$	-	4.9	-	V	
Output charge ⁹⁾	Q_{oss}	-	91	114	nC	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$

⁸⁾ See figure 16 for gate charge parameter definition.

⁹⁾ Defined by design.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current ¹⁰⁾	I_S	-	-	155	A	$T_C=25\text{ °C}$
Diode pulse current ¹⁰⁾	$I_{S,pulse}$	-	-	680	A	
Diode forward voltage	V_{SD}	-	0.81	1.0	V	$V_{GS}=0\text{ V}$, $I_F=50\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time ¹⁰⁾	t_{rr}	-	51	77	ns	$V_R=40\text{ V}$, $I_F=25\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁰⁾	Q_{rr}	-	72	108	nC	
Reverse recovery time ¹⁰⁾	t_{rr}	-	28	42	ns	$V_R=40\text{ V}$, $I_F=25\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁰⁾	Q_{rr}	-	302	453	nC	

¹⁰⁾ Defined by design.

4 Electrical characteristics diagrams

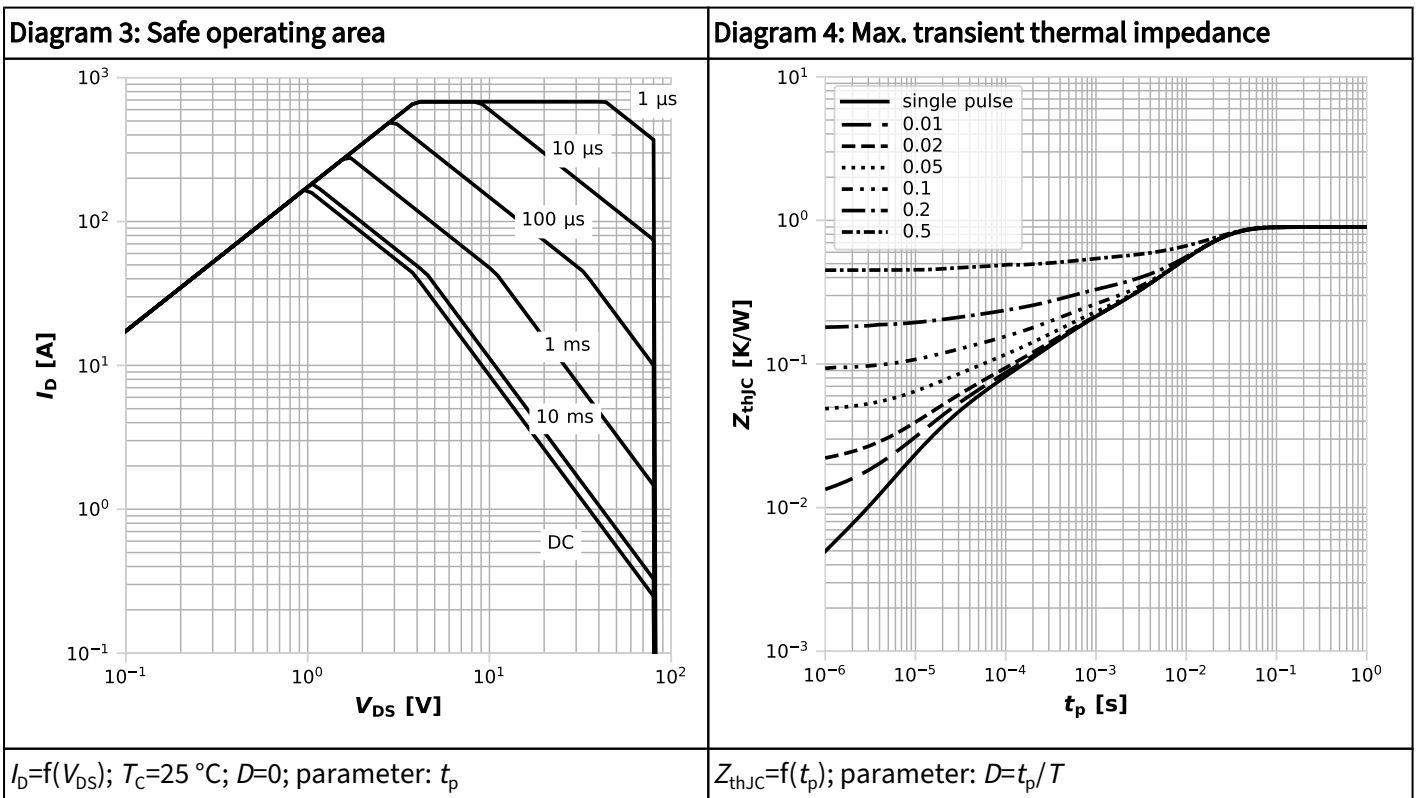
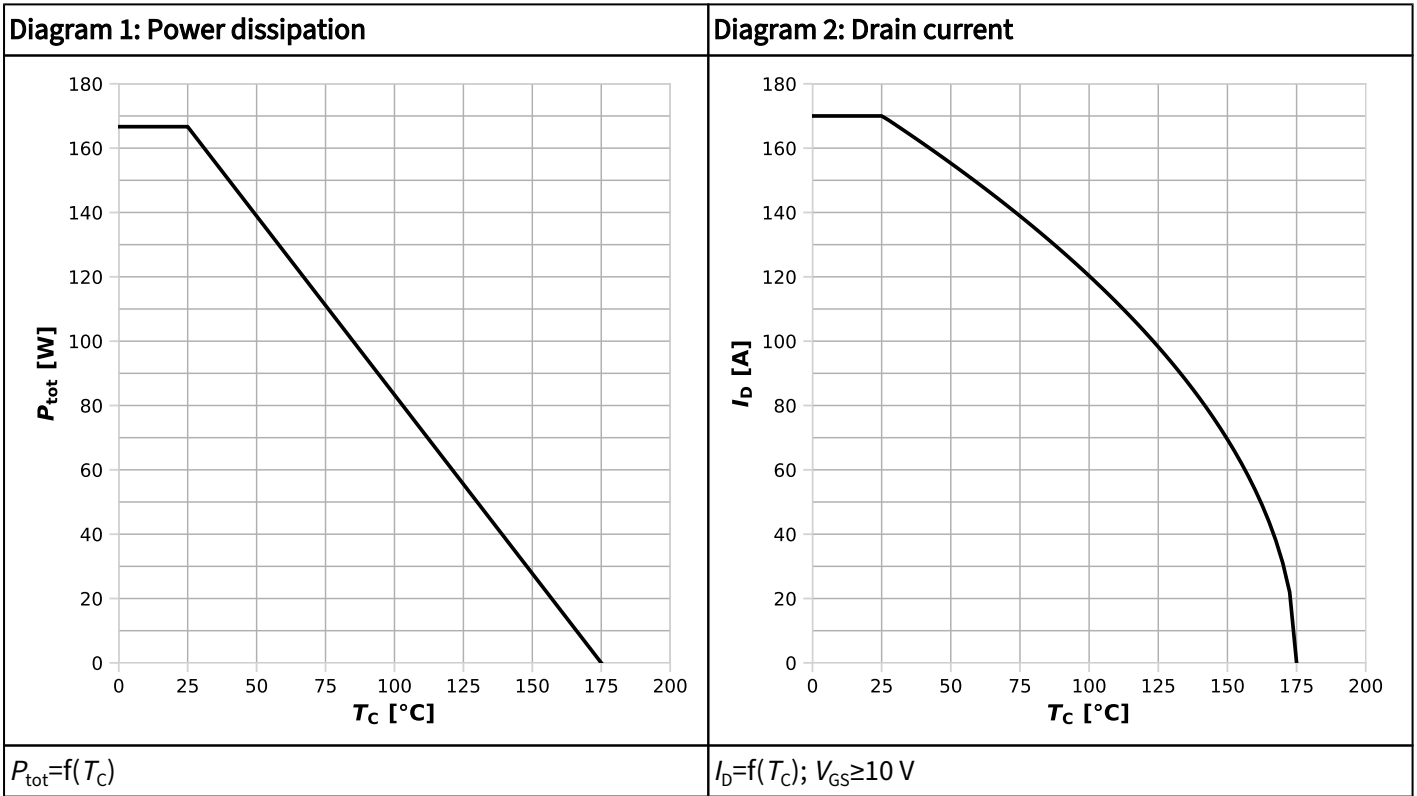
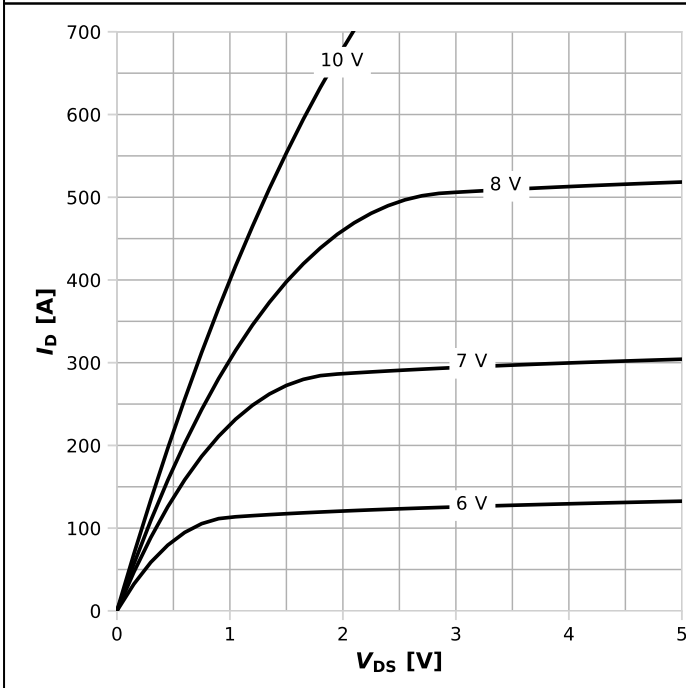
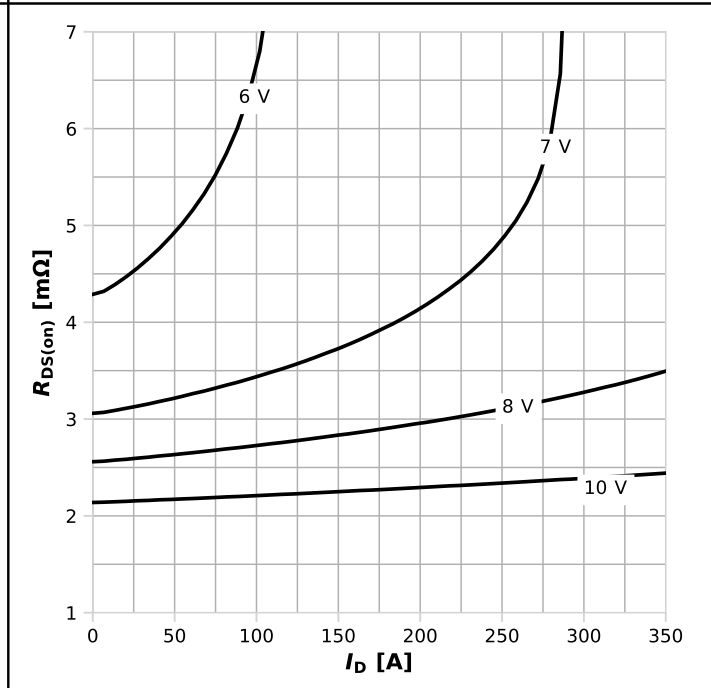


Diagram 5: Typ. output characteristics



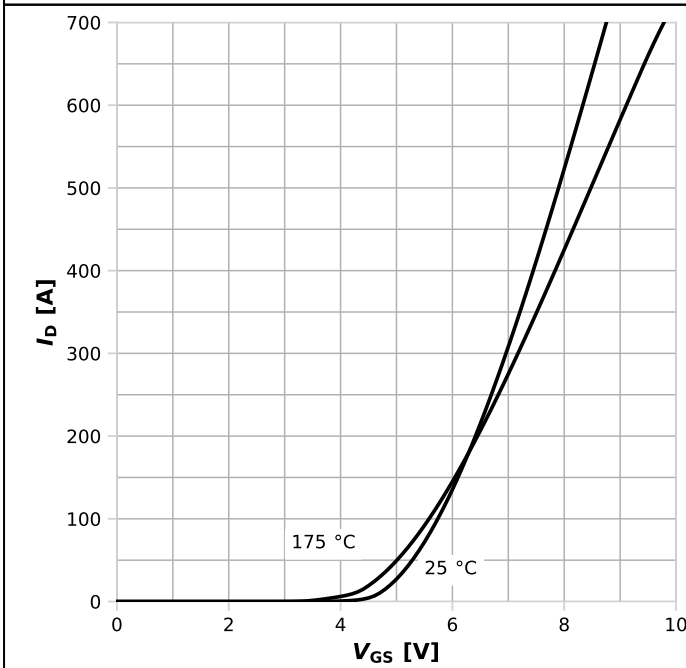
$I_D = f(V_{DS}), T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



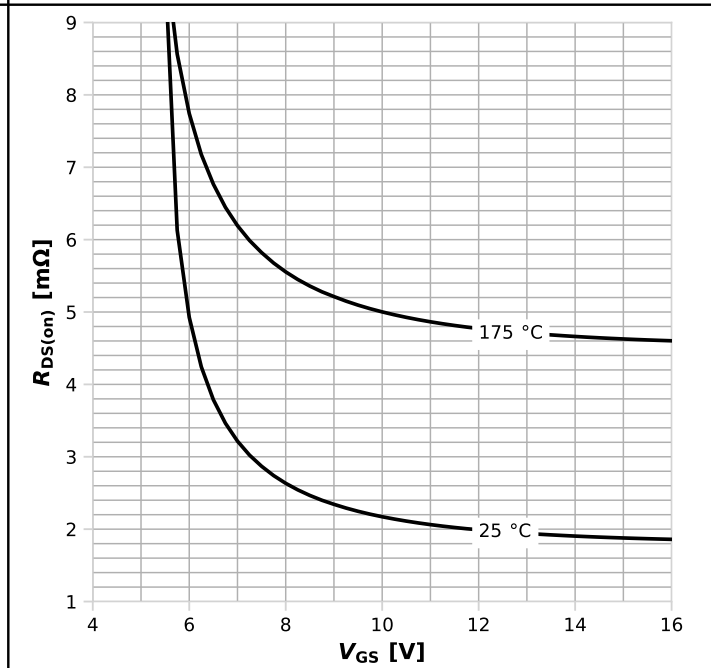
$R_{DS(on)} = f(I_D), T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



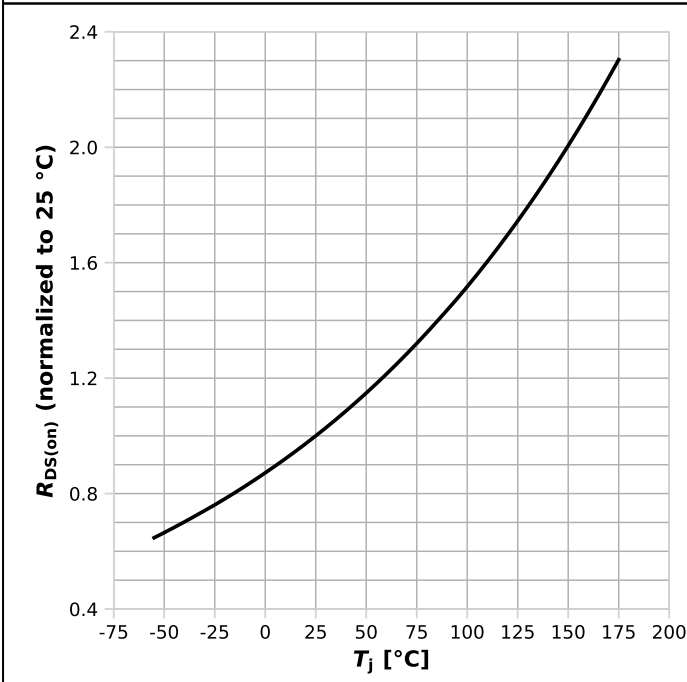
$I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)max};$ parameter: T_j

Diagram 8: Typ. drain-source on resistance



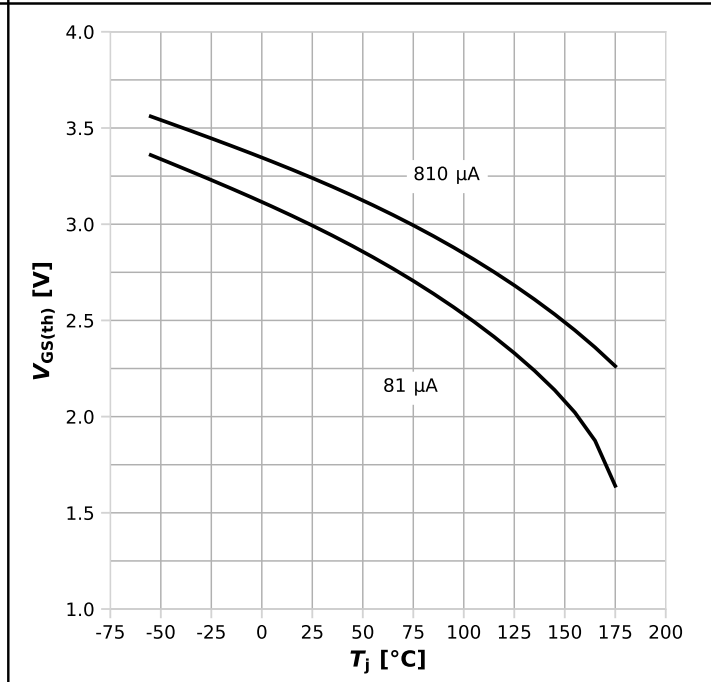
$R_{DS(on)} = f(V_{GS}), I_D = 50\text{ A};$ parameter: T_j

Diagram 9: Normalized drain-source on resistance



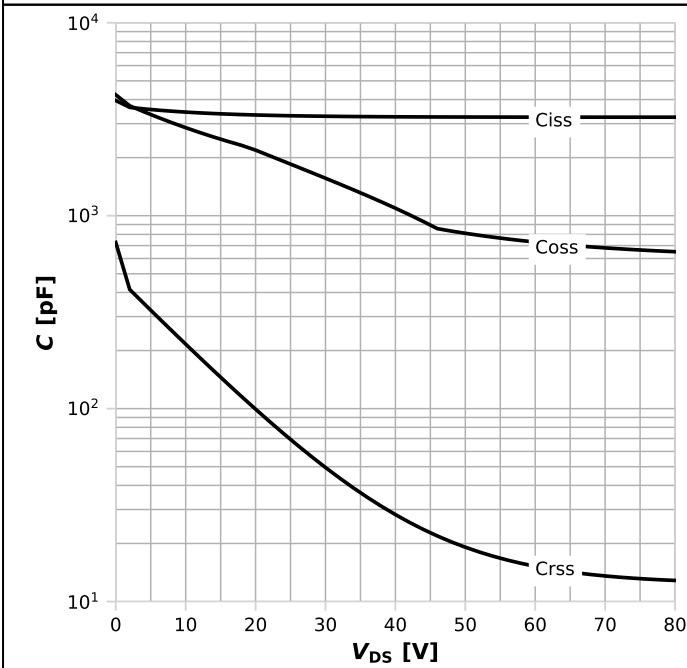
$R_{DS(on)}=f(T_j), I_D=50\text{ A}, V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



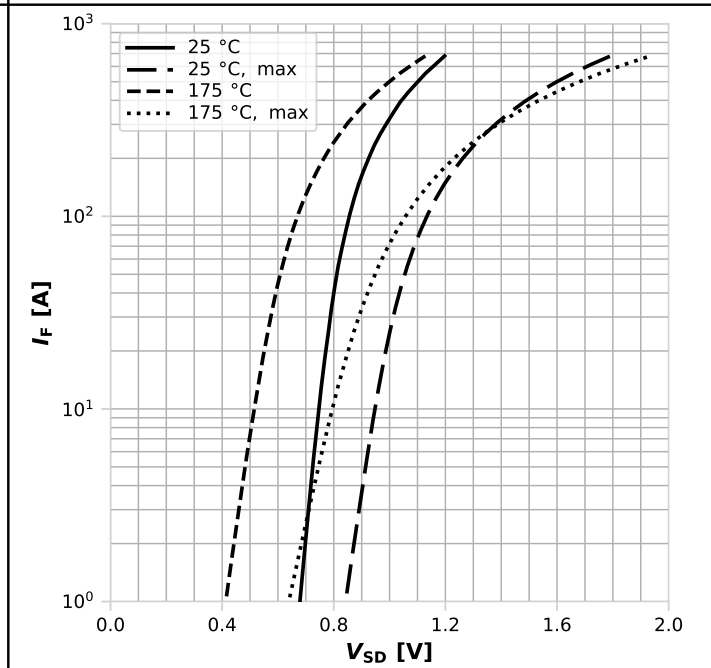
$V_{GS(th)}=f(T_j), V_{GS}=V_{DS};$ parameter: I_D

Diagram 11: Typ. capacitances



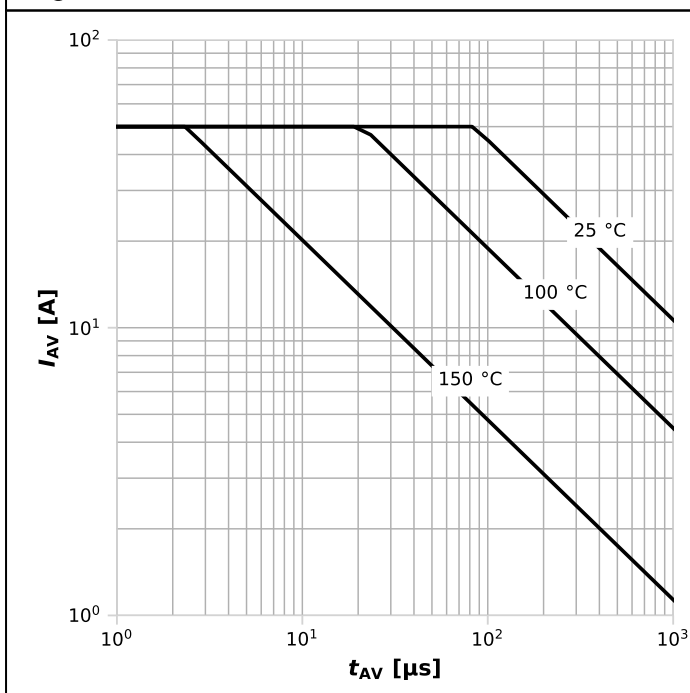
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



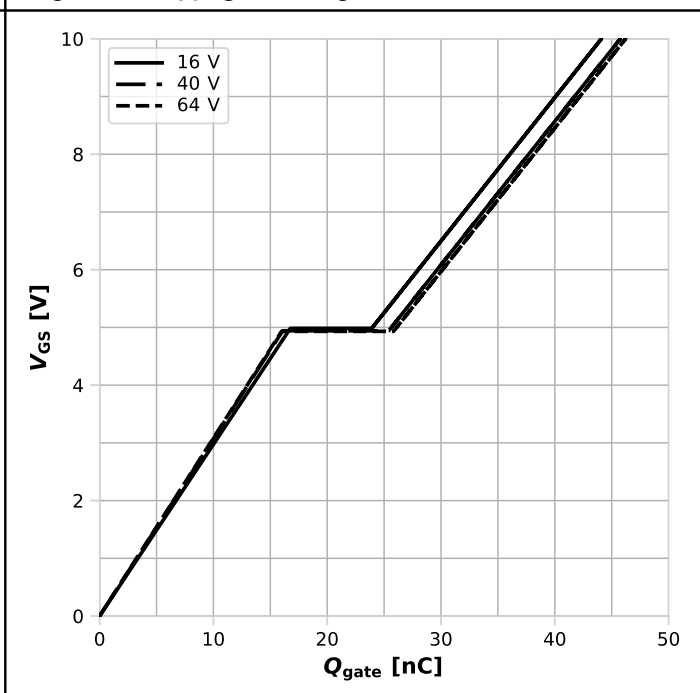
$I_F=f(V_{SD});$ parameter: T_j

Diagram 13: Avalanche characteristics



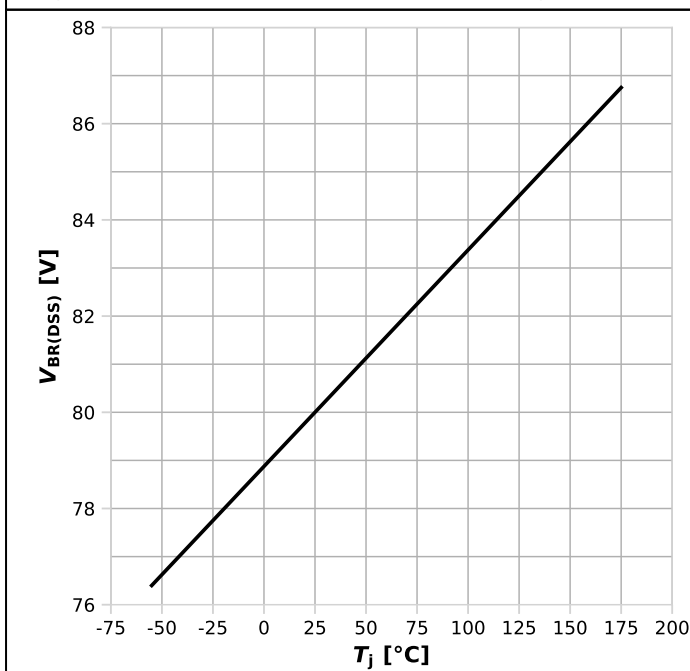
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



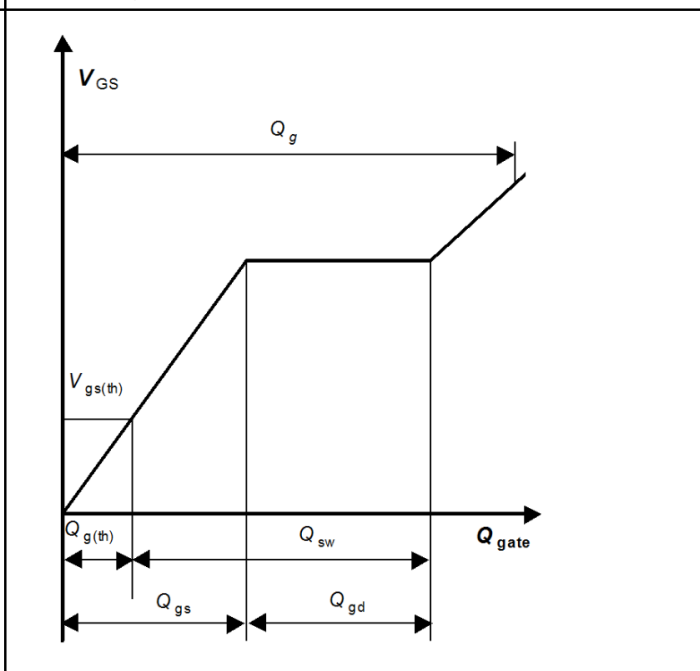
$V_{GS}=f(Q_{gate}), I_D=25 \text{ A pulsed}, T_j=25 \text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

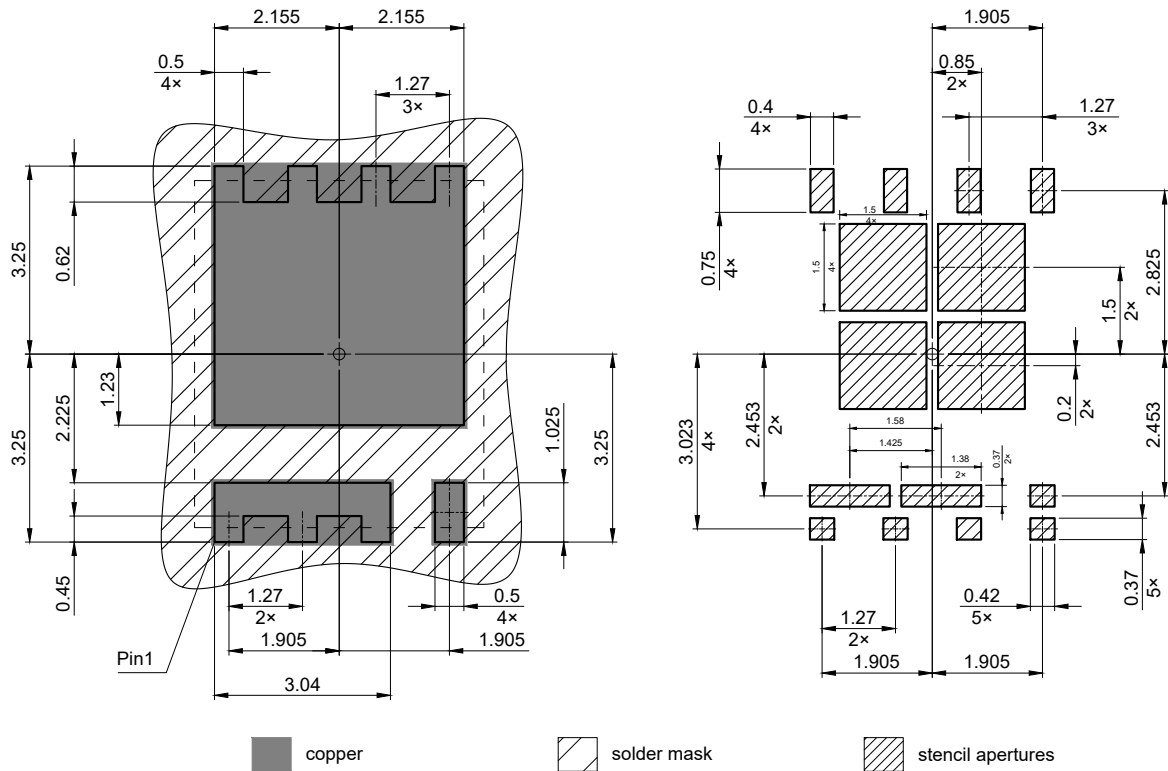


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms

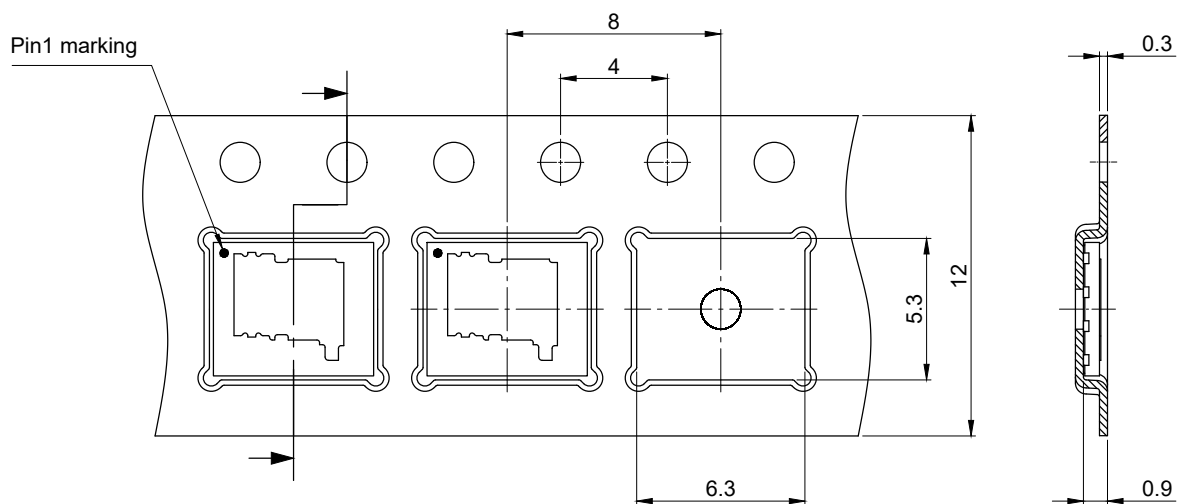


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All dimensions are in units mm

Figure 2 Footprint drawing PG-WSON-8, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant PG-WSON-8, dimensions in mm



Revision history

ISC025N08NM6SC

Revision 2026-03-16, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-03-16	Release of final version

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