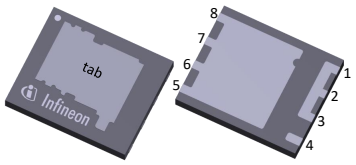
MOSFET

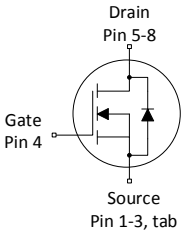
PG-WSON-8

OptiMOS™ 6 Power-Transistor, 80 V



Features

- Dual-side cooled package with lowest Junction-top thermal resistance
- Optimized for high performance SMPS
- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC6129-2-21

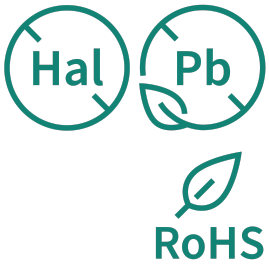


Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on),max}$	1.8	mΩ
I_D	230	A
Q_{oss}	126	nC
Q_G (0V...10V)	63	nC
Q_{rr} (100A/µs)	54	nC



Part number	Package	Marking	Related links
ISC018N08NM6SC	PG-WSON-8	018N08SC	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	230	A	V_{GS}=10 V, T_C=25 °C
				163		V_{GS}=10 V, T_C=100 °C
				138		V_{GS}=8 V, T_C=100 °C
				27		V_{GS}=10 V, T_A=25 °C, R_{THJA}=50 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	920	A	T_C=25 °C
Avalanche current, single pulse [4]	I_{AS}			50		
Avalanche energy, single pulse	E_{AS}	-	-	851	mJ	I_D=24 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	217	W	T_C=25 °C
				3.0		T_A=25 °C, R_{thJA}=50 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.35	0.69	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}		0.36	0.72		
Thermal resistance, junction - ambient, 6 cm² cooling area [5)]	R_{thJA}		-	50		

[5)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.4	3.0	3.5	V	V_{DS}=V_{GS}, I_D=114 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{DS}=64 V, V_{GS}=0 V, T_j=25 °C
			10	100		V_{DS}=64 V, V_{GS}=0 V, T_j=125 °C [6]
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=±20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.5	1.8	mΩ	V_{GS}=10 V, I_D=50 A
			1.8	2.3		V_{GS}=8 V, I_D=25 A
Gate resistance	R_G	0.5	0.77	1.0	Ω	-
Transconductance [6]	g_{fs}	55	110	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=50 A

[6] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [7]	C_{iss}	-	4500	5400	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Output capacitance [7]	C_{oss}		1500	1900		
Reverse transfer capacitance [7]	C_{rss}		37	52		
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=25 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r		6.0			
Turn-off delay time	$t_{d(off)}$		22			
Fall time	t_f		6.5			

[7] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [8]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge [9]	Q_{gs}	-	22	26	nC	V_{DD}=40 V, I_D=25 A, V_{GS}=0 to 10 V
Gate charge at threshold [9]	$Q_{g(th)}$		13.5	16.2	nC	
Gate to drain charge [9]	Q_{gd}		12.7	17.8	nC	
Switching charge	Q_{sw}		21	-	nC	
Gate charge total [9]	Q_g		63	76	nC	
Gate plateau voltage	$V_{plateau}$		4.8	-	V	
Output charge [9]	Q_{oss}	-	126	158	nC	V_{DS}=40 V, V_{GS}=0 V

[8] See "Gate charge waveforms" for parameter definition

[9] Defined by design. Not subject to production test.

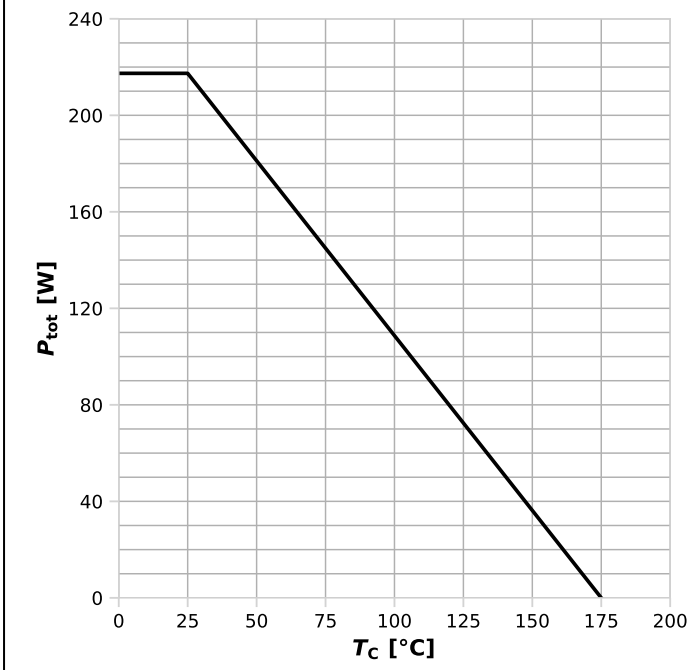
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	197	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			920		
Diode forward voltage	V_{SD}	-	0.80	1.0	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time [10]	t_{rr}	-	45	67.5	ns	V_R=40 V, I_F=25 A, di_F/dt=100 A/µs
Reverse recovery charge [10]	Q_{rr}		54	81	nC	
Reverse recovery time [10]	t_{rr}	-	26	39	ns	V_R=40 V, I_F=25 A, di_F/dt=1000 A/µs
Reverse recovery charge [10]	Q_{rr}		286	429	nC	

[10] Defined by design. Not subject to production test.

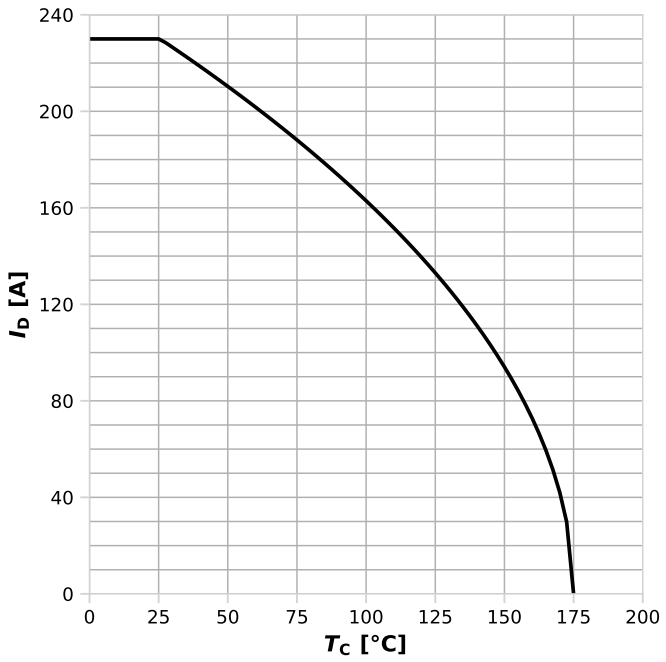
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



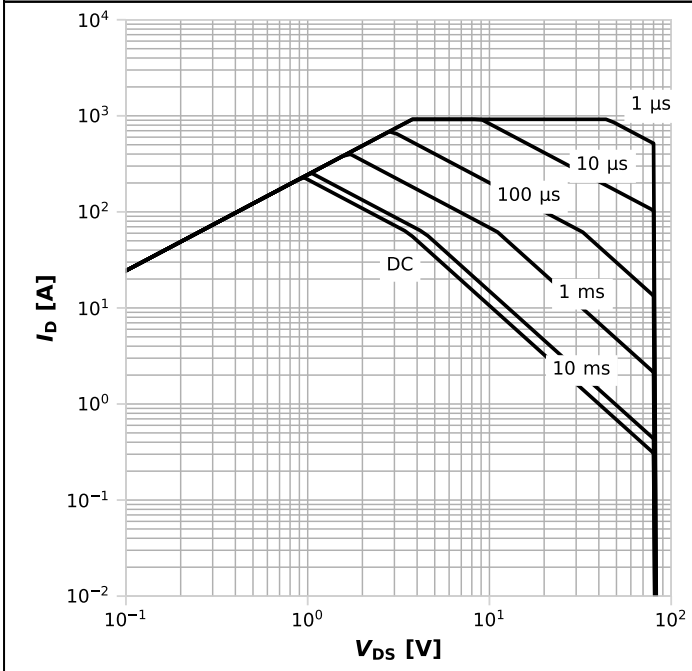
P_{tot}=f(T_C)

Diagram 2: Drain current



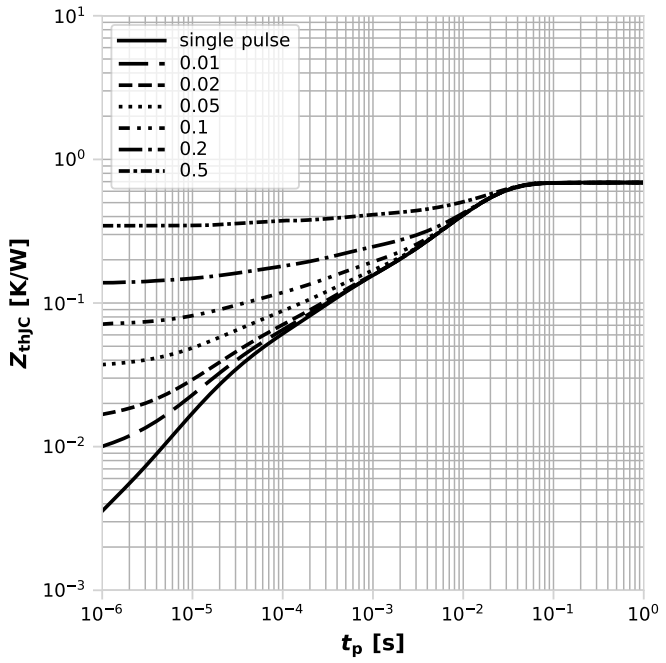
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



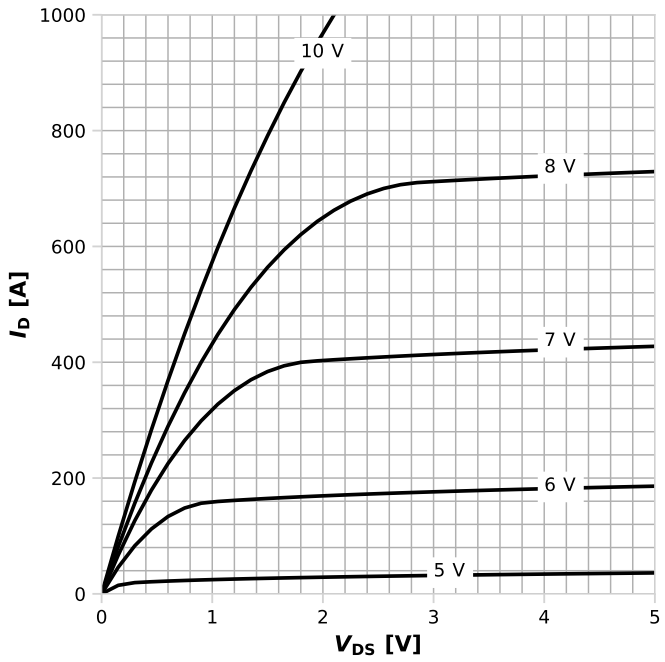
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



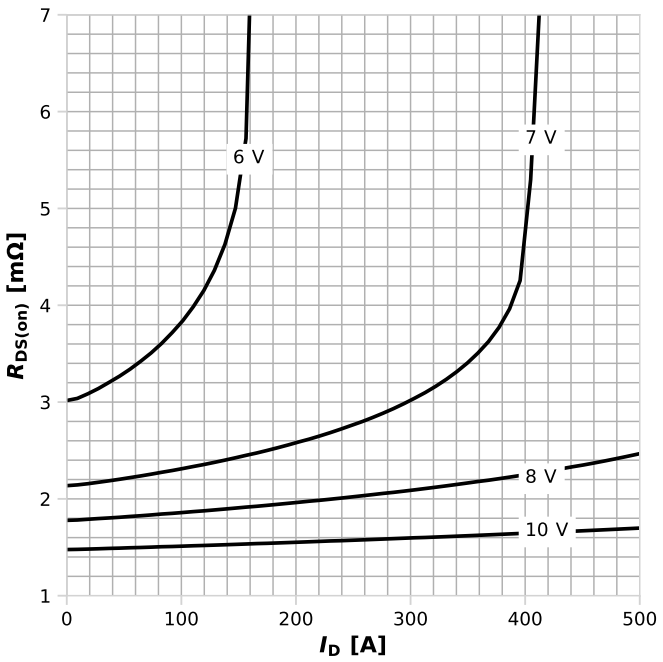
Z_{thJC}=f(t_p) *(Bottom)*; parameter: D=t_p/T

Diagram 5: Typ. output characteristics



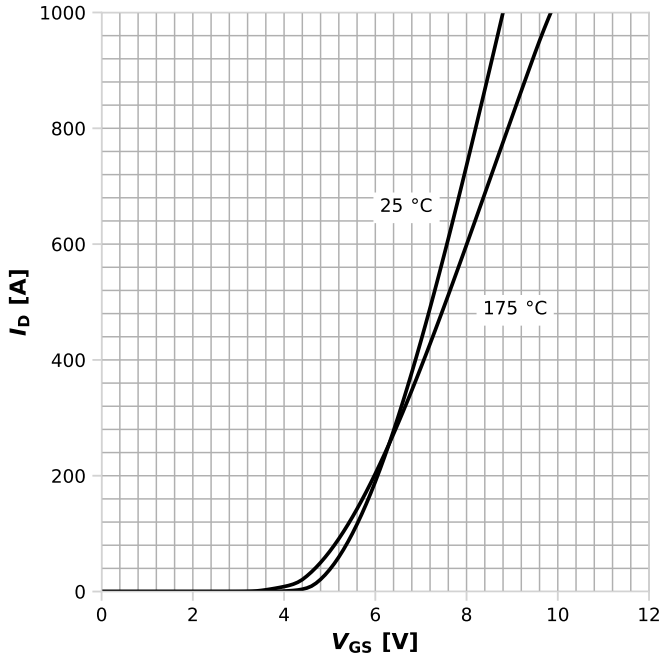
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



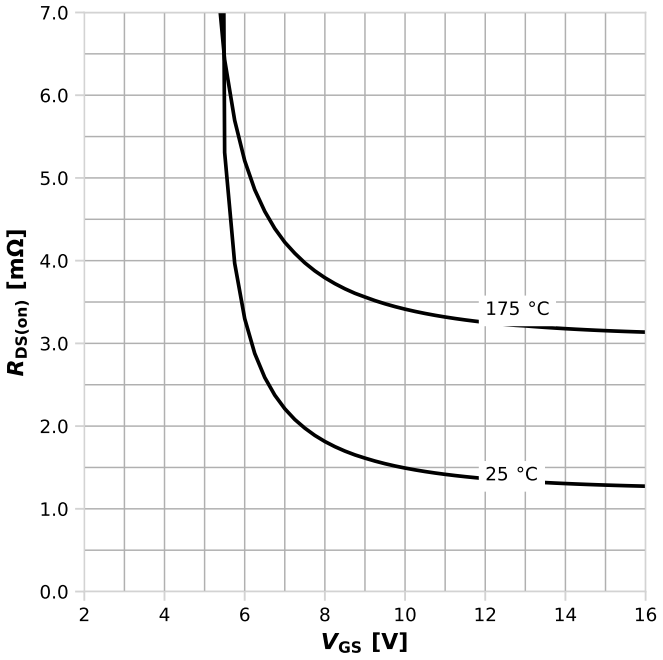
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}), $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}$=f(V_{GS}), I_D=50 A; parameter: T_j

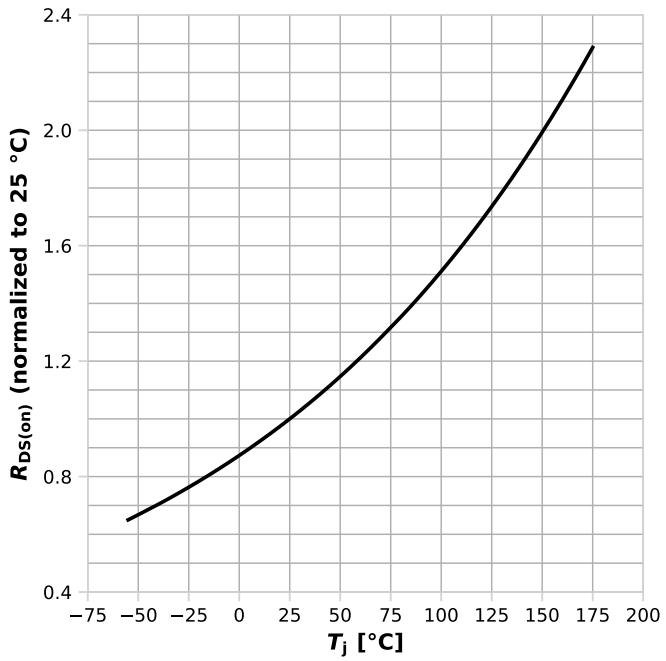
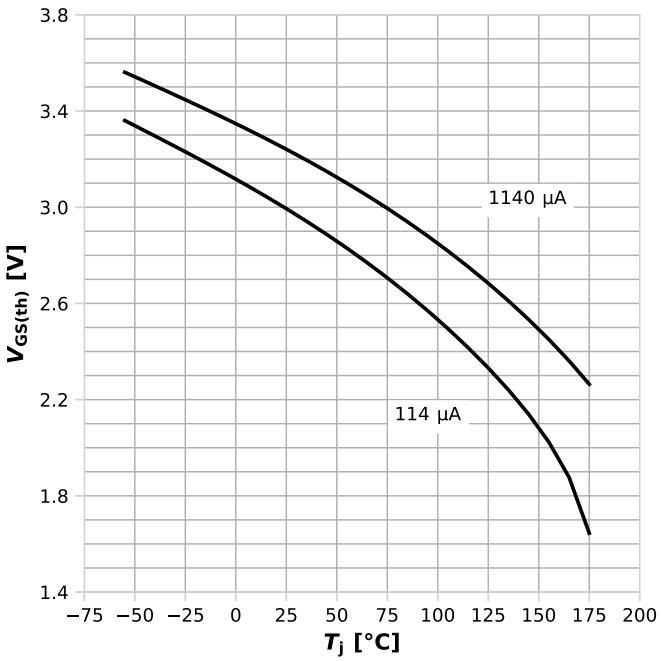
Diagram 9: Normalized drain-source on resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V	$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

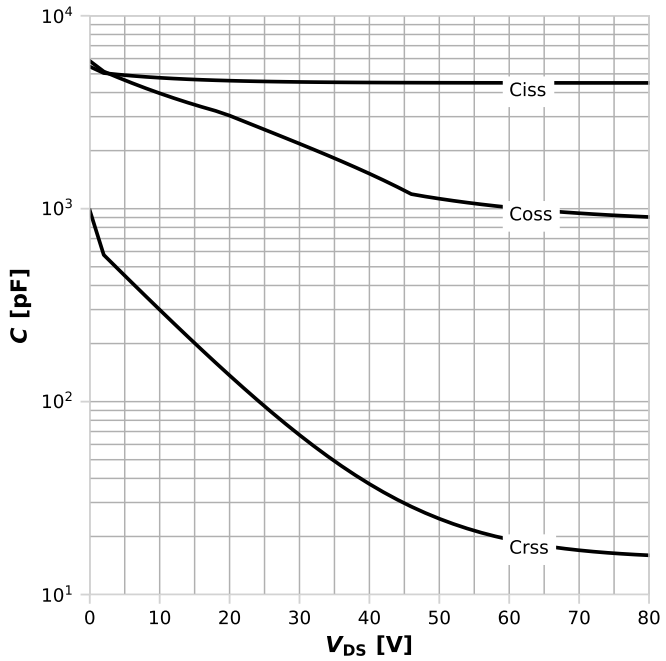
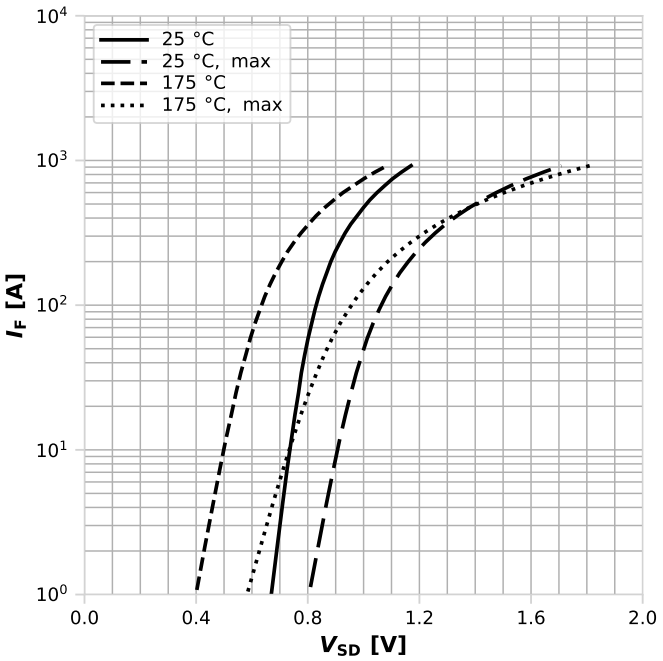
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

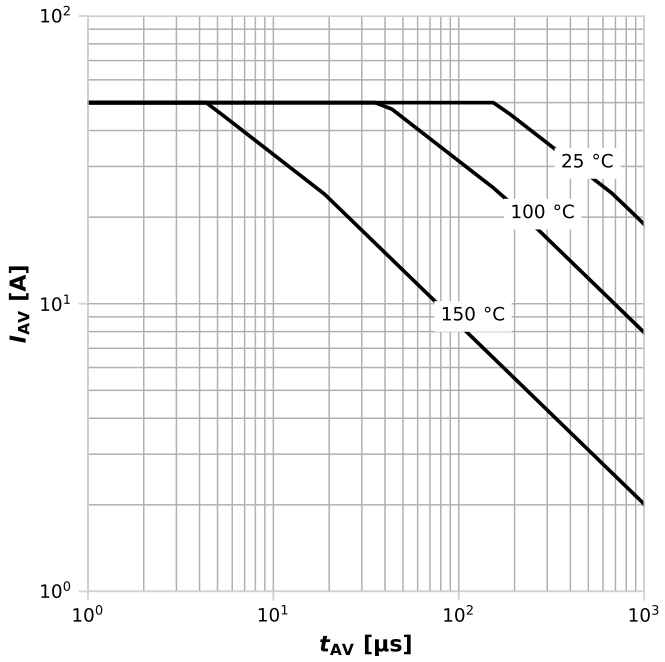
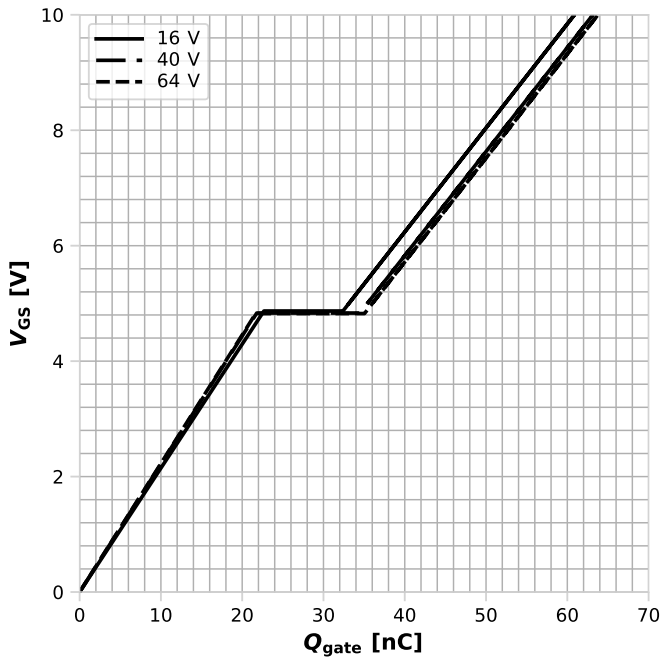
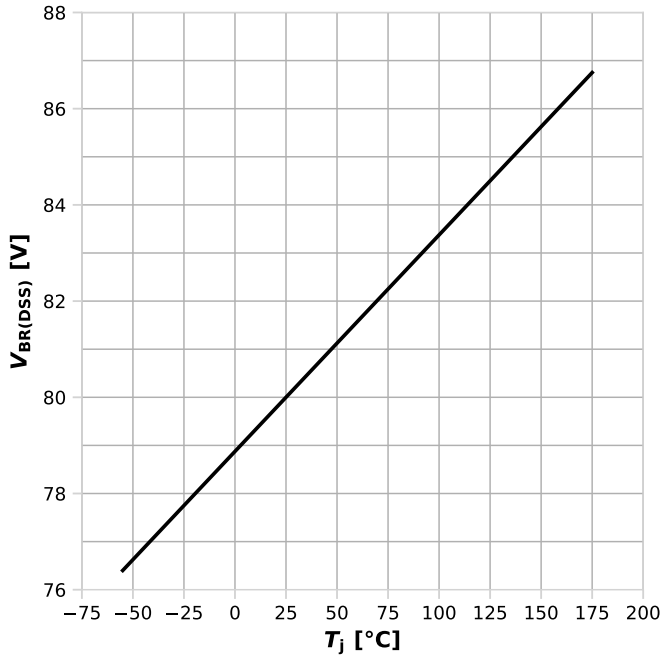
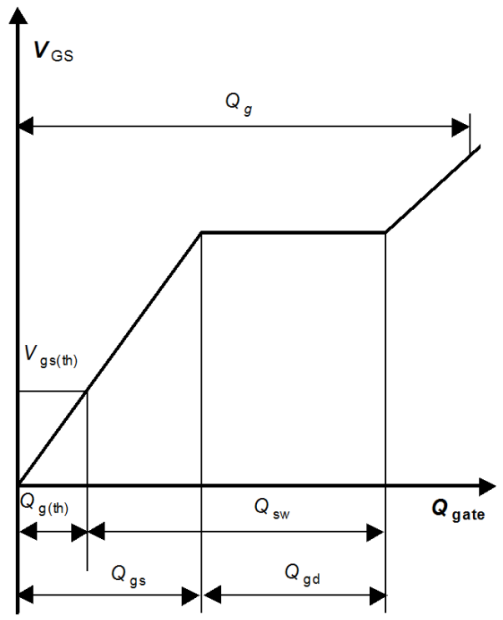
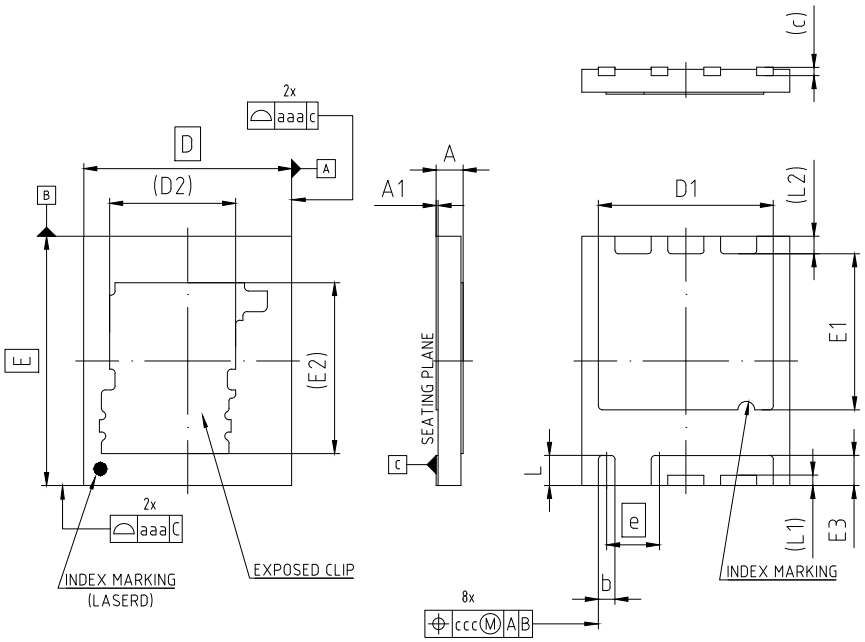
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=25 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 Package outlines



PACKAGE - GROUP NUMBER:	PG-WSON-8-U01				
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.55	0.75	e	1.27	
A1	0.00	0.05	L	0.68	0.78
b	0.35	0.45	L1	0.25	
c	0.20		L2	0.42	
D	5.00		aaa	0.05	
D1	4.11	4.31	ccc	0.10	
D2	3.03				
E	6.00				
E1	3.66	3.86			
E2	4.11				
E3	0.63	0.83			

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-WSON-8, dimensions in mm

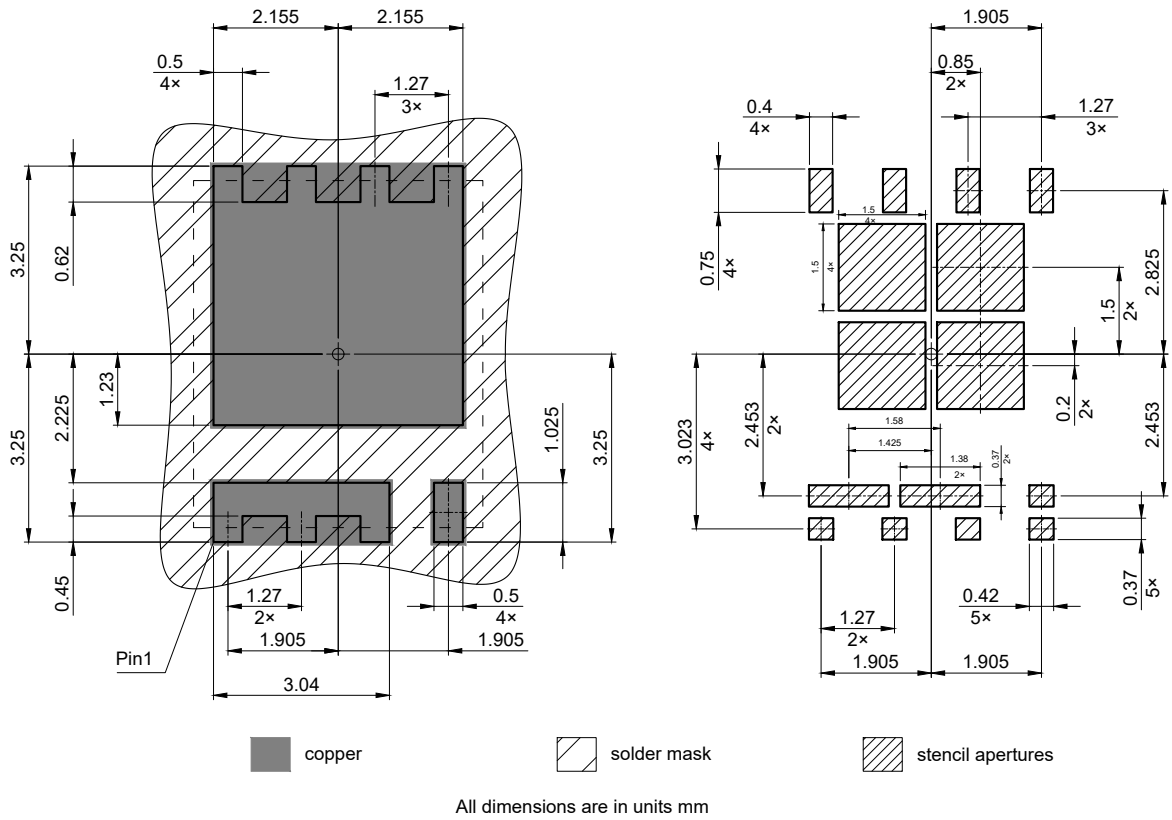


Figure 2 Footprint drawing PG-WSON-8, dimensions in mm

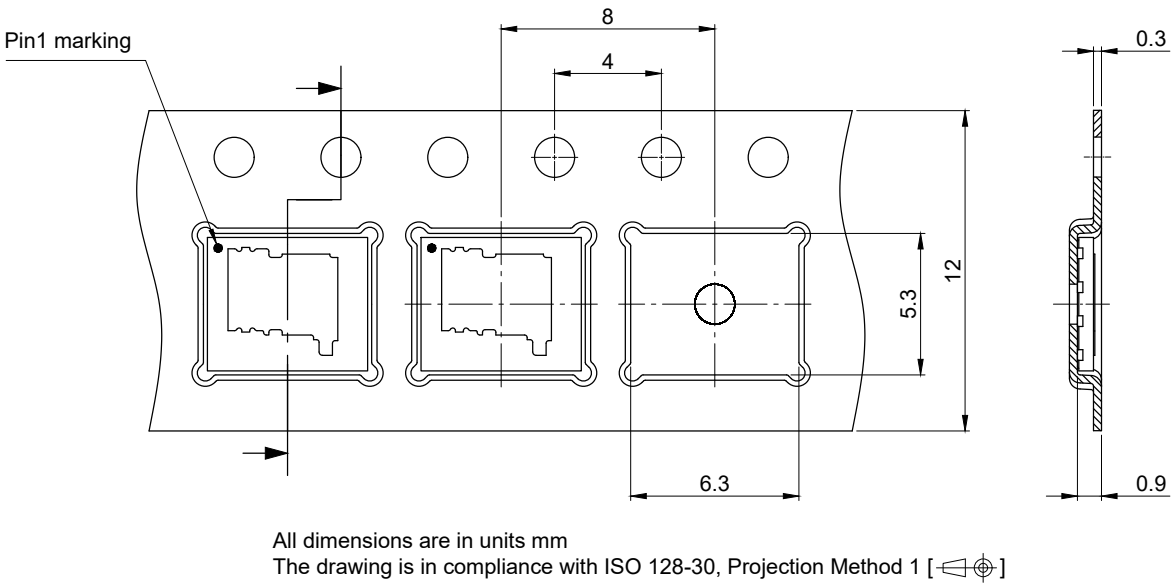


Figure 3 Packaging variant PG-WSON-8, dimensions in mm

Revision history

ISC018N08NM6SC

Revision 2025-02-17, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-02-17	Release of final version

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