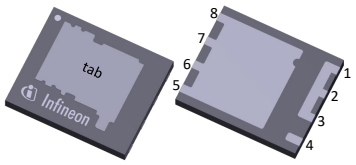
MOSFET

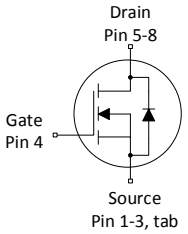
PG-WSON-8

OptiMOS™ 8 Power-MOSFET, 80 V



Features

- Dual-side cooled package with lowest junction-top thermal resistance
- N-channel, normal level
- Optimized for motor drives, synchronous rectification and battery protection
- Soft recovery body diode
- 100% avalanche tested
- Superior thermal resistance
- 175°C rated
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to JSTD020

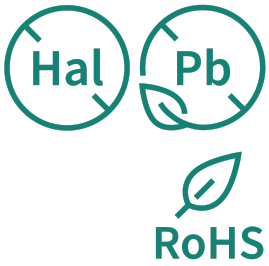


Product validation

Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on),max}$	1.64	mΩ
I_D	269	A
Q_{oss}	147	nC
Q_G (0 V..10 V)	76	nC
Q_{rr} (100 A/µs)	162	nC



Part number	Package	Marking	Related links
ISC016N08NM8SC	PG-WSON-8	016N08SC	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	269	A	V_{GS}=10 V, T_C=25 °C
				190		V_{GS}=10 V, T_C=100 °C
				196		V_{GS}=15 V, T_C=100 °C
				29		V_{GS}=10 V, T_A=25 °C, R_{THJA}=50 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	1076	A	T_C=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	442	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	263	W	T_C=25 °C
				3.0		T_A=25 °C, R_{THJA}=50 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.38	0.57	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}		0.36	0.72		
Thermal resistance, junction - ambient , 6 cm^2 cooling area [5)]	R_{thJA}		-	50		

[5)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.5	3.0	3.5	V	V_{DS}=V_{GS}, I_D=111 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C
Zero gate voltage drain current [6]	I_{DSS}	-	10	100	µA	V_{DS}=80 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.31	1.54	mΩ	V_{GS}=15 V, I_D=50 A
			1.44	1.64		V_{GS}=10 V, I_D=50 A
			1.61	1.87		V_{GS}=8 V, I_D=25 A
Gate resistance	R_G	-	0.95	-	Ω	-
Transconductance [6]	g_{fs}	55	110	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=50 A

[6] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [7]	C_{iss}	-	5500	7200	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Output capacitance [7]	C_{oss}		2230	2900		
Reverse transfer capacitance [7]	C_{rss}		24	42		
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r		6.1			
Turn-off delay time	$t_{d(off)}$		28			
Fall time	t_f		7.2			

[7] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [8)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	29	-	nC	V_{DD}=40 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$		17	-	nC	
Gate to drain charge [9)]	Q_{gd}		15	19	nC	
Switching charge	Q_{sw}		27	-	nC	
Gate charge total [9)]	Q_g		76	99	nC	
Gate plateau voltage	$V_{plateau}$		5.3	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	69	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge [9)]	Q_{oss}	-	147	191	nC	V_{DS}=40 V, V_{GS}=0 V

[8)] See figure 16 for gate charge parameter definition.

[9)] Defined by design. Not subject to production test.

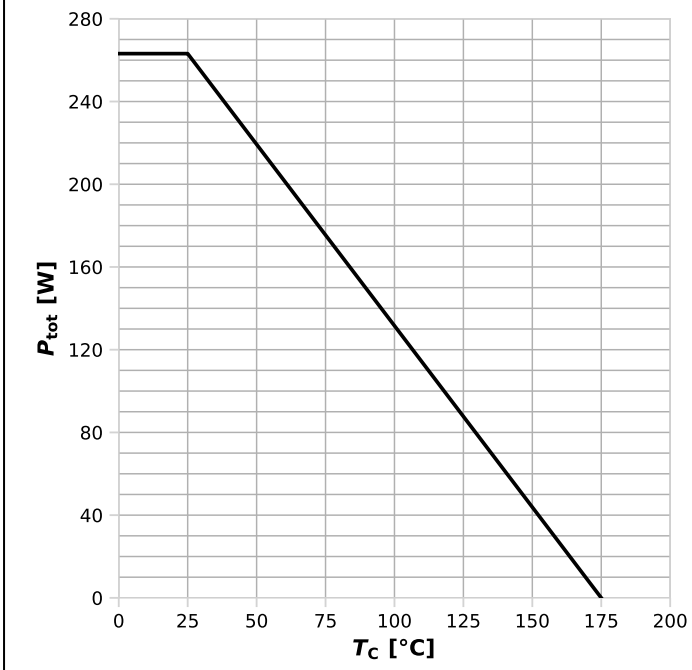
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	232	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			1076		
Diode forward voltage	V_{SD}	-	0.84	1.0	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time [10)]	t_{rr}	-	187	374	ns	V_R=40 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge [10)]	Q_{rr}		162	325	nC	
Reverse recovery time [10)]	t_{rr}	-	39	78	ns	V_R=40 V, I_F=50 A, di_F/dt=500 A/µs
Reverse recovery charge [10)]	Q_{rr}		209	418	nC	

[10)] Defined by design. Not subject to production test.

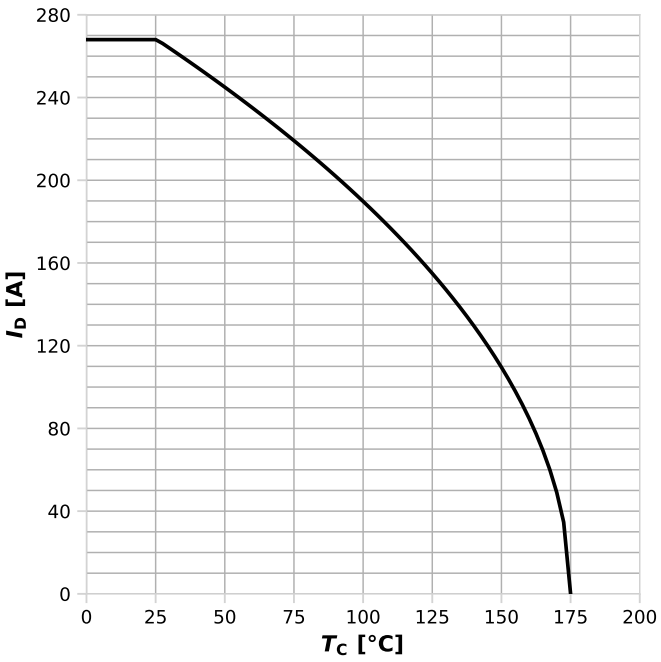
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



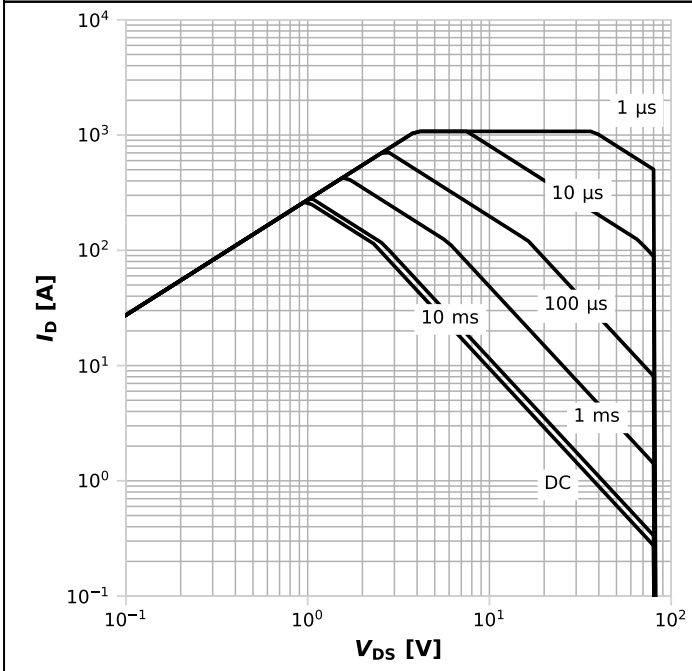
P_{tot}=f(T_C)

Diagram 2: Drain current



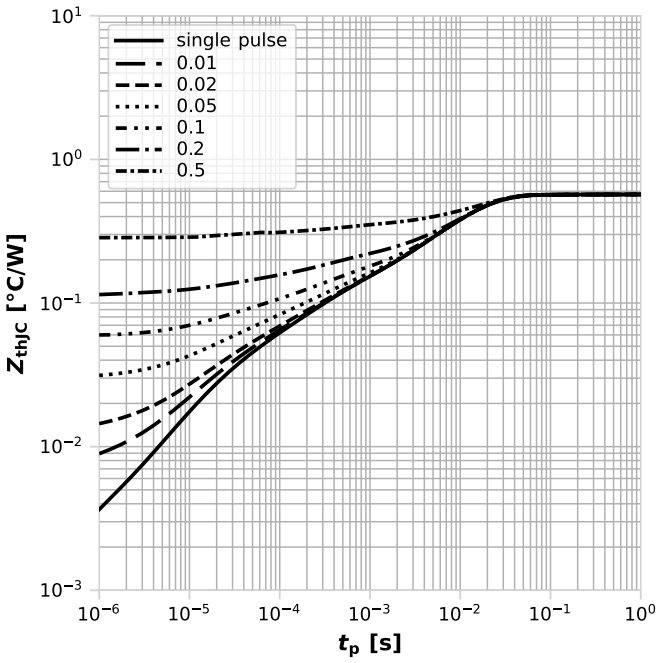
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



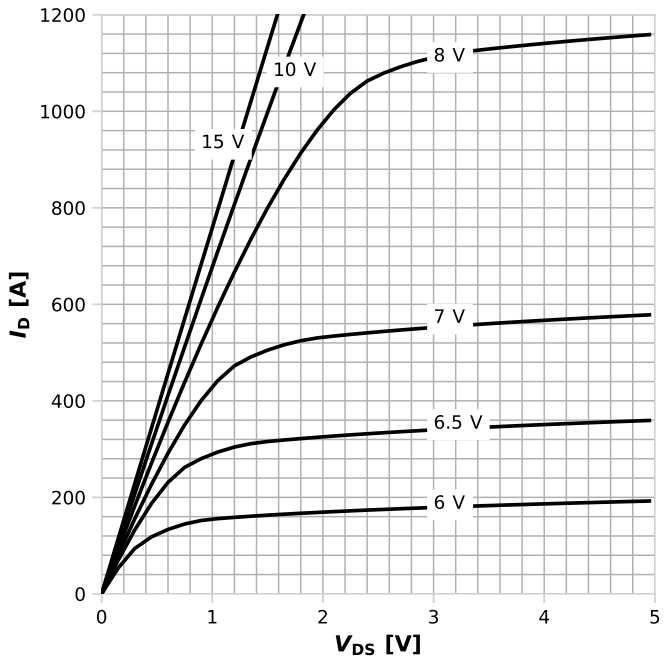
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



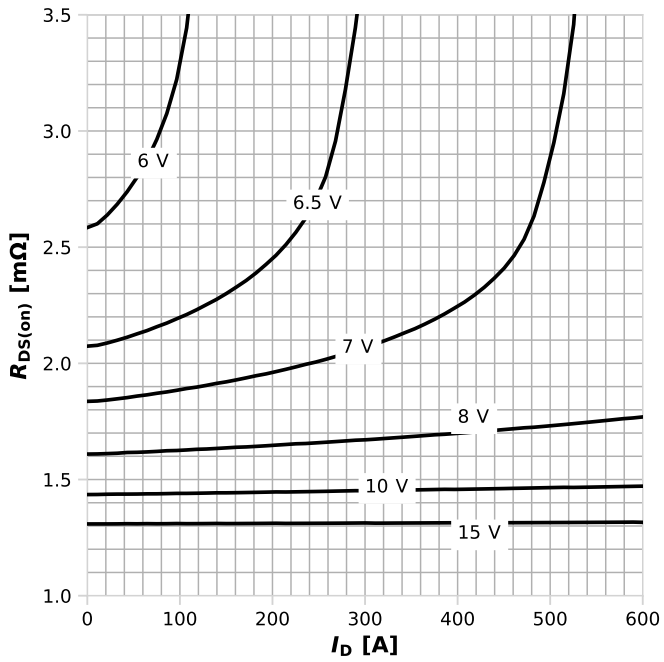
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



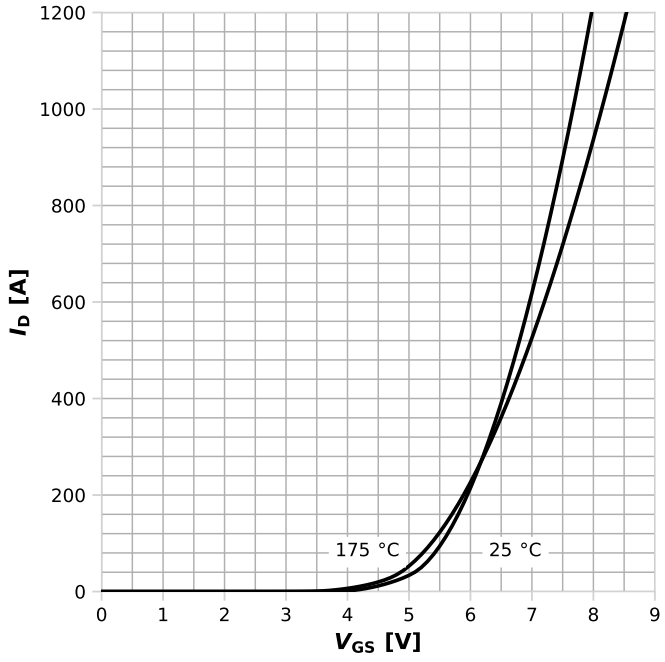
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



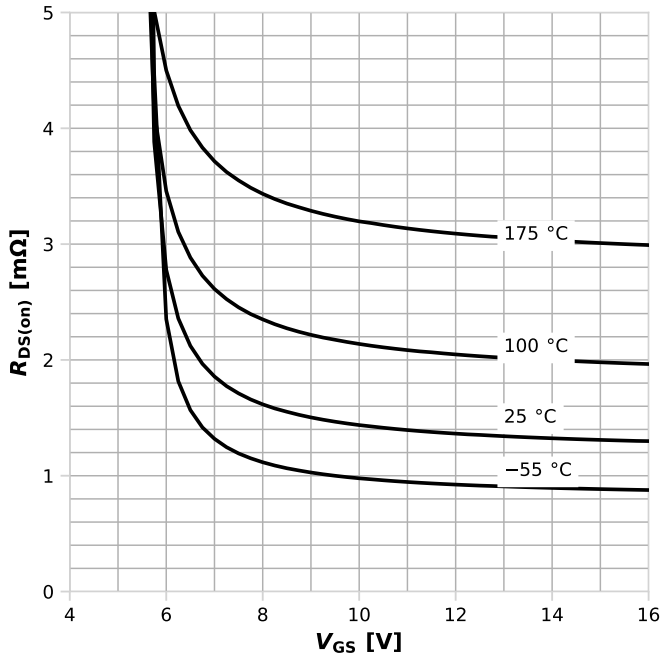
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



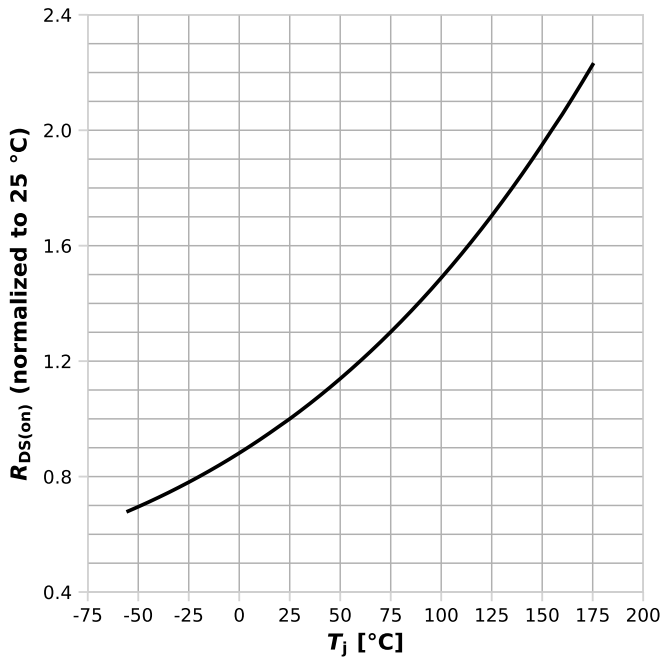
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



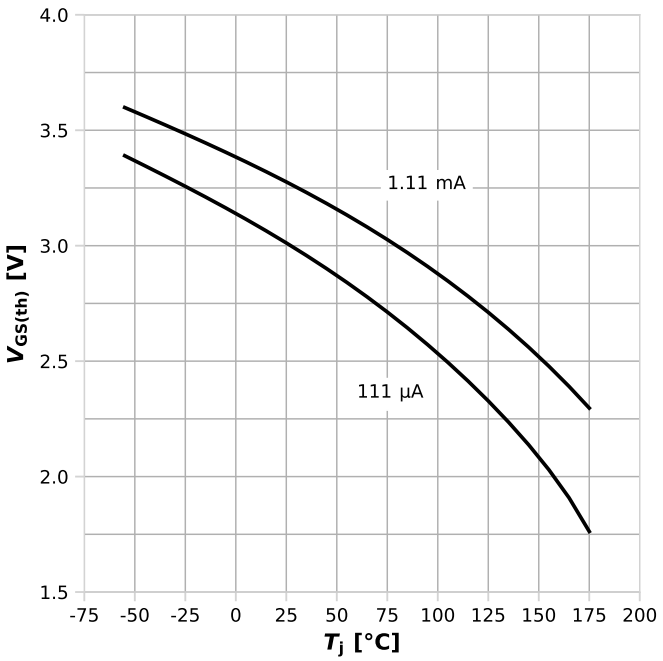
$R_{DS(on)}$=f(V_{GS}), I_D=50 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



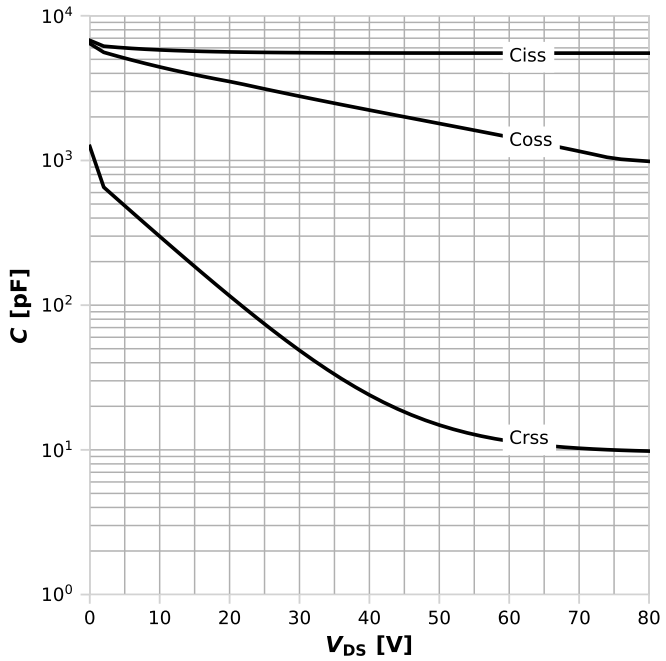
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



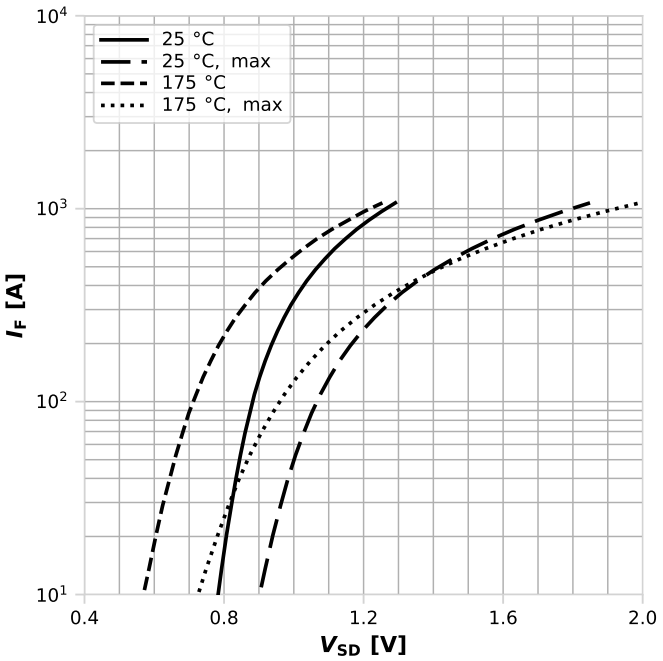
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

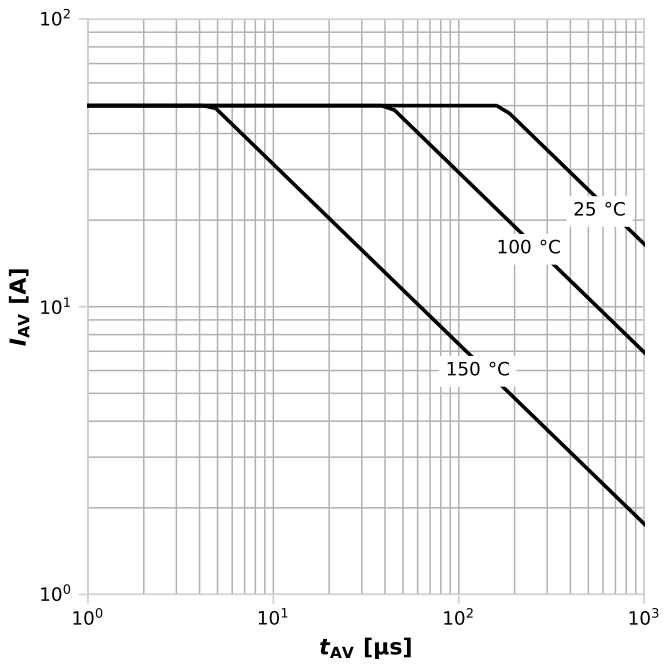
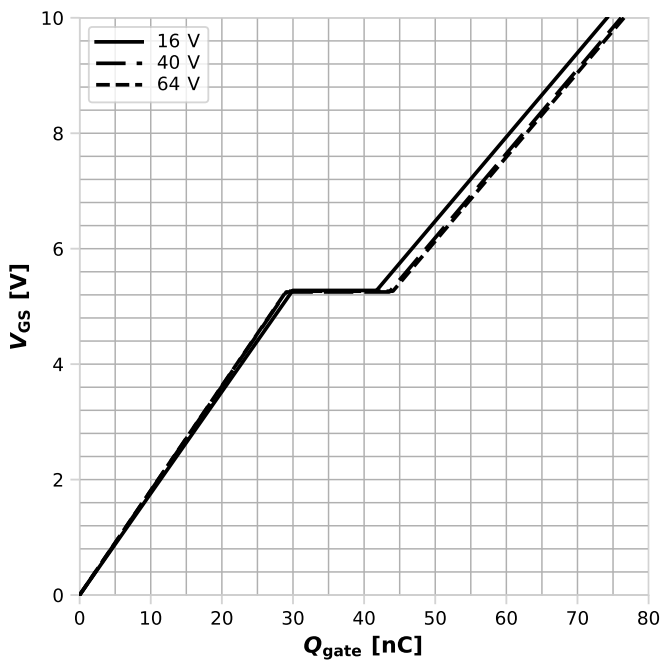
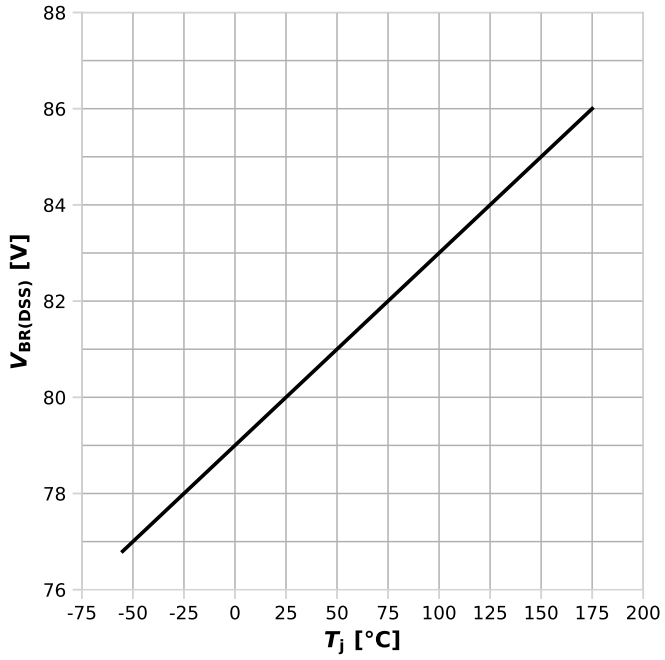
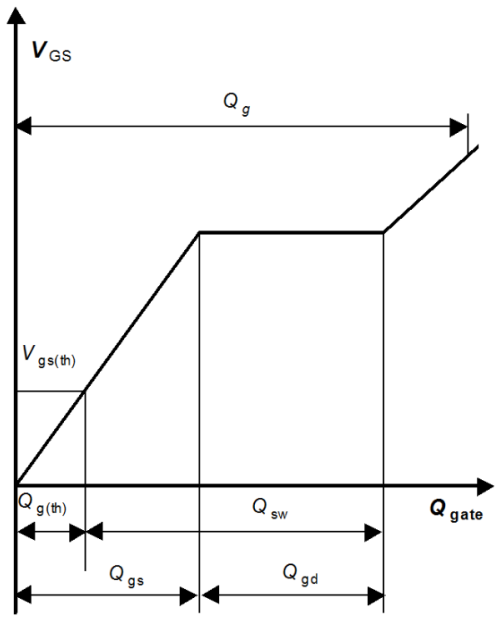
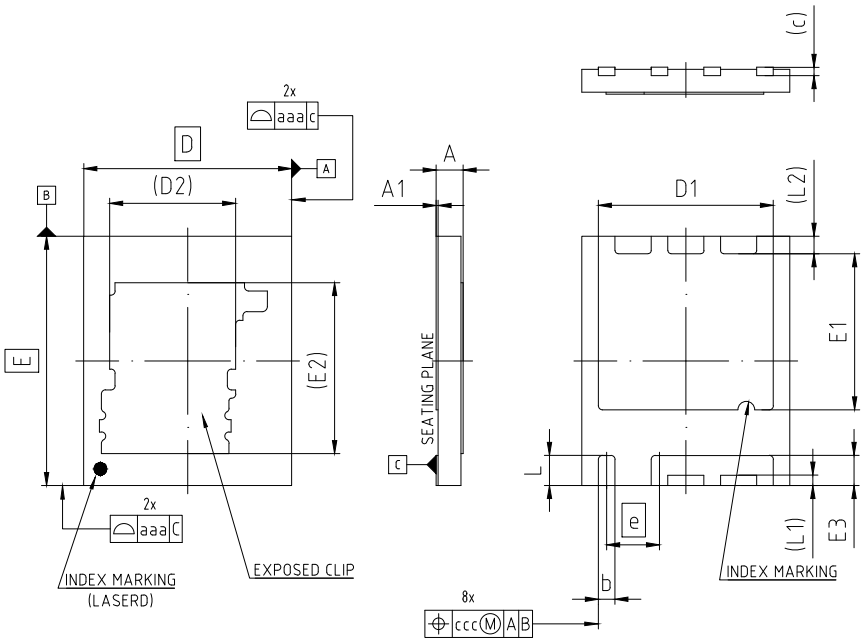
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 Package outlines



PACKAGE - GROUP NUMBER:	PG-WSON-8-U01				
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.55	0.75	e	1.27	
A1	0.00	0.05	L	0.68	0.78
b	0.35	0.45	L1	0.25	
c	0.20		L2	0.42	
D	5.00		aaa	0.05	
D1	4.11	4.31	ccc	0.10	
D2	3.03				
E	6.00				
E1	3.66	3.86			
E2	4.11				
E3	0.63	0.83			

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-WSON-8, dimensions in mm

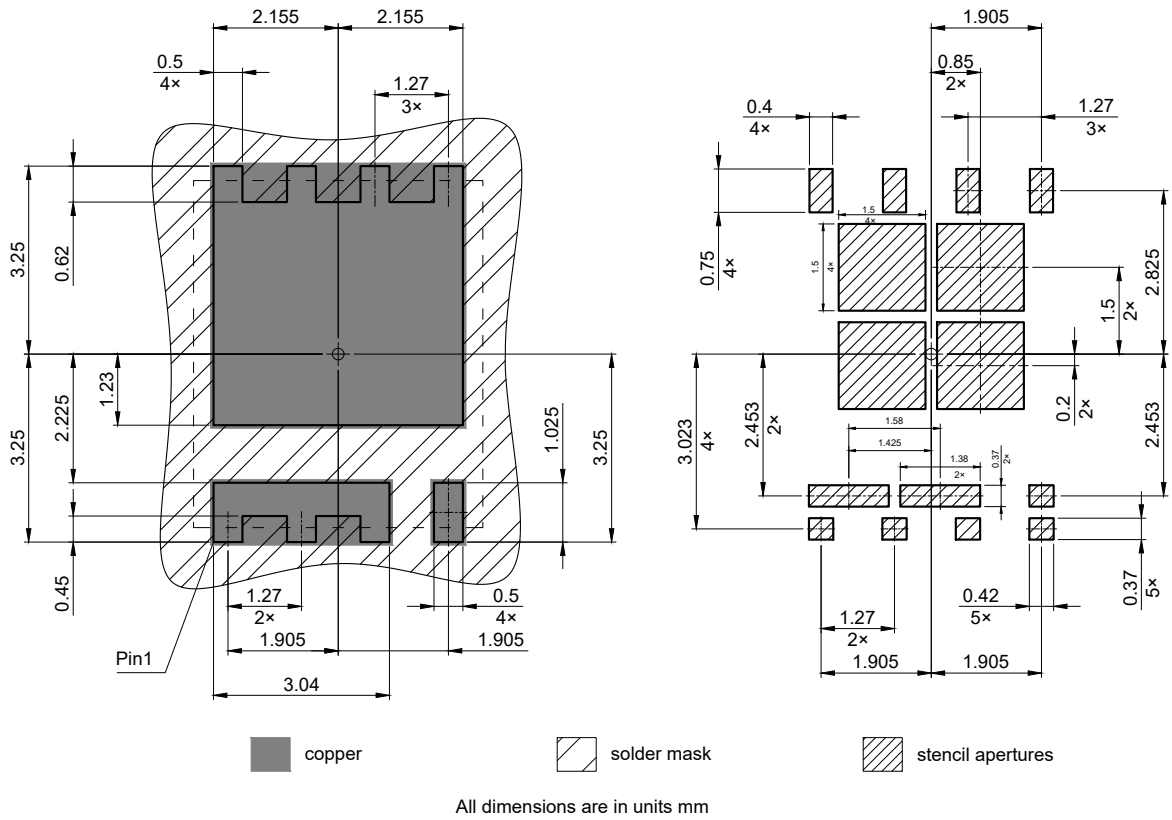


Figure 2 Footprint drawing PG-WSON-8, dimensions in mm

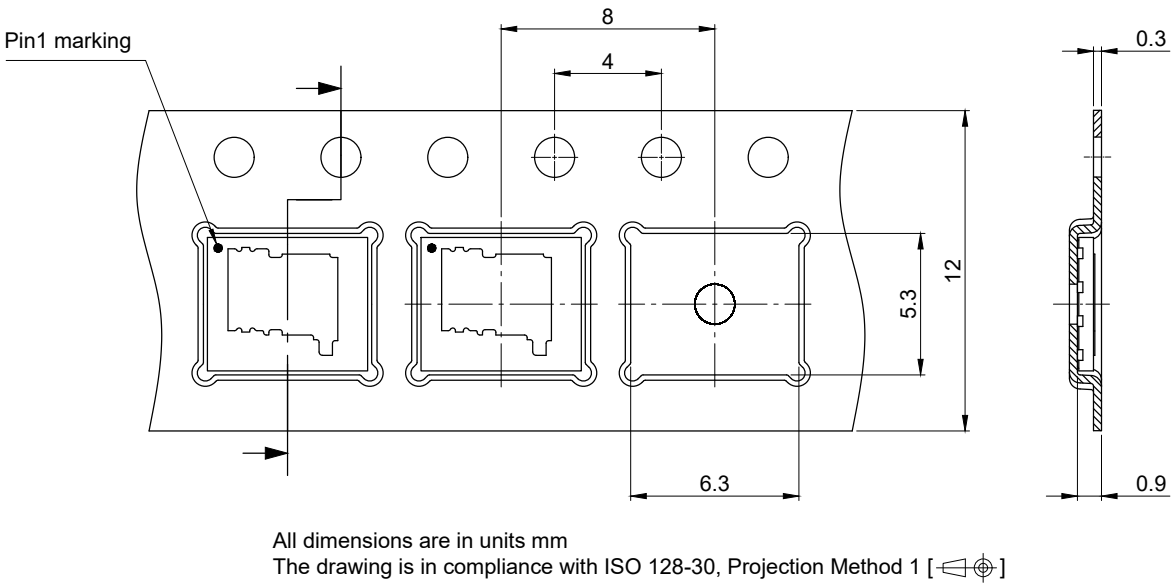


Figure 3 Packaging variant PG-WSON-8, dimensions in mm

Revision history

ISC016N08NM8SC

Revision 2025-12-17, Rev. 1.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-08-21	Release of final version
1.1	2025-10-17	Updated part marking from "16N08SC" to "016N08SC"
1.2	2025-12-17	Updated RthJC

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