

## MOSFET

### OptiMOS™ 5 Power-Transistor, 60 V

#### Features

- N-channel, normal level
- Very low on-resistance  $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

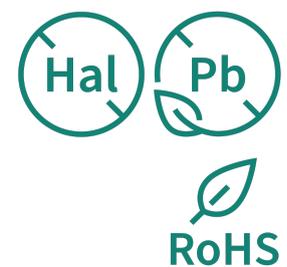
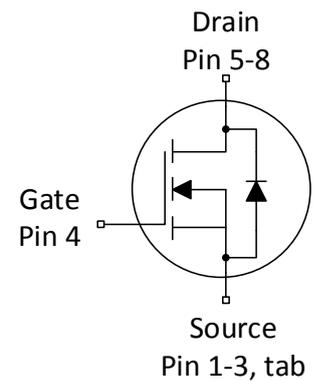
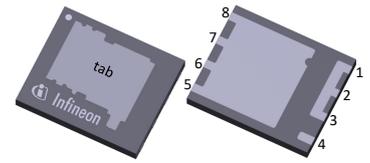
#### Product validation

Qualified according to relevant JEDEC tests.

**Table 1** Key performance parameters

Parameter	Value	Unit
$V_{DS}$	60	V
$R_{DS(on),max}$	1.6	m $\Omega$
$I_D$	249	A
$Q_{oss}$	80	nC
$Q_G$	74	nC

PG-WSO8-8



Part number	Package	Marking	Related links
ISC016N06NM5SC	PG-WSO8-8	16N06MSC	-



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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	249	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$
				176		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$
				144		$V_{GS}=6\text{ V}, T_C=100\text{ °C}$
				31		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=50\text{ °C/W}^2)$
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	996	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	380	mJ	$I_D=50\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	188	W	$T_C=25\text{ °C}$
				3.0		$T_A=25\text{ °C}, R_{thJA}=50\text{ °C/W}^2)$
Operating and storage temperature	$T_j, T_{stg}$	-55	-	175	°C	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$			0.8	°C/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>5)</sup>	$R_{thJA}$	-	-	50		

<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	$V_{DS}=V_{GS}$ , $I_D=95\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1	1	$\mu\text{A}$	$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$
			10	100		$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.3	1.6	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$
			1.8	2.4		$V_{GS}=6\text{ V}$ , $I_D=12.5\text{ A}$
Gate resistance	$R_G$	-	0.7	-	$\Omega$	-
Transconductance <sup>6)</sup>	$g_{fs}$	70	140	-	S	$ V_{DS} \geq 2 I_D $ , $R_{DS(on)max}$ , $I_D=50\text{ A}$

<sup>6)</sup> Defined by design. Not subject to production test.

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance <sup>7)</sup>	$C_{iss}$	-	5400	7000	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>7)</sup>	$C_{oss}$		1200	1600		
Reverse transfer capacitance <sup>7)</sup>	$C_{rss}$		49	86		
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$		5			
Turn-off delay time	$t_{d(off)}$		28			
Fall time	$t_f$		7			

<sup>7)</sup> Defined by design. Not subject to production test.

**Table 6 Gate charge characteristics** <sup>8)</sup>

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	23	-	nC	$V_{DD}=30\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	15	-	nC	
Gate to drain charge <sup>9)</sup>	$Q_{gd}$	-	13.6	20	nC	
Switching charge	$Q_{sw}$	-	22	-	nC	
Gate charge total <sup>9)</sup>	$Q_g$	-	74	93	nC	
Gate plateau voltage	$V_{plateau}$	-	4.3	-	V	
Output charge <sup>9)</sup>	$Q_{oss}$	-	80	106	nC	$V_{DS}=30\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>8)</sup> See "Gate charge waveforms" for parameter definition

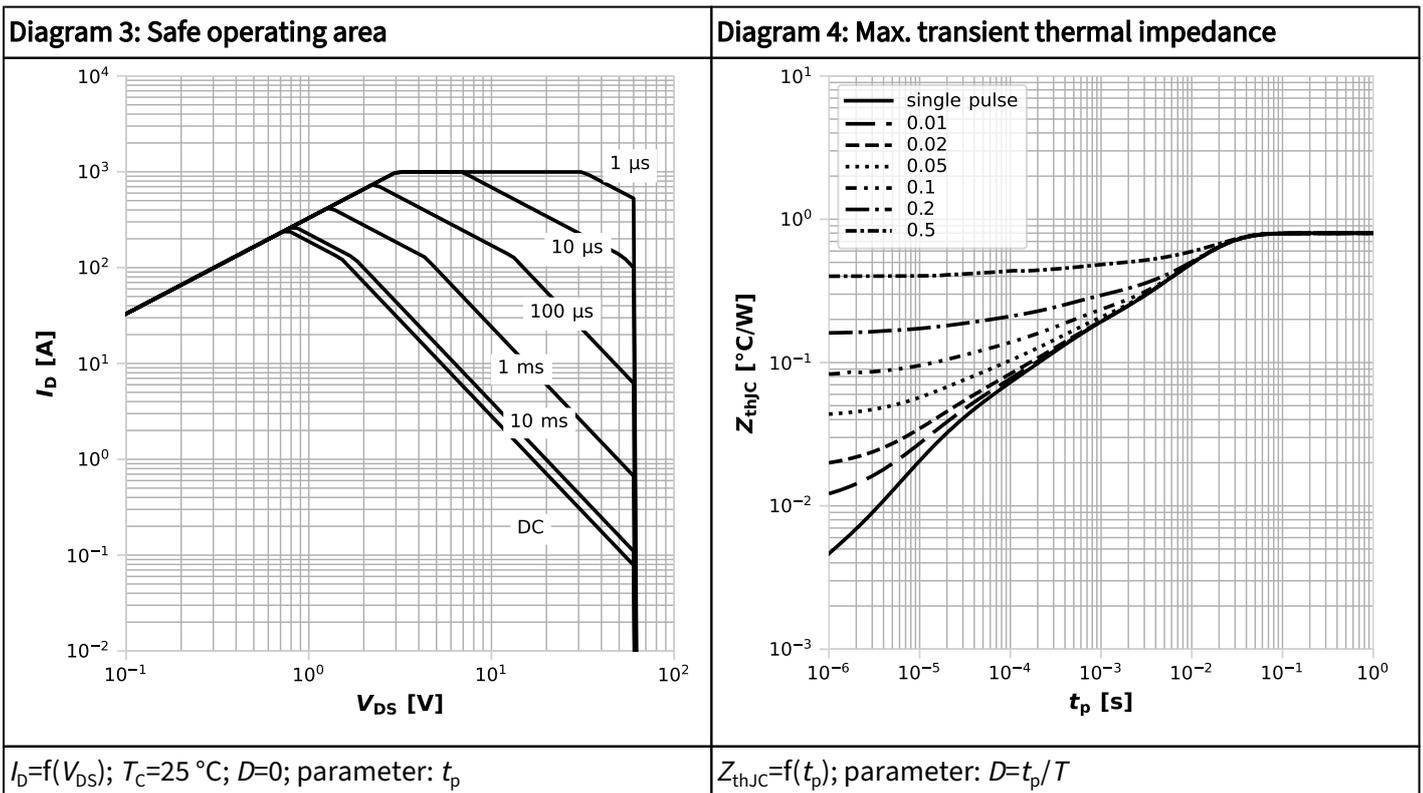
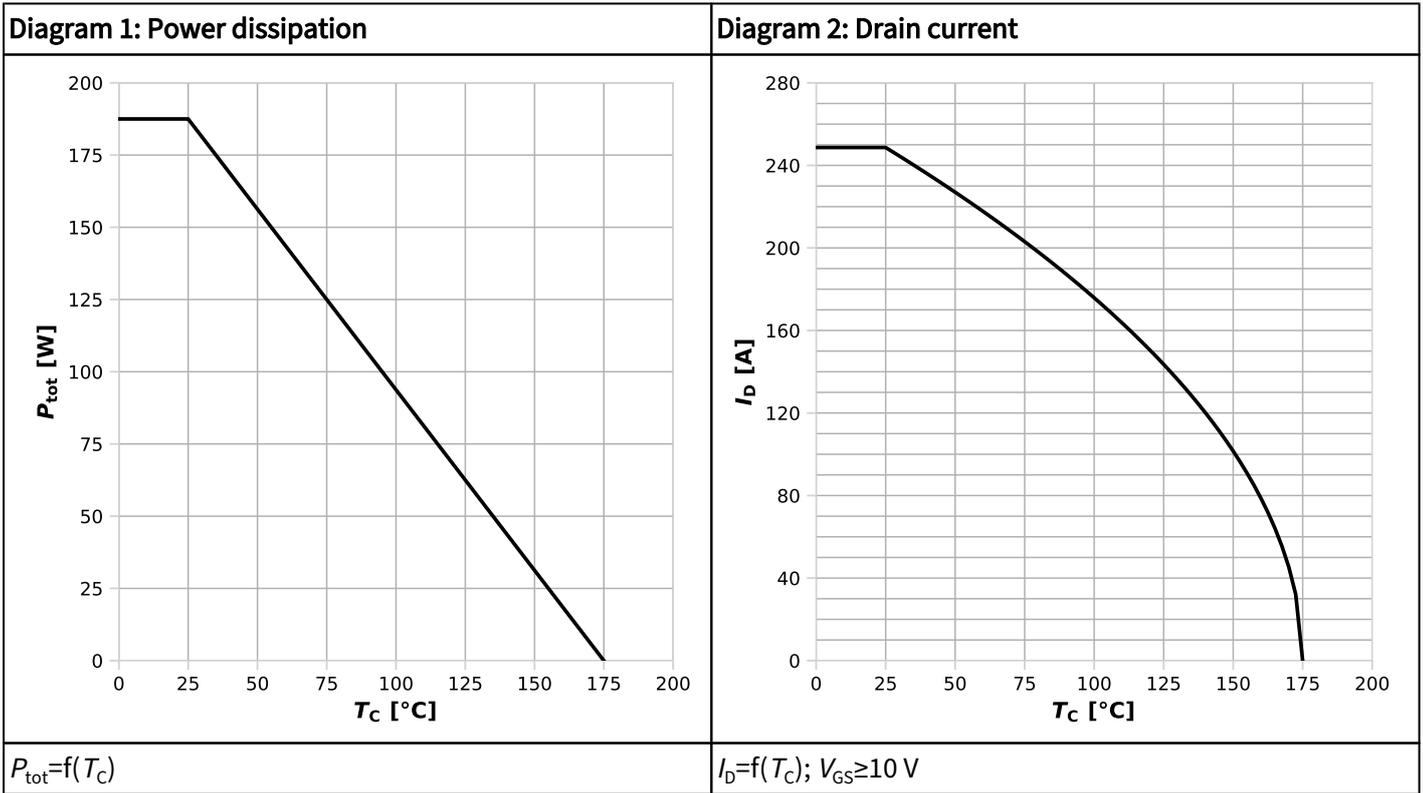
<sup>9)</sup> Defined by design. Not subject to production test.

**Table 7 Reverse diode**

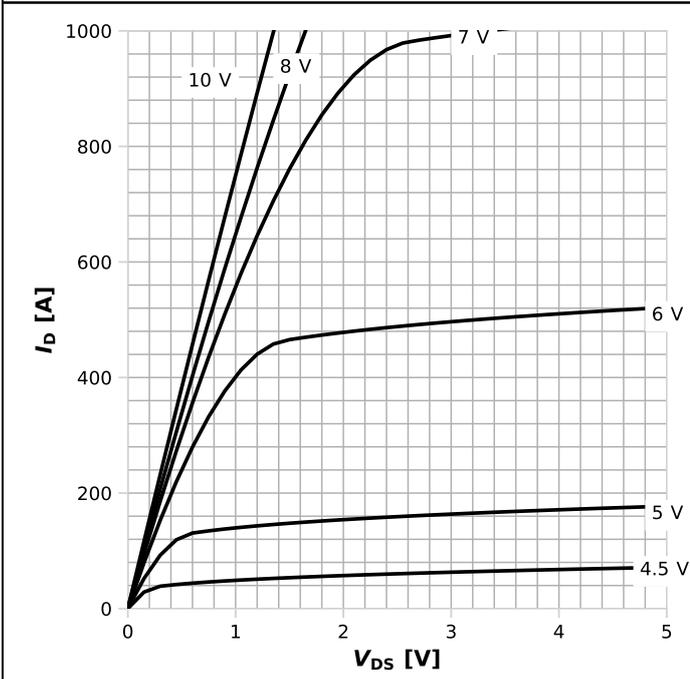
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	162	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	996		
Diode forward voltage	$V_{SD}$	-	0.83	1.0	V	$V_{GS}=0\text{ V}$ , $I_F=50\text{ A}$ , $T_J=25\text{ °C}$
Reverse recovery time <sup>10)</sup>	$t_{rr}$	-	35	70	ns	$V_R=30\text{ V}$ , $I_F=50\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>10)</sup>	$Q_{rr}$	-	32	64	nC	
Reverse recovery time <sup>10)</sup>	$t_{rr}$	-	28	56	ns	$V_R=30\text{ V}$ , $I_F=50\text{ A}$ , $di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>10)</sup>	$Q_{rr}$	-	117	234	nC	
Reverse recovery time <sup>10)</sup>	$t_{rr}$	-	23	46	ns	$V_R=30\text{ V}$ , $I_F=50\text{ A}$ , $di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>10)</sup>	$Q_{rr}$	-	175	350	nC	

<sup>10)</sup> Defined by design. Not subject to production test.

## 4 Electrical characteristics diagrams

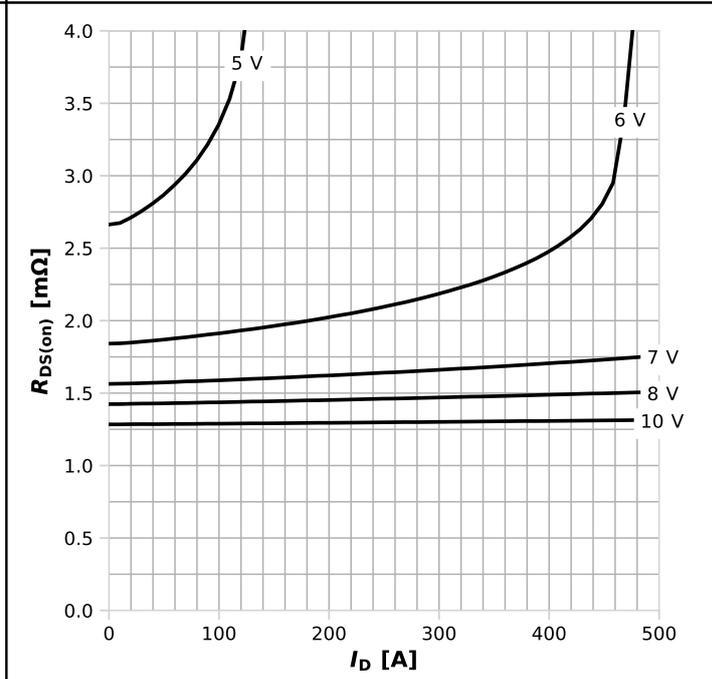


**Diagram 5: Typ. output characteristics**



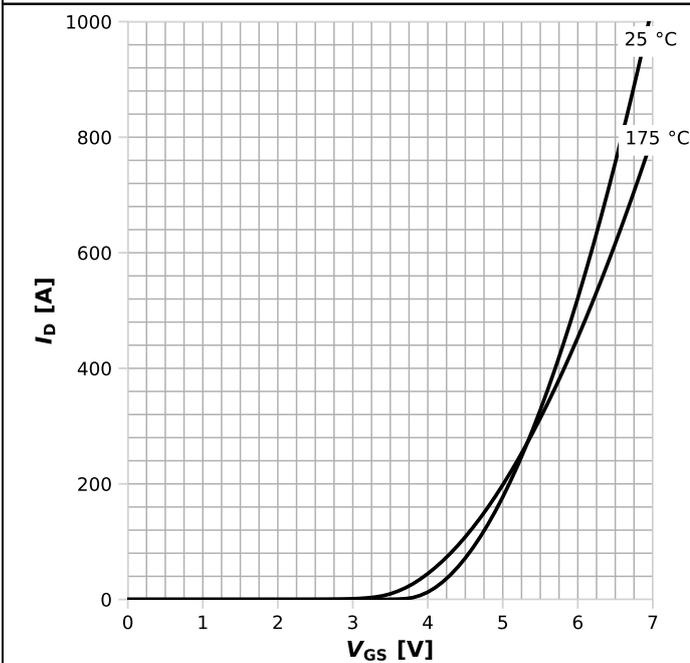
$I_D = f(V_{DS}), T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



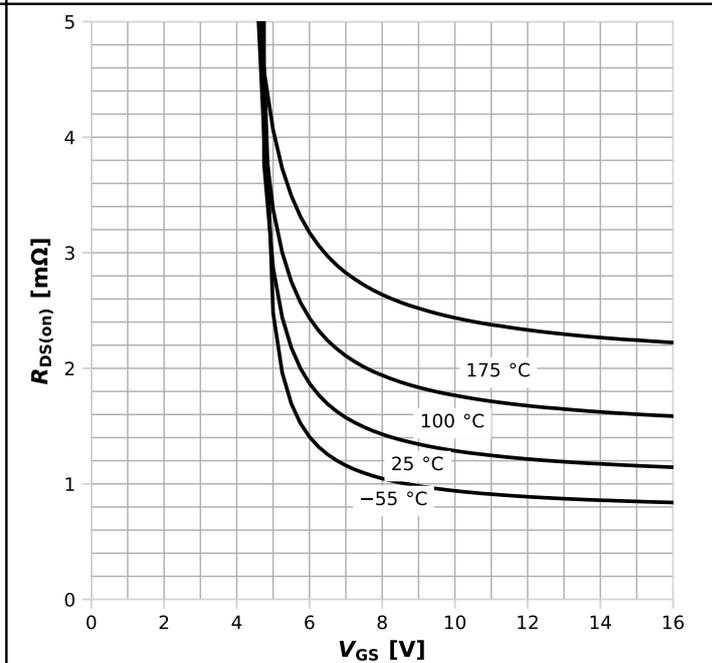
$R_{DS(on)} = f(I_D), T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



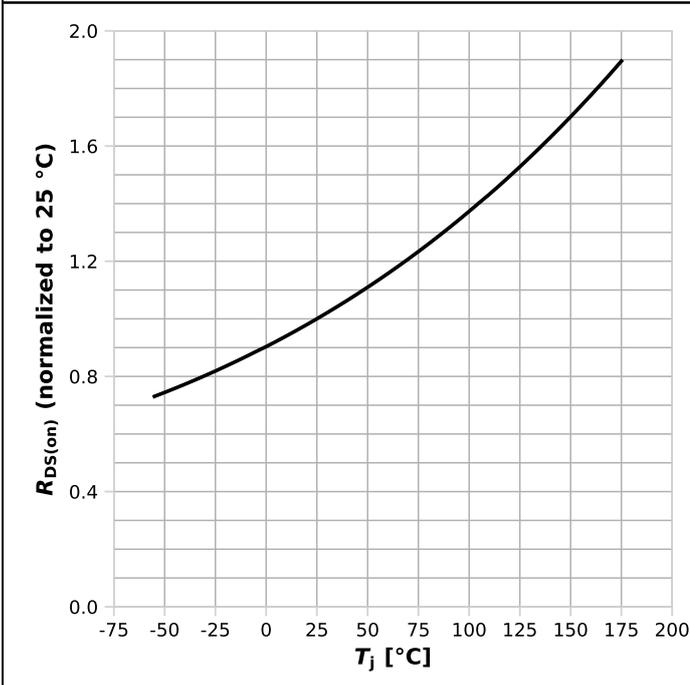
$I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)max};$  parameter:  $T_j$

**Diagram 8: Typ. drain-source on resistance**



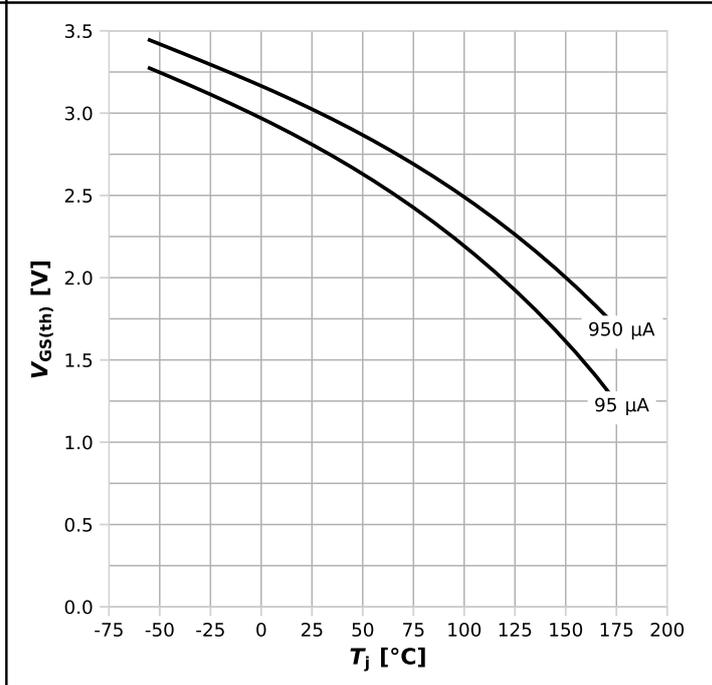
$R_{DS(on)} = f(V_{GS}), I_D = 50\text{ A};$  parameter:  $T_j$

**Diagram 9: Normalized drain-source on resistance**



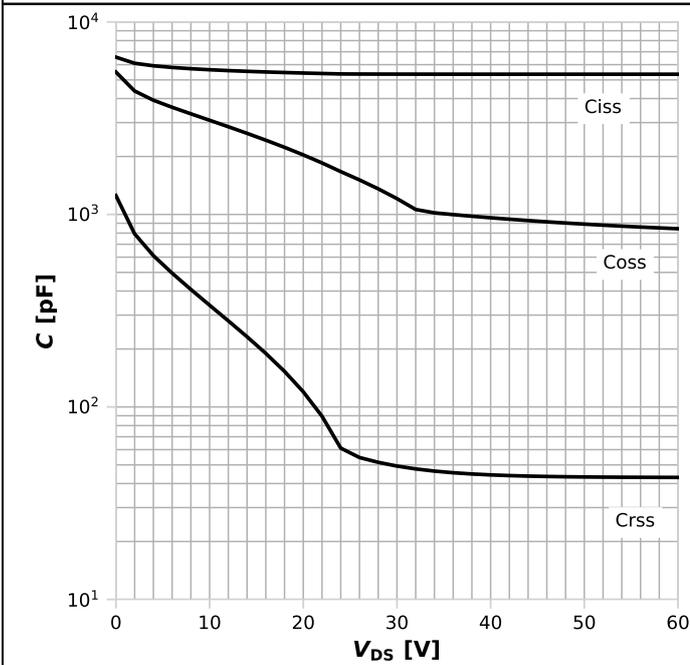
$R_{DS(on)}=f(T_j), I_D=50\text{ A}, V_{GS}=10\text{ V}$

**Diagram 10: Typ. gate threshold voltage**



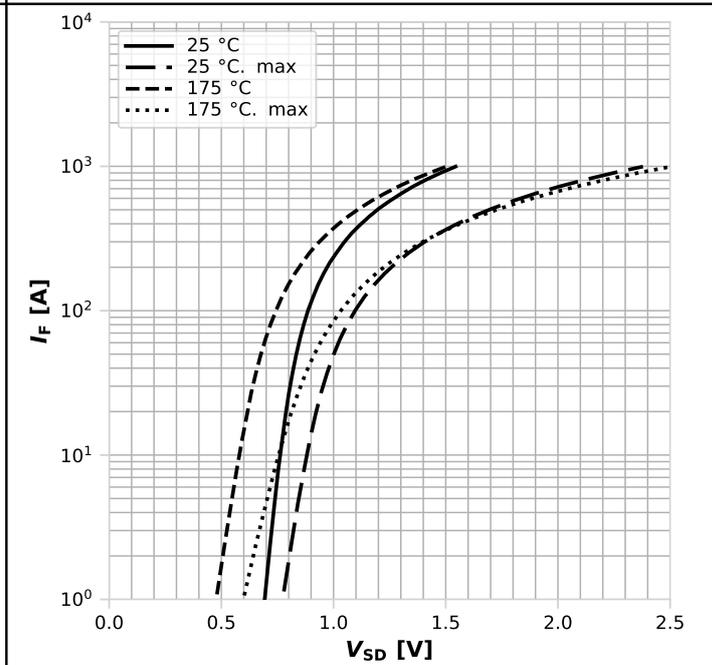
$V_{GS(th)}=f(T_j), V_{GS}=V_{DS}; \text{parameter: } I_D$

**Diagram 11: Typ. capacitances**



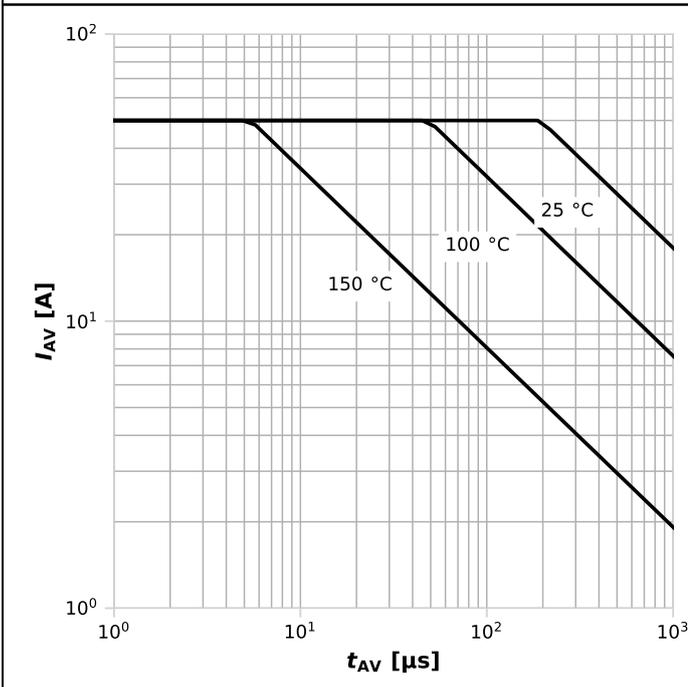
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

**Diagram 12: Forward characteristics of reverse diode**



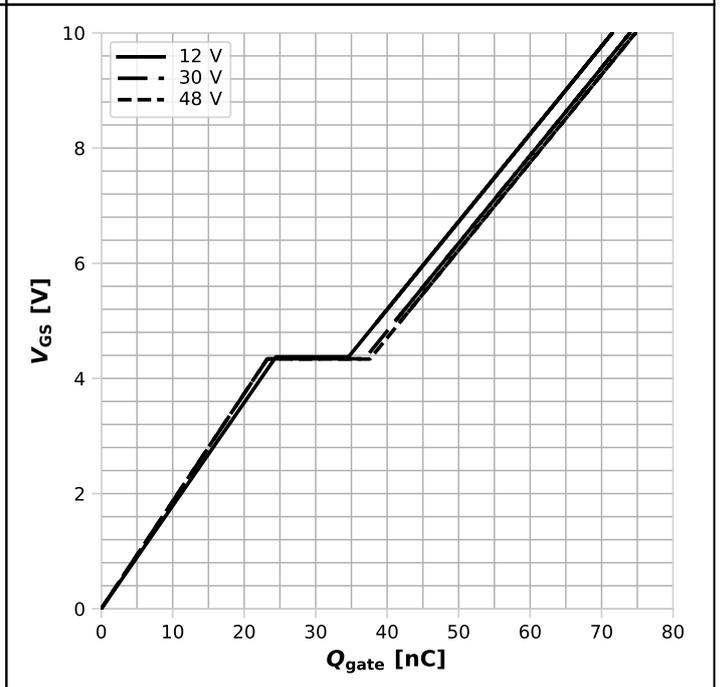
$I_F=f(V_{SD}); \text{parameter: } T_j$

**Diagram 13: Avalanche characteristics**



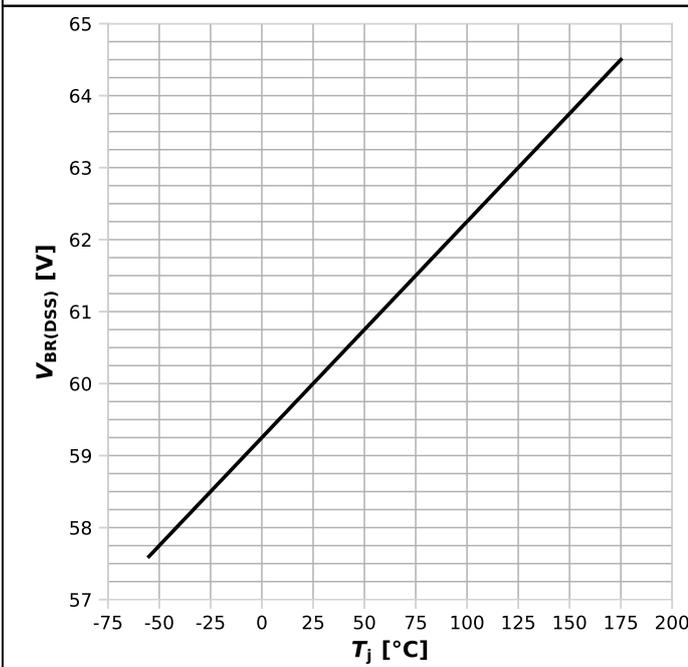
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega; \text{parameter: } T_{j,start}$

**Diagram 14: Typ. gate charge**



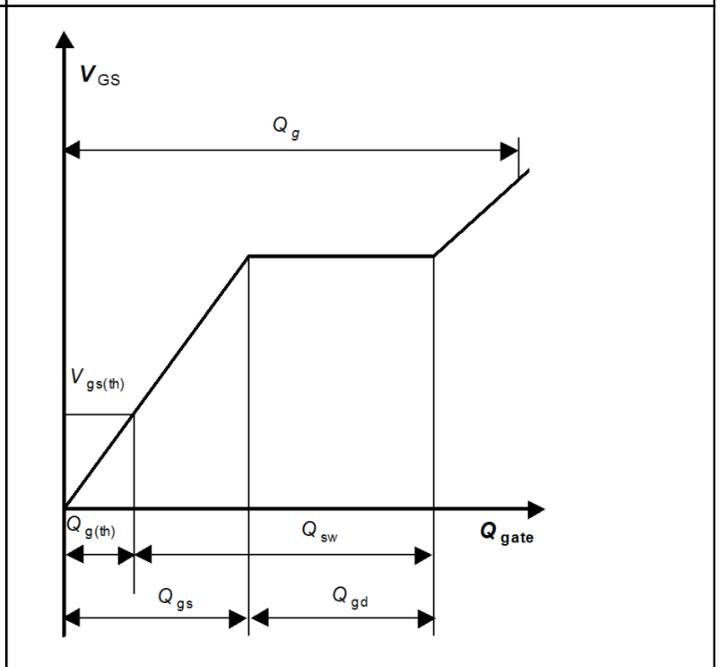
$V_{GS}=f(Q_{gate}), I_D=50 \text{ A pulsed}, T_j=25 \text{ °C}; \text{parameter: } V_{DD}$

**Diagram 15: Min. drain-source breakdown voltage**



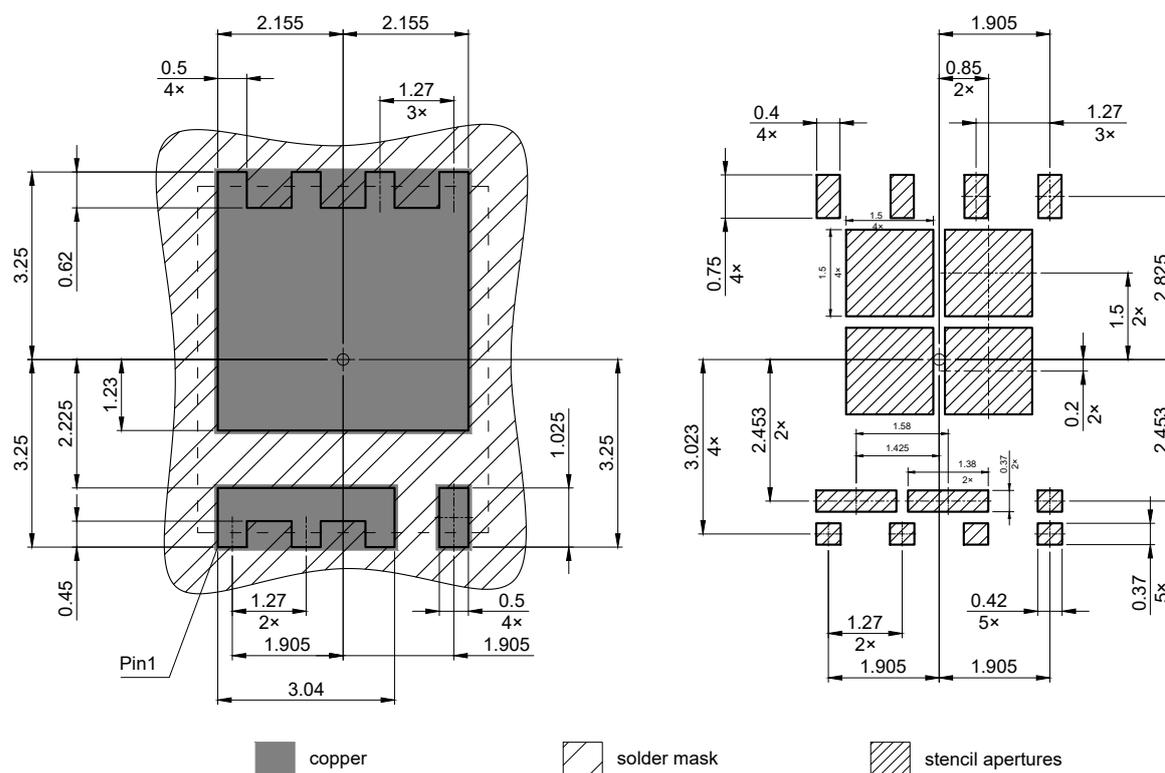
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Gate charge waveforms**



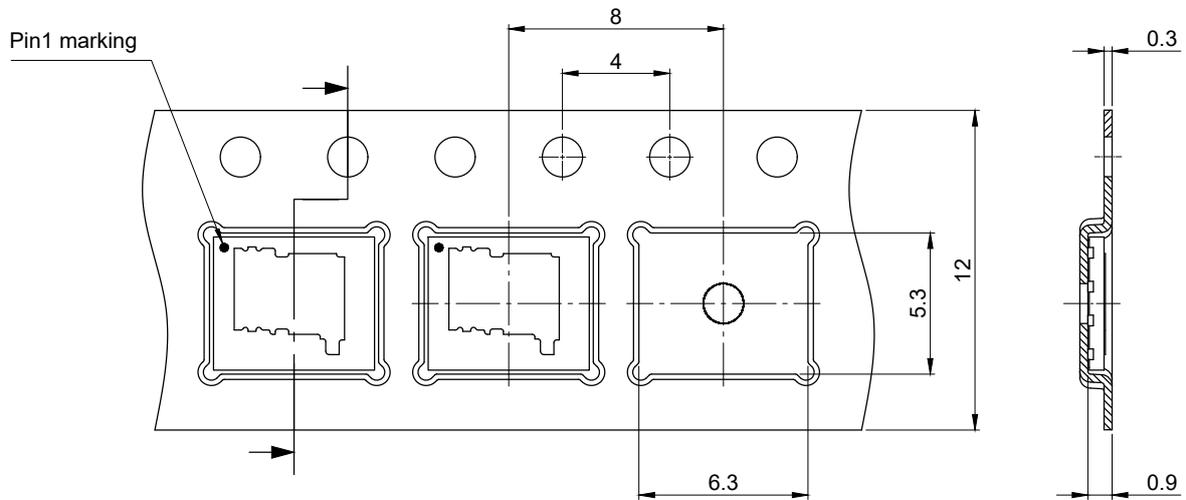
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All dimensions are in units mm

**Figure 2 Footprint drawing PG-WSON-8, dimensions in mm**



All dimensions are in units mm  
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

**Figure 3** Packaging variant PG-WSON-8, dimensions in mm



**Revision history**

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ISC016N06NM5SC

**Revision 2026-02-05, Rev. 1.1**

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Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-11-21	Release of final datasheet
1.1	2026-02-05	Update footnotes

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