IRXFR7446TR

PPD-98034A

Power MOSFET
Surface Mount (D-Pak)
40V, 56A, N-channel Technology

Features

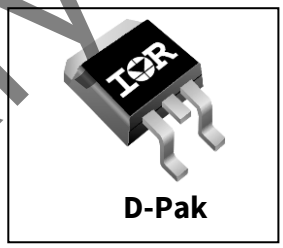
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully characterized Capacitance and Avalanche SOA
- Enhanced body diode dv/dt and di/dt Capability
- Lead solder dipped

Product Summary

- **BV_{DSS}:** 40V
- **I_D:** 56A
- **$R_{DS\ (on),\ max}$:** 3.9mΩ
- **$Q_{G,\ max}$:** 130nC

Potential Applications

- Brushed Motor drive applications
- BLDC Motor drive applications
- PWM Inverterized topologies
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters



D-Pak

Product Validation

JESD-22 Qualification

Description

IR HiRel technology provides high performance power MOSFETs.The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC-DC converters and motor controllers. These devices retain all the well-established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters. The package is offered in lead solder dipped.

Ordering Information

Table 1 Ordering options

Part number	Package	Part Marking	Standard Pack	
			Form	Quantity
IRXFR7446TR	D-Pak	XFR7446	Tape and Reel	500

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1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
I_D @ V_{GS} = 10V, T_C = 25°C	Continuous Drain Current	120 [1]	A
I_D @ V_{GS} = 10V, T_C = 100°C	Continuous Drain Current	84 [1]	A
I_D @ V_{GS} = 10V, T_C = 25°C	Continuous Drain Current	56*	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [2]	520	A
P_D @ T_C = 25°C	Maximum Power Dissipation	98	W
	Linear Derating Factor	0.66	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy [3, 6]	125	mJ
E_{AS}	Single Pulse Avalanche Energy [4]	251	mJ
I_{AR}	Avalanche Current [2]	See Fig 16, 17, 23, 24	A
E_{AR}	Repetitive Avalanche Energy [2]		mJ
dv/dt	Peak Diode Reverse Recovery [5]	4.8	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Lead Temperature	300 (1.6 mm from case for 10s)	

* Current is limited by package

[1] Calculated continuous current based on maximum allowable junction temperature. Current is limited to 56A by source bond technology. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refere to AN-1140)

[2] Repetitive rating: Pulse width limited by maximum junction temperature.

[3] Limited by $T_{jmax,}$ starting T_J = 25°C, L = 0.08mH, R_G=50Ω, I_{AS} =56A, V_{GS} = 10V

[4] Limited by $T_{jmax,}$ starting T_J = 25°C, L = 1mH, R_G=50Ω, I_{AS} = 22A, V_{GS} = 10V

[5] I_{SD} ≤ 56A, di/dt ≤ 1306A/µs, V_{DD} ≤ 40V, T_J ≤ 175°C

[6] 100% tested in final test production.

2 Device Characteristics

2.1 Electrical Characteristics

Table 3 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage [4]	40	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	26	—	mV/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance [4]	—	3.0	3.9	mΩ	V_{GS} = 10V, I_D = 56A [1]
		—	4.4	—		V_{GS} = 6.0V, I_D = 28A [1]
$V_{GS(th)}$	Gate Threshold Voltage [4]	2.2	3.0	3.9	V	V_{DS} = V_{GS}, I_D = 100µA
Gfs	Forward Transconductance	170	—	—	S	V_{DS} = 10V, I_{D2} = 56A
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	µA	V_{DS} = 40V, V_{GS} = 0V [4]
		—	—	150		V_{DS} = 40V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward [4]	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse [4]	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	65	130	nC	I_D = 56A V_{DS} = 20V V_{GS} = 10V
Q_{GS}	Gate-to-Source Charge	—	18	—		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	22	—		
$t_{d(on)}$	Turn-On Delay Time	—	9.8	—	ns	I_{D1} = 30A ** V_{DD} = 20V R_G = 2.7Ω V_{GS} = 10V
t_r	Rise Time	—	13	—		
$t_{d(off)}$	Turn-Off Delay Time	—	32	—		
t_f	Fall Time	—	20	—		
C_{iss}	Input Capacitance	—	3150	—	pF	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz
C_{oss}	Output Capacitance	—	480	—		
C_{rss}	Reverse Transfer Capacitance	—	330	—		
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	—	570	—		V_{GS} = 0V, V_{DS} = 0V to 32V [2]
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)	—	680	—		V_{GS} = 0V, V_{DS} = 0V to 32V [3]
R_G	Gate Resistance	—	1.5	—	Ω	f = 1.0MHz, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

[2] Coss eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

[3] Coss eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

[4] 100% tested in final test production.

2.2 Source-Drain Diode Ratings and Characteristics

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	120	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	480	A	
V_{SD}	Diode Forward Voltage [5]	—	0.9	1.3	V	T_J = 25°C, I_S = 56A, V_{GS} = 0V [2]
t_{rr}	Reverse Recovery Time	—	20	—	ns	T_J = 25°C, I_F = 56A, V_{DD} ≤ 34V di/dt = 100A/µs
Q_{rr}	Reverse Recovery Charge	—	13	—	nC	
I_{rrM}	Reverse Recovery Current	—	1.8	—	A	
t_{rr}	Reverse Recovery Time	—	21	—	ns	T_J = 125°C, I_F = 56A, V_{DD} ≤ 34V di/dt = 100A/µs
Q_{rr}	Reverse Recovery Charge	—	13	—	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) *				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case [3]	—	—	1.52	°C/W
$R_{\theta JA}$	Junction-to- Ambient (PCB mount) [4]	—	—	50	
$R_{\theta JA}$	Junction-to- Ambient [3]	—	—	110	

[1] Repetitive rating; Pulse width limited by maximum junction temperature.

[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

[3] R_θ is measured at T_J approximately 90°C

[4] When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

[5] 100% tested in final test production.

* L_D and L_S are Internal Drain Inductance and Internal Source Inductance.

3 Electrical Characteristics Curves

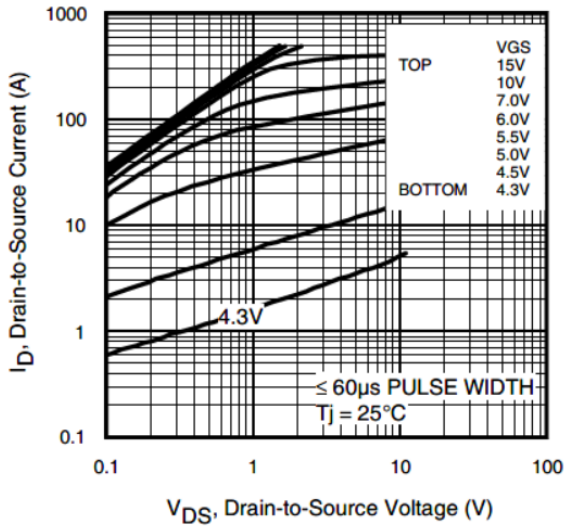


Figure 1 Typical Output Characteristics

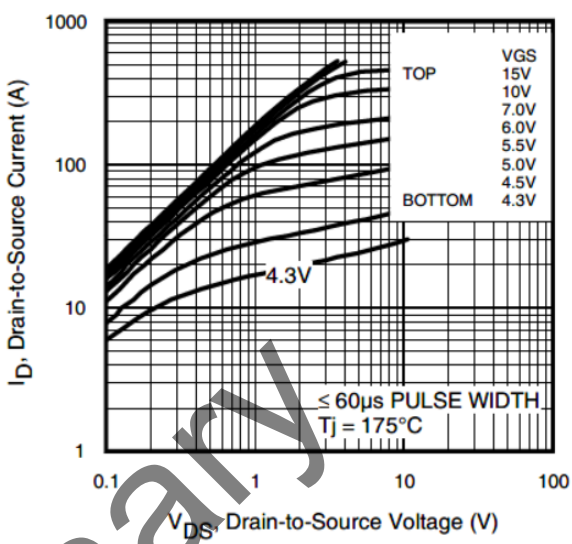


Figure 2 Typical Output Characteristics

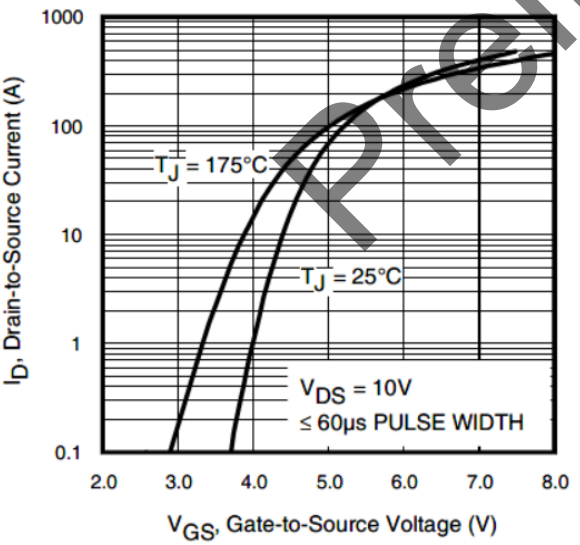


Figure 3 Typical Transfer Characteristics

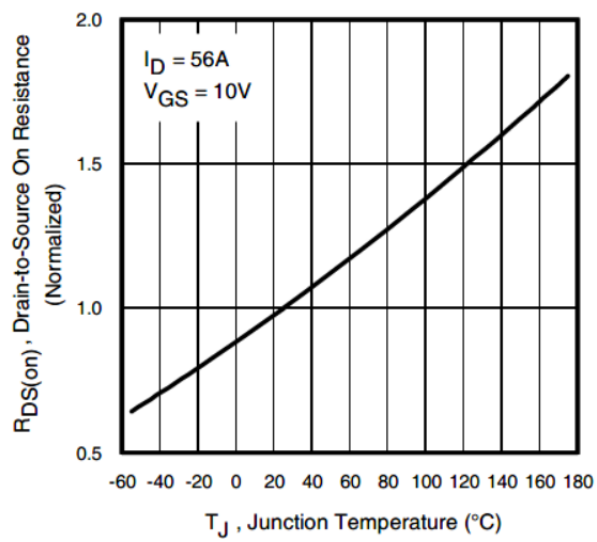


Figure 4 Normalized On-Resistance Vs. Temperature

Electrical Characteristics Curves

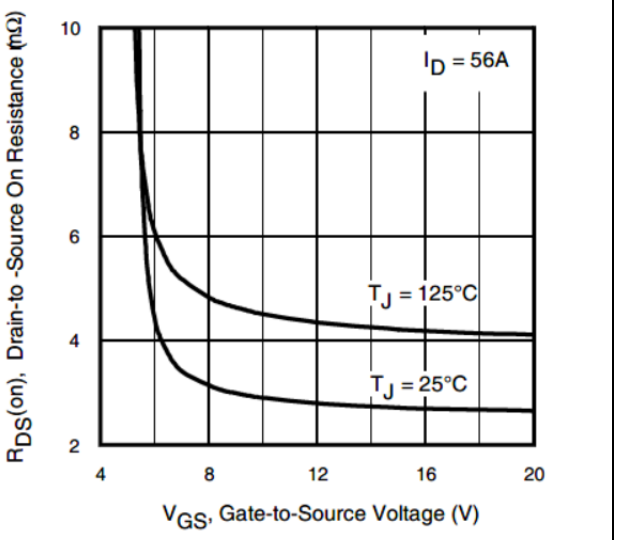


Figure 5 Typical On-Resistance Vs. Gate Voltage

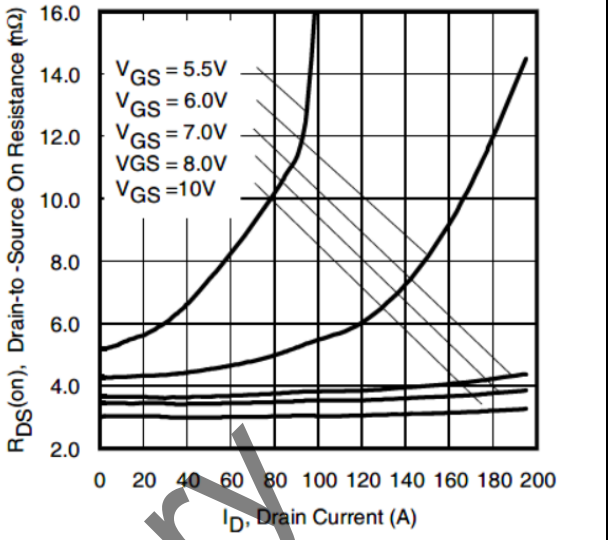


Figure 6 Typical On-Resistance Vs. Drain Current

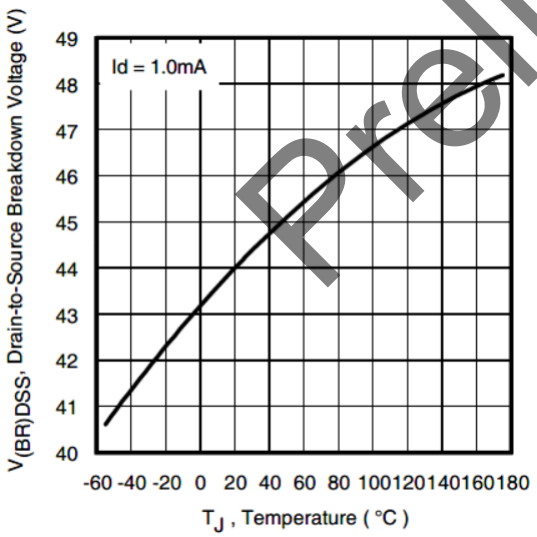


Figure 7 Typical Drain -to-Source Breakdown Voltage Vs. Temperature

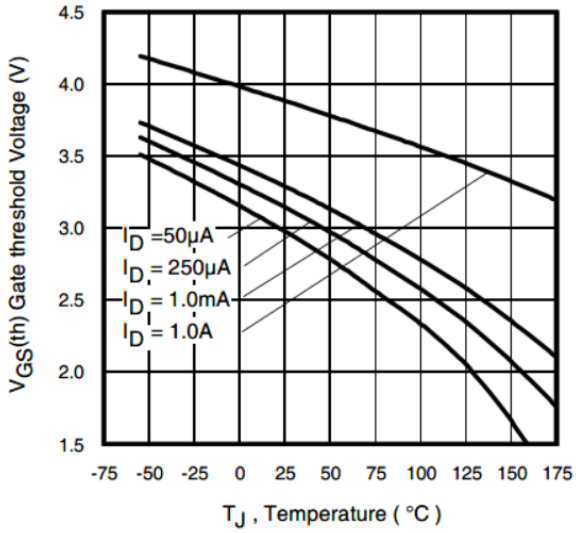


Figure 8 Typical Threshold Voltage Vs. Temperature

Electrical Characteristics Curves

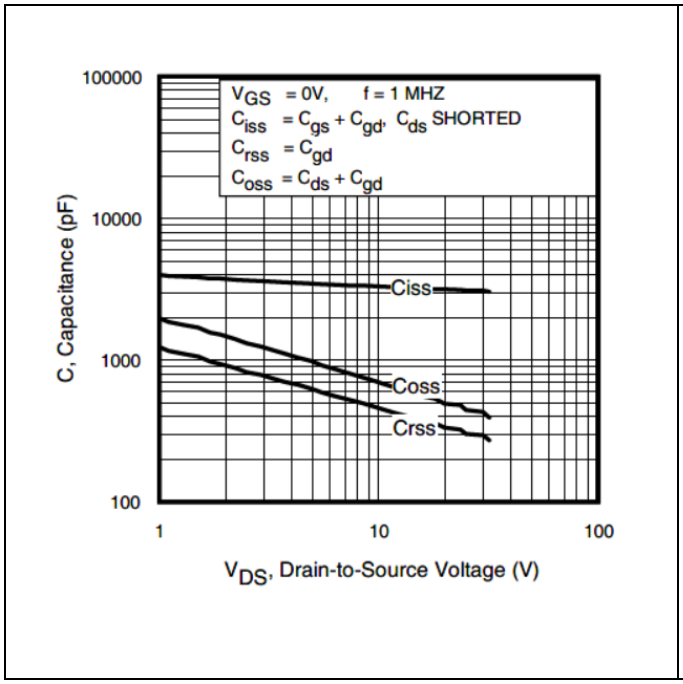


Figure 9 Typical Capacitance Vs. Drain-to-Source Voltage

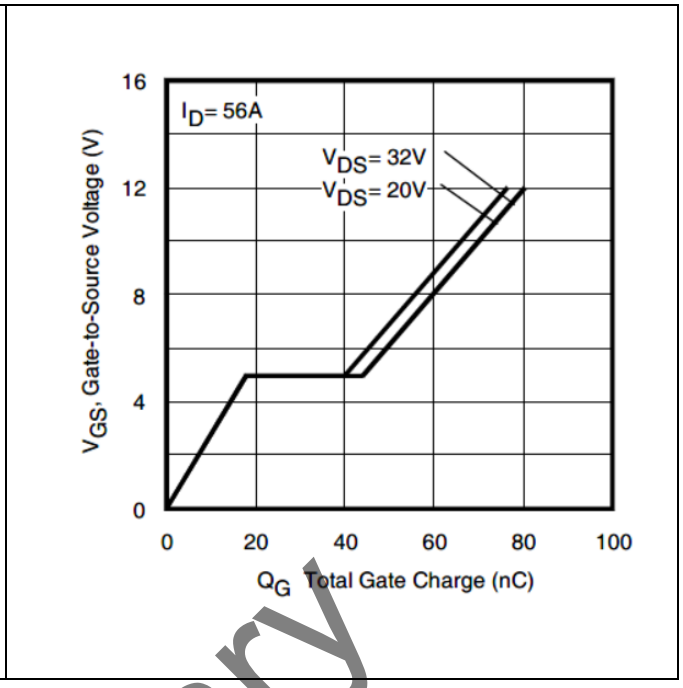


Figure 10 Typical Gate Charge Vs. Gate -to -Source Voltage

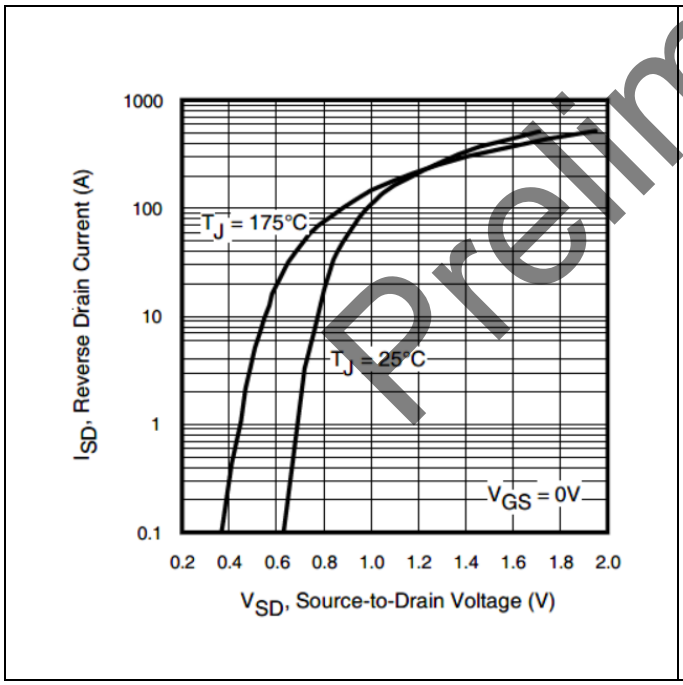


Figure 11 Typical Source-Drain Current Vs. Diode Forward Voltage

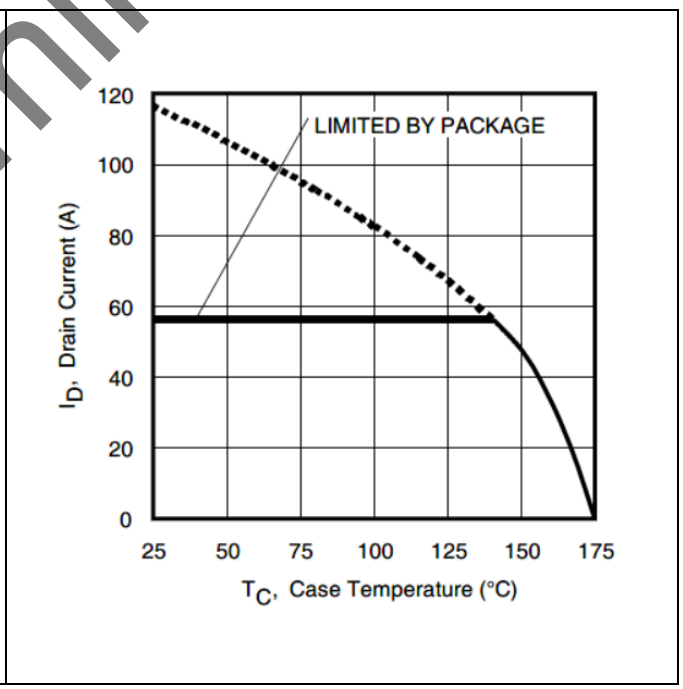


Figure 12 Maximum Drain Current Vs. Case Temperature

Electrical Characteristics Curves

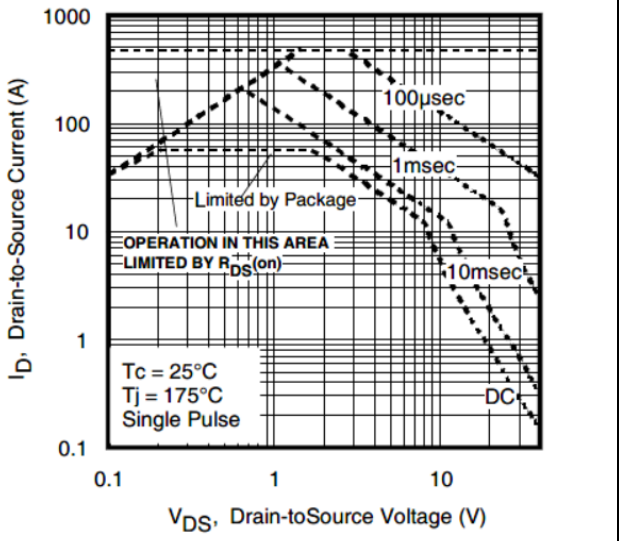


Figure 13 Maximum Safe Operating Area

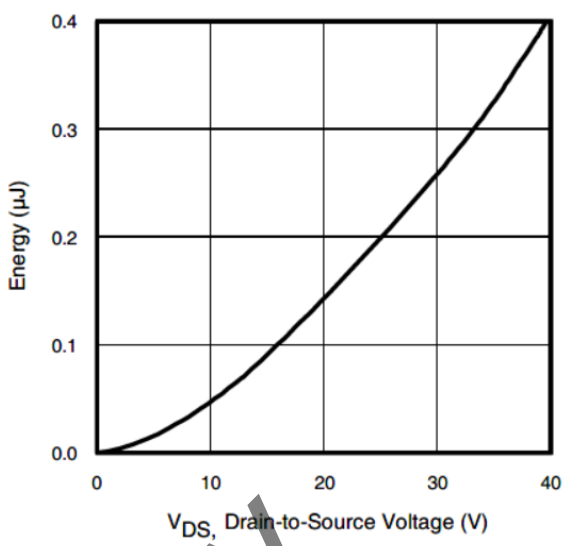


Figure 14 Typical C_{oss} Stored Energy

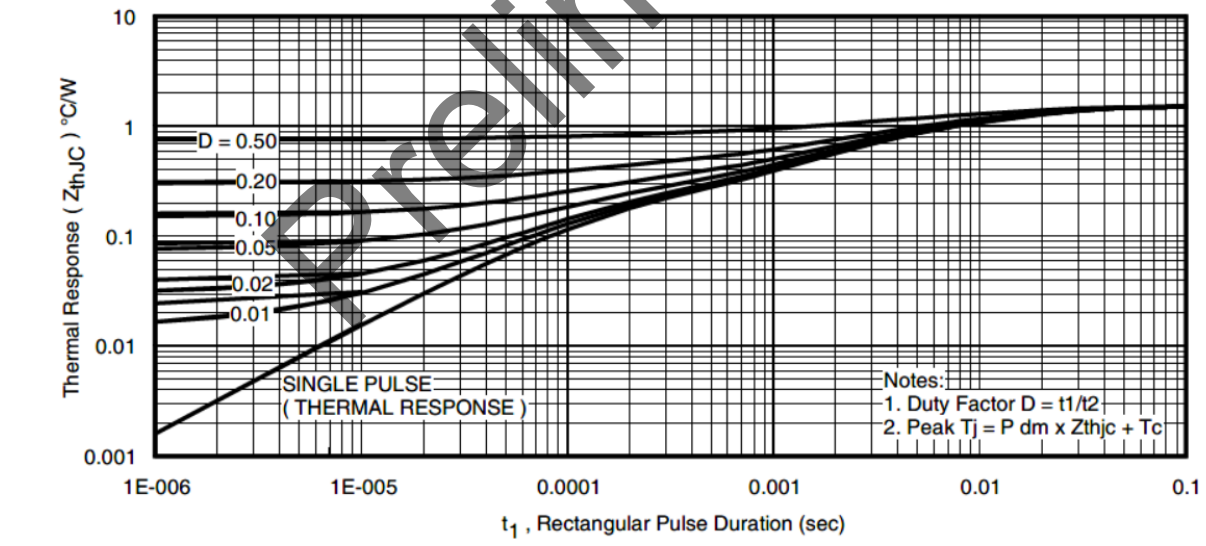
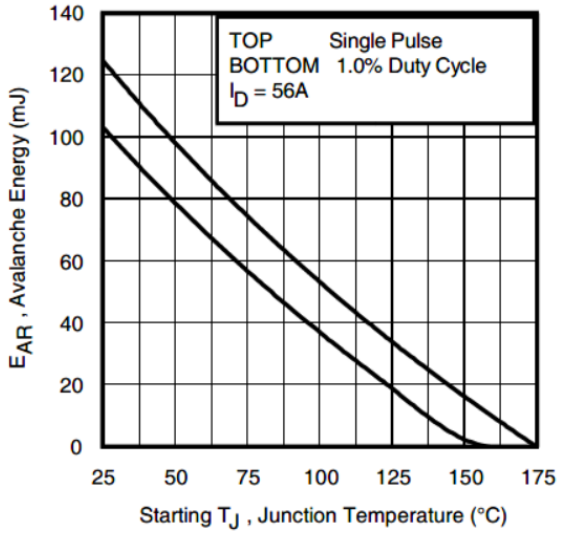


Figure 15 Maximum Effective Transient Thermal Impedance, Junction-to-Case

Electrical Characteristics Curves



Notes on Repetitive Avalanche Curves , Figures 17, 18:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of Tjmax. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asTjmax is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 24, 25.
4. PD (ave) = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase
during avalanche).
6. Iav = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed Tjmax (assumed as 25°C in Figure 17, 18).
tav = Average time in avalanche.
D = Duty cycle in avalanche = tav ·f

ZthJC(D, tav) = Transient thermal resistance, see Figures 16)

$$P_{D\,(ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\,(AR)} = P_{D\,(ave)} \cdot t_{av}$$

Figure 16 Maximum Avalanche Energy vs. Temperature

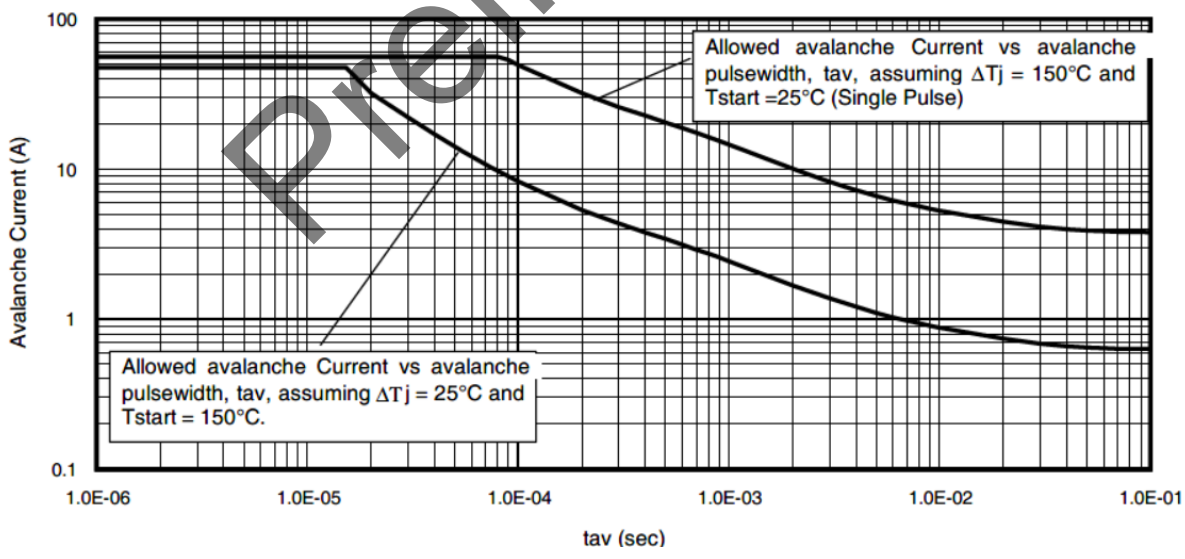


Figure 17 Typical Avalanche Current vs. Pulsewidth

Electrical Characteristics Curves

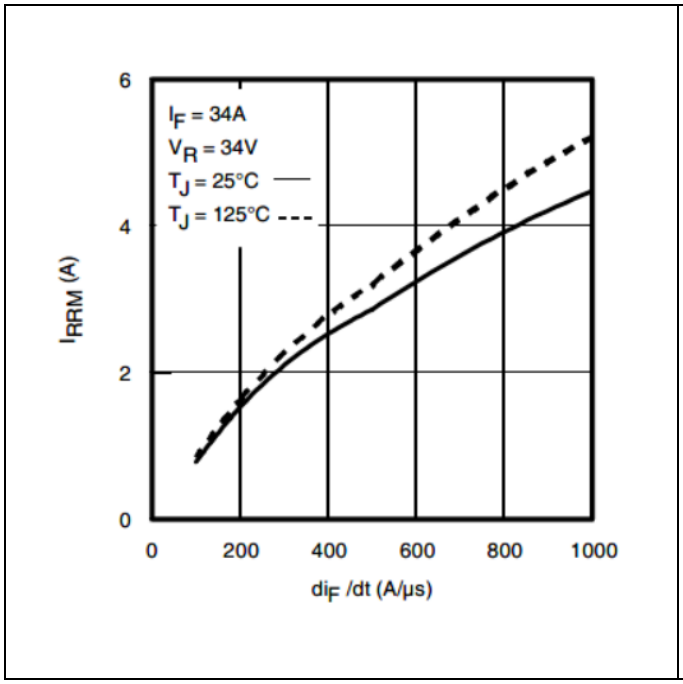


Figure 18 Typical Recovery Current Vs. di_f/dt

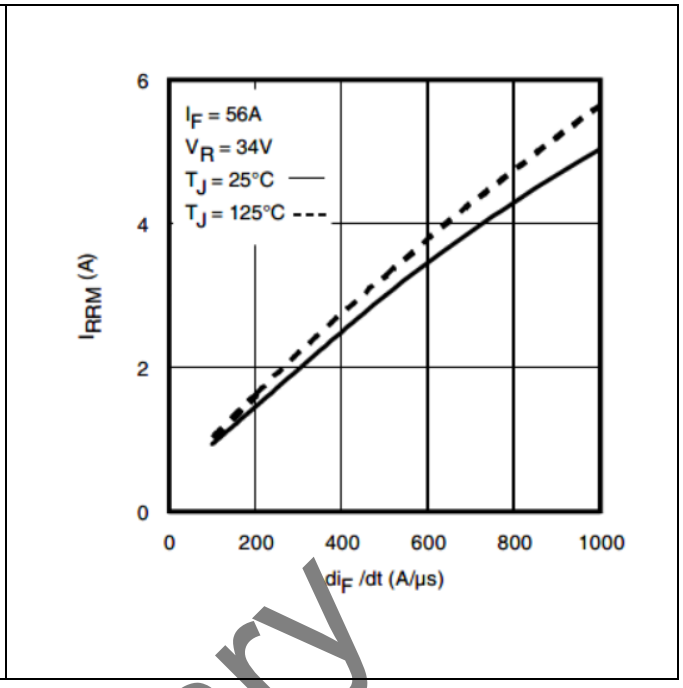


Figure 19 Typical Recovery Current Vs. di_f/dt

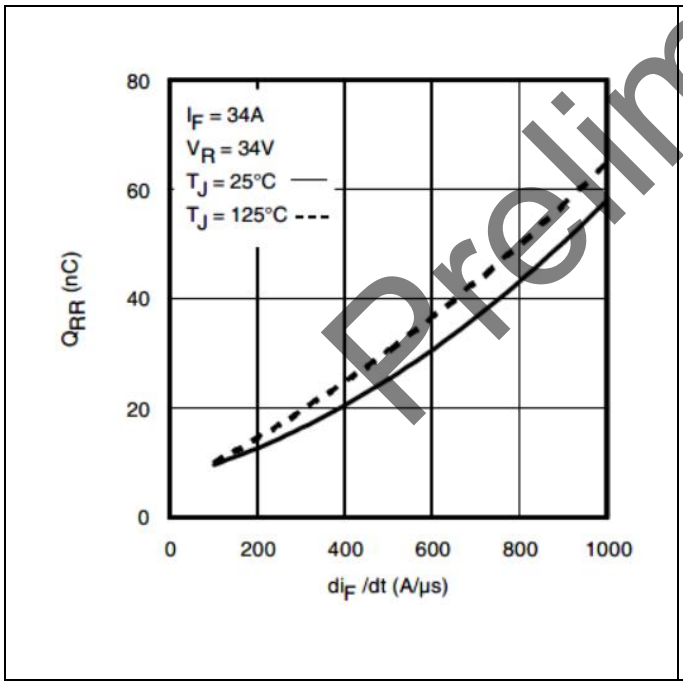


Figure 20 Typical Stored Charge Vs. di_f/dt

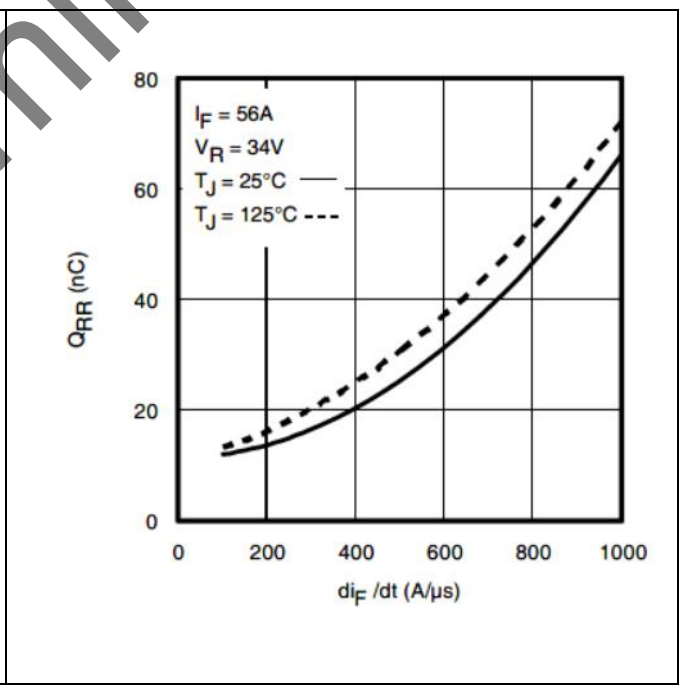


Figure 21 Typical Stored Charge Vs. di_f/dt

4 Test Circuits

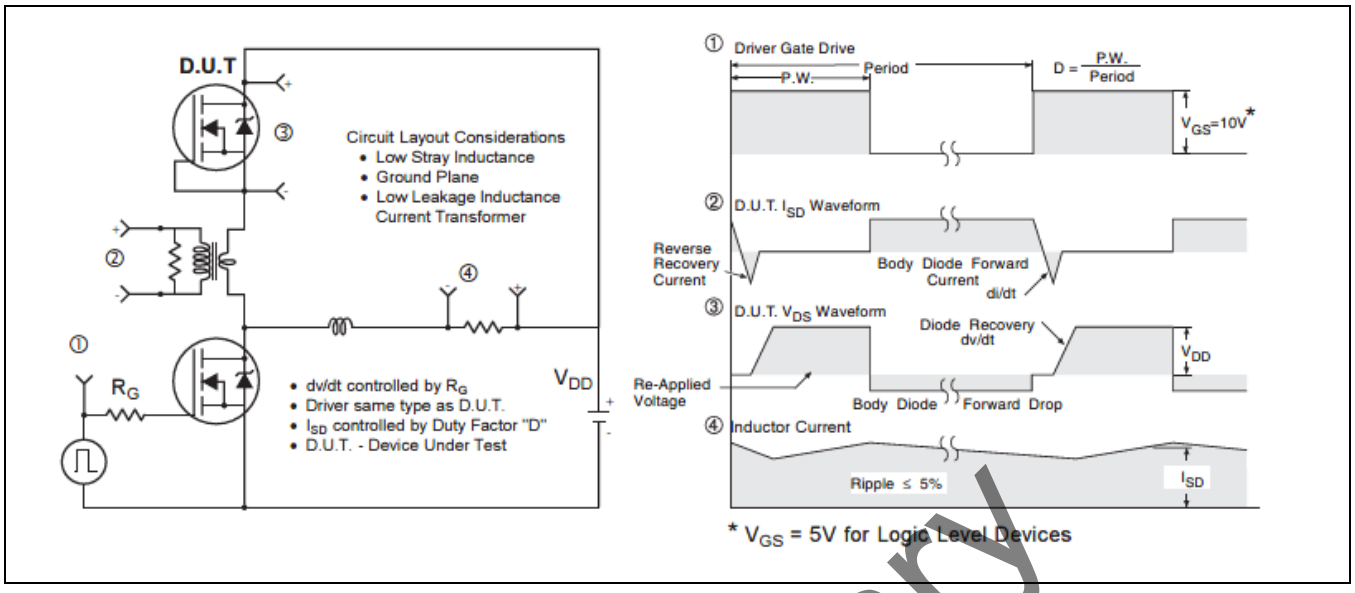


Figure 22 Peak Diode Recovery dv/dt Test Circuit for N -Channel

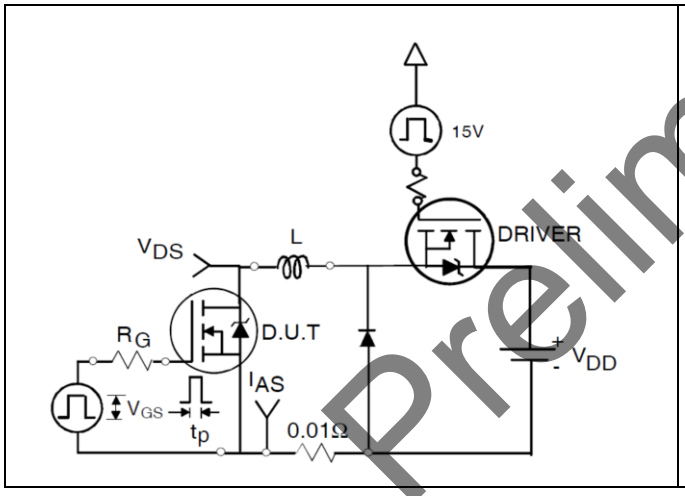


Figure 23 Unclamped Inductive Test Circuit

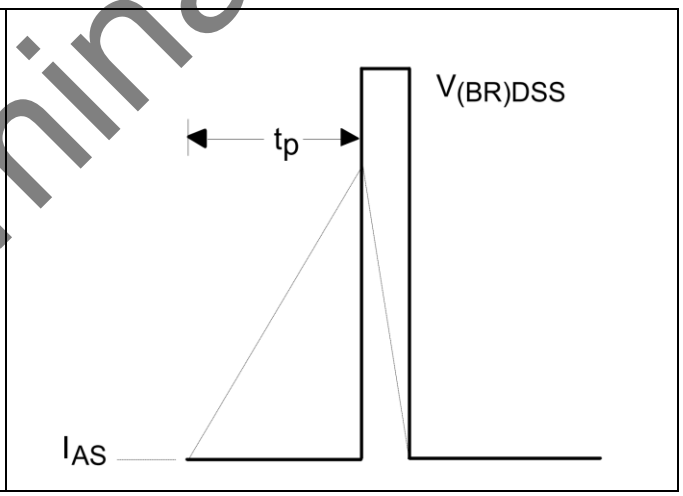


Figure 24 Unclamped Inductive Waveform

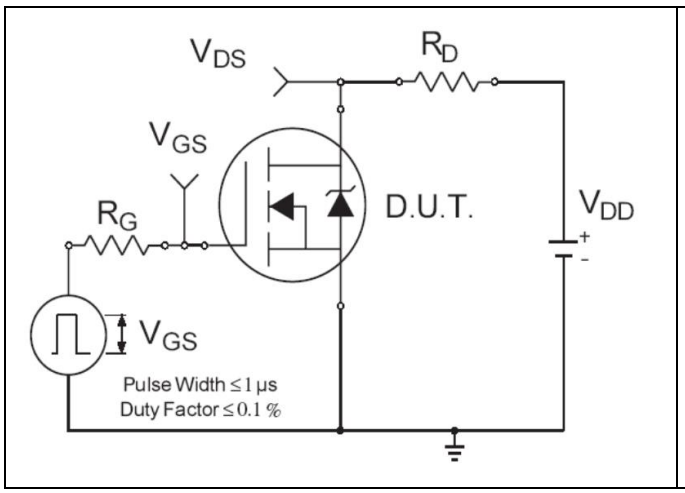


Figure 25 Switching Time Test Circuit

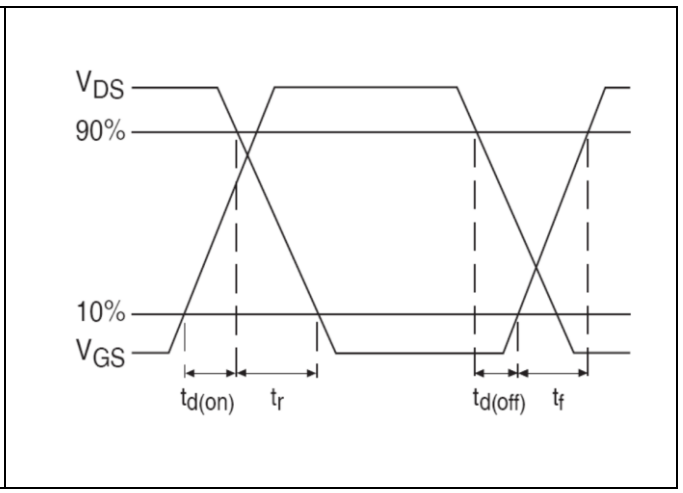


Figure 26 Switching Time Waveforms

Test Circuits

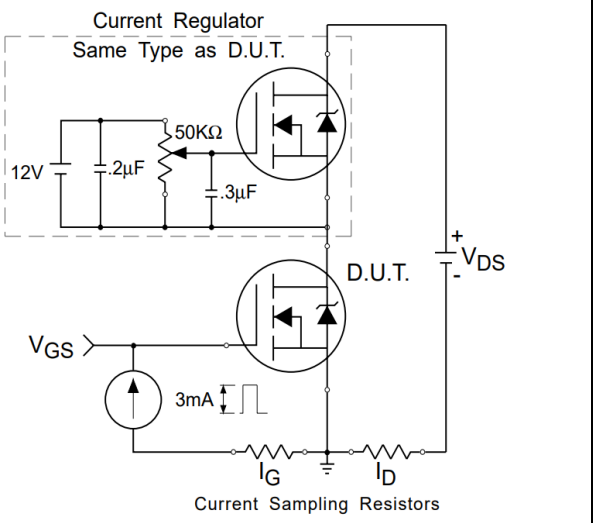


Figure 27 Gate Charge Test Circuit

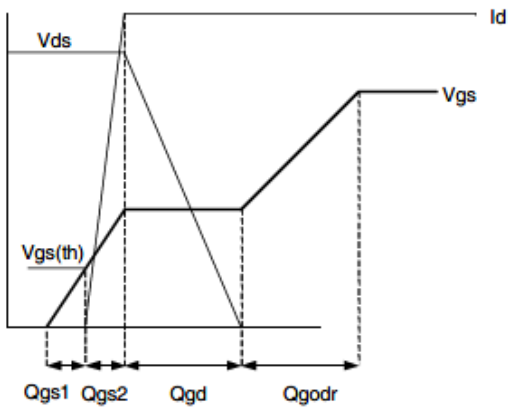
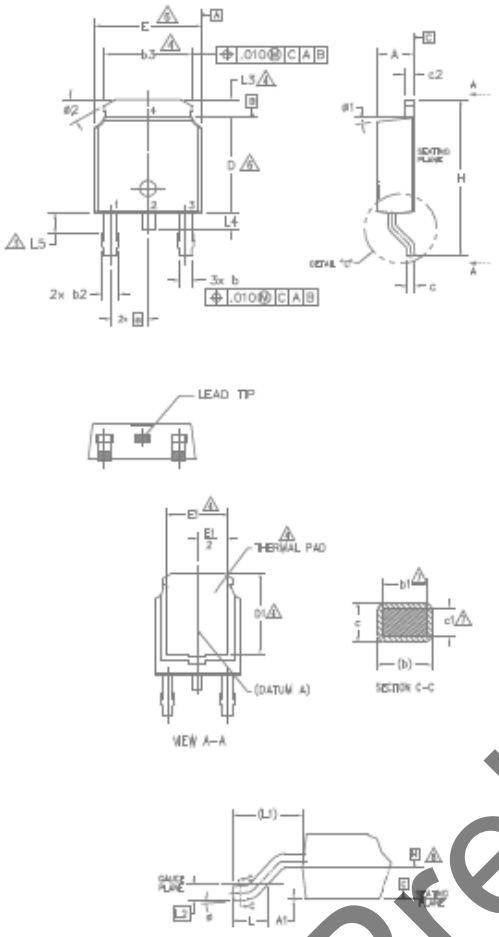


Figure 28 Gate Charge Waveform

5 Package Outline

Note: For the most updated package outline, please see the website: [D-Pak (TO-252AA)]



NOTES:
1.– DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2.– DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
3.– LEAD DIMENSION UNCONTROLLED IN L5.
4.– DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5.– SECTION C–C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
6.– DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
7.– DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
8.– DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
9.– OUTLINE CONFORMS TO JEDEC OUTLINE TO–252AA.

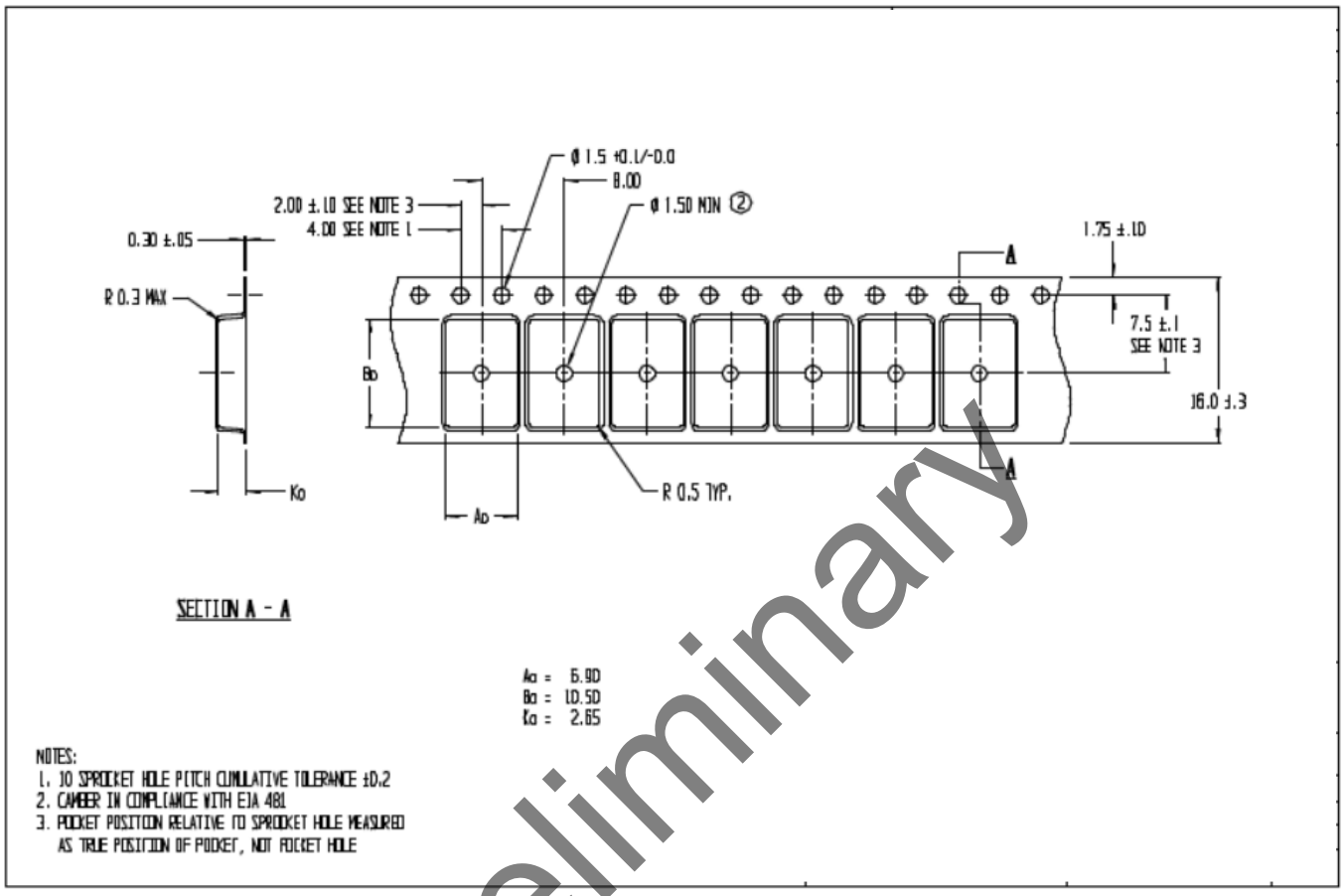
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	–	0.13	–	.005	
b	0.64	0.89	.025	.035	
b1	0.64	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	6
E1	4.32	–	.170	–	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L3	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	–	1.02	–	.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	
ø2	25°	35°	25°	35°	

LEAD ASSIGNMENTS

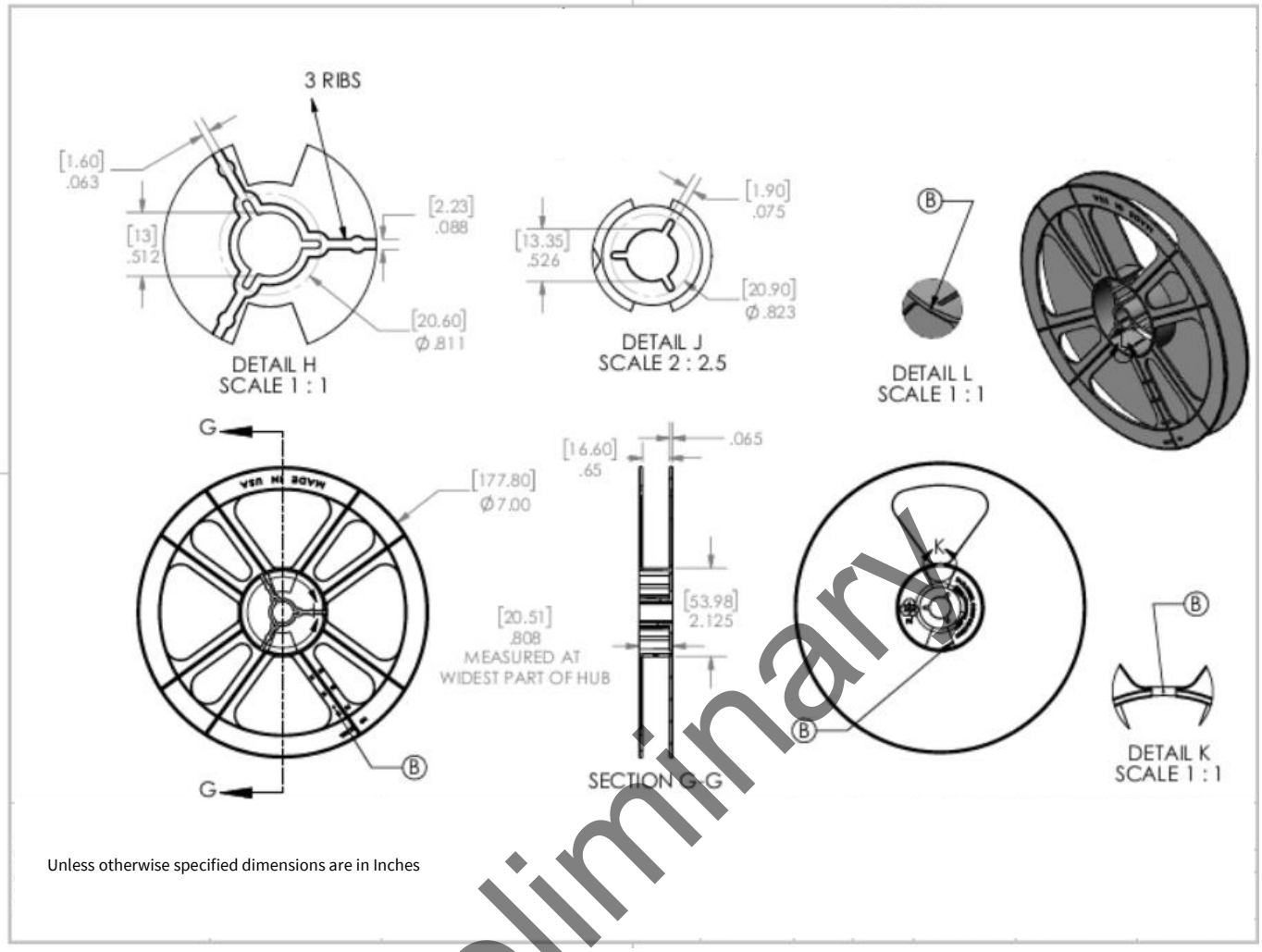
HEXFET
1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBT & CoPAK
1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

6 Tape and Reel Information



Tape and Reel Information



Revision history

Document version	Date of release	Description of changes
	12/16/2025	Preliminary datasheet with PPD number (PPD-98034)
Rev. A	01/27/2026	Added Tape and Reel -page 15 -16

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