

IRXF5210STRL

PPD-98017B

Power MOSFET Surface Mount (D²PAK (TO-263)) 100V, -38A, P-channel Technology

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead solder dipped

Potential Applications

- Brushed Motor drive applications
- BLDC Motor drive applications
- PWM Inverterized topologies

Product Validation

JESD-22 Qualification

Description

IR HiRel technology provides high performance power MOSFETs. The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC-DC converters and motor controllers. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters. The package is offered in lead solder dipped.

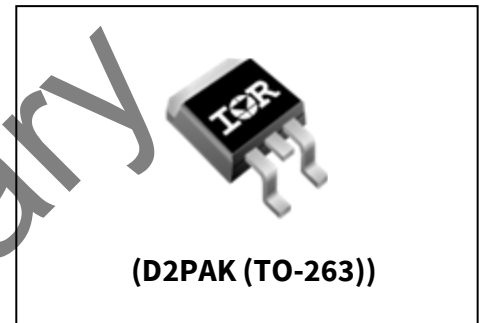
Ordering Information

Table 1 **Ordering options**

Part number	Package	Part Marking	Standard Pack	
			Form	Quantity
IRXF5210STRL	D2 PAK(TO-263)	XF5210S	Tape and Reel	500

Product Summary

- BV_{DSS} : -100V
- I_D : -38A
- $R_{DS(on), max}$: 60m Ω
- Q_G, max : 230nC



Power MOSFET Surface Mount (D2PAK (TO-263))

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Power MOSFET Surface Mount (D2PAK (TO-263))
Absolute Maximum Ratings
1 Absolute Maximum Ratings
Table 2 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
$I_D @ V_{GS} = -10V, T_C = 25^\circ C$	Continuous Drain Current	-38	A
$I_D @ V_{GS} = -10V, T_C = 100^\circ C$	Continuous Drain Current	-24	A
$I_{DM} @ T_C = 25^\circ C$	Pulsed Drain Current ¹	-140	A
$P_D @ T_A = 25^\circ C$	Maximum Power Dissipation	3.1	W
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	170	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ^{2, 4}	120	mJ
I_{AR}	Avalanche Current ¹	-23	A
E_{AR}	Repetitive Avalanche Energy ¹	17	mJ
dv/dt	Peak Diode Reverse Recovery ³	-7.4	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	

¹ Repetitive rating: Pulse width limited by maximum junction temperature.

² Starting $T_J = 25^\circ C$, $L = 0.46mH$, $R_G = 25\Omega$, $I_{AS} = -23A$, $V_{GS} = 10V$
³ $I_{SD} \leq -23A$, $di/dt \leq -650A/\mu s$, $V_{DD} \leq -100V$, $T_J \leq 150^\circ C$
⁴ 100% tested in final test production.

Power MOSFET Surface Mount (D2PAK (TO-263))
Device Characteristics
2 Device Characteristics
2.1 Electrical Characteristics
Table 3 Static and Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage ²	-100	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.11	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1.0\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ²	—	—	60	m Ω	$V_{GS} = -10V, I_D = -38A^1$
$V_{GS(th)}$	Gate Threshold Voltage ²	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
G_{fs}	Forward Transconductance	9.5	—	—	S	$V_{DS} = -50V, I_D = -23A$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-50	μA	$V_{DS} = -100V, V_{GS} = 0V^2$
		—	—	-250		$V_{DS} = -80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward ²	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Leakage Reverse ²	—	—	100		$V_{GS} = 20V$
Q_G	Total Gate Charge	—	150	230	nC	$I_D = -23A$
Q_{GS}	Gate-to-Source Charge	—	22	33		$V_{DS} = -80V$
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	81	120		$V_{GS} = -10V$
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$I_{D1} = -23A^{**}$
t_r	Rise Time	—	63	—		$V_{DD} = -50V$
$t_{d(off)}$	Turn-Off Delay Time	—	72	—		$R_G = 2.4\Omega$
t_f	Fall Time	—	55	—		$V_{GS} = -10V$
C_{iss}	Input Capacitance	—	2780	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	800	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	430	—		$f = 1.0\text{MHz}$

** Switching speed maximum limits are based on manufacturing test equipment and capability.

¹ Pulse width $\leq 300\mu s$; Duty Cycle $\leq 2\%$
² 100% tested in final test production.

Power MOSFET Surface Mount (D2PAK (TO-263))
Device Characteristics
2.2 Source-Drain Diode Ratings and Characteristics
Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-38	A	
I_{SM}	Pulsed Source Current (Body Diode) ¹	—	—	-140	A	
V_{SD}	Diode Forward Voltage ⁴	—		-1.6	V	$T_J = 25^\circ\text{C}$, $I_S = -23\text{A}$, $V_{GS} = 0\text{V}$ ²
t_{rr}	Reverse Recovery Time	—	170	260	ns	$T_J = 25^\circ\text{C}$, $I_F = -23\text{A}$, $V_{DD} \leq -25\text{V}$ $di/dt = -100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovery Charge	—	1180	1770	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible				

2.3 Thermal Characteristics
Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	0.75	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount) ³	—	—	40	

¹ Repetitive rating; Pulse width limited by maximum junction temperature.

² Pulse width $\leq 300 \mu\text{s}$; Duty Cycle $\leq 2\%$
³ When mounted on 1" square PCB (FR-4 for G-10 Material). For recommended footprint and soldering techniques refer to application note # AN-994

⁴ 100% tested in final test production.

Power MOSFET Surface Mount (D2PAK (TO-263))

Electrical Characteristics Curves

3 Electrical Characteristics Curves

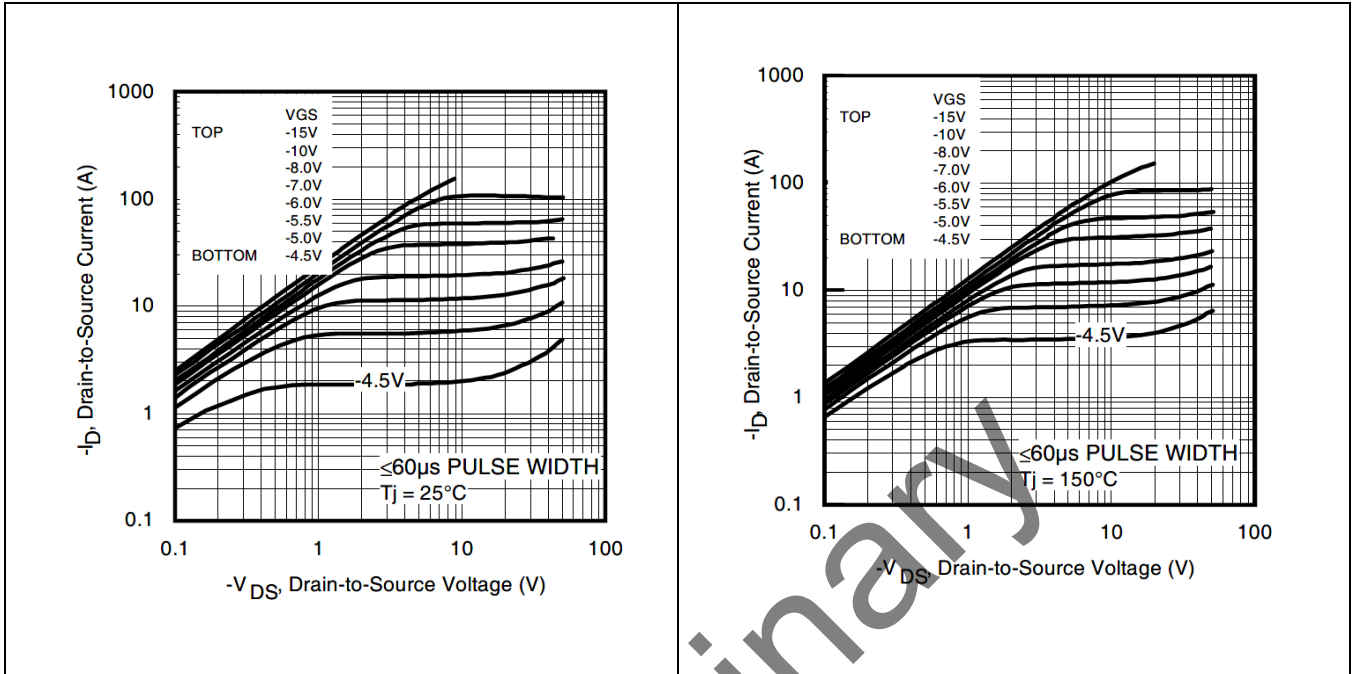


Figure 1 Typical Output Characteristics

Figure 2 Typical Output Characteristics

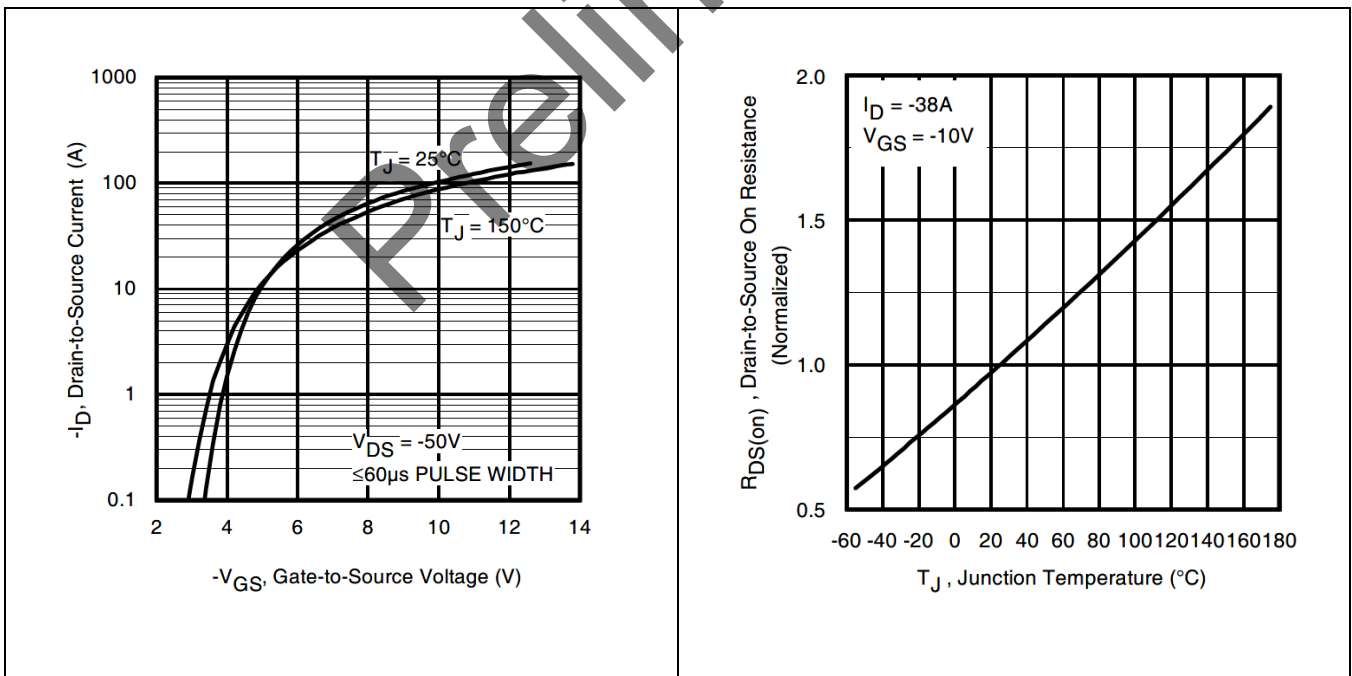


Figure 3 Typical Transfer Characteristics

Figure 4 Normalized On-Resistance Vs. Temperature

Power MOSFET Surface Mount (D2PAK (TO-263))

Electrical Characteristics Curves

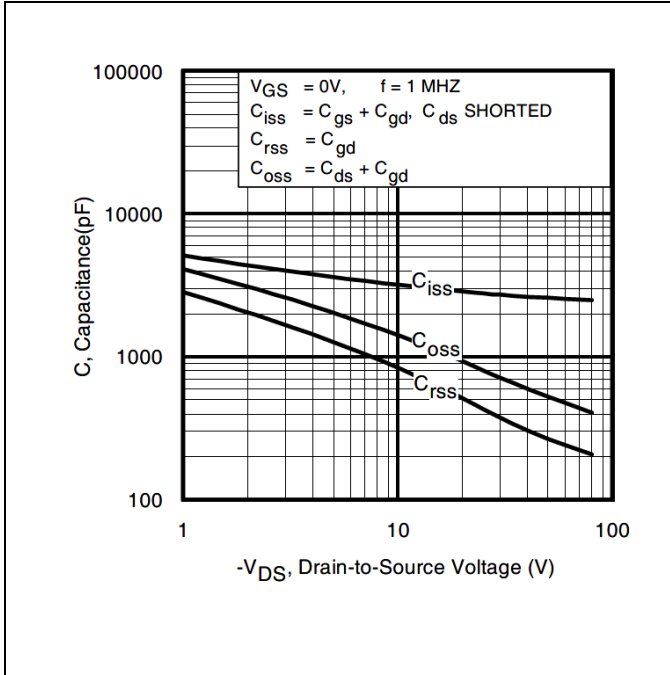


Figure 5 Typical Capacitance Vs. Drain-to-Source Voltage

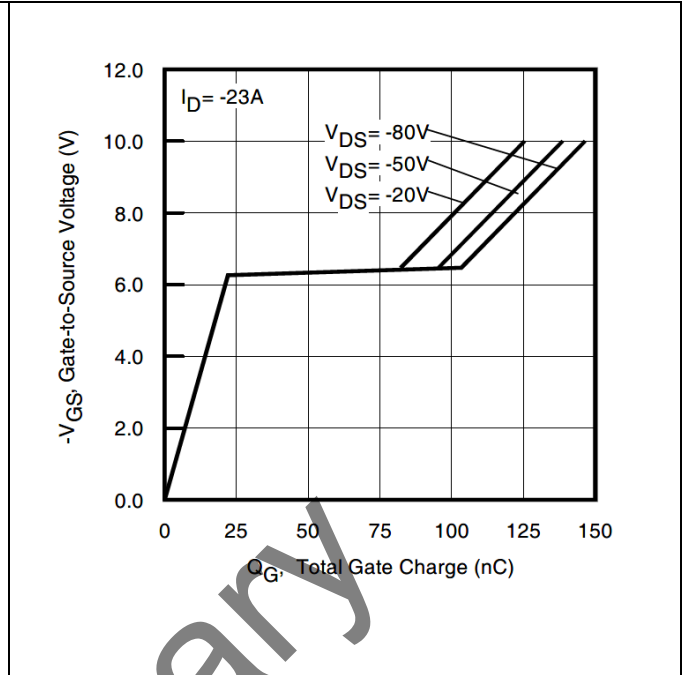


Figure 6 Typical Gate Charge Vs. Gate-to-Source Voltage

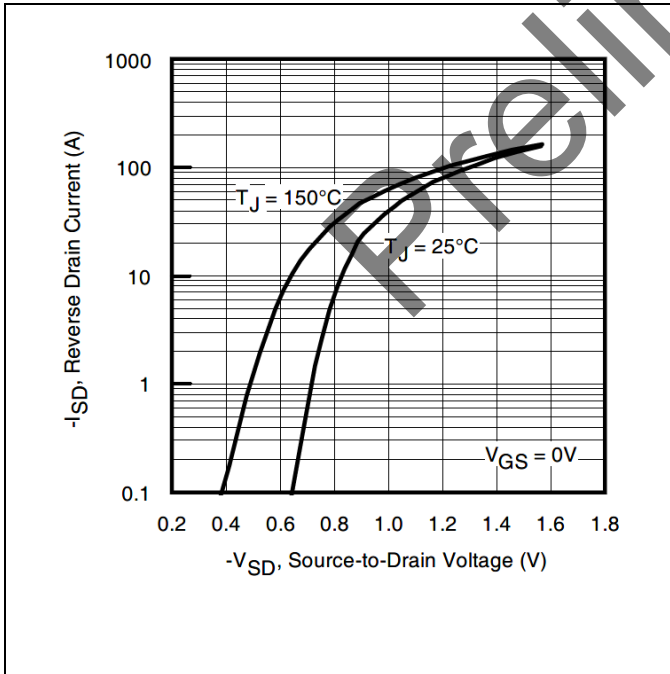


Figure 7 Typical Source-Drain Current Vs. Diode Forward Voltage

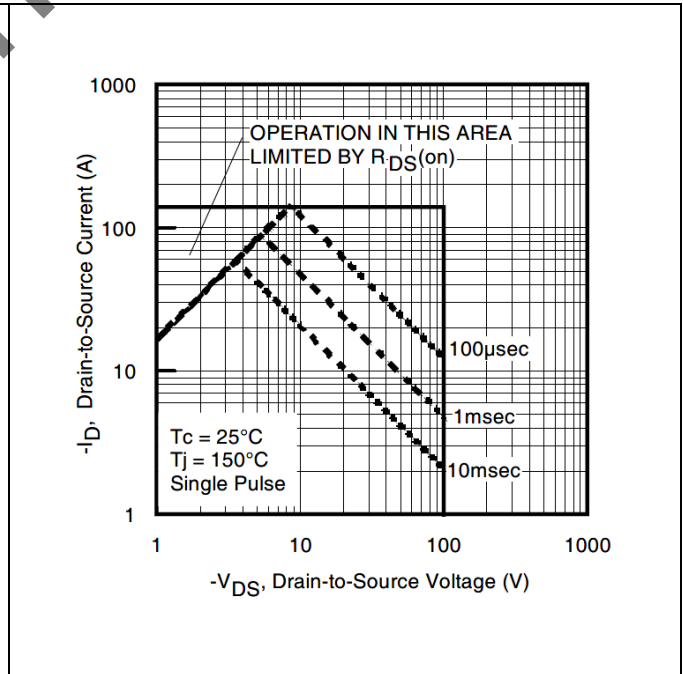


Figure 8 Maximum Safe Operating Area

Power MOSFET Surface Mount (D2PAK (TO-263))

Electrical Characteristics Curves

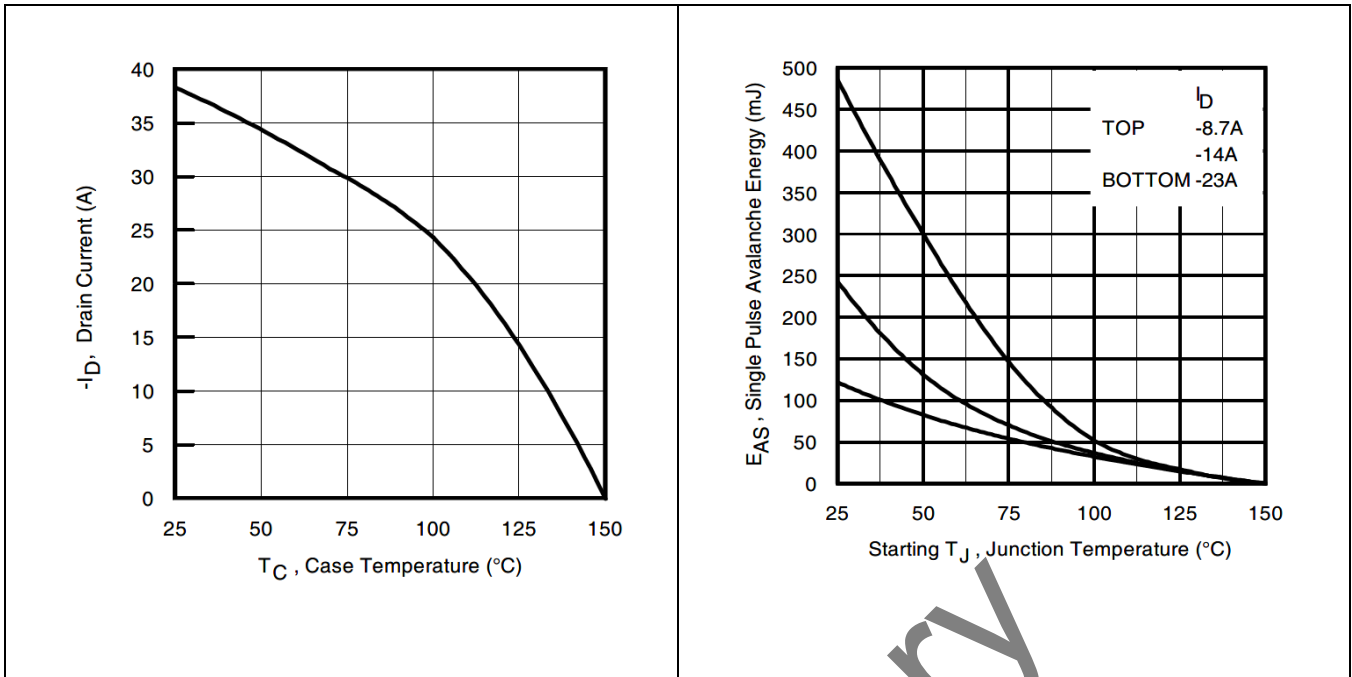


Figure 9 Maximum Drain Current vs. Case Temperature

Figure 10 Maximum Avalanche Energy vs. Temperature

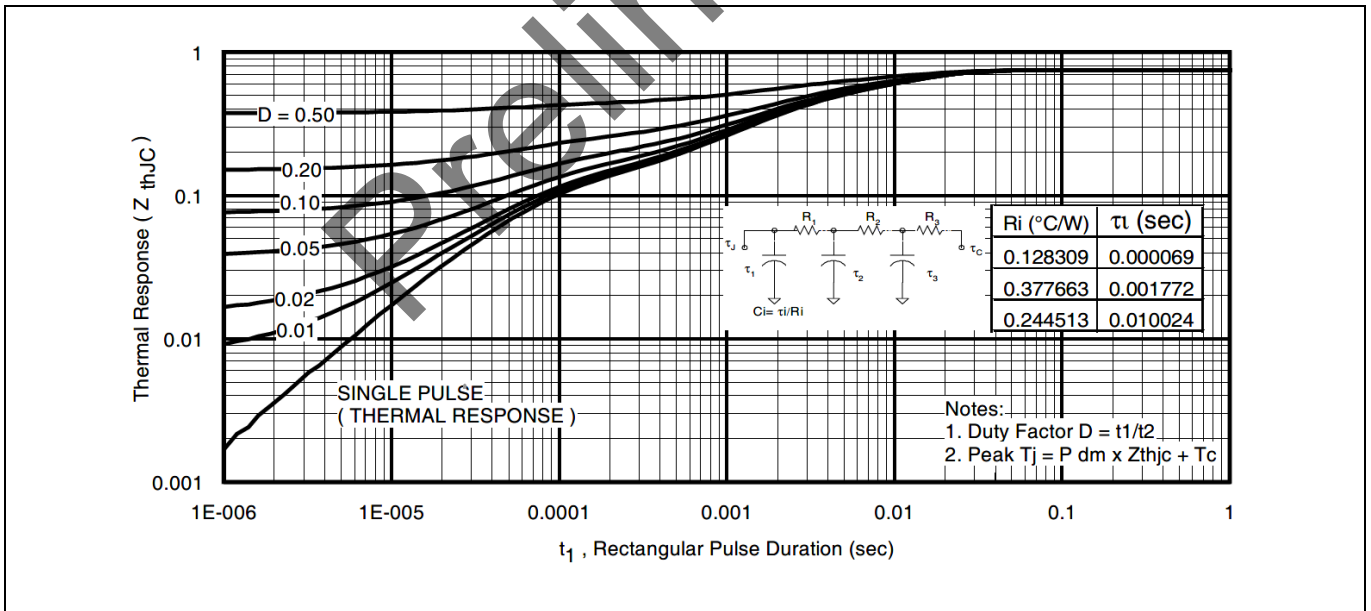


Figure 11 Maximum Effective Transient Thermal Impedance, Junction-to-Case

Power MOSFET Surface Mount (D2PAK (TO-263))

Test Circuits

4 Test Circuits

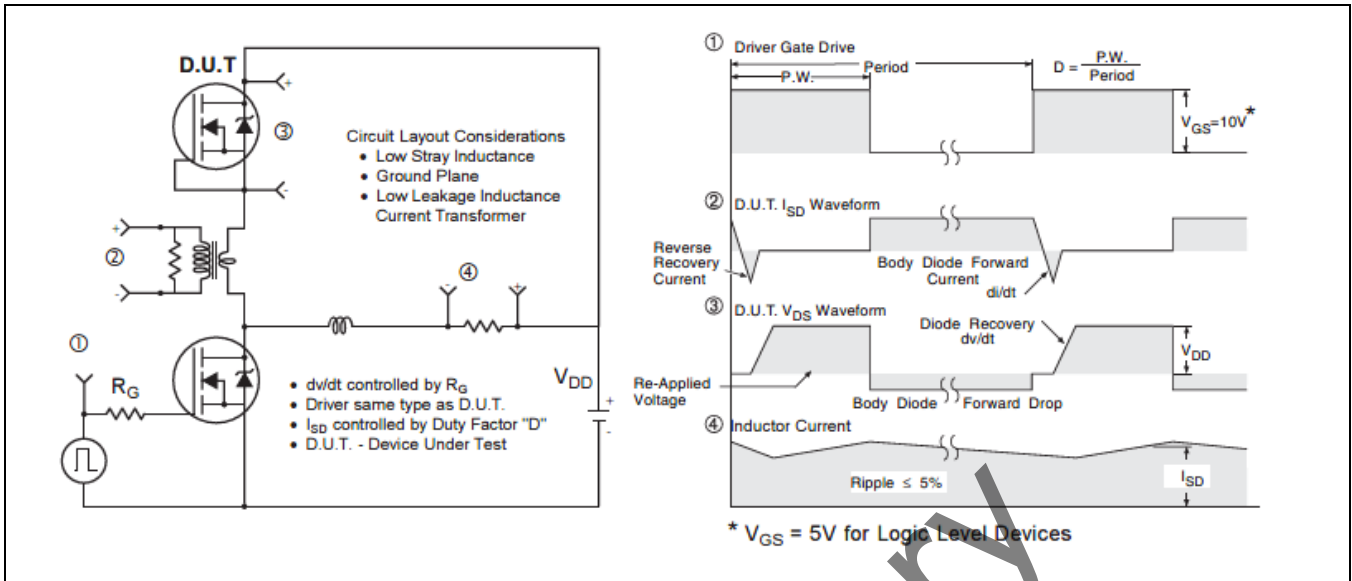


Figure 12 Peak Diode Recovery dv/dt Test Circuit for P-Channel

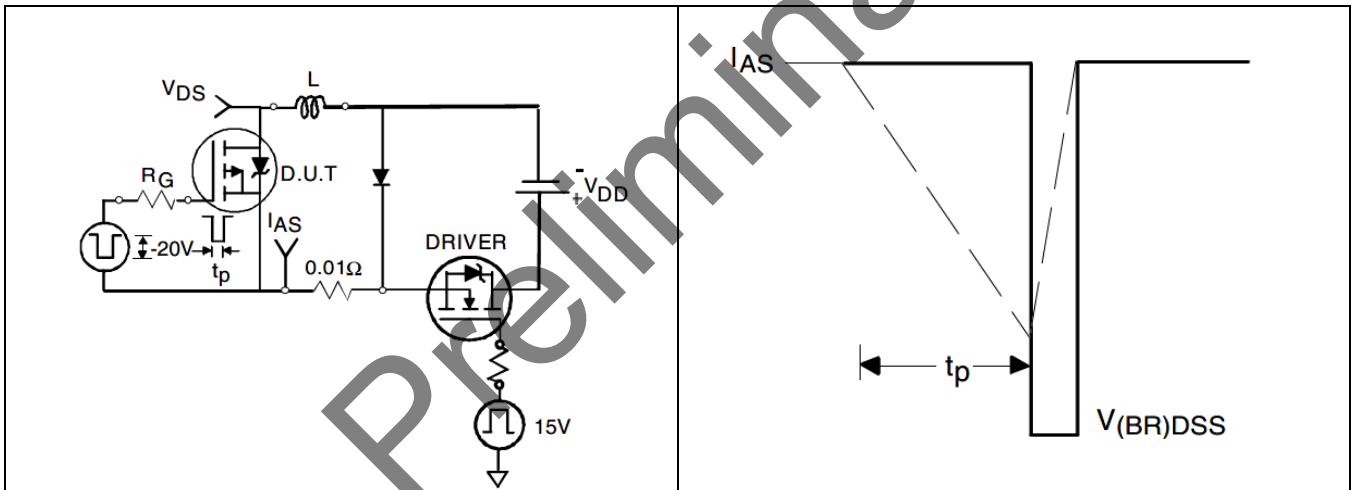


Figure 13 Unclamped Inductive Test Circuit

Figure 14 Unclamped Inductive Waveform

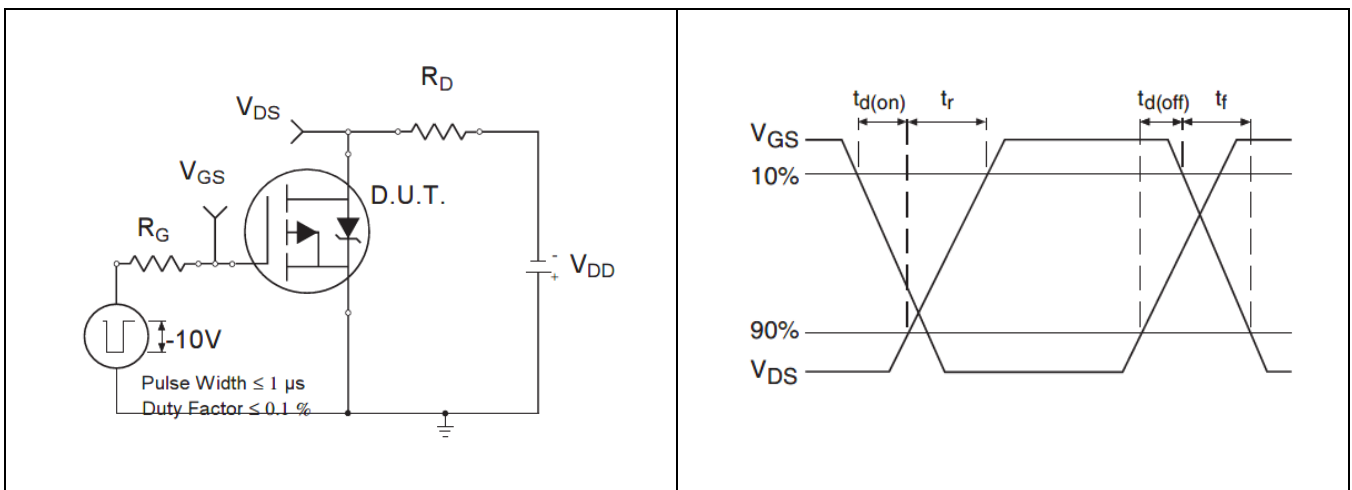


Figure 15 Switching Time Test Circuit

Figure 16 Switching Time Waveforms

Power MOSFET Surface Mount (D2PAK (TO-263))

Test Circuits

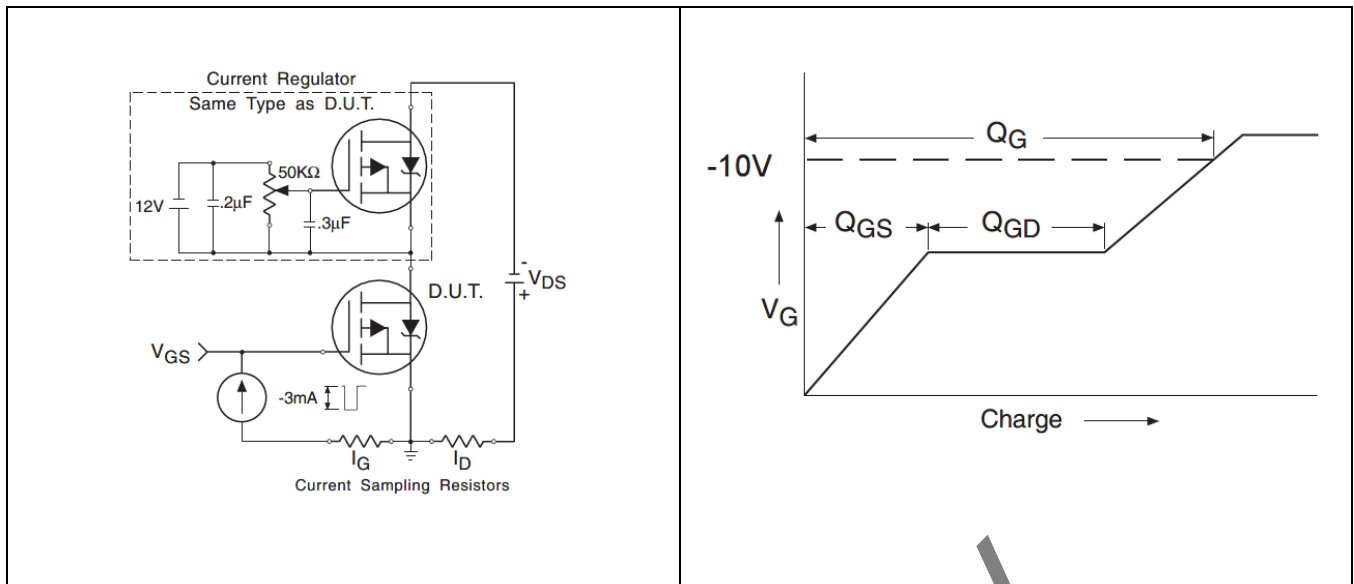


Figure 17 Gate Charge Test Circuit

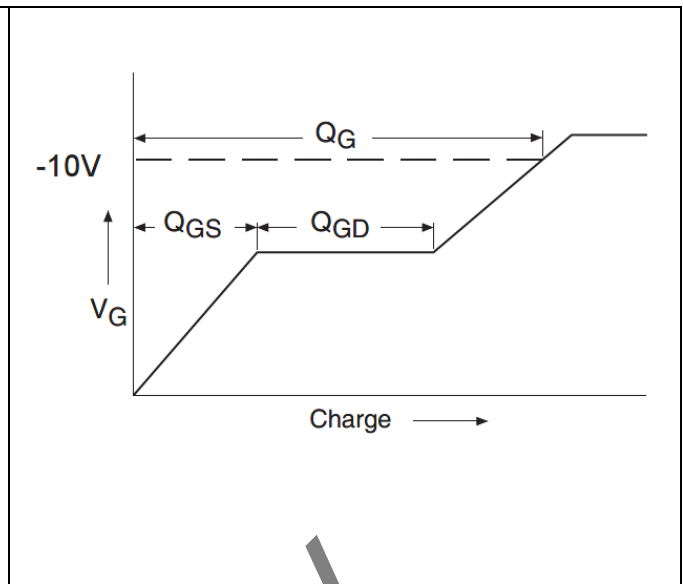


Figure 18 Gate Charge Waveform

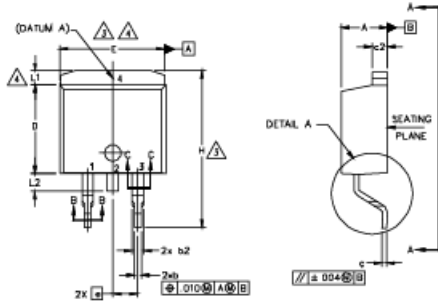
Preliminary

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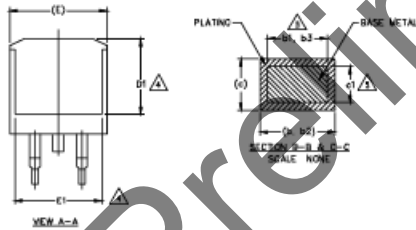
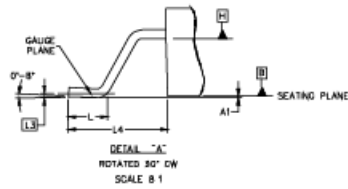
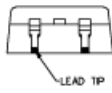
Package Outline

5 Package Outline

Note: For the most updated package outline, please see the website: [D² Pak \(TO263AB\)](#)



- NOTES
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
 4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
 5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
 7. CONTROLLING DIMENSION: INCH.
 8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.



SYMBOL	DIMENSIONS				REVISION
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.08	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.038	
b1	0.51	0.89	.020	.035	5
b2	1.14	.75	.045	.070	
b3	1.14	1.73	.045	.088	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.69	.045	.085	
D	8.38	9.85	.330	.380	3
D1	6.86	8.25	.270	.325	4
E	9.85	10.87	.380	.420	3,4
E1	8.22	-	.245	-	4
e	2.54 BSC		100 BSC		
F	14.81	15.88	.575	.625	
L	1.75	2.79	.070	.110	
L1	-	1.65	-	.066	4
L2	1.27	1.78	-	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

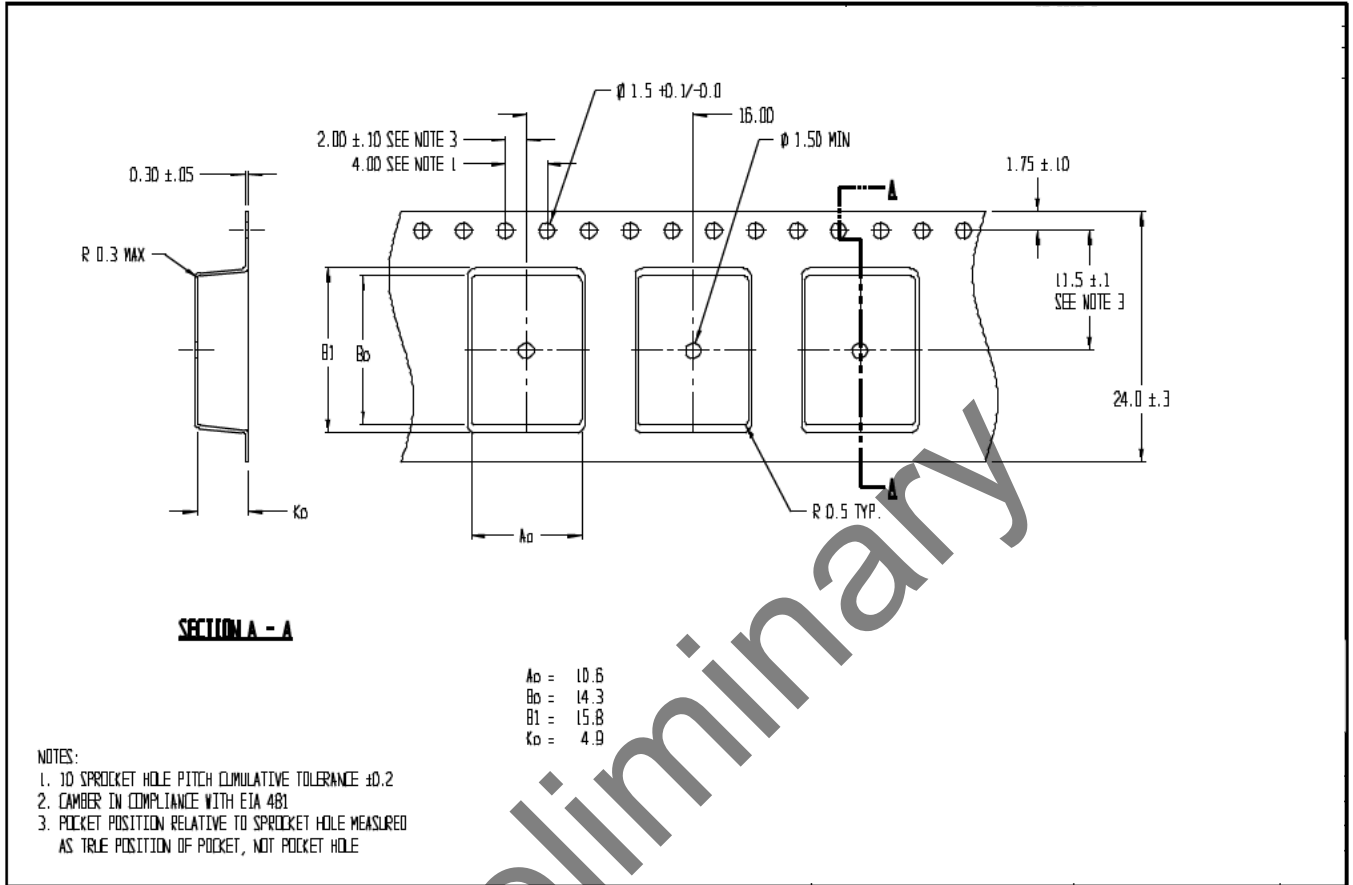
LEAD ASSIGNMENTS

- HEXFET
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE
- IGBTs CoPACK
- 1.- GATE
 - 2.- COLLECTOR
 - 3.- EMITTER
- DIODES
- 1.- ANODE *
 - 2.- CATHODE
 - 3.- ANODE
- * PART DEPENDENT

Power MOSFET Surface Mount (D2PAK (TO-263))

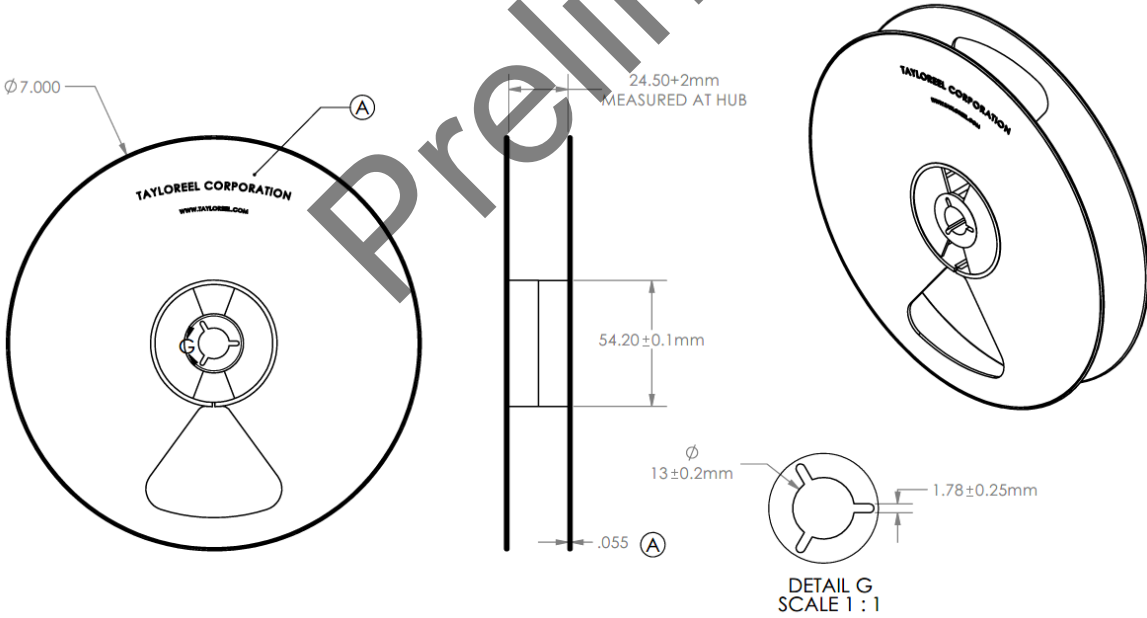
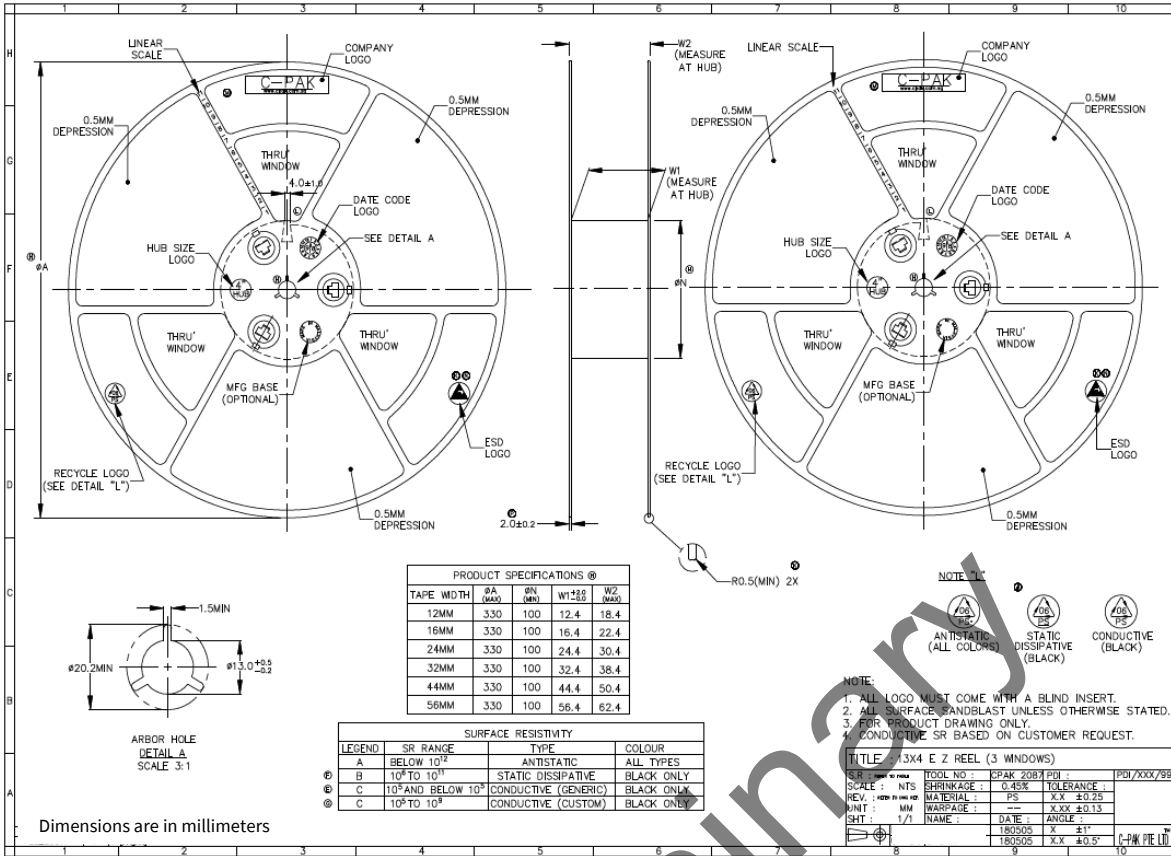
Tape and Reel Information

6 Tape and Reel Information



Power MOSFET Surface Mount (D2PAK (TO-263))

Tape and Reel Information



Unless otherwise specified dimensions are in Inches

Power MOSFET Surface Mount (D2PAK (TO-263))

Revision history

Revision history

Document version	Date of release	Description of changes
	06/03/2024	Preliminary datasheet with PPD number (PPD-98017)
Rev. A	06/21/2024	Added foot notes- 100% tested in final test production.
Rev. B	01/26/2026	Added Tape and Reel -page 12 -13

Preliminary

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