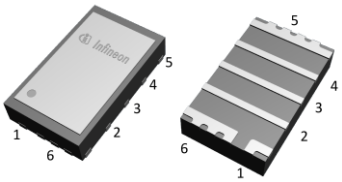
CoolGaN™

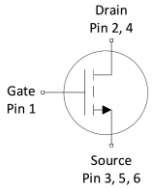
Radiation Tolerant 100V G3 Transistor

Features

- Single Event Effect (SEE) tolerant up to Linear Energy Transfer (LET) = 45 MeVcm²/mg [1]
- Ultra-fast switching and high efficiency
- Space saving and highly robust package
- No reverse recovery charge
- Ultra-low gate charge and output charge
- Exposed die for top-side thermal excellence
- Moisture rating MSL1
- Industrial grade 3x5 package

PG-TSON-6





Top side is exposed silicon substrate, internally connected to source terminal. Not recommended to use as an electrical connection.

Potential applications

- Sync Rectification for AC-DC and DC-DC converters
- Point of Load Converters

Product validation

- Qualified for space applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.
- RLAT tested according to ESCC25100

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on)}$	2.4	mΩ
I_D	76	A
Q_{OSS}	43	nC
Q_G	11	nC
Q_{rr}	0	nC

Part number	Package	Marking	Related links
IRTGC033S10S1	PG-TSON-6	33SRT	see Appendix A

[1] Full SEE report available

Table of contents

Description 1
Maximum ratings 3
Recommended operating conditions 4
Thermal characteristics 5
Electrical Characteristics 6
Electrical characteristics diagrams 8
Package outlines 13
Appendix A 16
Revision history 17
Trademarks 18
Disclaimer 18

1 Maximum ratings

at Tj = 25 °C, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80 % of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note / Test condition
Continuous drain-source voltage	V_{DS}	–	–	100	V	V_{GS} = 0 V
Pulsed drain-source voltage 1)	$V_{DS,\ pulse}$	–	–	120	V	V_{GS} = 0 V, 1 h total time
Continuous drain current	I_D	–	–	76 21	A	V_{GS} = 5 V, T_C = 25 °C V_{GS} = 5 V, T_A = 25 °C, R_{thJA} = 38 °C/W 2)
Pulsed drain current 3)	$I_{D,pulse}$	–	–	700 330	A	T_j = 25 °C T_j = 150 °C
Pulsed gate-source voltage 1)	V_{GS}	-6.5	–	6.5	V	Pulsed 100 h total time
Power dissipation	P_{tot}	–	–	45 3.3	W	T_C = 25 °C T_A = 25 °C, R_{thJA} = 38 °C/W 2)
Storage temperature	T_{stg}	-55	–	150	°C	–
Junction temperature	T_j	-40	–		°C	–

1) Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

2) Device on 4-layer FR4 PCB, vertical in still air.

3) Pulse current limited by transfer characteristic.

2 Recommended operating conditions

Table 3 Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note / Test condition
Gate-source voltage	V_{GS}	-4.0	5.0	5.5	V	–

3 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note / Test condition
Thermal resistance, junction-case, top	R_{thJC}	–	0.5	0.6	°C/W	–
Thermal resistance, junction-case, bottom	R_{thJC}	–	1.9	2.8	°C/W	–
Thermal resistance, junction-ambient 1s0p	R_{thJA}	–	60	–	°C/W	On 1 layer PCB, vertical in still air.
Thermal resistance, junction-ambient 2s2p	R_{thJA}	–	38	–	°C/W	With vias on 4 layer PCB, vertical in still air.

4 Electrical Characteristics

at Tj = 25 °C and pre-irradiation, unless otherwise specified. Refer to SEE report for post irradiation values.

Table 5 Static characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note / Test condition
Gate threshold voltage	$V_{GS(th)}$	1.2	1.9	2.9	V	V_{DS} = V_{GS}, I_D = 8.0 mA
Drain-source leakage current	I_{DSS}	–	0.3 6.0	1.5 50	µA	V_{DS} = 100 V, V_{GS} = 0 V, T_j = 25 °C V_{DS} = 100 V, V_{GS} = 0 V, T_j = 125 °C
Gate-source leakage current	I_{GSS}	–	16 0.01 120 0.01	250 0.1 1100 0.1	µA	V_{GS} = 5 V, T_j = 25 °C V_{GS} = -4 V, T_j = 25 °C V_{GS} = 5 V, T_j = 125 °C V_{GS} = -4 V, T_j = 125 °C
Drain-source on-state resistance	$R_{DS(on)}$	–	2.4	3.3	mΩ	V_{GS} = 5 V, I_D = 20 A
Gate resistance 4)	R_G	–	0.5	–	Ω	–

4) Defined by design. Not subject to production test.

Table 6 Capacitance characteristics 5)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note / Test condition
Input capacitance	C_{iss}	–	1200	1400	pF	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz
Output capacitance	C_{oss}	–	540	590	pF	
Reverse transfer capacitance	C_{rss}	–	6.1	8.0	pF	

5) Defined by design. Not subject to production test.

Table 7 Gate charge characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note / Test condition
Gate to source charge	Q_{gs}	–	2.8	–	nC	V_{DS} = 50 V, I_D = 20 A, V_{GS} = 0 to 5 V
Gate charge at threshold	$Q_{g(th)}$	–	2.1	–	nC	
Gate to drain charge 6)	Q_{gd}	–	2.6	–	nC	
Switching charge	Q_{sw}	–	3.3	–	nC	
Gate charge total 6)	Q_g	–	11	14	nC	
Gate plateau voltage	$V_{plateau}$	–	2.6	–	V	
Output charge 6)	Q_{oss}	–	43	47	nC	V_{DS} = 50 V, V_{GS} = 0 V

6) Defined by design. Not subject to production test.

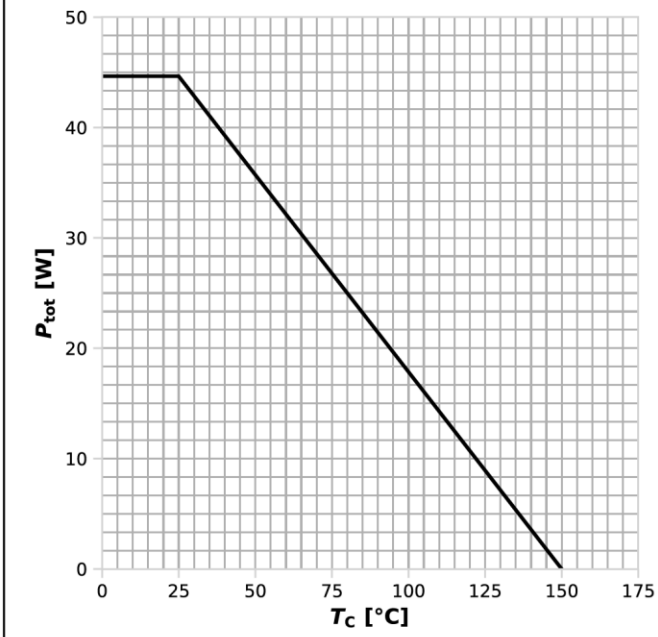
Table 8 Reverse operation

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note / Test condition
Reverse continuous current	I_S	–	–	16	A	T_C = 25 °C
Pulsed current, reverse	$I_{S,pulse}$	–	–	304	A	T_C = 25 °C
Source-Drain reverse voltage	V_{SD}	–	2.4 2.0	3.1 –	V	V_{GS} = 0 V, $I_{S,pulse}$ = 20 A, T_j = 25 °C V_{GS} = 0 V, $I_{S,pulse}$ = 0.5 A, T_j = 25 °C
Reverse recovery charge 7)	Q_{rr}	–	0	–	nC	V_R = 50 V, $I_{S,pulse}$ = 20 A, $di_{S,pulse}/dt$ = 100 A/µs

7) Defined by design. Not subject to production test.

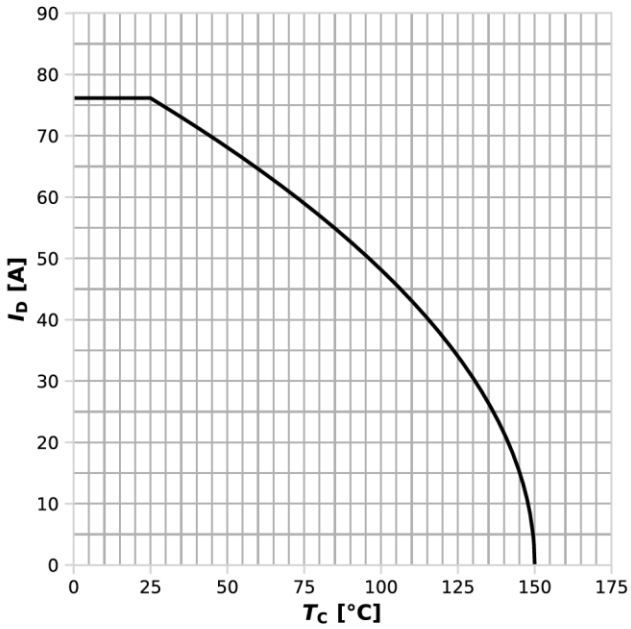
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



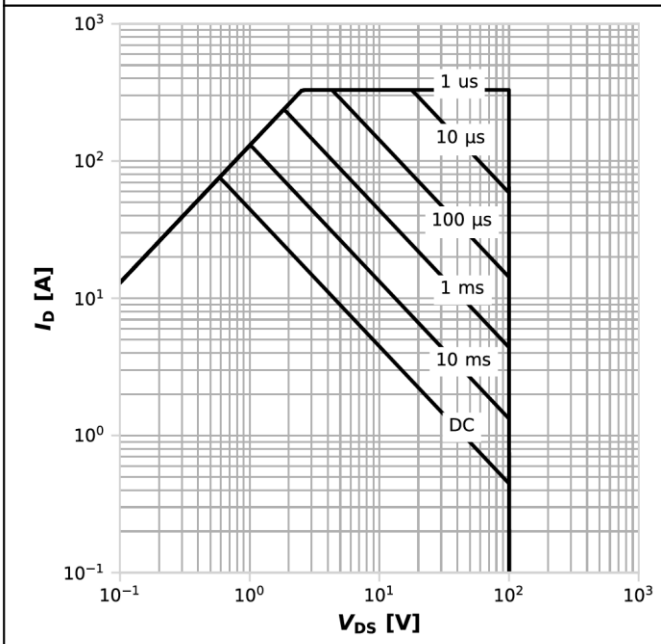
$P_{tot}=f(T_C)$

Diagram 2: Drain Current



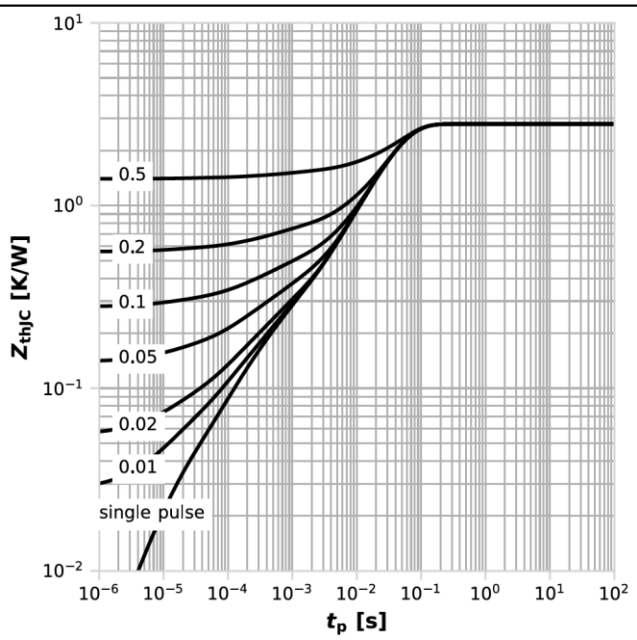
$I_D=f(T_C)$

Diagram 3: Safe operating area



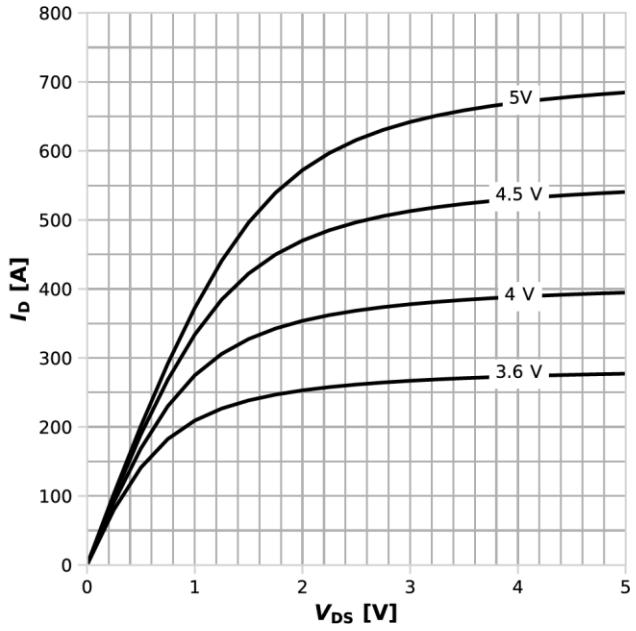
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



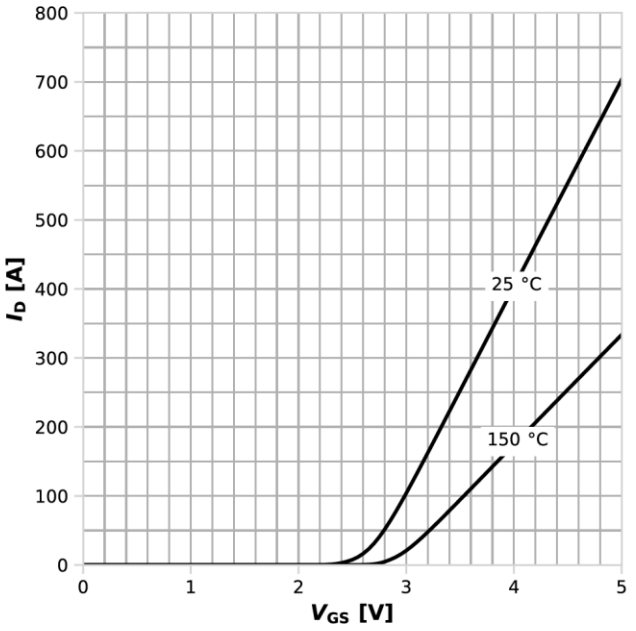
$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



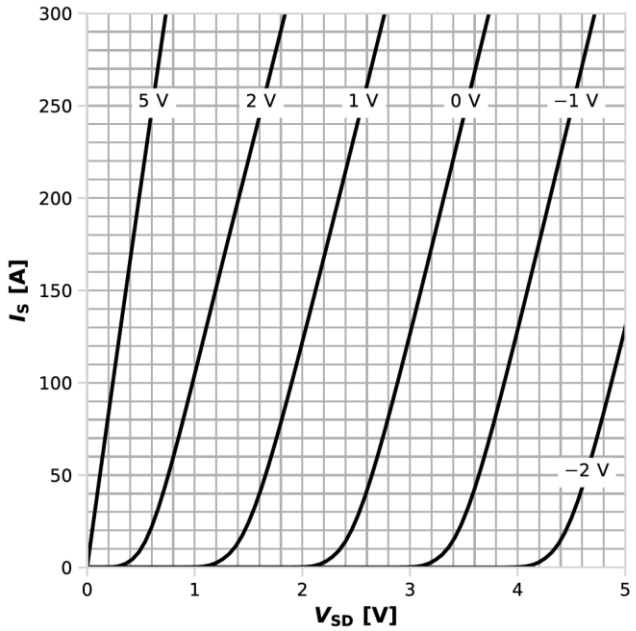
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. transfer characteristics



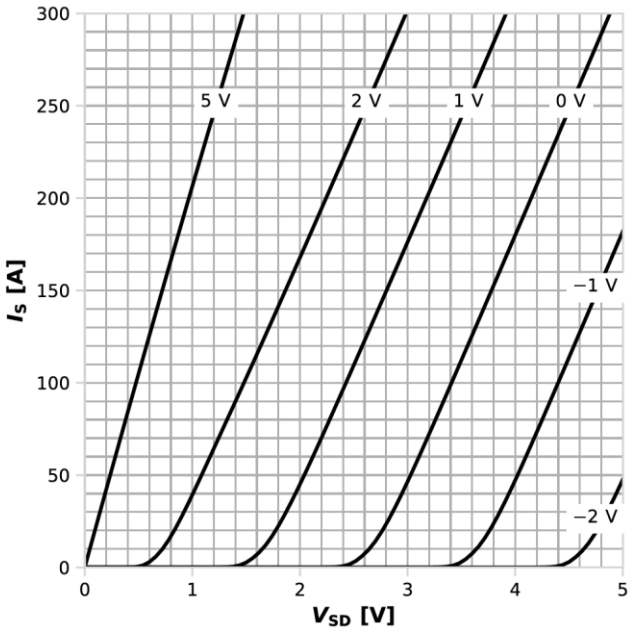
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 7: Typ. channel reverse characteristics



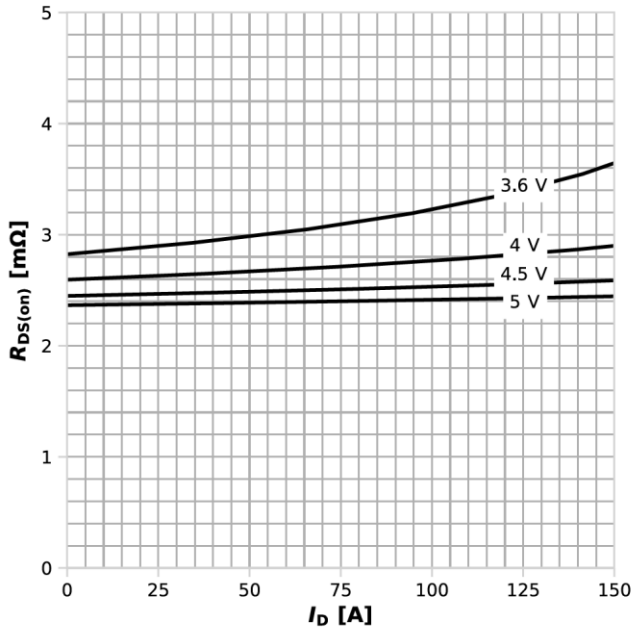
$I_S=f(V_{SD})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 8: Typ. channel reverse characteristics



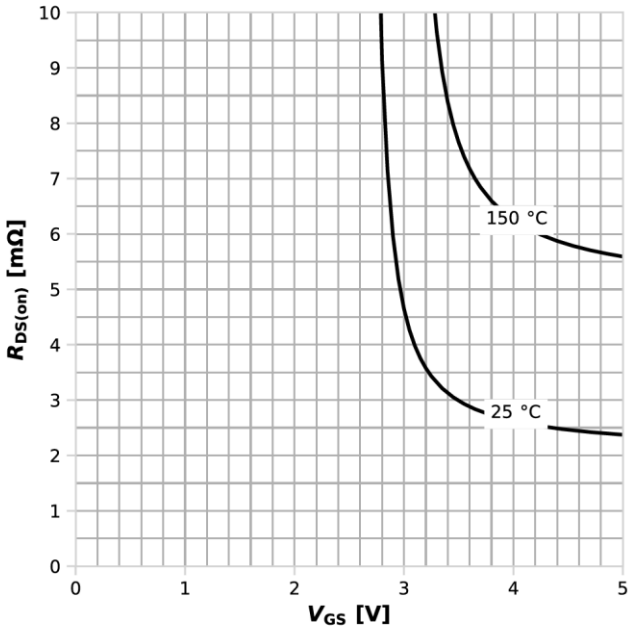
$I_S=f(V_{SD})$; $T_j=125$ °C; parameter: V_{GS}

Diagram 9: Typ. drain-source on-state resistance



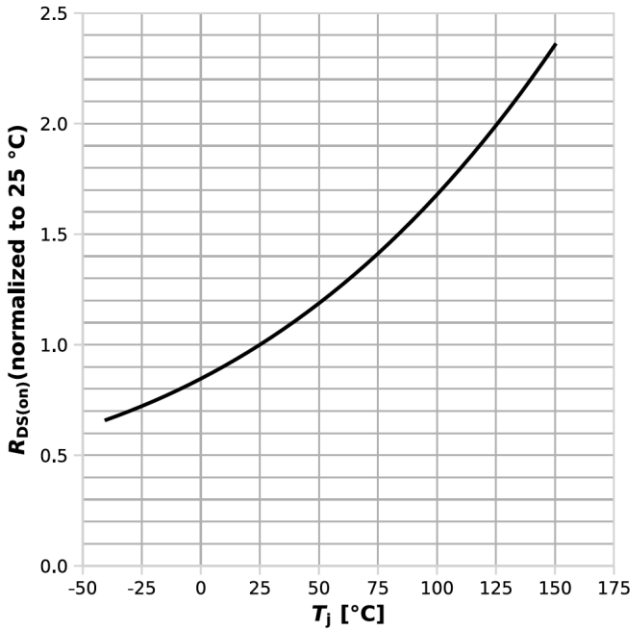
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 10: Typ. Drain-source on-state resistance



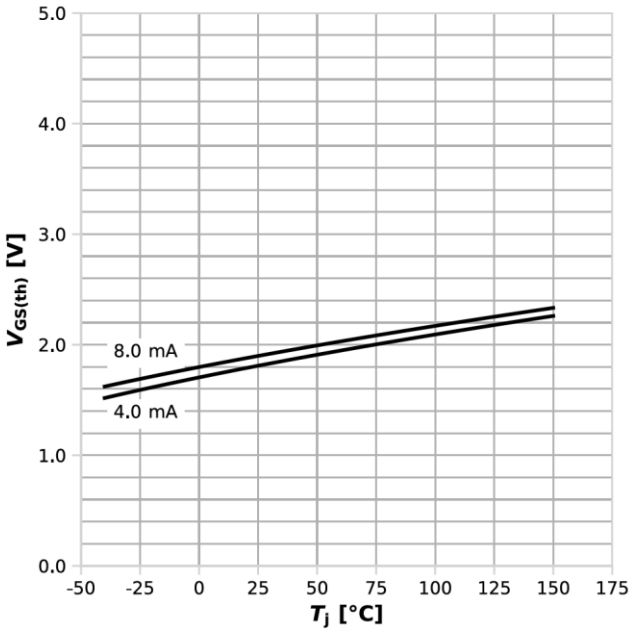
$R_{DS(on)}$=f(V_{GS}); I_D=20 A; parameter: T_j

Diagram 11: Drain-source on-state resistance



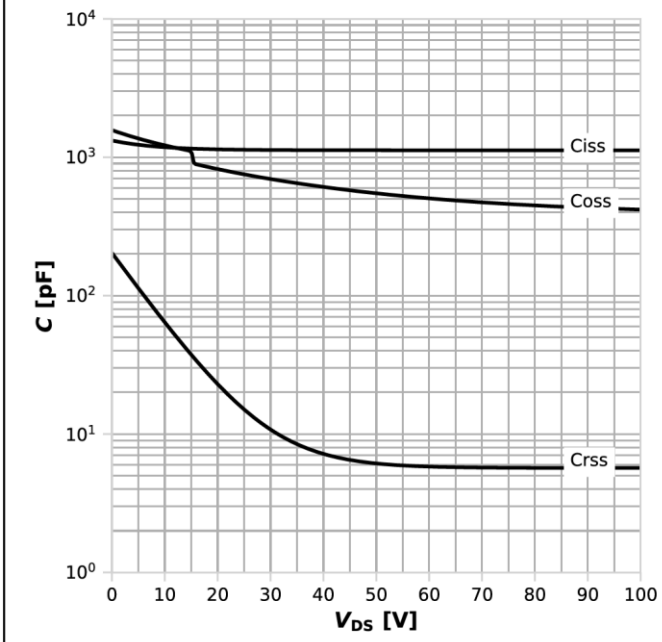
$R_{DS(on)}$=f(T_j); I_D=20 A, V_{GS}=5V

Diagram 12: Typ. gate threshold voltage



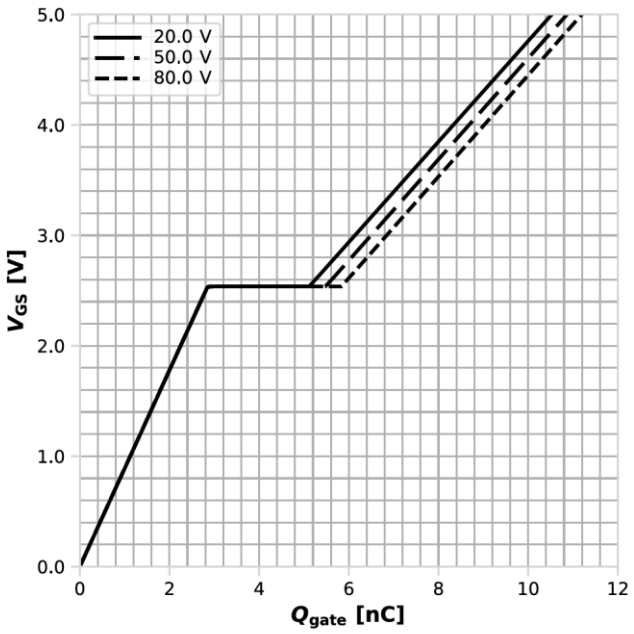
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 13: Typ. capacitances



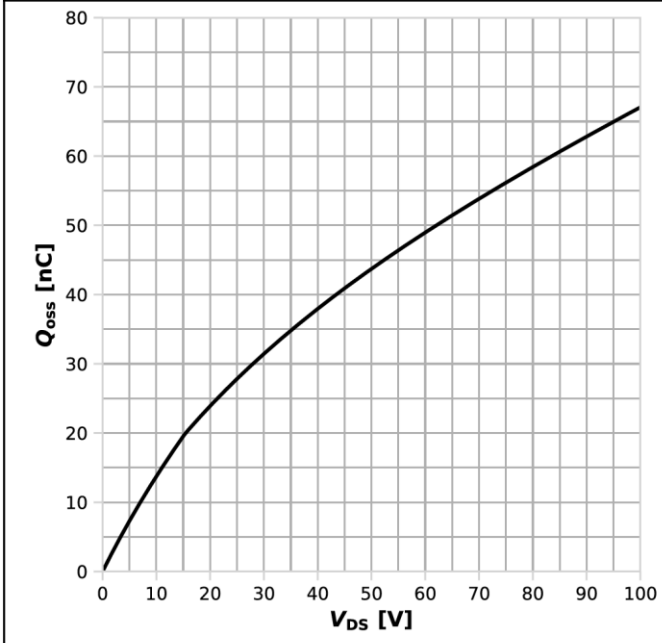
C=f(V_{DS}); V_{GS}=0 V

Diagram 14 Typ. gate charge



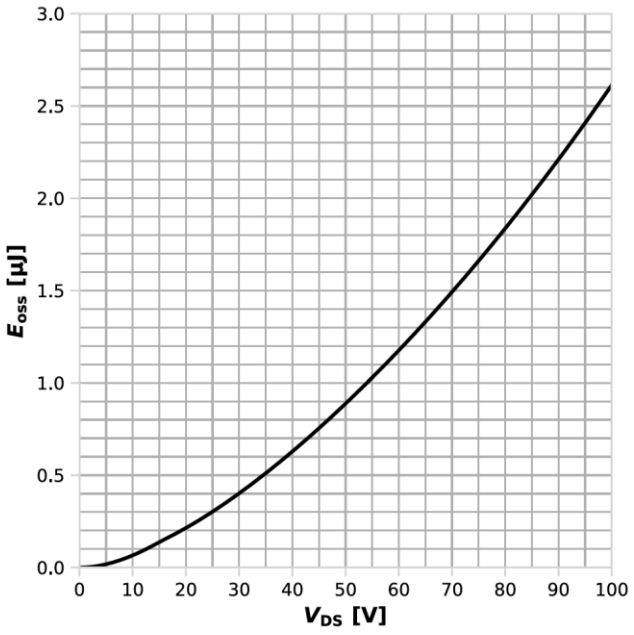
V_{GS}=f(Q_{gate}); I_D=20 A pulsed; parameter: V_{DS}

Diagram 15: Typ. output charge



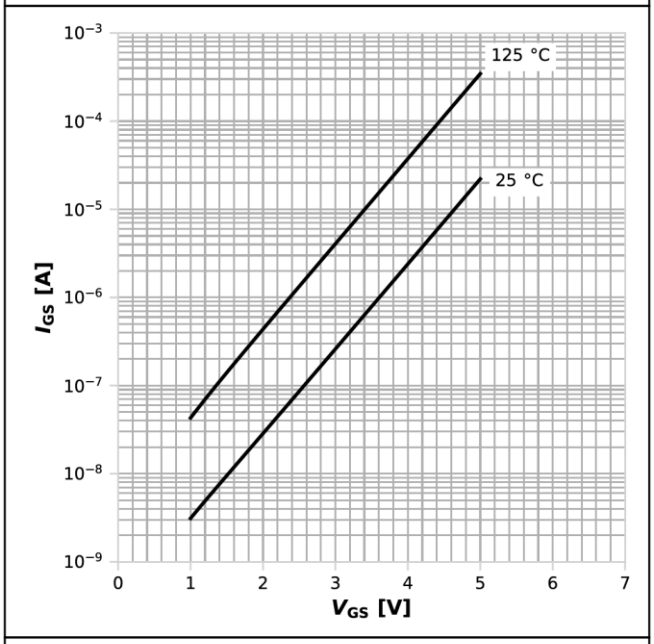
Q_{oss}=f(V_{DS}), V_{GS}=0 V

Diagram 16: Typ. Coss stored Energy



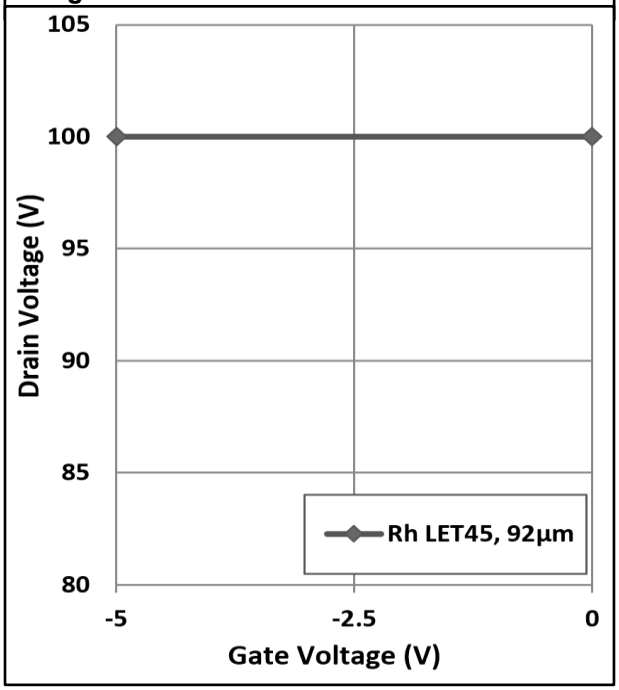
E_{oss}=f(V_{DS}), V_{GS}=0 V

Diagram 17: Typ. gate characteristics forward

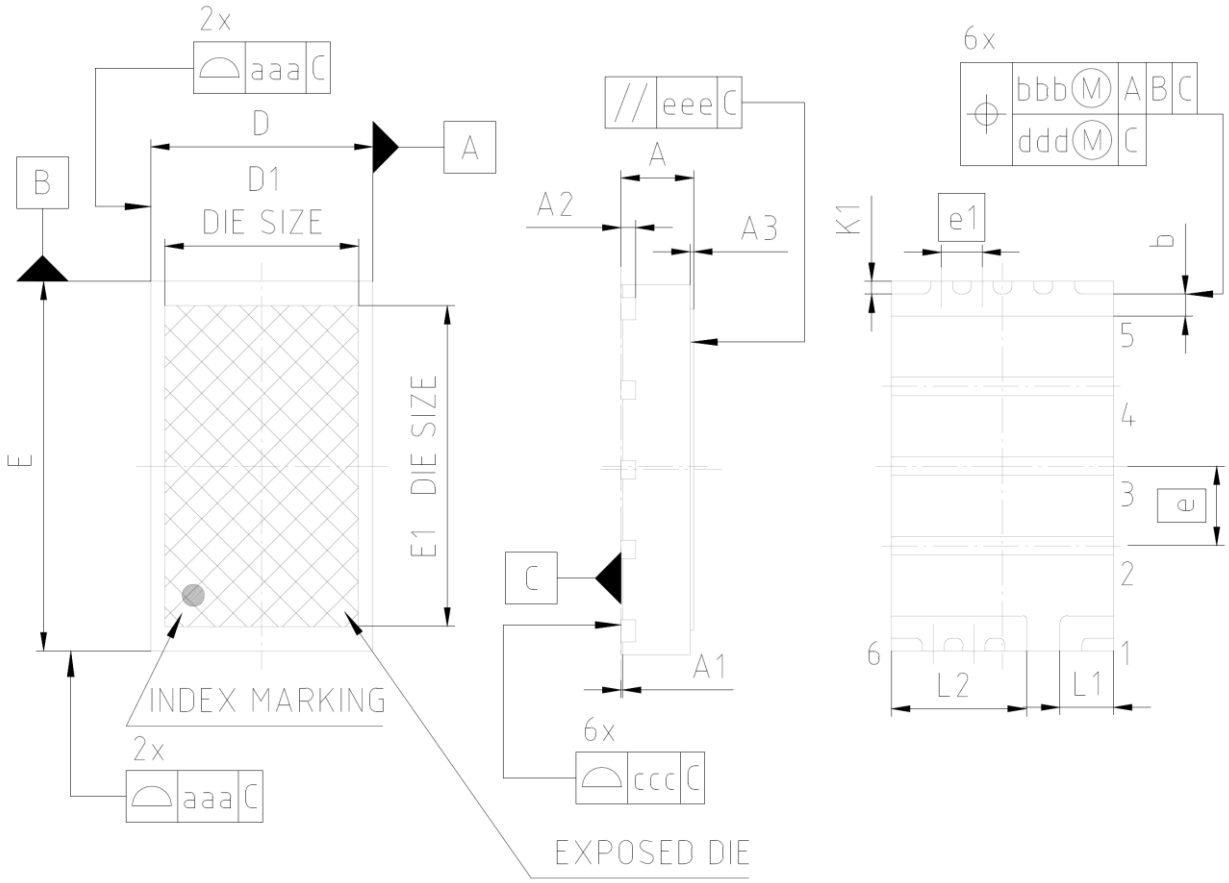


I_{GS}=f(V_{GS}); V_{DS}=0 V; parameter: T_j

Diagram 18: SEE-SOA



6 Package outlines



PACKAGE - GROUP NUMBER:	PG-TSON-6-U01	
DIMENSIONS	**MILLIMETERS**	
	MIN.	MAX.
A	-	1.032
A1	-	0.05
A2	0.20	
A3	-	0.05
b	0.18	0.30
D	2.90	3.10
D1	2.616	
E	4.90	5.10
E1	4.336	
e	1.075	
e1	0.55	
K1	0.125	0.225
L1	0.625	0.825
L2	1.725	1.925
aaa	0.05	
bbb	0.10	
ccc	0.08	
ddd	0.05	
eee	0.10	

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH,
PROTRUSION OR GATE BURRS

Figure 1 Outline PG-TSON-6, dimensions in mm

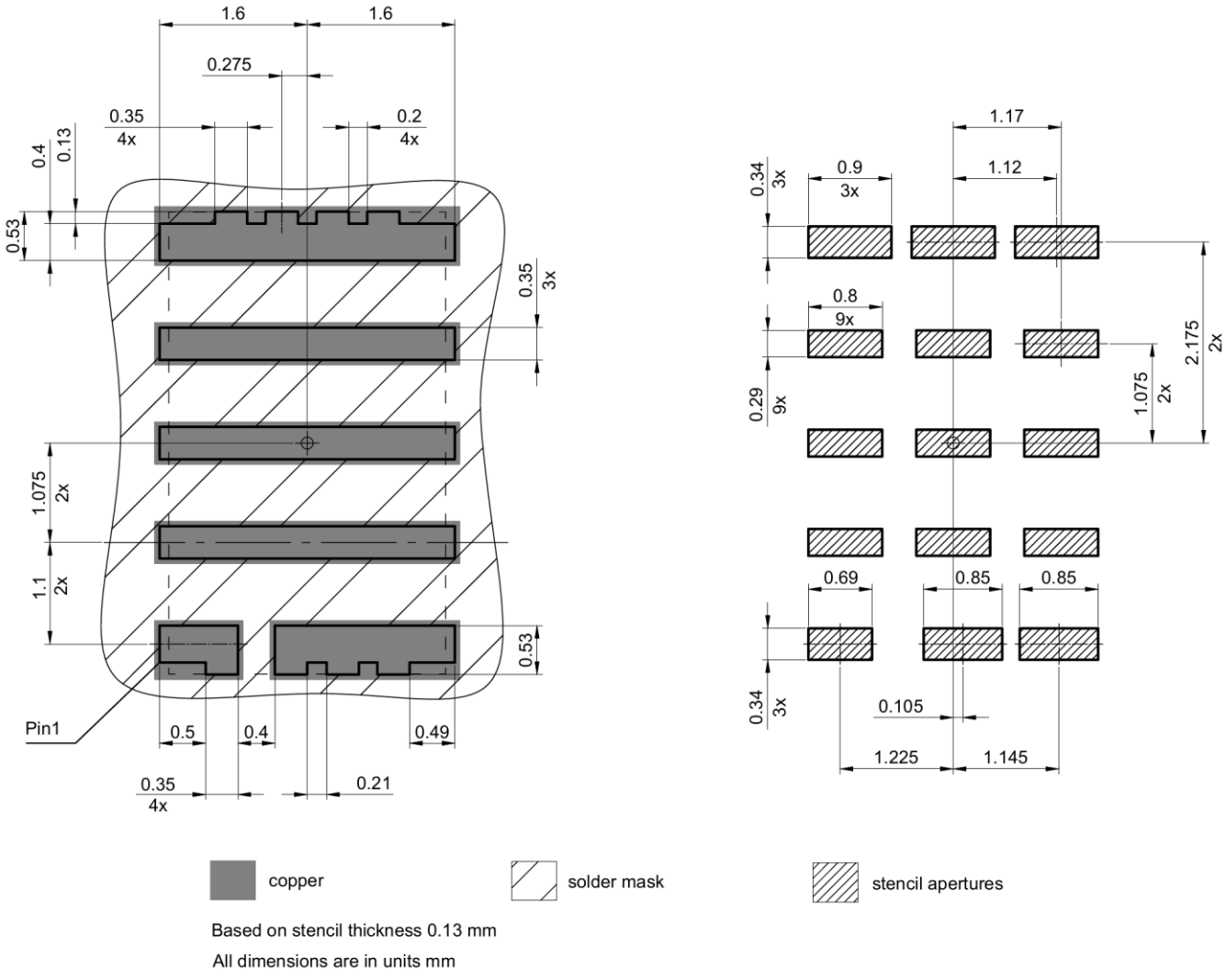


Figure 2 Footprint drawing PG-TSON-6, dimensions in mm

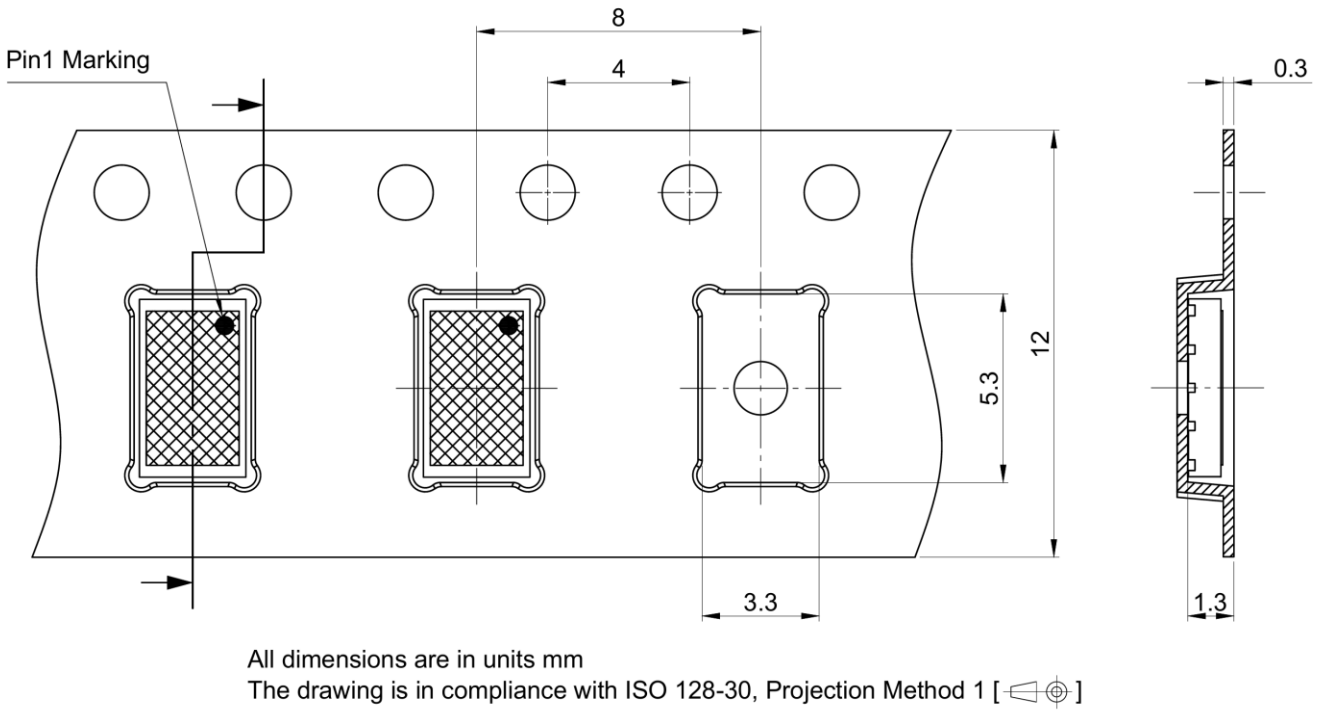


Figure 3 Packaging variant PG-TSON-6, dimensions in mm

7 Appendix A

Table 9 Related links

- IFX Radiation Tolerant webpage
- IFX CoolGaN™ reliability white paper
- IFX CoolGaN™ gate driver application note
- IFX CoolGaN™ Evaluation Boards
- IFX Packages Description-PG-TSON-6-2

Revision history

IRTGC033S10S1

Revision 2026-11-6, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-11-6	Release of Initial version

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