IRS9103A
REAL3™ Laser diode driver for automotive

Features

- Driver for fast switching laser diodes, e.g. within Time-of-Flight systems
- Laser (typically a VCSEL) current up to 10 A
- Laser voltage up to 14 V (dual and triple junction VCSEL support)
- Fast rise and fall times < 1 ns
- Modulation frequency up to 130 MHz
- Switch on-resistance < 120 mΩ
- External LVDS load resistor allows to daisy chain multiple devices
- Build-in fail safe function for
  - LVDS input with always defined state
  - Thermal shut-down
  - Low supply voltage
  - Pulse width limiter ensuring maximum on-time lower than 5µs
- Supply voltage 3.3V
- 1.35 x 1.35 mm PG-WFWLB-9-21 package
- Qualification according to AEC-Q100, grade 2 (Tamb of -40°C to 105°C)

Attention: ***The IRS9103A does not provide any measurements to support laser safety or general safety functions. For laser class definition and safety measures the user needs to take care in the design and documentation of the end device.***

Potential applications

The laser driver is addressing all applications where fast switching VCSEL illumination is required like in Time-of-Flight systems, targeting following applications:

- In-cabin sensing
- Gesture control
- Occupant detection and classification
- Driver monitoring systems (DMS)
- Secure face authentication
- Close range collision avoidance
- Parking assist
- ADAS and other LIDAR applications

Product validation

Qualified for automotive applications.

Product validation according to AEC-Q100, Grade 2.

Description

The IRS9103A is a low cost, small footprint, laser diode driver IC optimized for indirect Time-of-Flight (ToF) image sensors with support for high modulation frequencies and efficient conversion from electrical to optical power. The laser driver is designed for automotive grade applications and is perfectly aligned with the REAL3™ image sensor family.

The IRS9103A is not limited to indirect ToF applications, but can be utilized as a general purpose low-side laser driver in voltage-mode topologies.

Type	Package	Marking
IRS9103A	PG-WFWLB-9-21	-

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1 Block diagram and application

1.1 Block diagram

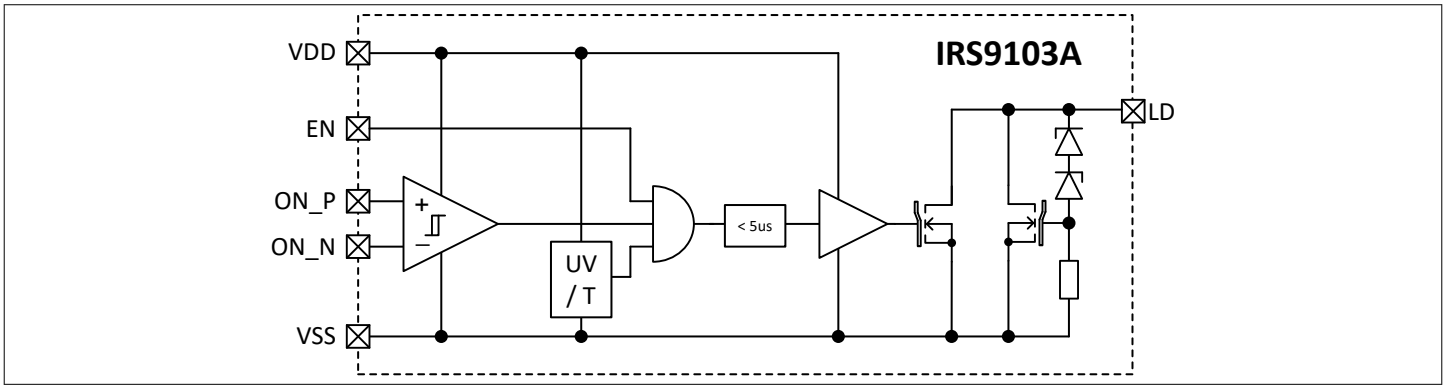

Figure 1 IRS9103A block diagram

The block diagram above shows a simplified overview of the main functional blocks of the IRS9103A:

- LVDS receiver with a built-in fail-safe circuit
- Under-voltage and over-temperature monitor
- Pulse width limiter
- Low side NMOS switch with a gate driver and transient voltage protection clamp for the LD

1.2 Application circuit

The figure below shows the simplified application circuit of the IRS9103A in a combination with Infineon's REAL3™ ToF image sensor. This combination provides the lowest cost solution and minimized BoM, utilizing the ToF sensor's built in integrated current monitor (iCM) for laser safety support and a shared supply rail between the image sensor and the driver. Using the device in different applications as a general purpose low-side driver may require schematic changes in order to fit the specific requirements.

The IRS9103A receives modulation signal over a standard LVDS interface. In order to enable device operation the Enable signal has to be driven high. In case of floating input (LVDS and/or EN) the switch is turned off.

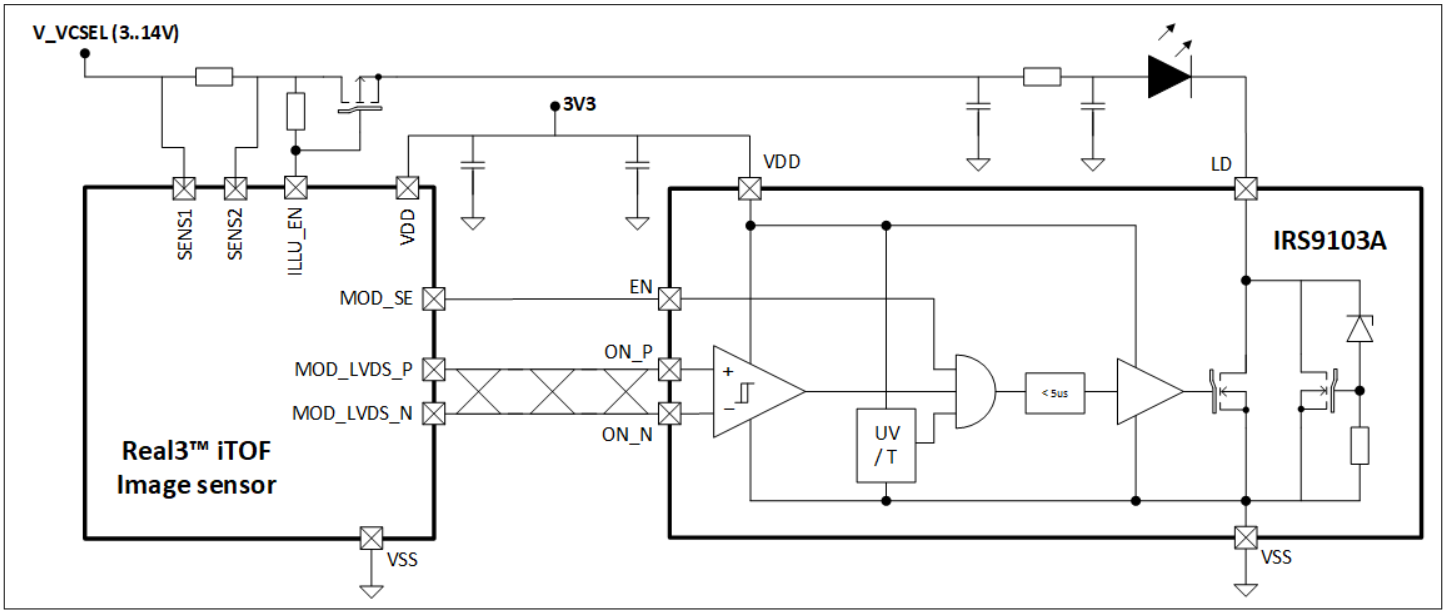

Figure 2 Simplified application diagram

2 Pin configuration

2.1 Pinout

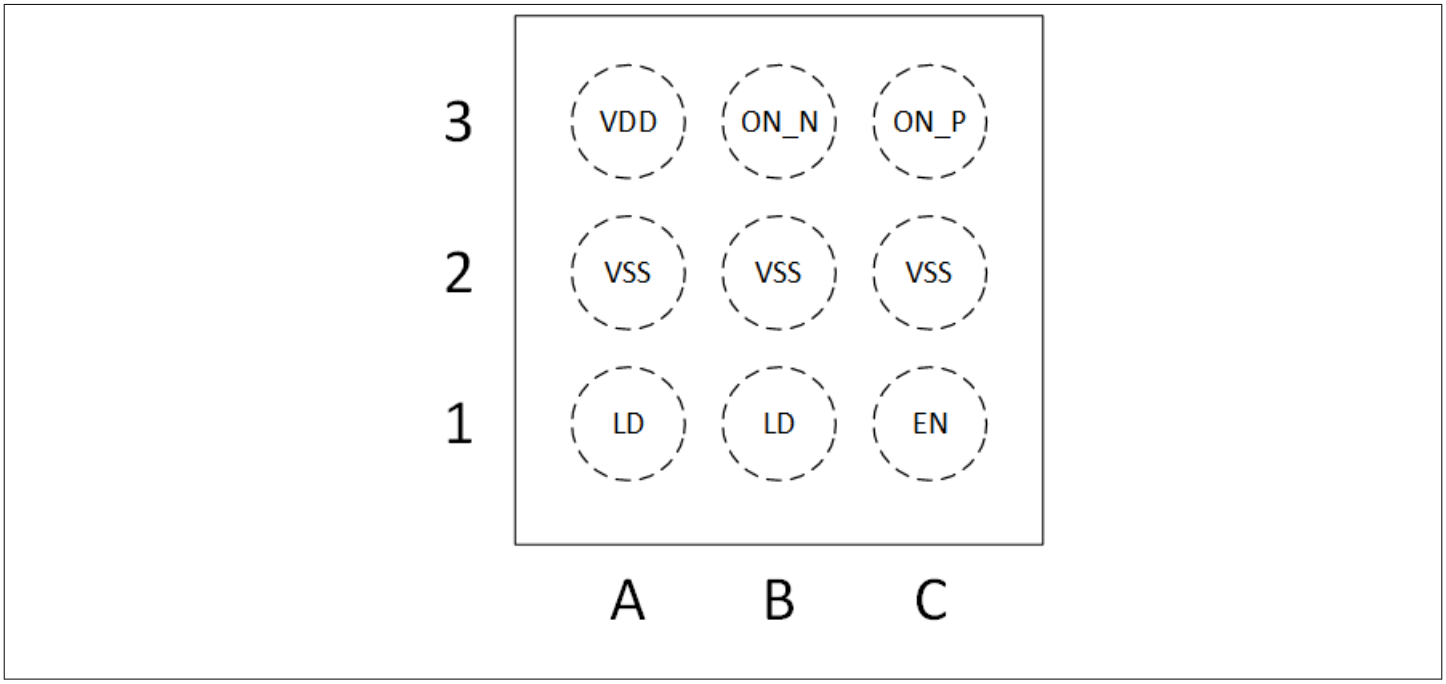

Figure 3 IRS9103A pinout

2.2 Pin description

Table 1 Pin description

Pin	Pin Name	Type	Description
A1, B1	LD	Load	Laser diode cathode
C1	EN	Input	Driver enable input
C3	ON_P	Input	LVDS modulation input, positive
B3	ON_N	Input	LVDS modulation input, negative
A3	VDD	Supply	Analog supply
A2,B2,C2	VSS	Supply	Reference potential

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

T_j = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltages						
Supply voltage at VDD	VDD_{MAX}	-0.3	–	3.6	V	
Load voltage at LD, static	V_{LD_MAX}	-0.3	–	14.5	V	Static
Load voltage at LD, dynamic	$V_{LD\_DYN\_MAX}$	-0.3	–	20	V	maximum clamping voltage of short transients
Maximum input voltage at EN	V_{EN_MAX}	-0.3	–	14.5	V	
Maximum input voltage at ON_P, ON_N	V_{MOD_MAX}	-0.3	–	VDD+0.3	V	
Supply voltage at VSS	VSS_{MAX}	0	0	0	V	
Currents						
Load current	I_{LD_MAX}	–	–	10	A	–
Temperatures						
Junction temperature	*TJ_MAX*	-40	–	150	°C	–
Storage temperature	*TSTG_MAX*	-55	–	150	°C	–
ESD susceptibility						
ESD Resistivity HBM (all Pins)	V_{HBM}	-2		+2	kV	ESD robustness, HBM according to AEC-Q100-002 (1.5 kΩ, 100 pF)

***Note**:* *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.*

Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as outside the normal operating range. Protection functions are not designed for continuous repetitive operation.

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage at VDD	VDD	3.1	3.3	3.6	V	–
Load voltage at LD	V_{LD}	0		14	V	
Modulation Frequency	f_{MOD}	10	100	130	MHz	
Junction temperature	T_j	-40	–	150	°C	–
Ambient temperature	T_{AMB}	-40		105	°C	
Pulse Width	t_{PULSE}	1.5		2500	ns	
Load Current - average	I_{ID_AV}		1.5		A	120Mhz, 33%DC, 6A peak Based on R_{thJA}
Load Current	I_{ld}			10	A	peak current

***Note**: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.*

3.3 Thermal resistance

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance junction to ambient	R_{thJA}	–	101	–	K/W	Device soldered to a JEDEC 2s2p PCB
Thermal resistance junction to bottom	R_{thJB}	–	12	–	K/W	25°C, device only
Thermal resistance junction to top	R_{thJC}	–	56	–	K/W	25°C, device only

3.4 Current consumption

Table 5 Current consumption

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Current consumption idle	$I_{VDD,idle}$			4	mA	EN=1, no modulation, VDD = 3.3V
Current consumption active	$I_{VDD,active}$		1.9	2.4	mA/MHz	EN=1, VDD= 3.3V, standard load

(table continues...)

Table 5 (continued) Current consumption

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Current consumption power down	$I_{VDD,pd}$			1.6	uA	EN=0, Temp=25°C, VDD=3.3V

3.5 Electrical characteristics

Table 6 Electrical characteristics

T_j = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output stage						
ON resistance (LD to VSS)[1)]	R_{ON}	40	70	120	mΩ	V_{DS}=300mV
OFF current (LD to VSS)	I_{OFF}	0.001	–	10	µA	V_{LD} = 6V V_{LD} = 14V[1)]
DC Clamping Voltage	V_{CLAMP}	14.5	17	20	V	I_{LD}=10mA
Clamping Resistance (differential Ron)[1)]	R_{clamp}	0.3	–	2.9	Ω	clamping current > 100mA
Monitoring						
Undervoltage threshold	V_{UV}	2.3	2.6	2.9	V	
Undervoltage threshold release	V_{UV_REL}	2.4	2.7	3	V	
Thermal Shut-Down	T_{SD}	150	165	180	°C	
Thermal Shut-Down Release	T_{SD_REL}	135	150	165	°C	
Inputs						
High level input voltage EN pin	V_{EN_HIGH}	1.2		3.6	V	
Low level input voltage EN pin	VEN_LOW	-0.3		0.8	V	
EN Pull Down current	I_{PD_EN}	3	4.8	6	uA	V_{EN}=1.2V
Inputs						
Input differential voltage	V_{IN_DIF}	250		400	mV	
Input Voltage Range	V_{IN_SE}	0	1200	2400	mV	
Input differential threshold	V_{IDTH}	-100		100	mV	
Input differential voltage hysteresis	V_{ID_HYST}	25			mV	

***Note**: 1) Not subject to production test*

3.6 Timing characteristics

Table 7 Timing characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
LD Rise and Fall time	t_{RISE}, t_{FALL}			0.8	ns	Not covered by production test, standard load
Propagation Delay	t_{PROP}			5	ns	[Standard Load]
Propagation delay: Rising vs. falling	Δt_{PROP_RF}	-2		2	%	[Standard Load] percentage of the modulation frequency
Propagation delay variation with supply	dt_{PROP}/dV_{VDD}			640	ps/V	[Standard Load]
Propagation Delay: Temperature Coefficient	$_{TCTPROP}$	2.1	3.2	4.8	ps/K	Standard load
LD ON time limit	t_{LDON_LIM}	2.5	3.75	5	us	
Ramp-up time	tRAMP			25	us	EN=VDD, VDD=0->3.3V within 1us
Start-up time	t_{EN}			5	us	VDD ON, EN=0->1
Shut-off time	t_{EN_OFF}			2	us	EN=1->0

4 Package dimensions

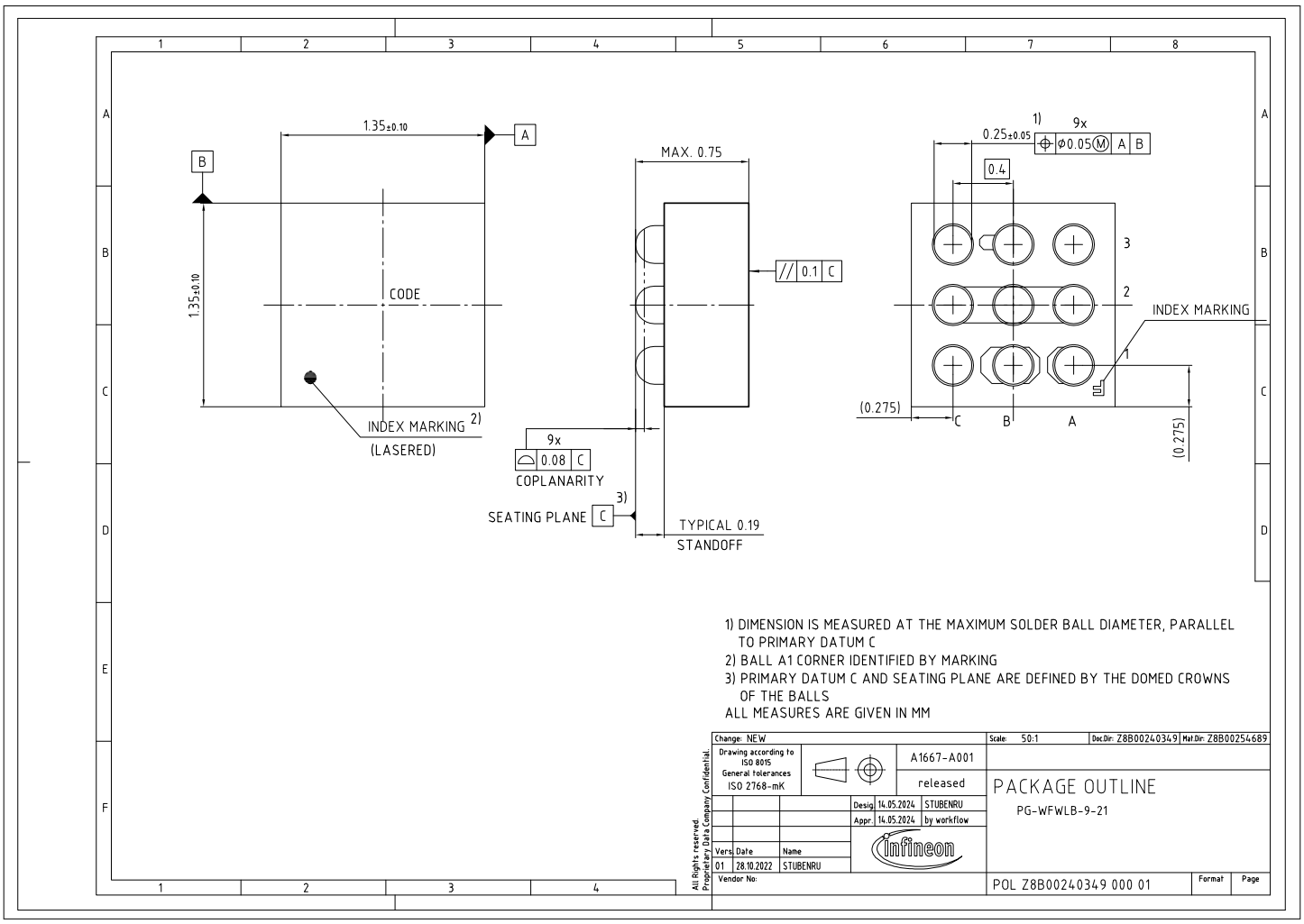

Figure 4 PG-WFWLB-9-21 package drawing

Revision history

Document version	Date of release	Description of changes
0.1	22.02.2022	• Initial release of Target Datasheet
0.2	21.12.2022	• Updated EC tables, package drawing
0.3	05.02.2024	• Update to Preliminary datasheet
0.4	14.03.2024	• Updated EC tables, package drawing
0.5	01.08.2024	• Wording updates, fixes
1.0	07.10.2024	• Datasheet release, minor updates
1.1	26.11.2024	• Updated LD leakage current conditions
1.2	23.04.2025	• Updated clamping resistance • Updated Ron

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