英飞凌D类功放

英飞凌D类音频功放芯片

IRS2452AM

特性

- 2 声道集成模拟输入的D 类音频放大器驱动器
- 差分或单端输入
- 多种保护控制模式，有故障锁定关断模式、故障重启模式或主机控制关断模式
- 可以灵活设置过流保护值。
- 可编程死区时间
- 过温保护外接温度传感器
- 减少点击噪音
- 欠压保护
- 高抗噪性

产品概述

Topology	Half-Bridge/Full-Bridge
$V_{OFFSET\ (max)}$	+/- 200 V
I_{O+} & I_{O-} (typical)	0.5 A & 0.6 A
Selectable deadtime	45/65/85/105 ns
DC offset	<18 mV
OC protection delay	500 ns (max)
Shutdown propagation delay	250 ns (max)
Error amplifier open loop gain	>60 dB

封装选项

MLPQ 7X7mm 32L (0.50 mm pitch)

订购信息

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRS2452AM	MLPQ 32 7x7	Tape and Reel	3000	IRS2452AM

本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。为确认准确性，请务必访问 infineon.com 参考最新的英文版本（控制文档）。

描述

IRS2452AM 集成了两个通道的高压、高性能 D 类音频放大器驱动器，带有 PWM 调制器和保护功能。与外部 MOSFET 配合使用，IRS2452AM 可构成一个完整的双通道 D 类音频放大器。IRS2452AM 设计有浮动模拟输入和保护控制接口引脚，方便半桥应用。高、低压侧都有可编程过流保护电路，保护MOSFET并防止过流。PWM 调制器部分的基本要素可实现灵活的系统设计。小型 MLPQ 7x7mm 封装增强了 D 类拓扑结构体积更小的优势。IRS2452AM 无铅，符合 ROHS 标准。

资质信息†

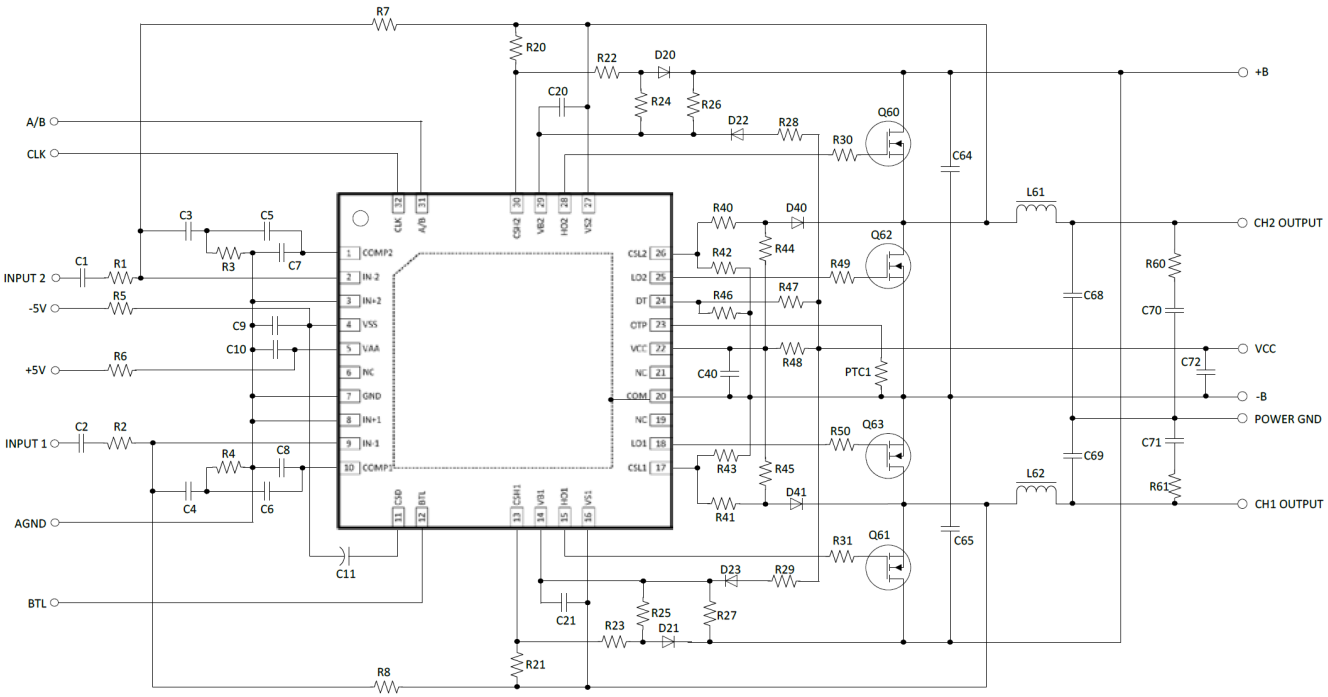
Qualification Level		Industrial†† Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level		MSL2†††, 260°C (per IPC/JEDEC J-STD-020)
ESD	**Machine Model**	Class B (per JEDEC standard EIA/JESD22-A115)
	Human Body Model	Class 1B (per EIA/JEDEC standard JESD22-A114)
	Charge Device Model	Class 0B (per EIA/JEDEC standard JESD22-C101)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

† Qualification standards can be found at Infineon web site http://www.infineon.com/product-info/reliability/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon Technology sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon Technology sales representative for further information.

典型连接图


R7
R20
R22
D20
+B
C20
R24
R26
A/B
D22
R28
Q60
CLK
R30
C64
L61
C3
C5
R40
D40
CH2 OUTPUT
Q62
R42
R44
R49
C1
R1
R3
C7
INPUT 2
R46
R47
R60
R5
C68
-5V
C9
C70
C10
R48
VCC
R6
C40
PTC1
C72
+5V
-B
C2
R2
POWER GND
INPUT 1
R50
Q63
C71
R4
C8
R43
R45
C69
L62
C4
C6
R41
D41
R61
AGND
CH1 OUTPUT
C65
R31
Q61
C11
D23
R29
BTL
C21
R25
R27
R23
D21
R21
R8
CCOMP2
IN-2
IN+2
VSS
VAA
NC
GND
IN+1
IN-1
CCOMP1
CSL2
LO2
DT
OTP
VCC
NC
COM
NC
LO1
CSL1
CLK
A/B
CSH2
VB2
HO2
VS2
CSD
BTL
CSH1
VB1
HO1
VS1

绝对最大额定值

绝对最大额定值指器件必须应用在极限参数以内，否则可能导致器件损坏。所有电压参数均为以 COM 为基准的绝对电压；所有电流均为任何引线的正值。热阻和功率耗散额定值是在装板和静止空气条件下测得的。

Symbol	Definition	Min.	Max.	Units
V_{Bn}	High side floating supply voltage	-0.3	415	V
V_{Sn}	High side floating supply voltage††, n=1-2	V_{Bn} -15	V_{Bn} +0.3	V
V_{Hon}	High side floating output voltage, n=1-2	V_{Sn} -0.3	V_{Bn} +0.3	V
V_{CSHn}	CSH pin input voltage, n=1-2	V_{Sn} -0.3	V_{Bn} +0.3	V
V_{CC}	V_{CC} low side fixed supply voltage††	-0.3	15.5	V
V_{Lon}	Low side output voltage, n=1-2	-0.3	V_{CC} +0.3	V
V_{AA}	Floating input positive supply voltage††	(See I_{AAZ})	210	V
V_{SS}	Floating input negative supply voltage††	-1 (See I_{SSZ})	V_{AA} +0.3	V
V_{GND}	Floating input supply ground voltage	V_{SS} -0.3	V_{AA} +0.3	V
I_{IN-n}	Inverting input current †, n=1-2	-	±3	mA
V_{CSD}	SD pin input voltage	V_{GND} -0.3	V_{AA} +0.3	V
V_{COMPn}	COMP pin input voltage, n=1-2	V_{SS} -0.3	V_{AA} +0.3	V
V_{CLK}	CLK pin input voltage	V_{SS} -0.3	V_{AA} +0.3	V
V_{BTL}	BTL pin input voltage	V_{SS} -0.3	V_{AA} +0.3	V
V_{AB}	A/B pin input voltage	V_{SS} -0.3	V_{AA} +0.3	V
V_{DT}	DT pin input voltage	-0.3	V_{CC} +0.3	V
V_{OTP}	OTP pin input voltage	-0.3	V_{CC} +0.3	V
V_{CSLn}	CSL pin input voltage, n=1-2	-0.3	V_{CC} +0.3	V
I_{AAZ}	Floating input positive supply zener clamp current††	-	10	mA
I_{CCZ}	Low side V_{CC} supply zener clamp current††	-	10	mA
I_{BSZn}	Floating supply zener clamp current††, n=1-2	-	10	mA
dV_{Sn}/dt	Allowable Vs voltage slew rate, n=1-2	-	50	V/ns
dV_{SS}/dt	Allowable Vss voltage slew rate†††	-	50	V/ms

绝对最大额定值（续）

Symbol	Definition	Min.	Max.	Units
Pd	Maximum power dissipation @ $T_A \leq +25°C$ ††††	-	6	W
Rth_{JA}	Thermal resistance, Junction to ambient††††	-	20	°C/W
T_J	Junction Temperature	-	150	°C
T_S	Storage Temperature	-55	150	°C
T_L	Lead temperature (Soldering, 10 seconds)	-	300	°C

† IN-1 and IN-2 contain clamping diode to GND.
†† VAA-VSS, VCC-COM, VB1-VS1 and VB2-VS2 contain internal shunt zener diodes. Note that the voltage ratings of these can be limited by the clamping current.
††† For the rising and falling edges of step signal of 10V. VSS=15V to 200V.
†††† According to JESD51-5. JEDEC still air chamber.

推荐操作条件

为保证正常运行，器件应在以下推荐条件下使用。Vs 和 COM 偏移额定值是在电源偏置为V_{AA}-V_{SS}=10V 、V_{CC} =12V、COM2=COM 和 V_B-V_S=12V 时进行测试的。所有电压参数均为以 COM 为基准的绝对电压；所有电流均为任何引线的正值。

Symbol	Definition	Min.	Max.	Units
V_{Bn}	High side floating supply absolute voltage, n=1-2	V_{Sn} +10	V_{Sn} +14	V
V_{Sn}	High side floating supply offset voltage	(Note1)	400	V
V_{AA}	Floating input supply voltage	V_{SS} + 4.5	V_{SS} + 15	V
I_{AAZ}	Floating input positive supply zener clamp current	1	11	mA
V_{SS}	Floating input supply absolute voltage	0	200	V
V_{Hon}	High side floating output voltage, n=1-2	Vs	V_B	V
V_{CC}	Low side fixed supply voltage	10	14	V
V_{Lon}	Low side output voltage, n=1-2	0	V_{CC}	V
V_{GND}	GND pin input voltage	V_{SS} (Note2)	V_{AA} (Note2)	V
V_{IN-n}	Inverting input voltage, n=1-2	V_{GND} -0.5 (Note2)	V_{GND} +0.5 (Note2)	V
V_{CSD}	CSD pin input voltage	V_{GND}	V_{AA}	V
V_{COMPn}	COMP pin input voltage, n=1-2	V_{SS}	V_{AA}	V
C_{COMPn}	COMP pin phase compensation capacitor to GND, n=1-2	2.2	-	nF
V_{CLK}	CLK pin input voltage	V_{GND}	V_{AA}	V
V_{BTL}	BTL pin input voltage	V_{SS}	V_{AA}	V
V_{AB}	A/B pin input voltage	V_{SS}	V_{AA}	V
V_{DT}	DT pin input voltage	0	V_{CC}	V
V_{OTP}	OTP pin input voltage	0	V_{CC}	V
V_{CSHn}	CSH pin input voltage, n=1-2	V_{Sn}	V_{Bn}	V
V_{CSLn}	CSL pin input voltage, n=1-2	0	V_{CC}	V
dV_{SS}/dt	Allowable V_{SS} voltage slew rate upon power-up (Note3)	-	50	V/ms
f_{SW}	Switching frequency	-	800	kHz
f_{CLK}	CLK frequency (Note4)	-	800	kHz
T_A	Ambient Temperature	-40	125	°C

(注释 1）Vsn 等于 -5V 至 +400V 时逻辑工作。在 Vsn 等于 -5V 至 -VBSn 时保持逻辑状态。

(注释 2）GND 输入电压受 IIN-n 限制。

(注释 3）Vss 从 0V 升至 200V。

(注释 4）CLK 输入频率需要在自振荡频率的 +/-10% 范围内，以便在典型的自振荡应用中同步 PWM。

电气特性

除非另有说明，否则V_{CC}=V_{BS1}=V_{BS2}=V_{DT}=12V, V_{SS}=V_{S1}=V_{S2}=COM =0V, V_{GND}=5V, V_{AA}=V_{BTL}=V_{AB}=10V, C_L=1nF 和T_A=25°C。

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Side Supply						
UV_{CC+}	Vcc supply UVLO positive threshold	8.4	8.9	9.4	V	
UV_{CC-}	Vcc supply UVLO negative threshold	8.2	8.7	9.2	V	
UV_{CCHYS}	UV_{CC} hysteresis	-	0.2	-	V	
I_{QCC}	Low side quiescent current	-	-	6	mA	V_{DT}=V_{CC}
V_{CLAMPL}	Low side zener diode clamp voltage	14.7	15.3	16.2	V	I_{CC}=5mA
High Side Floating Supply						
UV_{BS+n}	High side well UVLO positive threshold, n=1-2	8.0	8.5	9.0	V	
UV_{BS-n}	High side well UVLO negative threshold, n=1-2	7.8	8.3	8.8	V	
UV_{BSHYSn}	UV_{BS} hysteresis, n=1-2	-	0.2	-	V	
I_{QBSn}	High side quiescent current, n=1-2	-	-	1	mA	
I_{LKHn}	High to Low side leakage current, n=1-2	-	-	50	µA	V_{Bn}=V_{Sn}=400V
$V_{CLAMPHn}$	High side zener diode clamp voltage, n=1-2	14.7	15.3	16.2	V	I_{BSn}=5mA
Floating Input Supply						
UV_{AA+}	V_{AA} floating supply UVLO positive threshold from V_{SS}	8.2	8.7	9.2	V	GND pin floating
UV_{AA-}	V_{AA} floating supply UVLO negative threshold from V_{SS}	7.7	8.2	8.7	V	GND pin floating
UV_{AAHYS}	UV_{AA} hysteresis	-	0.5	-	V	GND pin floating
I_{QAASD}	Floating Input positive quiescent supply current in shutdown mode	-	2.5	4	mA	V_{CSD}=V_{GND}
I_{QAA0}	Floating Input positive quiescent supply current, positive input	-	8	11	mA	V_{IN-} = VSS+5.2V
I_{QAA1}	Floating Input positive quiescent supply current, negative input	-	5	8	mA	V_{IN-} = VSS+4.8V
I_{QAAST}	Floating Input positive quiescent supply current in start-up mode	-	6	8	mA	V_{CSD} = V_{GND}+2.5V
I_{QAABTL}	Floating Input positive quiescent supply current, negative input	-	5	8	mA	V_{IN-} = VSS+4.8V, VBTL=GND
I_{LKM}	Floating input side to Low side leakage current	-	-	50	µA	V_{AA}=V_{SS}=V_{GND}= 100V
V_{CLAMPM}	Floating supply zener diode clamp voltage	14.7	15.3	16.2	V	I_{AA}=5mA, V_{CSD}=V_{GND}

电气特性（续）

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Audio Input (GND=0V, V_{AA}=5V, V_{SS}=-5V, COM =V_{CC} =-5V, V_{S1}=V_{S2}=CSH1=CSH2=-5V, DT=-5V)						
V_{Osn}	CHn input offset voltage, n=1-2	-18	0	18	mV	
I_{BINn}	CHn input bias current, n=1-2	-	-	40	nA	
GBWn	CHn small signal bandwidth, n=1-2	-	5 Note 1	-	MHz	C_{COMPn}=2.2nF, Rfn=10k, Note 1
V_{COMPn}	CHn OTA Output voltage, n=1-2	V_{AA}-1	-	V_{SS}+1	V	
g_{mn}	CHn OTA transconductance, n=1-2	80	200	260	mS	V_{IN-n}=10mV
G_{Vn}	CHn OTA gain, n=1-2	60	-	-	dB	
V_{Nrmsn}	CHn OTA input noise voltage, n=1-2	-	250	-	mVrms	BW=20kHz, Resolution BW=22Hz Fig.5
SRn	CHn slew rate, n=1-2	-	±5	-	V/us	C_{COMPn}=2.2nF
CMRRn	CHn common-mode rejection ratio, n=1-2	-	60	-	dB	
PSRRn	CHn supply voltage rejection ratio, n=1-2	-	65	-	dB	
PWM Comparator						
Vth_{PWM}	PWM comparator threshold in COMP	-	(V_{AA} – V_{SS})/2	-	V	
f_{OTAn}	CHn COMP pin star-up local oscillation frequency, n=1-3	-	0.6	-	MHz	V_{CSD} =V_{GND}+2.5V
Clock Input (GND=0V, V_{AA}=5V, V_{SS}=-5V, COM =V_{CC} =-5V, V_{S1}=V_{S2}=CSH1=CSH2=-5V, DT=-5V)						
V_{IHCLK}	CLK high level input threshold	8		-	V	
V_{ILCLK}	CLK low level input threshold	-		2	V	
I_{IHCLK+}	CLK high level input bias current	-35		35	µA	V_{CLK}=V_{AA}
I_{ILCLK-}	CLK low level input bias current	-45		45	µA	V_{CLK}=V_{SS}
V_{THAB}	AB high level input threshold	0.40x (V_{AA}-GND)	0.50x (V_{AA}-GND)	0.60x (V_{AA}-GND)	V	
I_{IHAB+}	AB high level input bias current	-35		35	µA	V_{AB}=V_{AA}
I_{ILAB-}	AB high level input bias current	-45		45	µA	V_{AB}=GND
BTL Mode (GND=0V, V_{AA}=5V, V_{SS}=-5V, COM =V_{CC} =-5V, V_{S1}=V_{S2}=CSH1=CSH2=-5V, DT=-5V)						
V_{THBTL}	BTL high level input threshold	0.40x (V_{AA}-GND)	0.50x (V_{AA}-GND)	0.60x (V_{AA}-GND)	V	
I_{IHBTL+}	BTL high level input bias current	-35		35	µA	V_{BTL}=V_{AA}
I_{ILBTL-}	BTL high level input bias current	-45		45	µA	V_{BTL}=GND

电气特性（续）

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Protection						
Vth_{OCLn}	CHn low side OC threshold in V_{CSLn}, n=1-2	1.1	1.2	1.3	V	
Vth_{OCHn}	CHn high side OC threshold in V_{CSHn}, n=1-2	1.1+ Vs	1.2+ Vs	1.3+ Vs	V	Vs=400V
Vth1	CSD pin shutdown release threshold	$0.52xV_{AA-GND}$	$0.68xV_{AA-GND}$	$0.84xV_{AA-GND}$	V	
Vth2	CSD pin self reset threshold	$0.26xV_{AA-GND}$	$0.30xV_{AA-GND}$	$0.34xV_{AA-GND}$	V	
I_{CSD+}	CSD pin discharge current	70	100	130	µA	$V_{CSD} = V_{GND} + 2.4V$
I_{CSD-}	CSD pin charge current	70	100	130	µA	$V_{CSD} = V_{GND} + 2.4V$
t_{SSDn}	CHn shutdown propagation delay from $V_{CSD} < V_{GND}$+ Vth1 to Shutdown, n=1-2	-	140	250	ns	
t_{OCHn}	CHn propagation delay time from $V_{CSHn} > Vth_{OCHn}$ to Shutdown, n=1-2	-	400	500	ns	
t_{OCLn}	CHn propagation delay time from Vsn> Vth_{OCL} to Shutdown, n=1-2	-	270	350	ns	
V_{OTP}	OTP pin input threshold	-	2.8	-	V	
I_{OTP}	OTP bias sourcing current	-	0.6	-	mA	OTPn=0V

电气特性（续）

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Gate Driver						
Io+n	CHn output high short circuit current (Source) , n=1-2	-	0.5	-	A	Vo=0V, PW≤10µS, Note 1
Io-n	CHn output low short circuit current (Sink) , n=1-2	-	0.6	-	A	Vo=12V, PW≤10µS, Note 1
V_{OLn}	CHn low level out put voltage LO – COM, HO - VS, n=1-2	-	-	0.1	V	Io=0A
V_{OHn}	CHn high level out put voltage VCC – LO, VB - HO, n=1-2	-	-	1.4	V	
Ton0n	CHn high and low side turn-on propagation delay, n=1-2	-	385	-	ns	$V_{DT} = V_{CC}$
Toff0n	CHn high and low side turn-off propagation delay, n=1-2	270	340	410	ns	
Toffskwn	CHn Toff skew, Toffhon – Tofflon, n=1-2	-30	0	30	ns	
tr	Turn-on rise time	-	12	25	ns	
tf	Turn-off fall time	-	12	25	ns	
DT1n	CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HOn turn-off to LnO turn-on (DT_{HO-LO})	30	45	65	ns	$V_{DT}>V_{DT1}$, V_{DTM}=COM
DT2n	CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HOn turn-off to LOn turn-on (DT_{HO-LO})	45	65	85	ns	$V_{DT1}>V_{DT}> V_{DT2}$, V_{DTM}=COM
DT3n	CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HOn turn-off to LOn turn-on (DT_{HO-LO})	60	85	110	ns	$V_{DT2}>V_{DT}> V_{DT3}$, V_{DTM}=COM
DT4n	CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HO turn-off to LOn turn-on (DT_{HO-LO})$V_{DT}= V_{DT4}$	80	105	145	ns	$V_{DT}<V_{DT3}$, V_{DTM}=COM
V_{DT1}	DT mode select threshold 1	0.51xVcc	0.57xVcc	0.63xVcc	V	V_{DTM}=COM
V_{DT2}	DT mode select threshold 2	0.32xVcc	0.36xVcc	0.40xVcc	V	
V_{DT3}	DT mode select threshold 3	0.21xVcc	0.23xVcc	0.25xVcc	V	

注释1　由设计保证，但未经生产测试。

波形定义

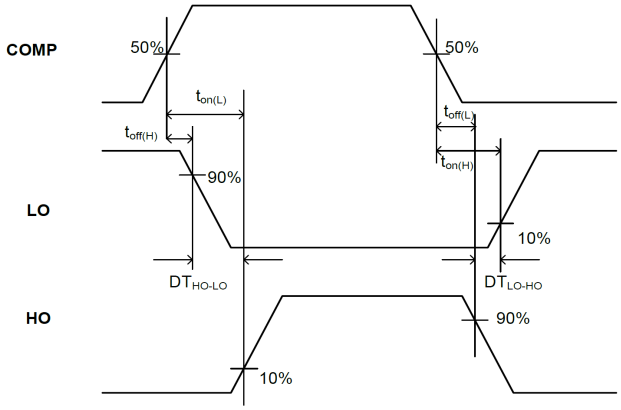


图 1 开关时间波形定义

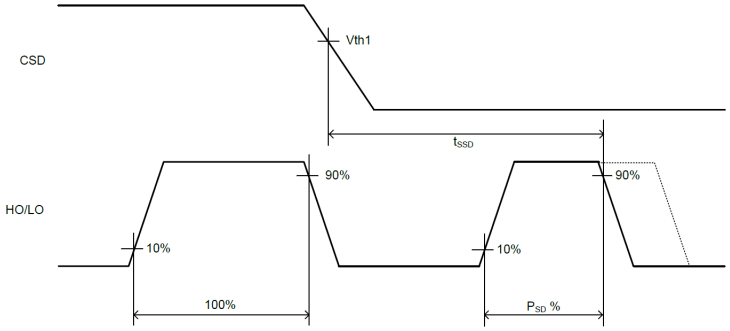


图2 CSD与关断波形定义

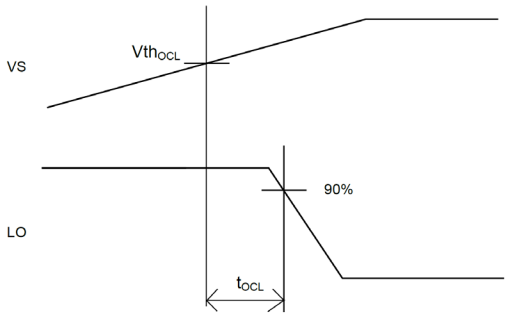


图 3 V_S> Vth_{OCL}至关机波形

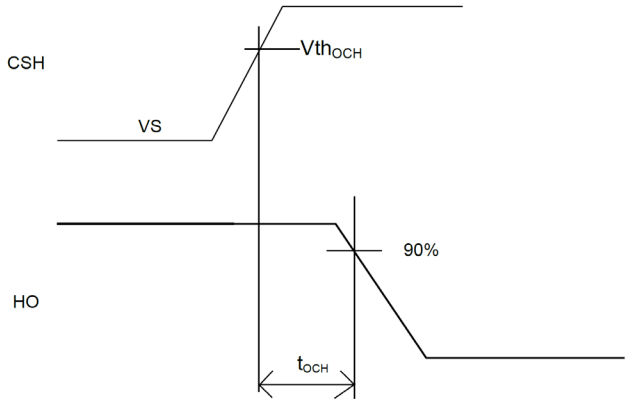


图 4 V_{CSH} > Vth_{OCH} 至关机波形

波形定义（续）

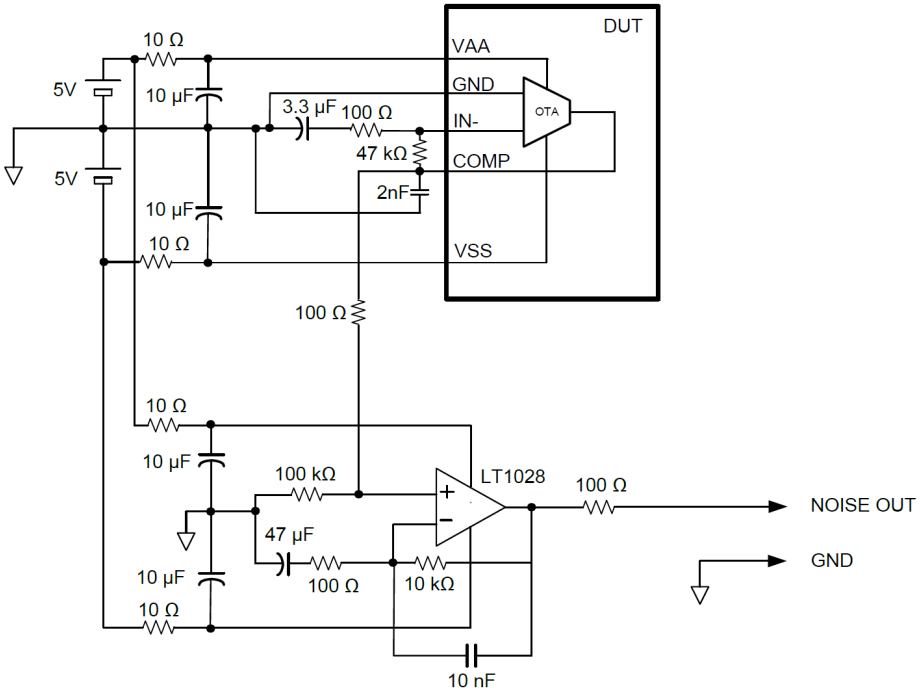
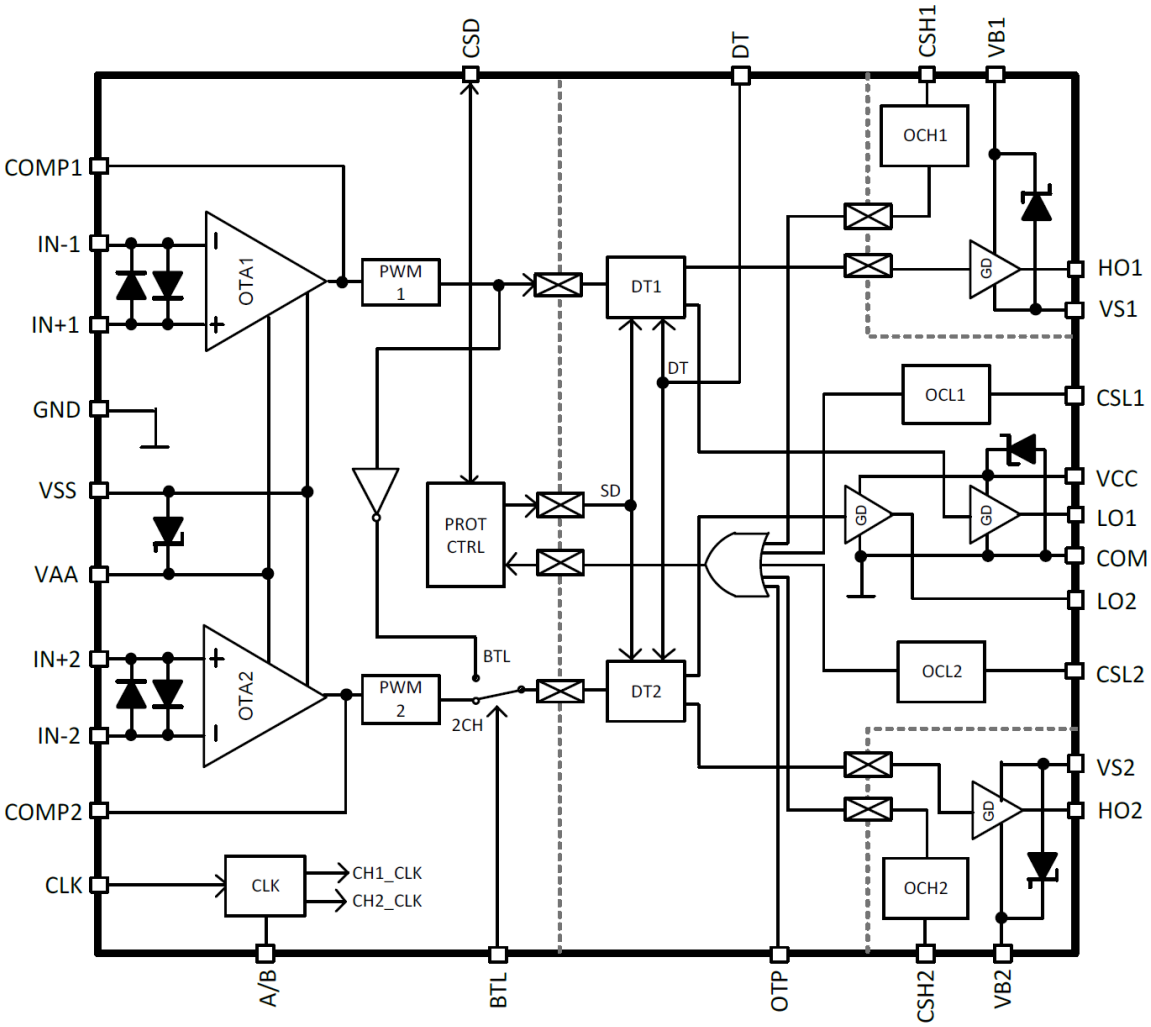
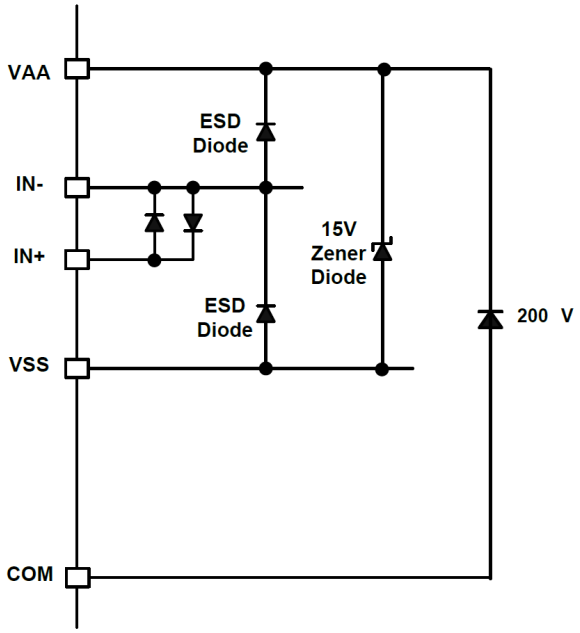


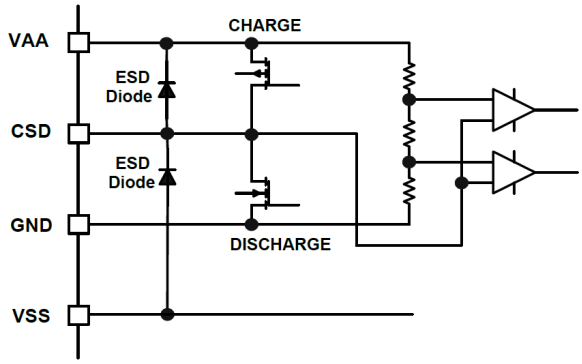
图 5：OTA 输入噪声电压测量电路

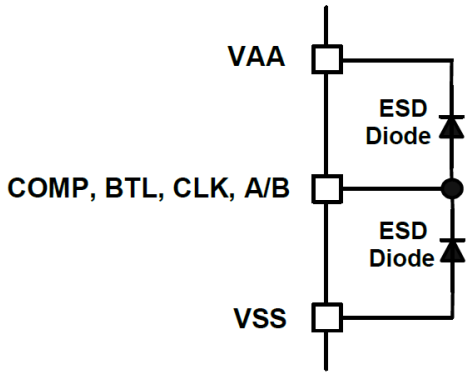
功能框图

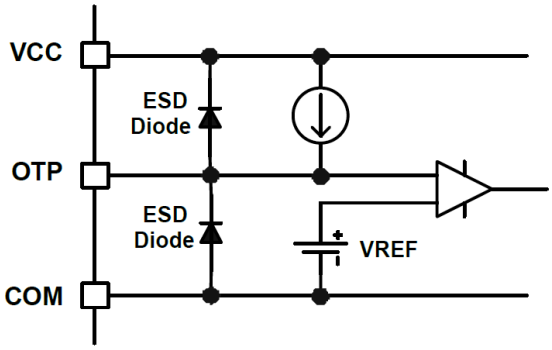

CSD
DT
CSH1
VB1
COMP1
IN-1
IN+1
GND
VSS
VAA
IN+2
IN-2
COMP2
CLK
OTA1
OTA2
PWM 1
PWM 2
DT1
DT2
DT
SD
PROT CTRL
BTL
2CH
CLK
CH1_CLK
CH2_CLK
OCH1
OCL1
OCL2
OCH2
GD
HO1
VS1
CSL1
VCC
LO1
COM
LO2
CSL2
VS2
HO2
A/B
BTL
OTP
CSH2
VB2

输入/输出引脚等效电路图

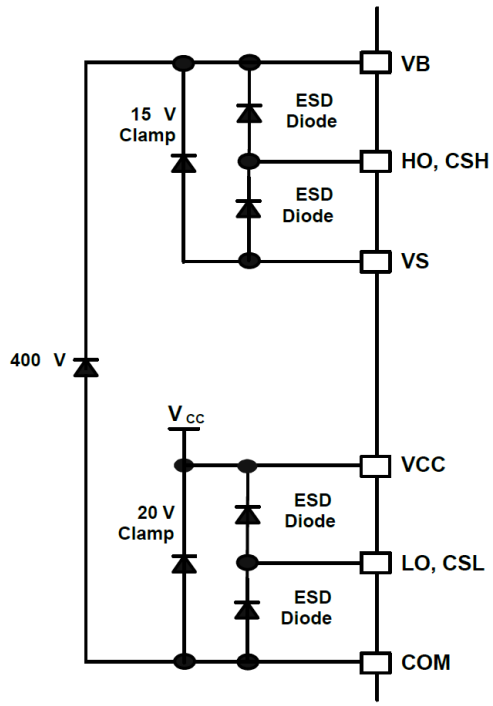








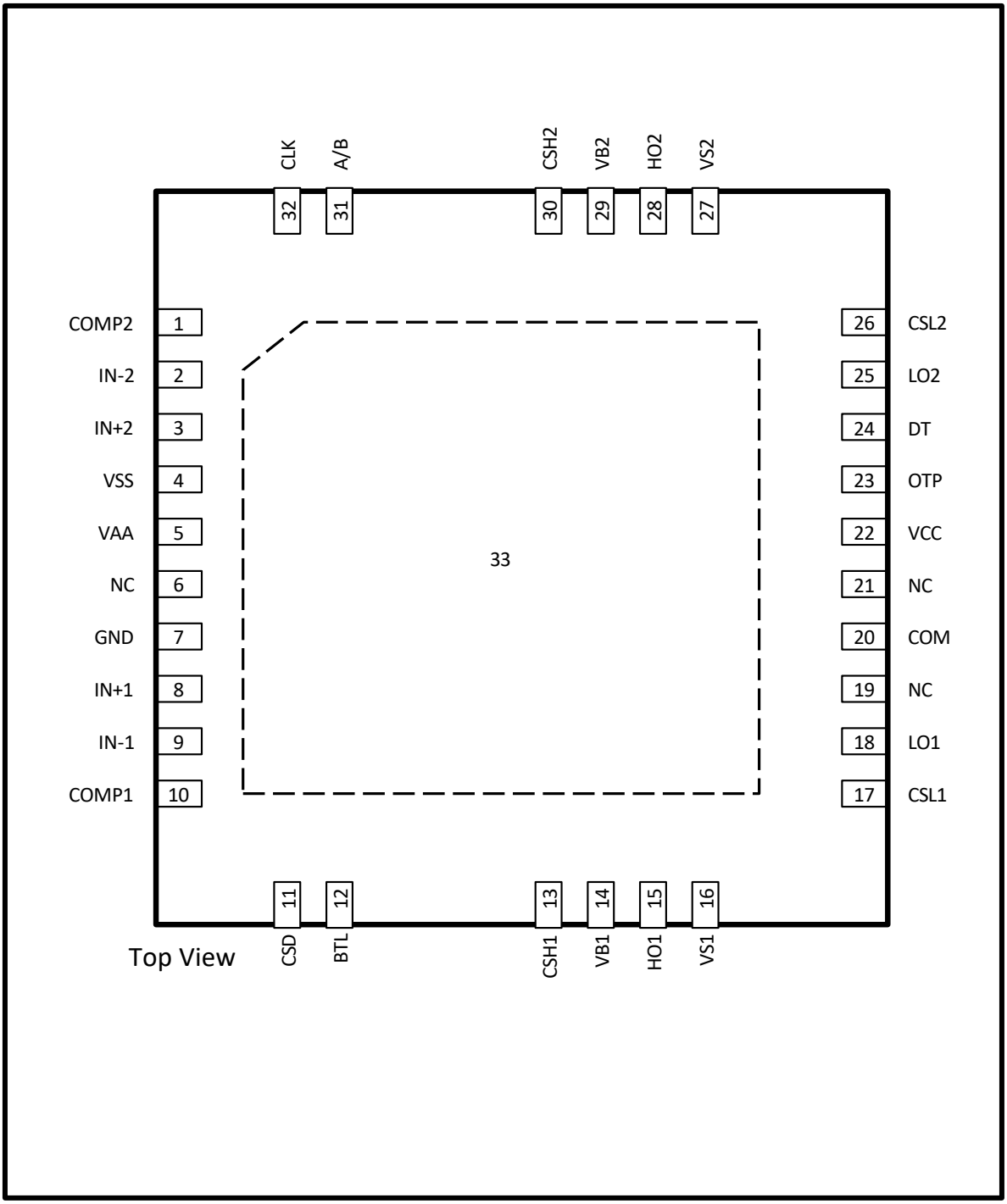
输入/输出引脚等效电路图（续）



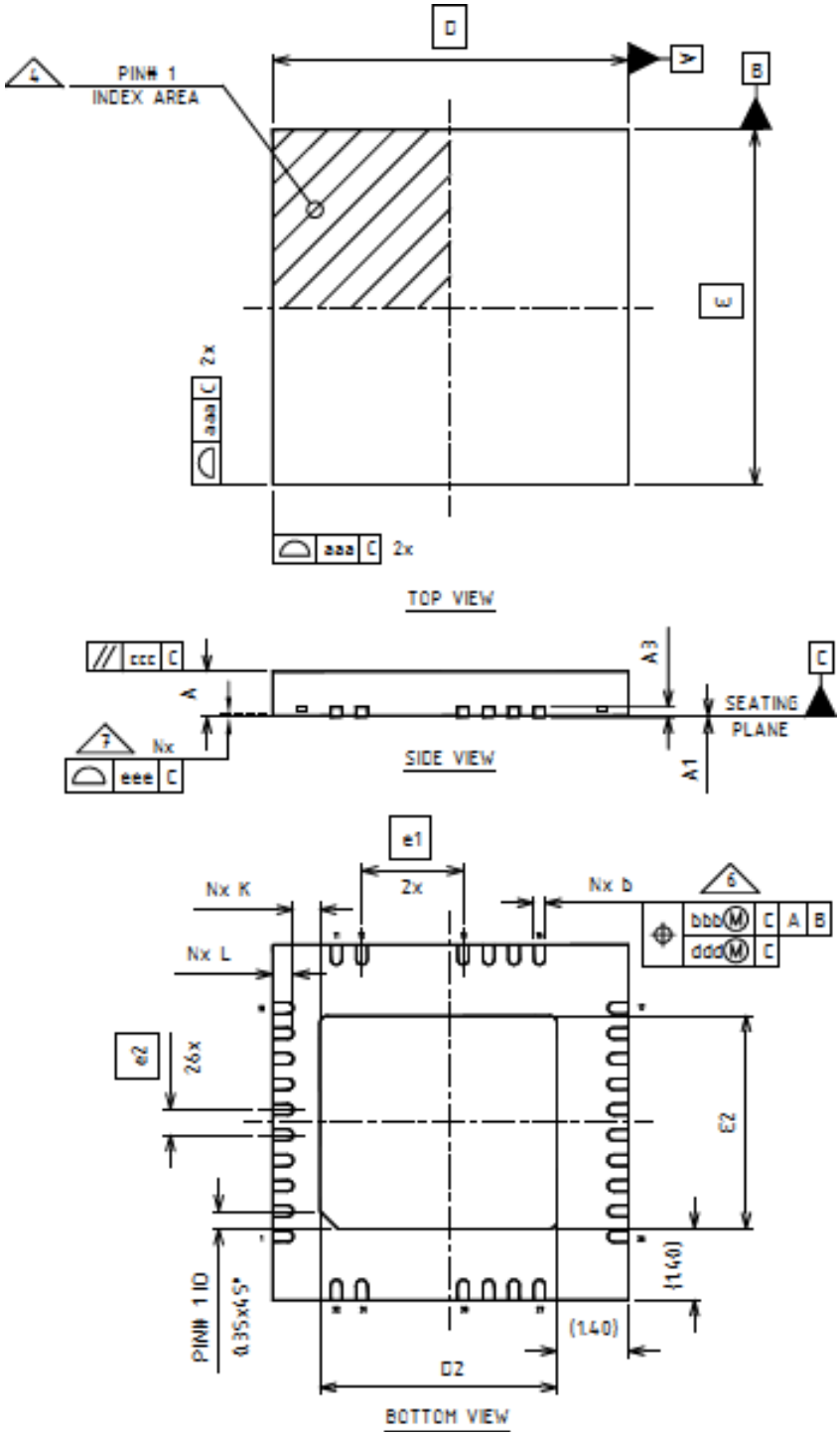
引线定义

Pin #	Symbol	I/O	Description
1	COMP2	O	CH2 PWM comparator input
2	IN-2	I	CH2 inverting analog input
3	IN+2	I	CH2 non-inverting analog input
4	VSS	I	Floating input negative supply
5	VAA	I	Floating input positive supply
6	NC		
7	GND	I	Input reference GND
8	IN+1	I	CH1 non-inverting analog input
9	IN-1	I	CH1 inverting analog input
10	COMP1	O	CH1 PWM comparator input
11	CSD	I/O	Protection control
12	BTL	I	BTL mode select (VAA: 2CH mode, GND-VSS: BTL mode)
13	CSH1	I	CH1 High side over current sensing input, referenced to VS1
14	VB1	I	CH1 High side floating supply
15	HO1	O	CH1 High side output
16	VS1	I	CH1 High side floating supply return
17	CSL1	I	CH1 Low side over current sensing input, referenced to COM
18	LO1	O	CH1 Low side output
19	NC		
20	COM	I	Low side gate drive supply return
21	NC		
22	VCC	I	Low side gate drive supply
23	OTP	I	OTP sensor input
24	DT	I	Deadtime program, reference to COM
25	LO2	O	CH2 Low side output
26	CSL2	I	CH2 Low side over current sensing input, referenced to COM
27	VS2	I	CH2 High side floating supply return
28	HO2	O	CH2 High side output
29	VB2	I	CH2 High side floating supply
30	CSH2	I	CH2 High side over current sensing input, referenced to VS2
31	A/B	I	Clock phase select (VAA: In-phase, VSS: Out-of-phase)
32	CLK	I	Clock input, reference to GND
33	SUB	I	Internally connected to COM (Do not use as supply return)

引线分配 (MLPQ_7x7mm_32L)



封装详情


PIN# 1
INDEX AREA
TOP VIEW
SIDE VIEW
SEATING
PLANE
BOTTOM VIEW
PIN# 1 ID
0.35x45°

Dimension Table				
Thickness / Symbol	V			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.203 Ref	---	
b	0.18	0.25	0.30	6
D	7.00 BSC			
E	7.00 BSC			
e1	2.00 BSC			
e2	0.50 BSC			
D2	4.525	4.675	4.775	
E2	4.05	4.20	4.30	
K	0.20	---	---	
L	0.30	0.40	0.50	
aaa	0.05			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			
N	32			3
ND	6			5
NE	10			5
NOTES	1, 2			
LF DWG NO.	B-4396			
REV.	1			

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.

2. All dimensions are in millimeters.

3. N is the total number of terminals.

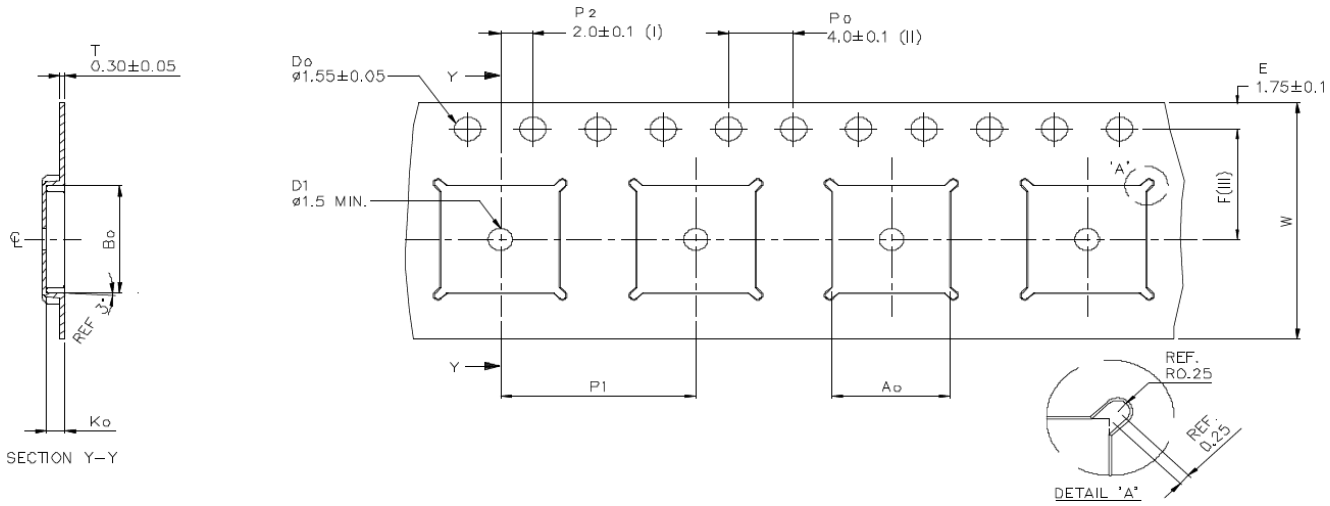
4. The location of the marked terminal #1 identifier is within the hatched area.

5. ND and NE refer to the number of terminals on each D and E side respectively.

6. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.

7. Coplanarity applies to the terminals and all other bottom surface metallization.

卷带详情



Ao	7.25 +/−0.1
Bo	7.25 +/−0.1
Ko	1.10 +/−0.1
F	7.50 +/−0.1
P1	12.00 +/−0.1
W	16.00 +/−0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Typical SR of form tape Max 10^9 OHM/SQ

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

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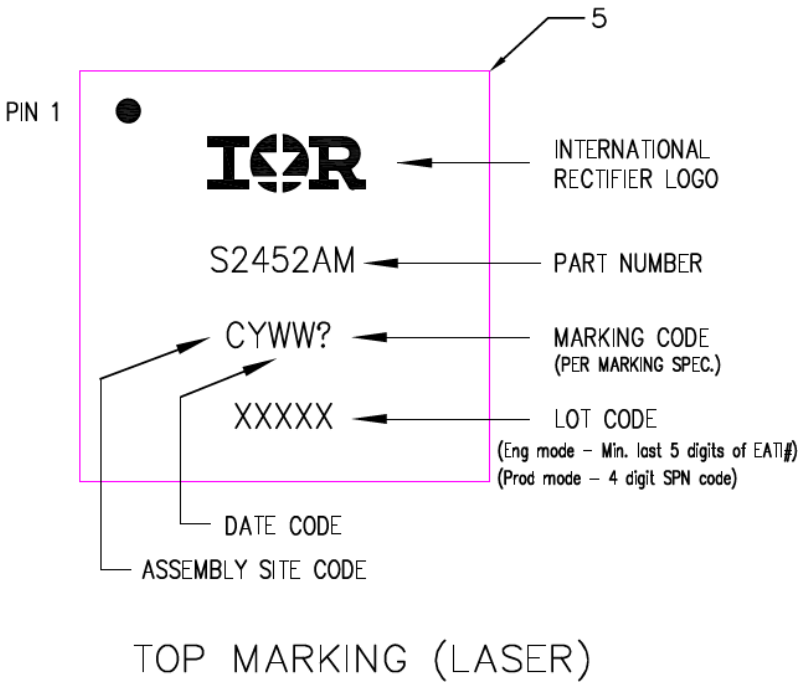
PQFN 封装产品的可靠性取决于电路板安装工艺。焊接工艺至关重要。有关具体焊接方法，请参阅应用说明 AN-1170 音频功率四扁平无引线 (PQFN) 电路板安装应用说明。

零件标记信息



TOP MARKING (LASER)

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