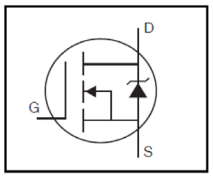
IRLR2705PbF

英飞凌HEXFET ®功率MOSFET

特性

- 逻辑电平栅极驱动
- 超低导通电阻
- 先进工艺技术
- 快速开关
- 雪崩完全额定
- 无铅



V_{DSS}	55V
$R_{DS(on)}$	0.040Ω
I_D	28A⑤

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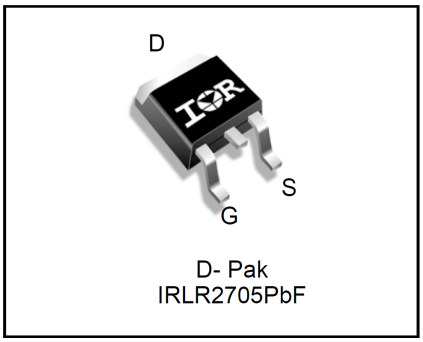
说明

英飞凌第五代 HEXFET 采用先进的加工技术，实现了单位硅面积上最低的导通电阻。这一优点与 HEXFET众所周知的快速开关速度和坚固耐用的器件设计相结合，为设计人员提供了一种可用于各种应用的极为高效的器件。

D-PAK 封装专为表贴工艺设计，可兼容气相焊、红外焊或波峰焊工艺。在典型的表贴应用中，功耗最高可达 1.5 瓦。



D- Pak
IRLR2705PbF

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRLR2705PbF	D-Pak	Tape and Reel	2000	IRLR2705TRPbF

绝对最大额定值

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	28	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	20	
I_{DM}	Pulsed Drain Current ①	110	
P_D @T_C = 25°C	Maximum Power Dissipation	68	W
	Linear Derating Factor	0.45	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy②	110	mJ
I_{AR}	Avalanche Current①	16	A
E_{AR}	Repetitive Avalanche Energy ①	6.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

热阻

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	2.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑥	---	50	
$R_{\theta JA}$	Junction-to-Ambient	---	110	

本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。为确认准确性，请务必访问 infineon.com 参考最新的英文版本（控制文档）。

电气特性 @T_J = 25°C（除非另有说明）

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	---	---	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	---	0.065	---	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	---	---	0.040	Ω	V_{GS} = 10V, I_D = 17A ④
		---	---	0.051		V_{GS} = 5.0V, I_D = 17A ④
		---	---	0.065		V_{GS} = 4.0V, I_D = 14A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	---	2.0	V	V_{DS} = V_{GS}, I_D = 250µA
gfs	Forward Trans conductance	11	---	---	S	V_{DS} = 25V, I_D = 16A ⑦
I_{DSS}	Drain-to-Source Leakage Current	---	---	25	µA	V_{DS} = 55V, V_{GS} = 0V
		---	---	250		V_{DS} = 44V,V_{GS} = 0V,T_J =150°C
I_{GSS}	Gate-to-Source Forward Leakage	---	---	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	---		-100		V_{GS} = -16V
Q_g	Total Gate Charge	---	---	25	nC	I_D = 16A
Q_{gs}	Gate-to-Source Charge	---	---	5.2		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ('Miller') Charge	---		14		V_{GS} = 5.0V, See Fig. 6 and 13 ④⑦
$t_{d(on)}$	Turn-On Delay Time	---	8.9	---	ns	V_{DD} = 28V
t_r	Rise Time	---	100	---		I_D = 16A
$t_{d(off)}$	Turn-Off Delay Time	---	21	---		R_G = 6.5Ω,V_{GS} = 5.0V
t_f	Fall Time	---	29	---		R_D = 1.8Ω, See Fig. 10 ④⑦
L_D	Internal Drain Inductance	---	4.5	---	nH	Between lead, 6mm (0.25in.)
L_S	Internal Source Inductance	---	7.5	---		from package and center of die contact
C_{iss}	Input Capacitance	---	880	---	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	---	220	---		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	---	94	---		f = 1.0MHz, See Fig. 5⑦

源极-漏极额定值与特性

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	---	---	28	A	MOSFET symbol showing the
I_{SM}	Pulsed Source Current (Body Diode) ①	---	---	110		integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage	---	---	1.3	V	T_J = 25°C,I_S = 17A,V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	---	76	110	ns	T_J = 25°C ,I_F = 16A
Q_{rr}	Reverse Recovery Charge	---	190	290	nC	di/dt = 100A/µs ④⑦
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

注：

① 重复额定值；脉冲宽度受最高结温限制。（见图11）

② V_{DD} = 25V, starting T_J = 25°C, L = 610µH, R_G = 25Ω, I_{AS} = 16A. (见图 12)

③ I_{SD} ≤ 16A, dv/dt ≤ 270A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ 175°C

④ 脉冲宽度 ≤ 300µs; 占空比 ≤ 2%。

⑤ 根据最大允许结温计算连续电流。封装限制电流为 20A。

⑥ 安装在 1 英寸方形PCB （FR-4 或 G-10 材料）上时。关于推荐的封装和焊接技术，请参阅应用笔记 #AN-994。

⑦ 使用 IRFZ34N 数据和测试条件。

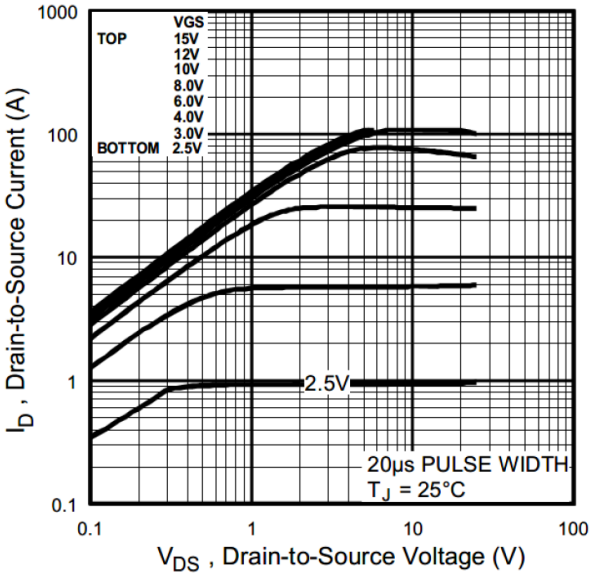


Fig. 1 Typical Output Characteristics

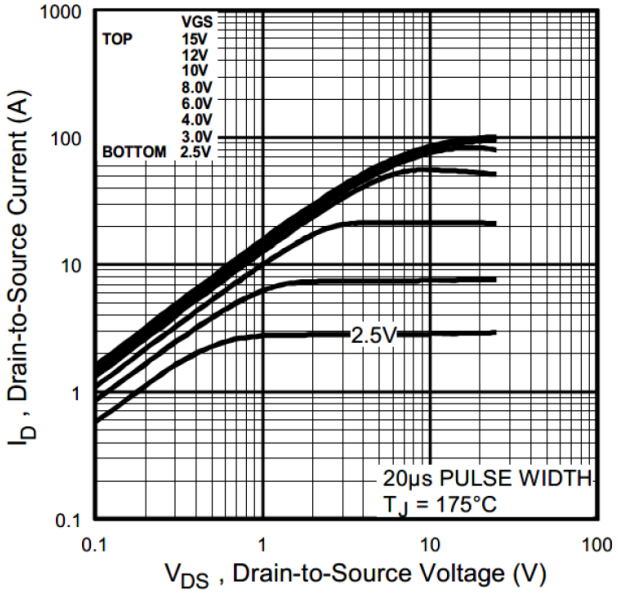


Fig. 2 Typical Output Characteristics

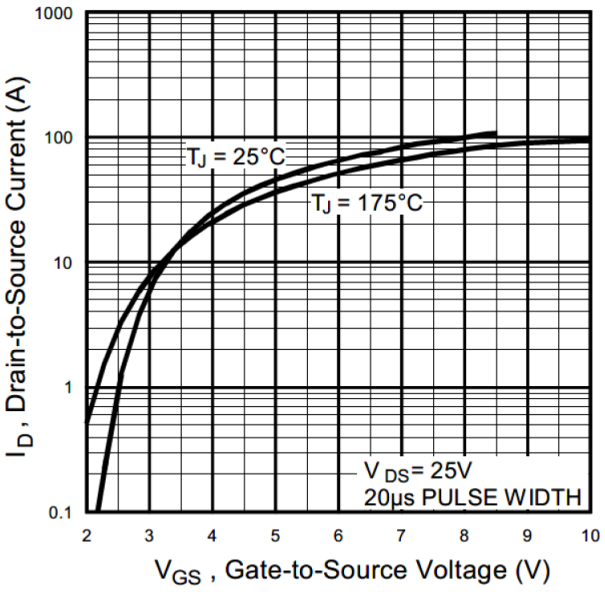


Fig. 3 Typical Transfer Characteristics

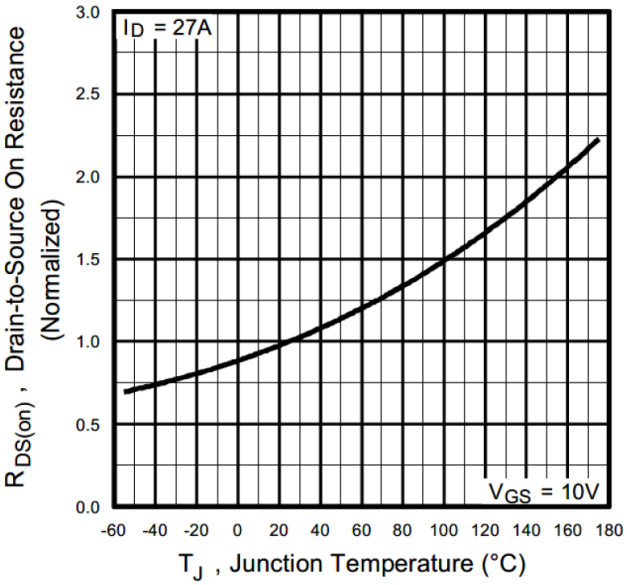


Fig. 4 Normalized On-Resistance vs. Temperature

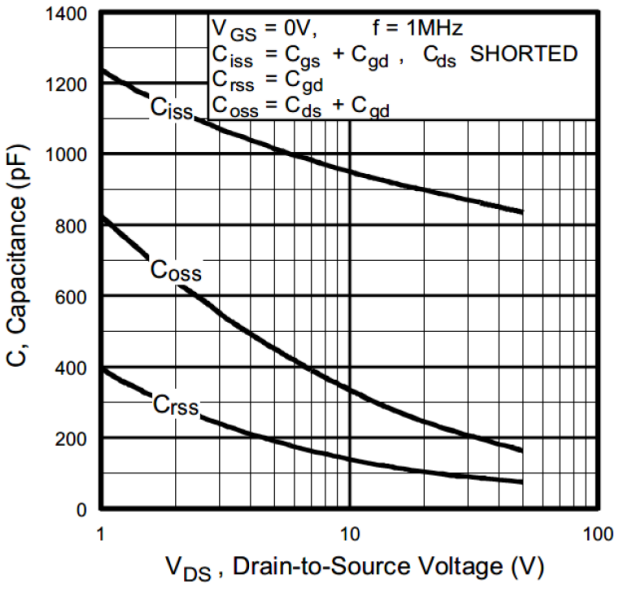


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

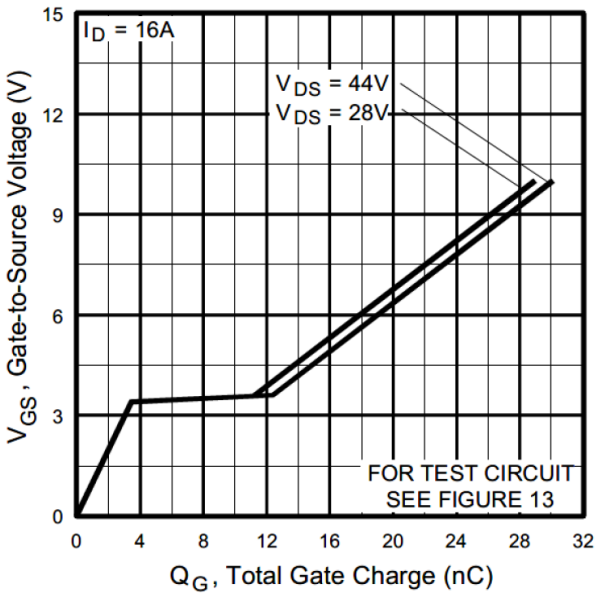


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

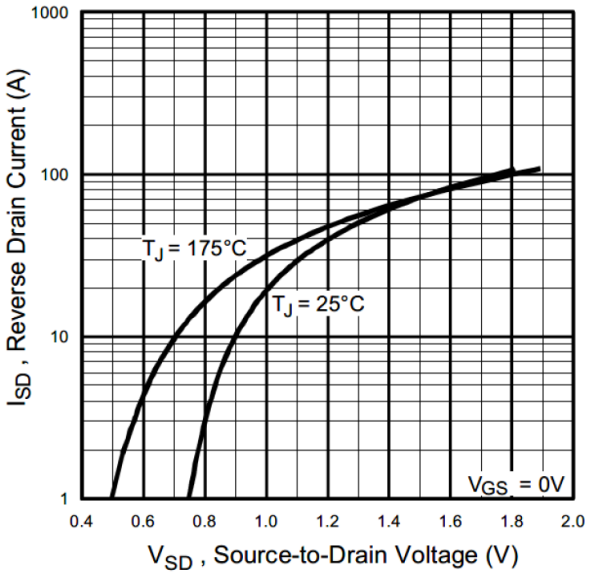


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

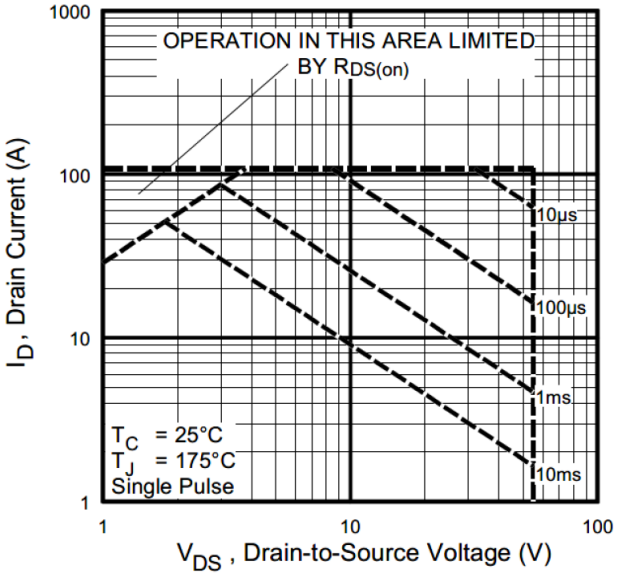


Fig 8. Maximum Safe Operating Area

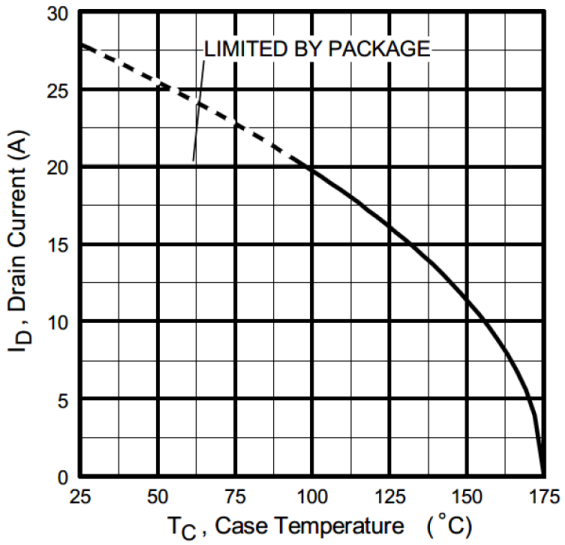


Fig 9. Maximum Drain Current vs. Case Temperature

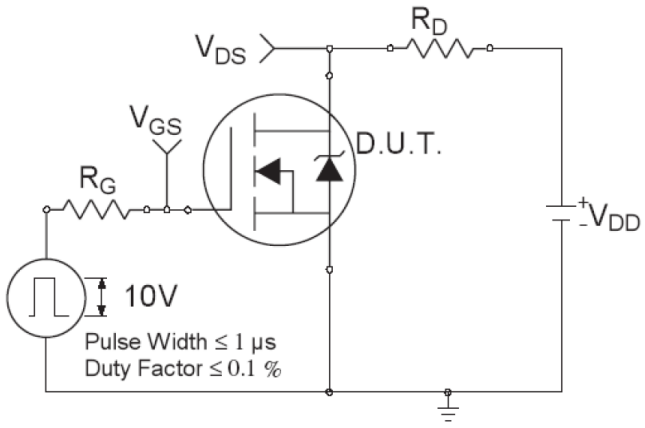


Fig 10a. Switching Time Test Circuit

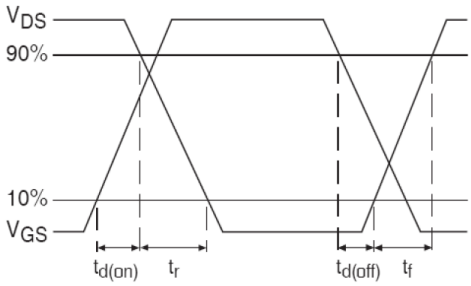


Fig 10b. Switching Time Waveforms

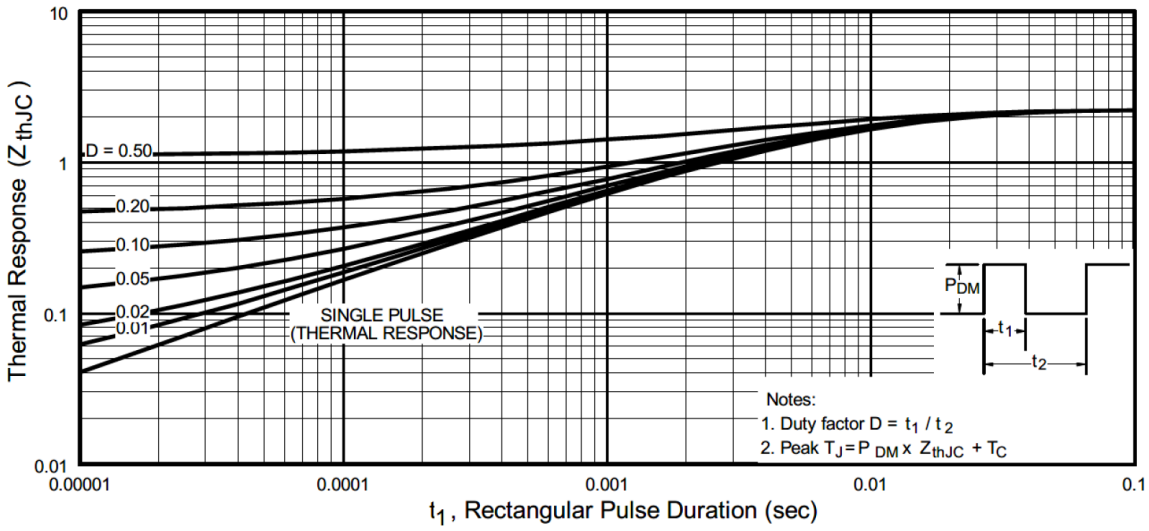


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

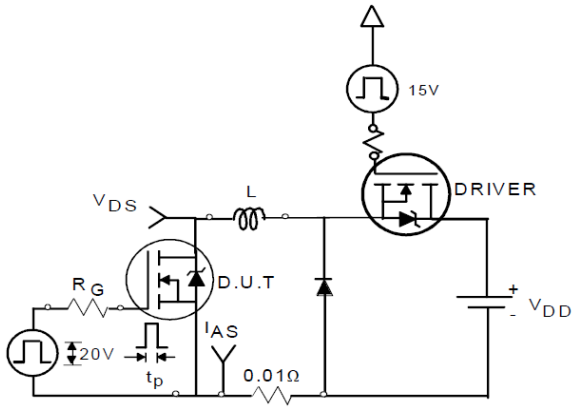


Fig 12a. Unclamped Inductive Test Circuit

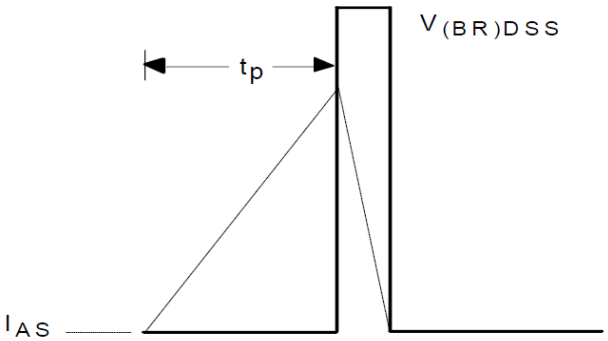


Fig 12b. Unclamped Inductive Waveforms

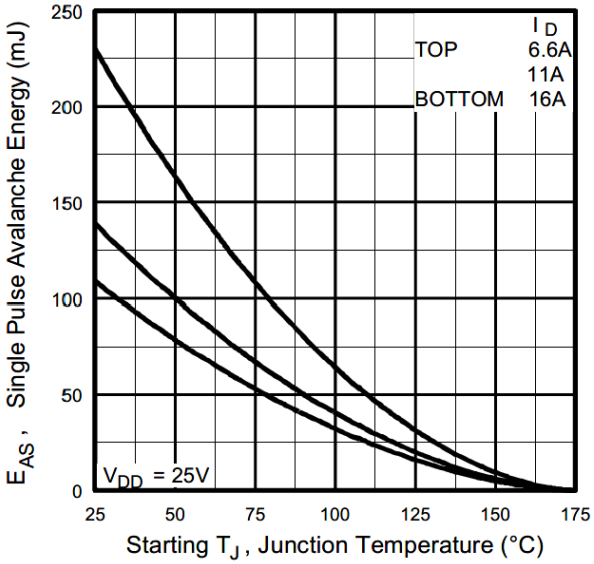


Fig 12c. Maximum Avalanche Energy vs. Drain Current

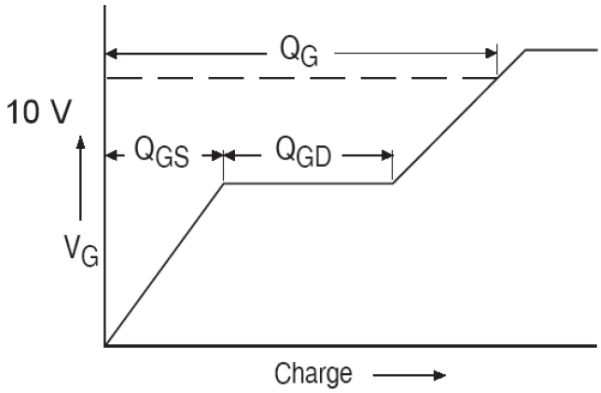


Fig 13a. Gate Charge Waveform

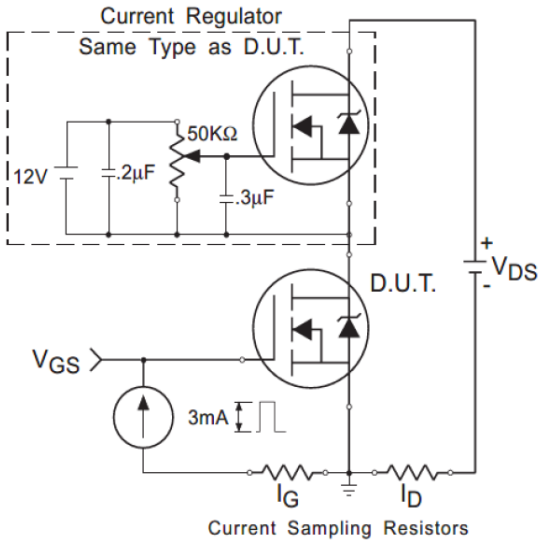


Fig 13b. Gate Charge Test Circuit

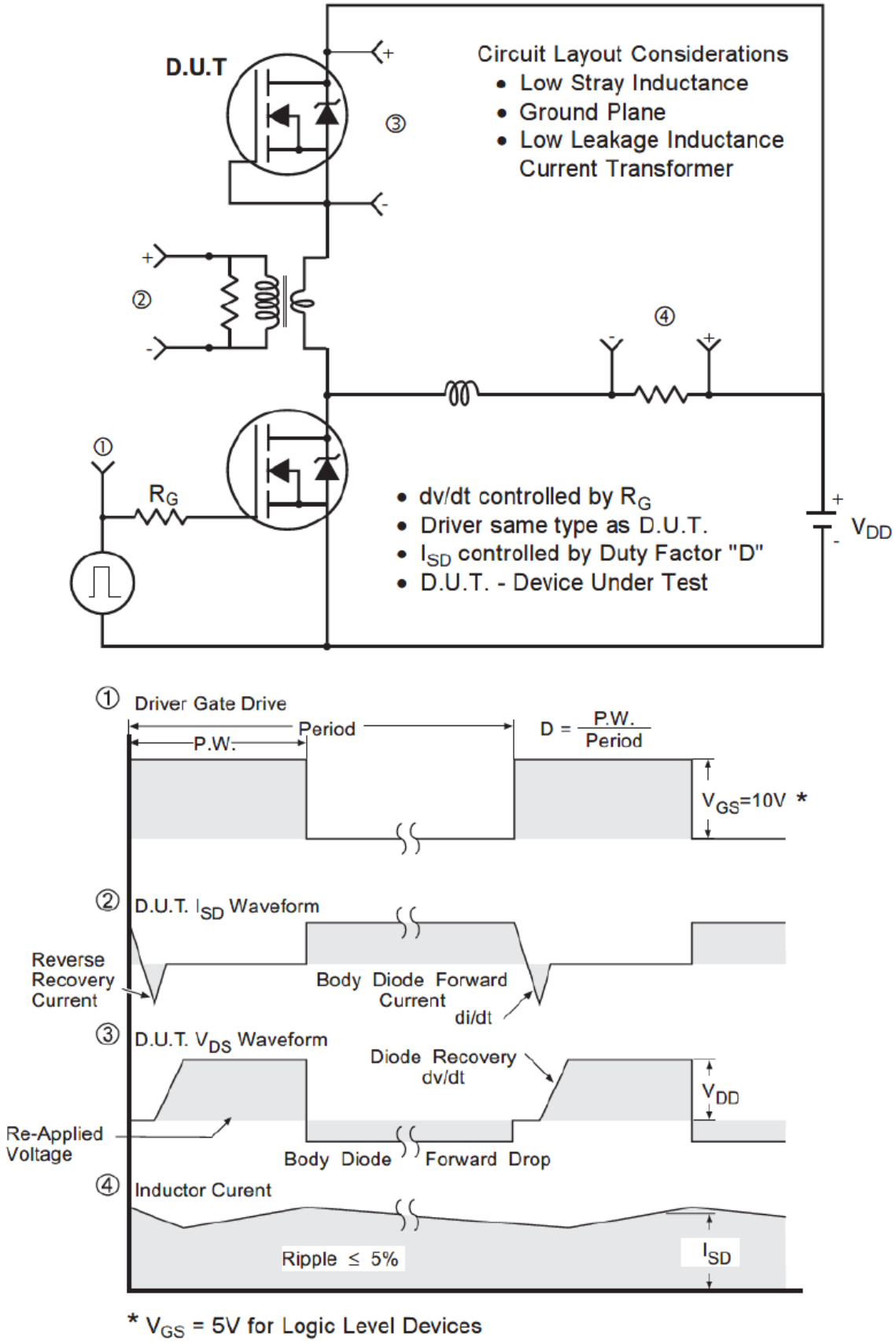
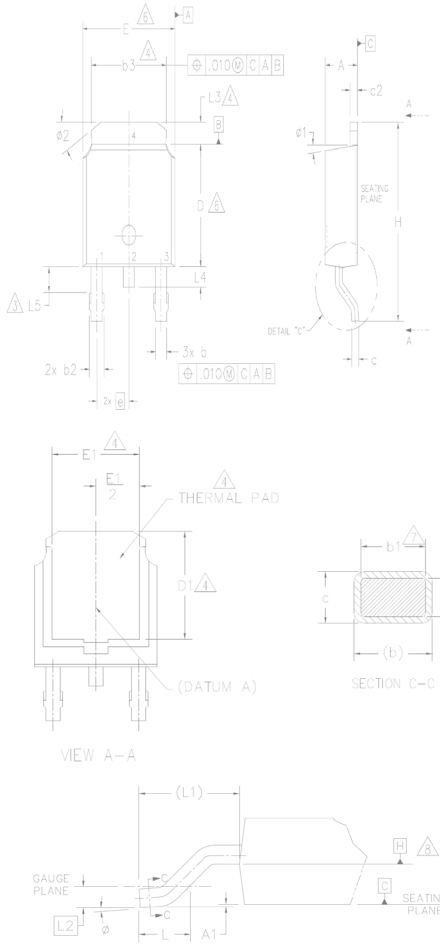


Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

D-Pak (TO-252AA) 封装外形（尺寸以毫米（英寸）为单位）



NOTES:
1.– DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2.– DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
3.– LEAD DIMENSION UNCONTROLLED IN L5.
4.– DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5.– SECTION C–C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
6.– DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
7.– DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
8.– DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
9.– OUTLINE CONFORMS TO JEDEC OUTLINE TO–252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	–	0.13	–	.005	
b	0.64	0.89	.025	.035	
b1	0.64	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	6
E1	4.32	–	.170	–	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	–	1.02	–	.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	
ø2	25°	35°	25°	35°	

LEAD ASSIGNMENTS

HEXFET
1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

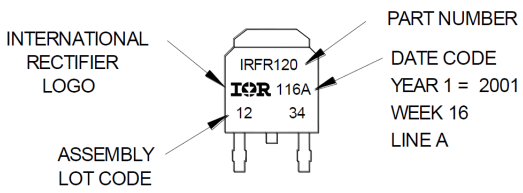
IGBT & CoPAK
1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

D-Pak (TO-252AA) 零件标识信息

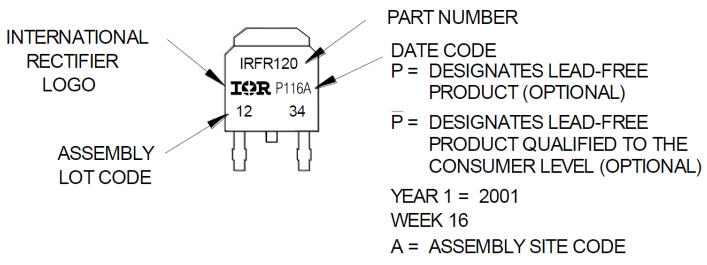
EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 2001
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"

"P̄" in assembly line position indicates "Lead-Free" qualification to the consumer-level

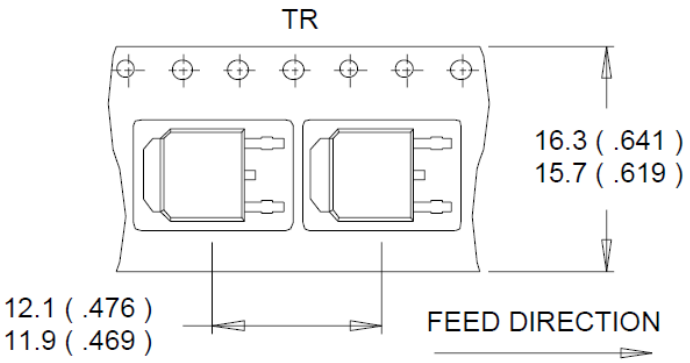


OR

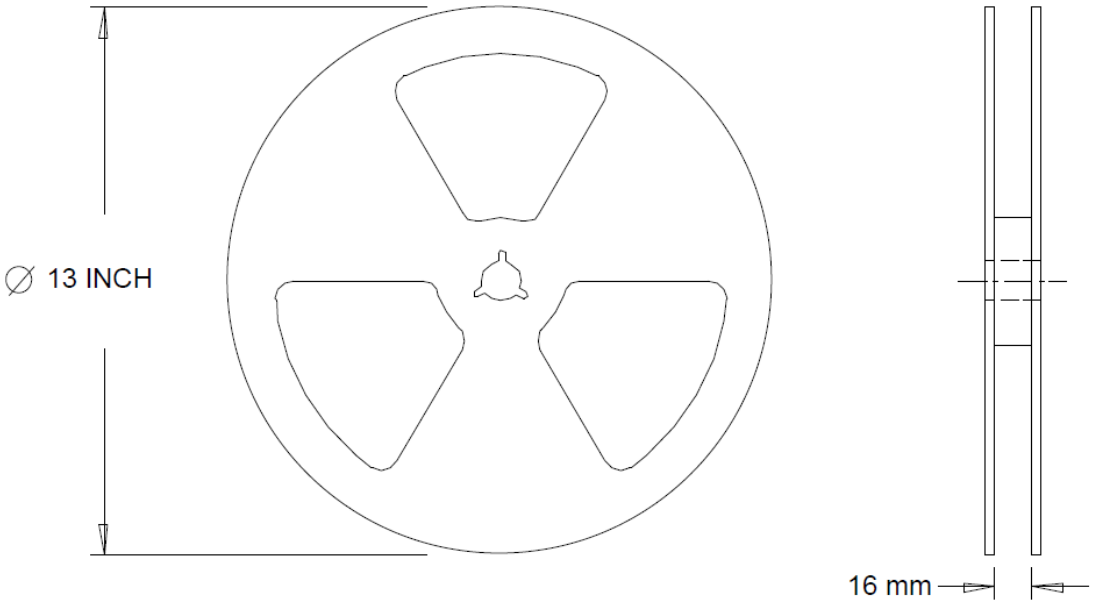


注：
1. 如需查看最新图纸，请访问英飞凌网站：http://www.infineon.com/package/

D-Pak (TO-252AA) 卷带信息（尺寸以毫米（英寸）为单位）



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

注：有关最新图纸，请参阅英飞凌网站 https://www.infineon.cn/ 及其链接。

修订记录

Date	Rev.	Comments
01/09/2025	2.1	• Changed datasheet with corporate template. • Removed I-Pack “(IRLU2705PbF)-All pages • Updated typo Rdson unit from “W” to “Ω”-page 2 • Updated disclaimer on last page.

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