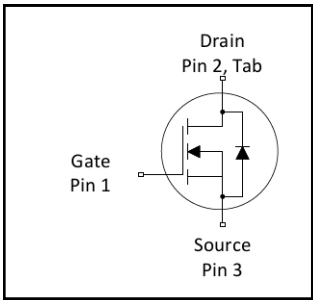
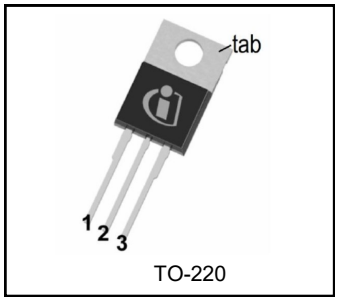
IRLB8748PbF

V_{DSS}	30V
$R_{DS(ON)}$ max	4.8mΩ
Q_G	15nC





G	D	S
Gate	Drain	Source

Applications

- Optimized for UPS/Inverter Applications
- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial use

Benefits

- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- Lead-Free

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRLB8748PbF	TO-220	Tube	50	IRLB8748PbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	92④	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	65	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	78	
I_{DM}	Pulsed Drain Current ①	370	
P_D @ T_C = 25°C	Power Dissipation ⑥	75	W
P_D @ T_C = 100°C	Power Dissipation ⑥	38	
	Linear Derating Factor	0.5	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw ⑦	10 lbf•in (1.1N•m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	2.0	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	62	

Notes ① through ⑦ are on page 2

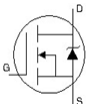
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	21	—	mV/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.8	4.8	mΩ	V_{GS} = 10V, I_D = 40A ③
		—	5.5	6.8		V_{GS} = 4.5V, I_D = 32A ③
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.8	2.35	V	V_{DS} = V_{GS}, I_D = 50µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold VoltageTemp. Coefficient	—	-7.1	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	µA	V_{DS} = 24V, V_{GS} = 0V
		—	—	150		V_{DS} = 24V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
gfs	Forward Trans conductance	196	—	—	S	V_{DS} = 15V, I_D = 32A
Q_g	Total Gate Charge	—	15	23	nC	V_{DS} = 15V I_D = 32A, V_{GS} = 4.5V③
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	3.6	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	2.2	—		
Q_{gd}	Gate-to-Drain Charge	—	5.9	—		
Q_{godr}	Gate Charge Overdrive	—	3.9	—		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	8.1	—		
Q_{oss}	Output Charge	—	11	—		V_{DS} = 16V,V_{GS} = 0V
R_G	Gate Resistance	—	2.0	3.5	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	14	—		V_{DS} = 15V, V_{GS} = 4.5V I_D = 32A R_G = 1.8Ω
t_r	Rise Time	—	96	—		
$t_{d(off)}$	Turn-Off Delay Time	—	16	—		
t_f	Fall Time	—	34	—		
C_{iss}	Input Capacitance	—	2139	—	pF	V_{GS} = 0V V_{DS} = 15V f = 1.0MHz
C_{oss}	Output Capacitance	—	464	—		
C_{rss}	Reverse Transfer Capacitance	—	199	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	114	mJ
I_{AR}	Repetitive Avalanche Current ①	—	32	A
E_{AR}	Repetitive Avalanche Energy ①	—	7.5	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	92④	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	370		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	T_J = 25°C,I_S = 32A,V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	23	35	ns	T_J = 25°C, I_F = 32A , V_{DD} = 15V
Q_{rr}	Reverse Recovery Charge	—	39	59	nC	di/dt = 200A/µs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 0.22mH, R_G = 25Ω, I_{AS} = 32A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 78A.

⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑥ R_θ is measured at T_J approximately 90°C.

⑦ This is only applied to TO-220AB package.

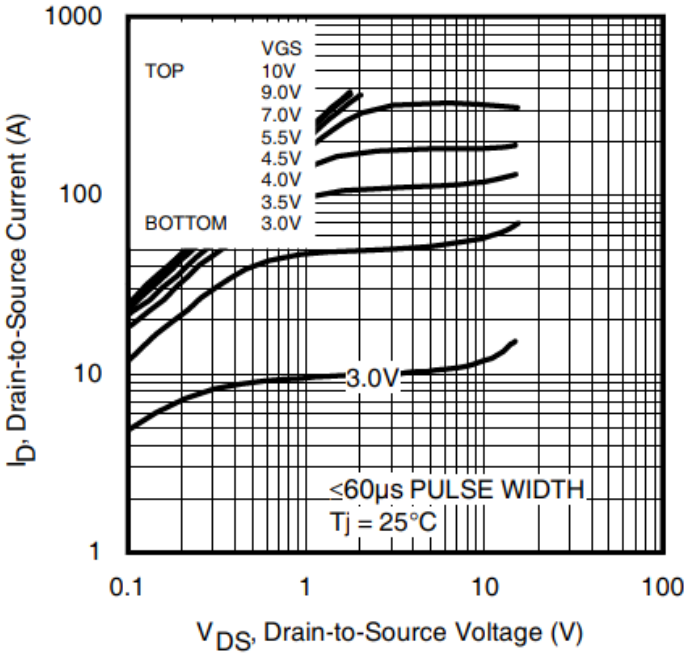


Fig. 1 Typical Output Characteristics

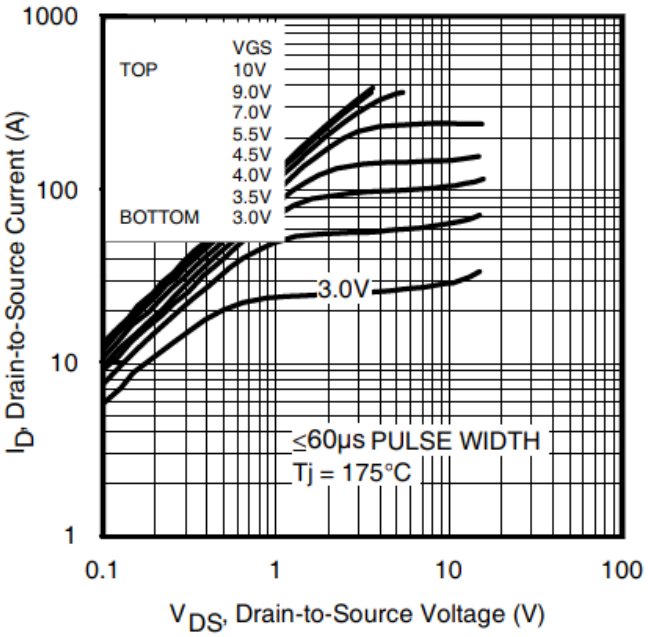


Fig. 2 Typical Output Characteristics

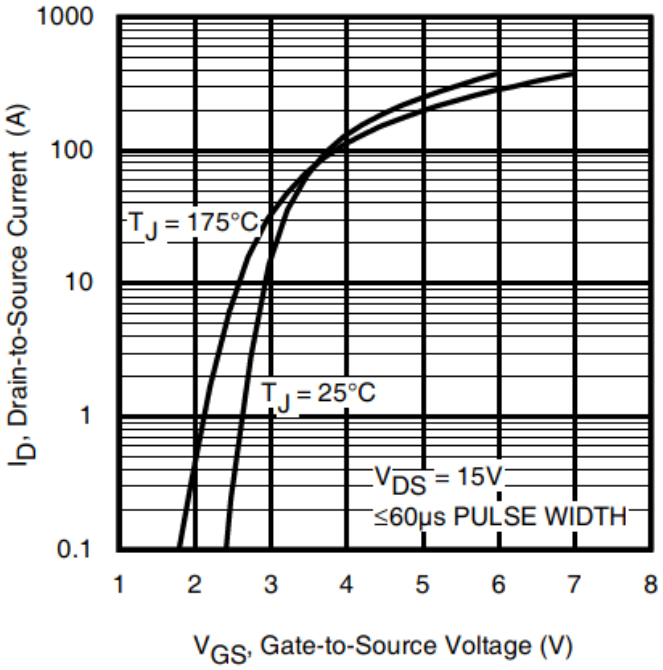


Fig. 3 Typical Transfer Characteristics

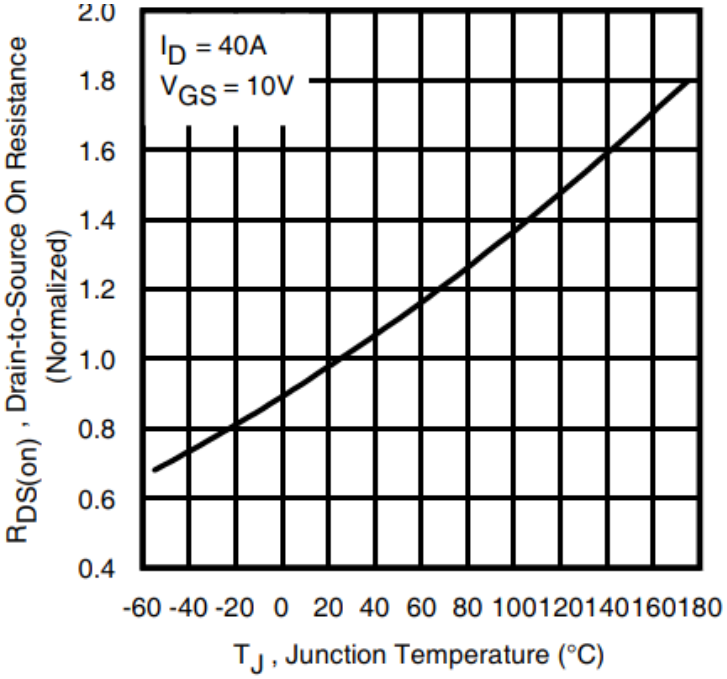


Fig. 4 Normalized On-Resistance vs. Temperature

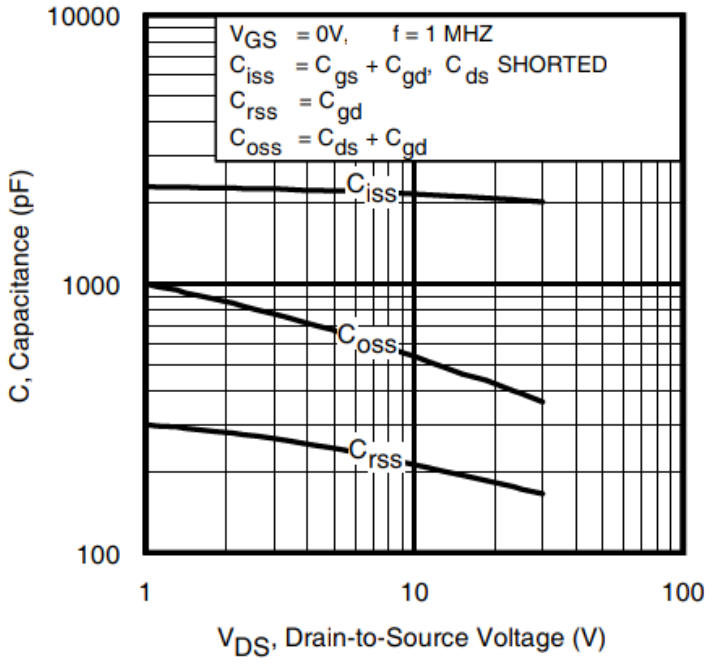


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

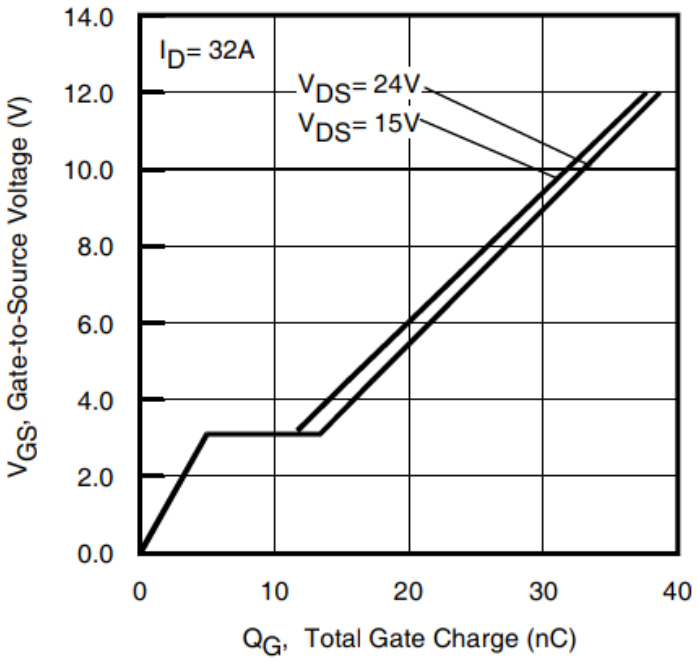


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

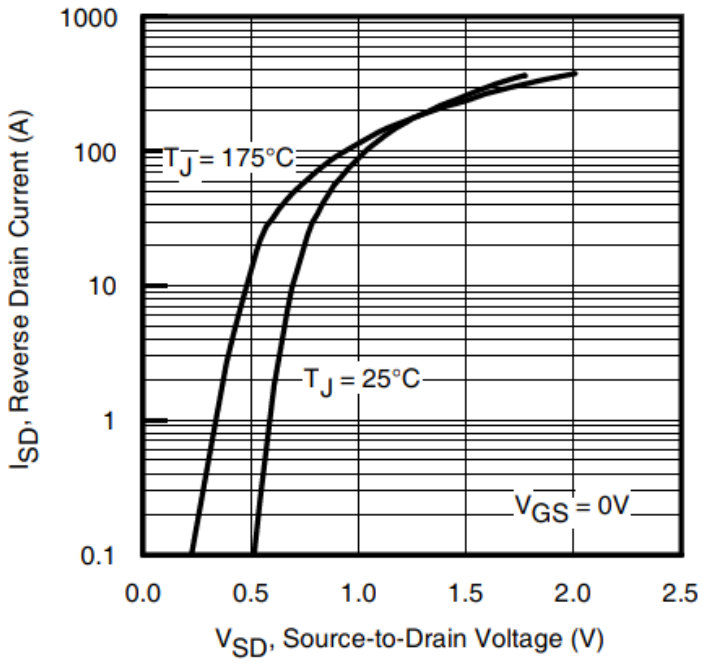


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

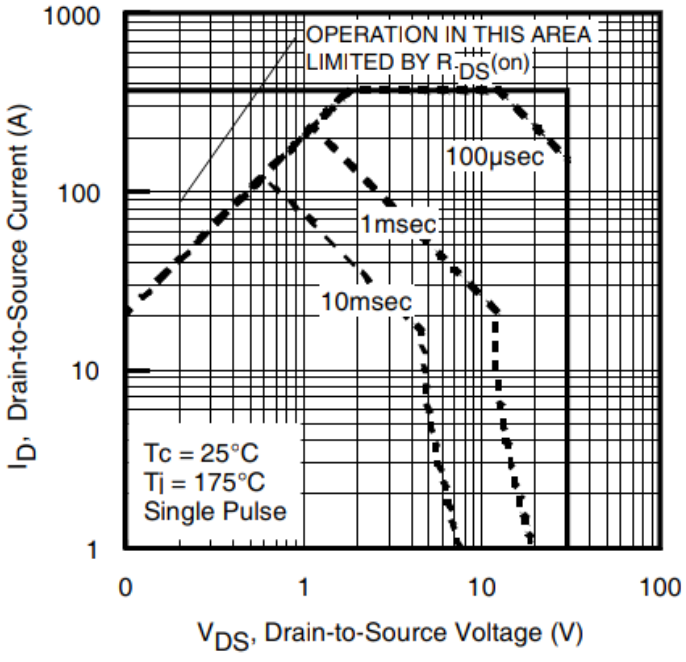


Fig 8. Maximum Safe Operating Area

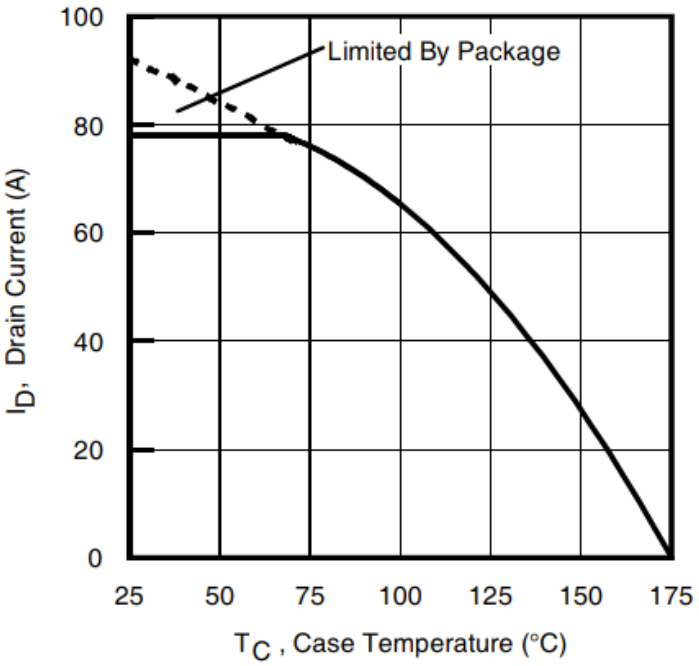


Fig 9. Maximum Drain Current vs. Case Temperature

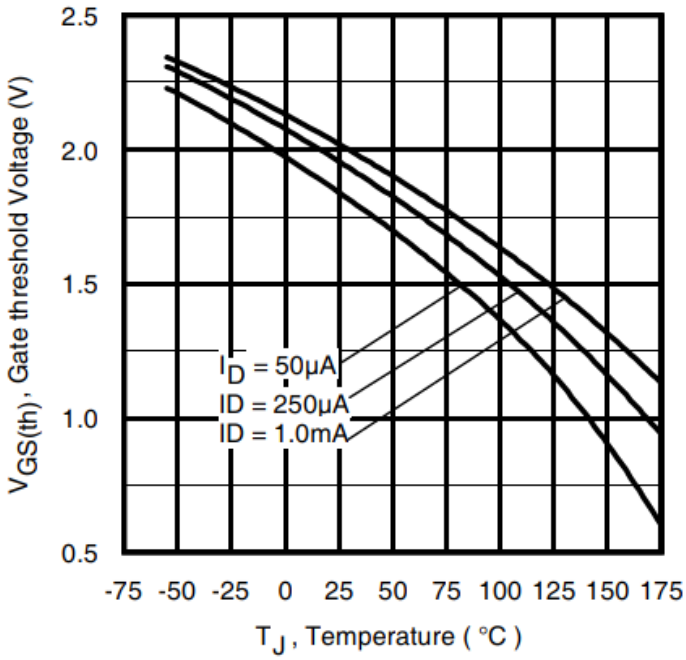


Fig 10. Threshold Voltage vs. Temperature

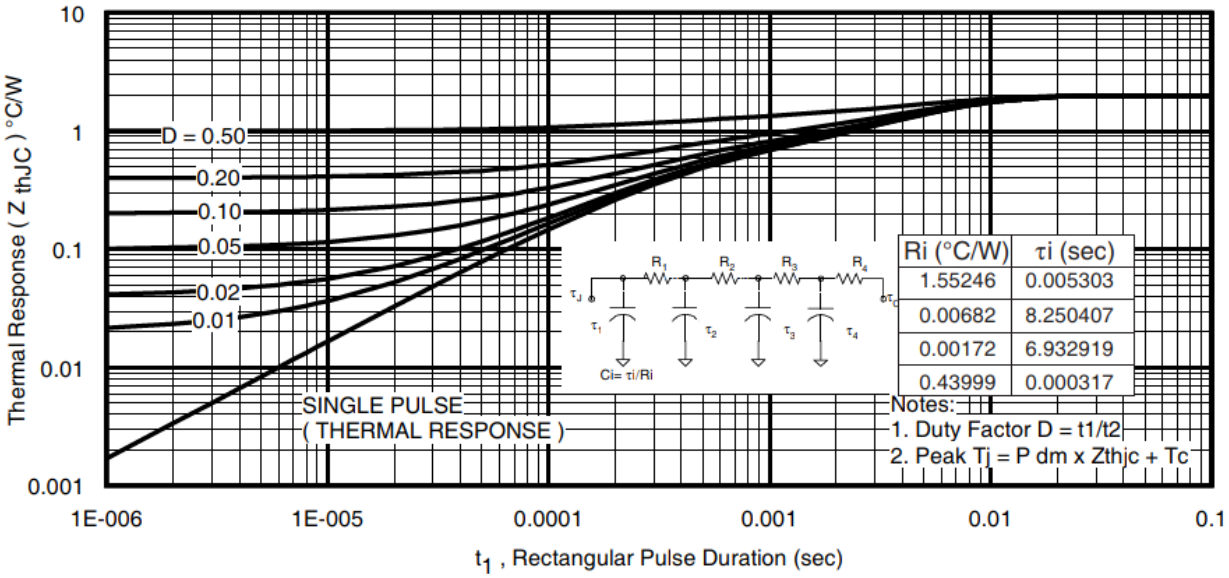


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

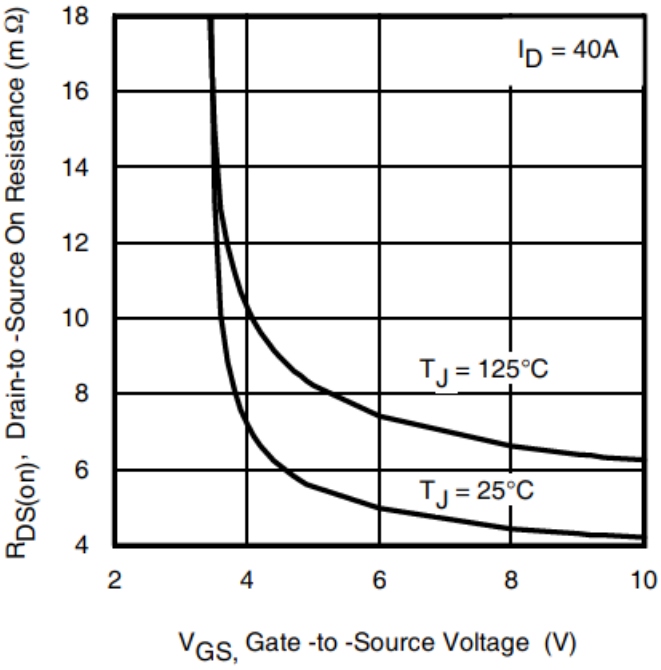


Fig 12. On-Resistance vs. Gate Voltage

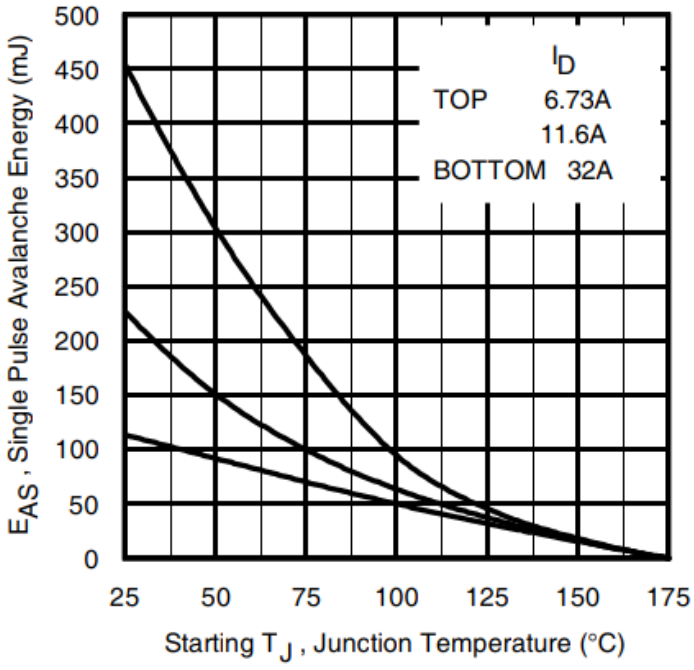


Fig 13c. Maximum Avalanche Energy vs. Drain Current

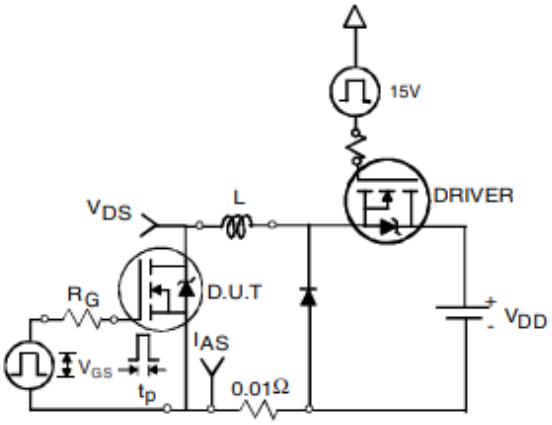


Fig 13a. Unclamped Inductive Test Circuit

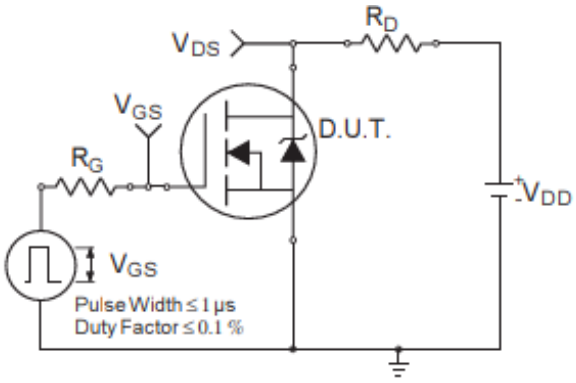


Fig 14a. Switching Time Test Circuit

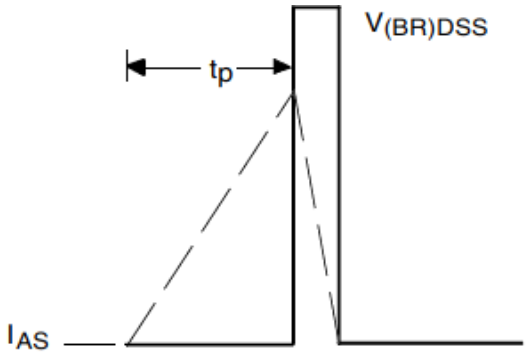


Fig 13b. Unclamped Inductive Waveforms

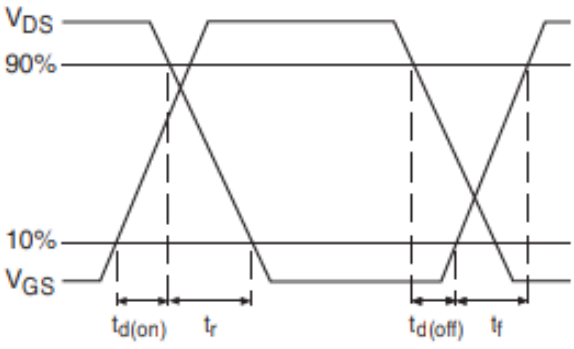


Fig 14b. Switching Time Waveforms

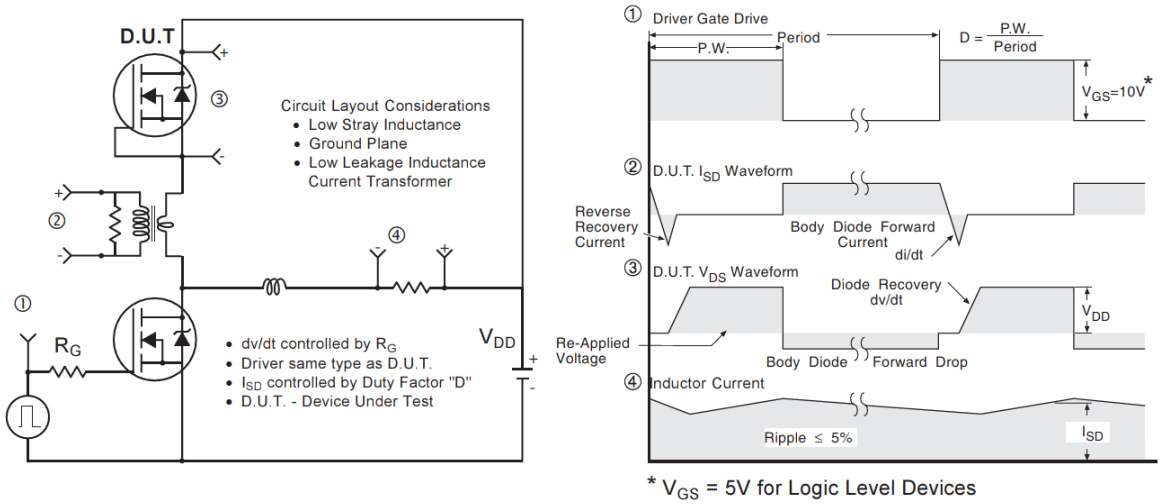


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

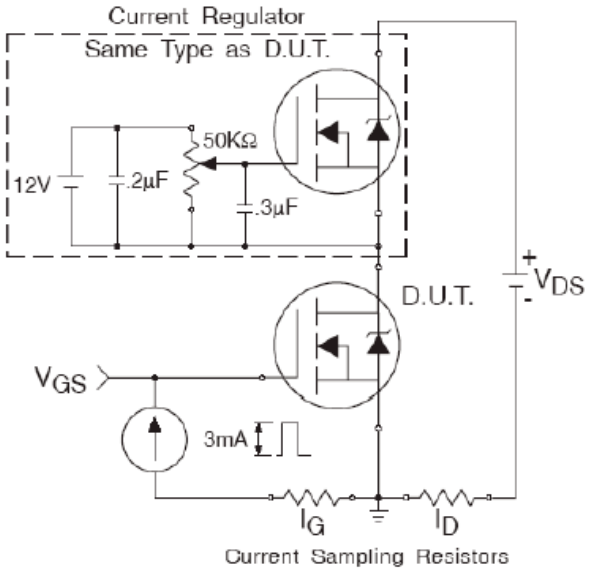


Fig 16. Gate Charge Test Circuit

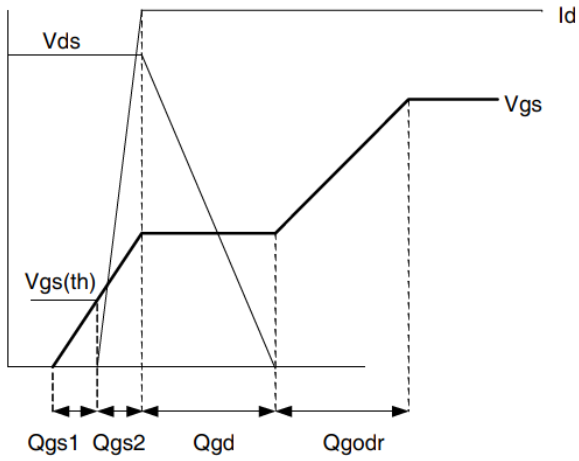
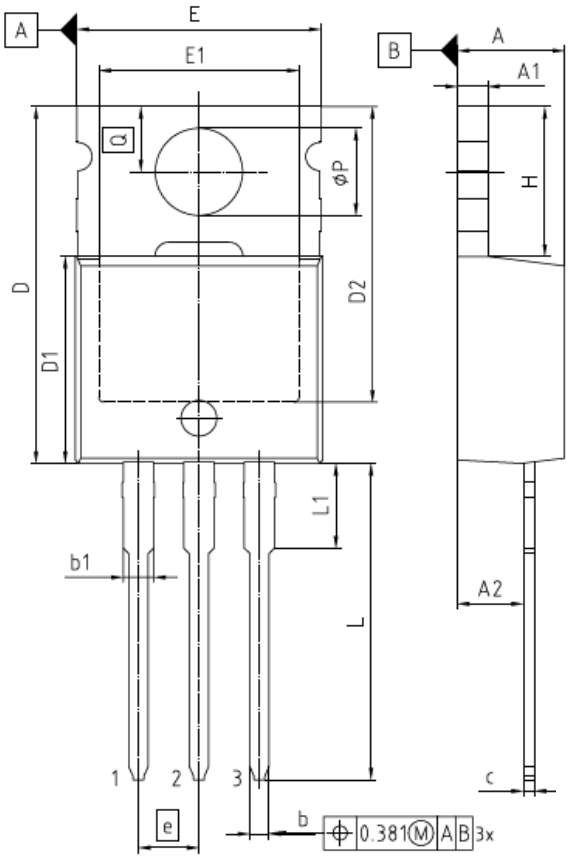


Fig 17. Gate Charge Waveform

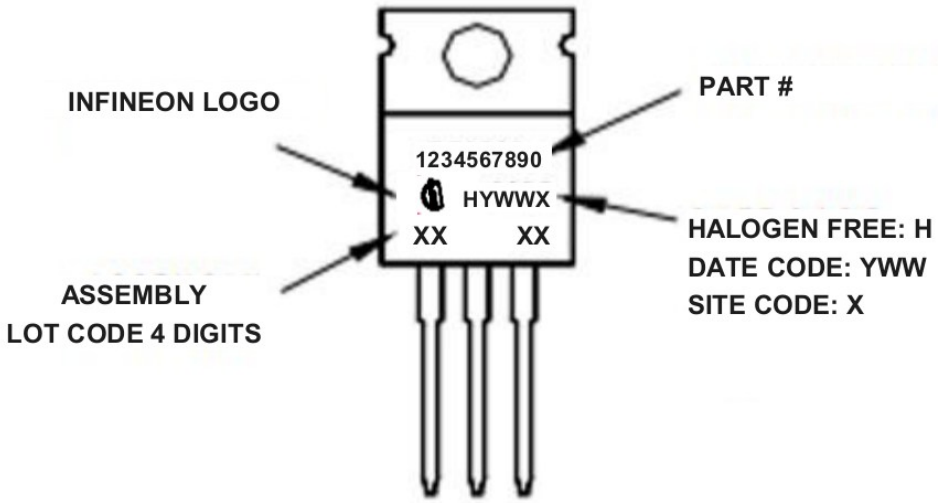
TO-220 Package Outline (Dimensions are shown in millimeters (inches))



NOTES:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

PACKAGE - GROUP NUMBER:	PG-TO220-3-U05	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	3.56	4.83
A1	1.14	1.40
A2	2.03	2.92
b	0.38	1.01
b1	1.14	1.78
c	0.36	0.61
D	14.22	16.51
D1	8.38	9.20
D2	11.68	12.88
E	9.65	10.67
E1	6.86	8.89
e	2.54	
N	3	
H	5.84	6.86
L	12.70	14.73
L1	3.56	4.06
øP	3.54	4.08
Q	2.54	3.42

TO-220 Part Marking Information



TO-220 packages are not recommended for Surface Mount Application.

Revision History

Date	Rev.	Comments
2026-09-26	2.1	• Update datasheet to Infineon format • Updated Package Outline and Part marking –page 8 • Added disclaimer on last page.

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