

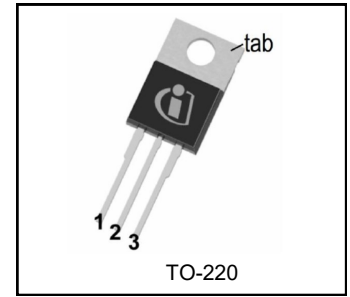
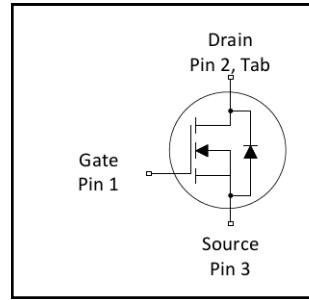
$V_{(BR)DSS}$	100V
$R_{DS(on)}$ typ.	3.4m Ω
	max. 4.3m Ω
I_D (Silicon Limited)	180A

Applications

- DC Motor Drive
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Optimized for Logic Level Drive
- Very Low $R_{DS(ON)}$ at 4.5V V_{GS}
- Superior R^*Q at 4.5V V_{GS}
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead Free



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRLB4030PbF	TO-220	Tube	50	IRLB4030PbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	180	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	130	
I_{DM}	Pulsed Drain Current ①	730	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	370	W
	Linear Derating Factor	2.5	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 16	V
dv/dt	Peak Diode Recovery ③	21	V/ns
T_J	Operating Junction and	-55 to + 175	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Avalanche Characteristics

E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	305	mJ
I_{AR}	Avalanche Current ①	See Fig.14,15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ④		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	0.40	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑦⑧	—	62	

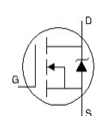
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.10	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 5mA$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.4	4.3	m Ω	$V_{GS} = 10V, I_D = 110A$ ④
		—	3.6	4.5		$V_{GS} = 4.5V, I_D = 92A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 100V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
R_G	Gate Resistance	—	2.1	—	Ω	

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

gfs	Forward Trans conductance	320	—	—	S	$V_{DS} = 25V, I_D = 110A$
Q_g	Total Gate Charge	—	87	130	nC	$I_D = 110A$
Q_{gs}	Gate-to-Source Charge	—	27	—		$V_{DS} = 50V$
Q_{gd}	Gate-to-Drain Charge	—	45	—		$V_{GS} = 4.5V$ ④
Q_{sync}	otal Gate Charge Sync. ($Q_g - Q_{gd}$)	—	42	—		$I_D = 110A, V_{DS} = 0V, V_{GS} = 4.5V$
$t_{d(on)}$	Turn-On Delay Time	—	74	—	ns	$V_{DD} = 65V$
t_r	Rise Time	—	330	—		$I_D = 110A$
$t_{d(off)}$	Turn-Off Delay Time	—	110	—		$R_G = 2.7\Omega$
t_f	Fall Time	—	170	—		$V_{GS} = 4.5V$ ④
C_{iss}	Input Capacitance	—	11360	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	670	—		$V_{DS} = 50V$
C_{rss}	Reverse Transfer Capacitance	—	290	—		$f = 1.0MHz$, See Fig. 5
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	760	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑥
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	1140	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑤

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	180	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	730		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 110A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	50	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 85V$
		—	60	—		$T_J = 125^\circ\text{C}$ $I_F = 110A$,
Q_{rr}	Reverse Recovery Charge	—	88	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ④
		—	130	—		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	3.3	—	A	$T_J = 25^\circ\text{C}$

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.05mH$, $R_G = 25\Omega$, $I_{AS} = 110A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ③ $I_{SD} \leq 110A$, $di/dt \leq 1330A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss \text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note# [AN-994](#).
- ⑧ R_θ is measured at T_J approximately 90°C .

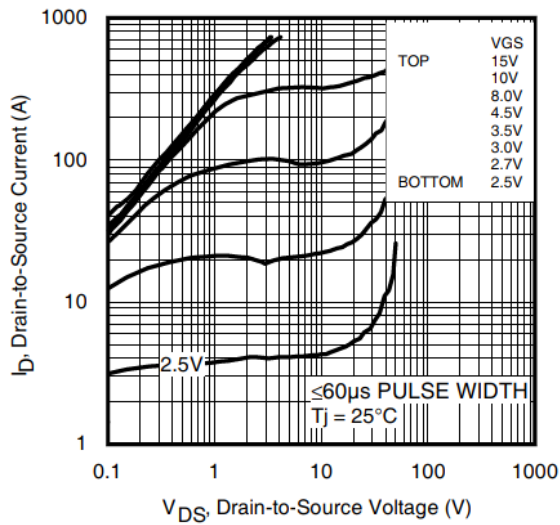


Fig. 1 Typical Output Characteristics

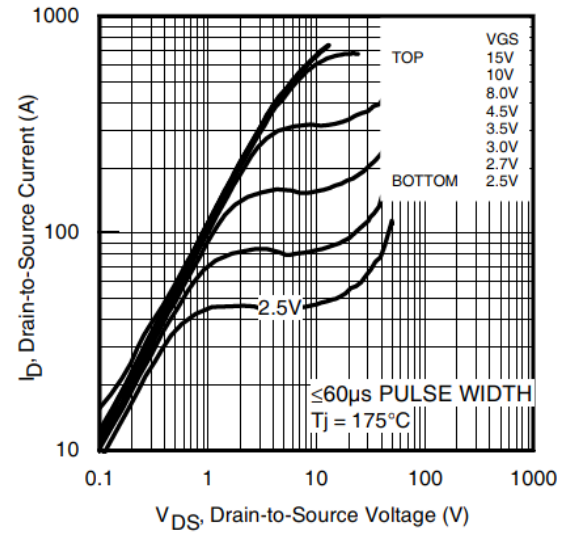


Fig. 2 Typical Output Characteristics

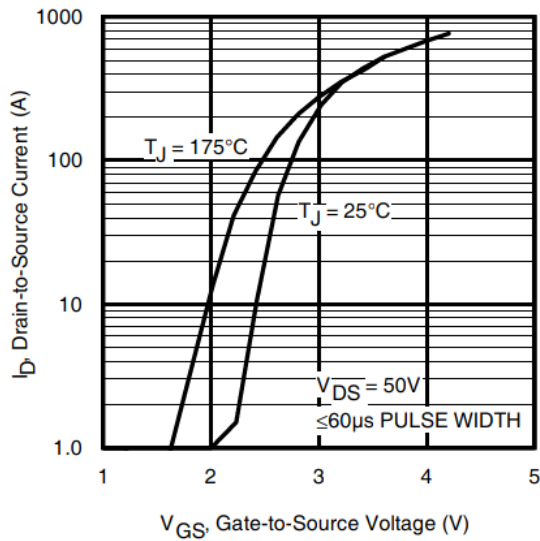


Fig. 3 Typical Transfer Characteristics

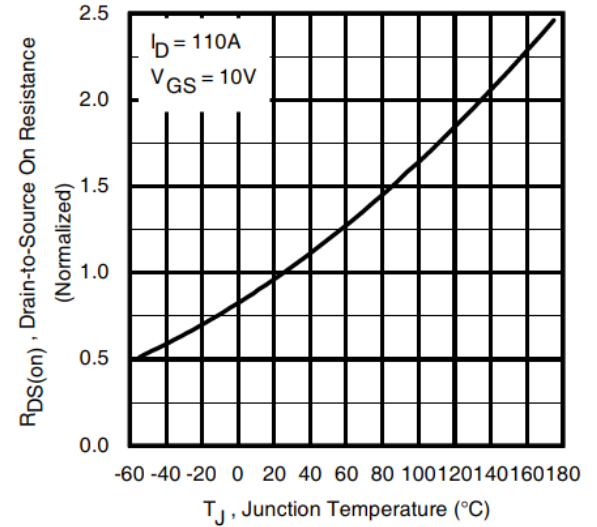


Fig. 4 Normalized On-Resistance vs. Temperature

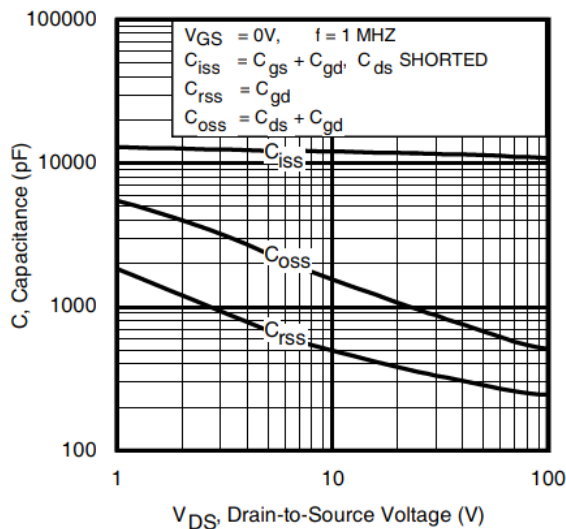


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

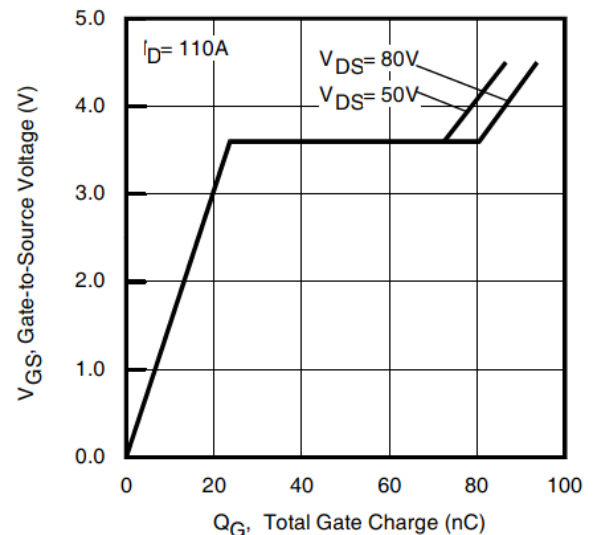


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

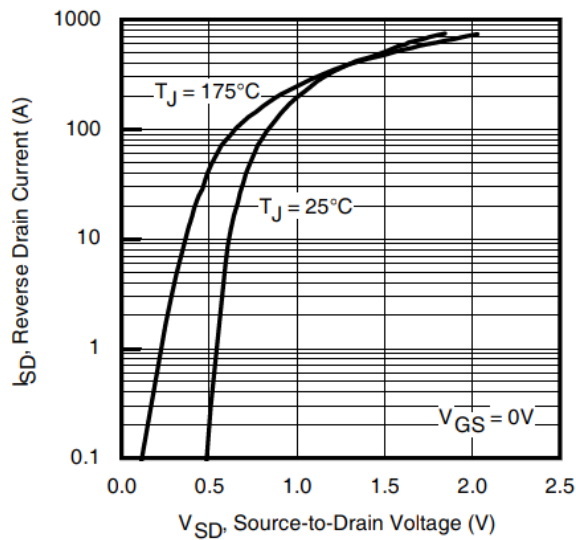


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

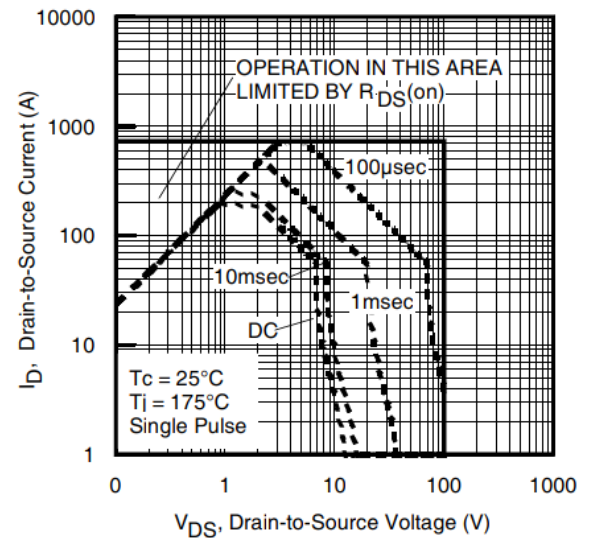


Fig 8. Maximum Safe Operating Area

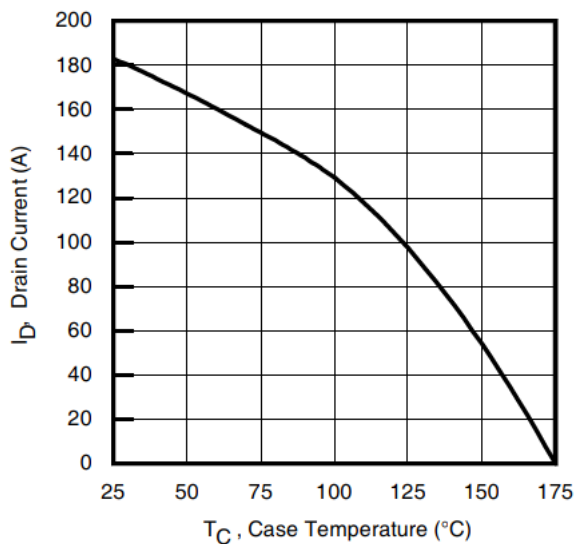


Fig 9. Maximum Drain Current vs. Case Temperature

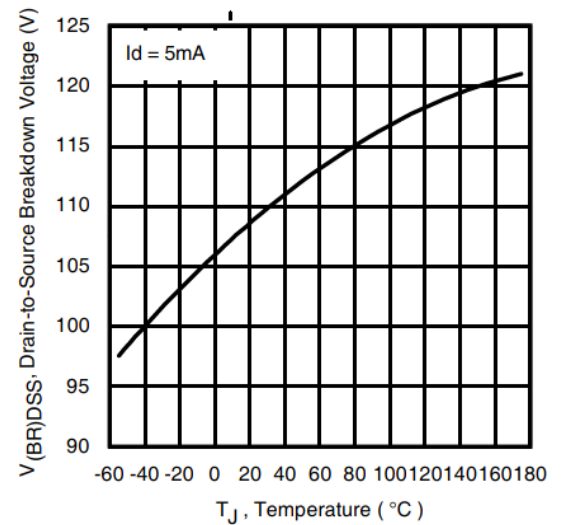


Fig 10. Drain-to-Source Breakdown Voltage

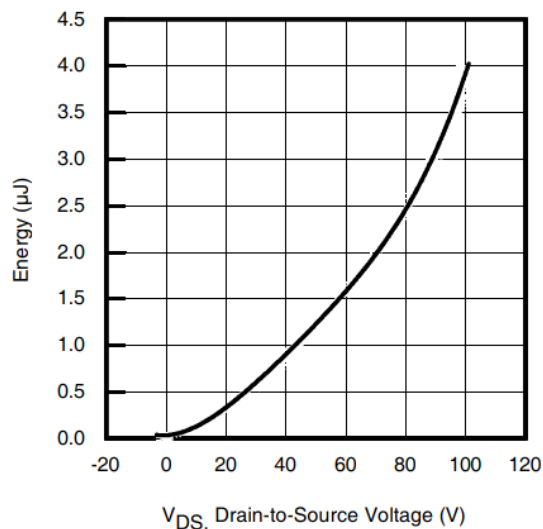


Fig 11. Typical Coss Stored Energy

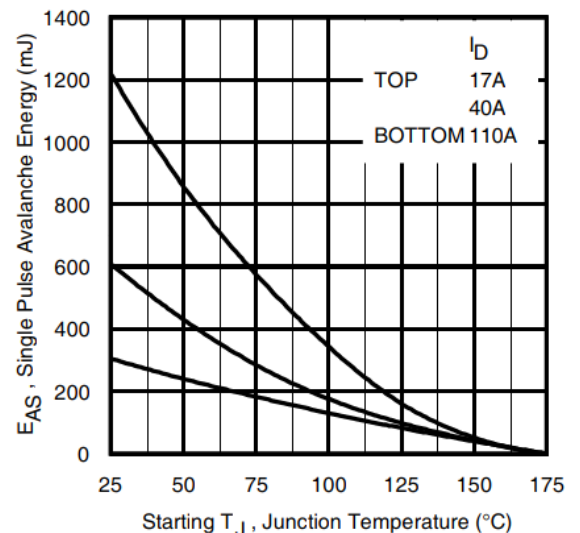


Fig 12. Maximum Avalanche Energy vs. Drain Current

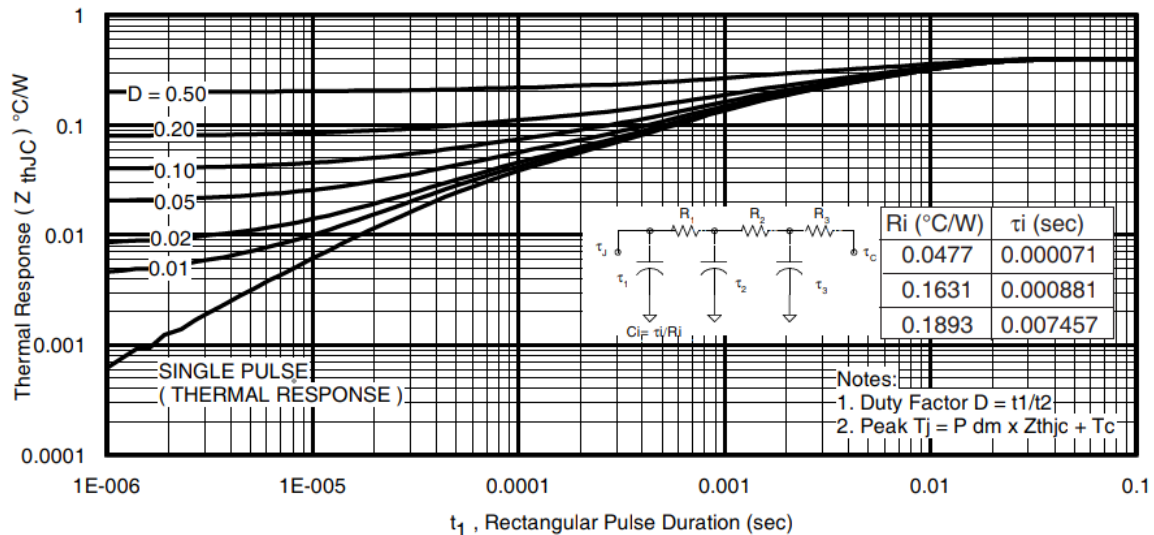


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

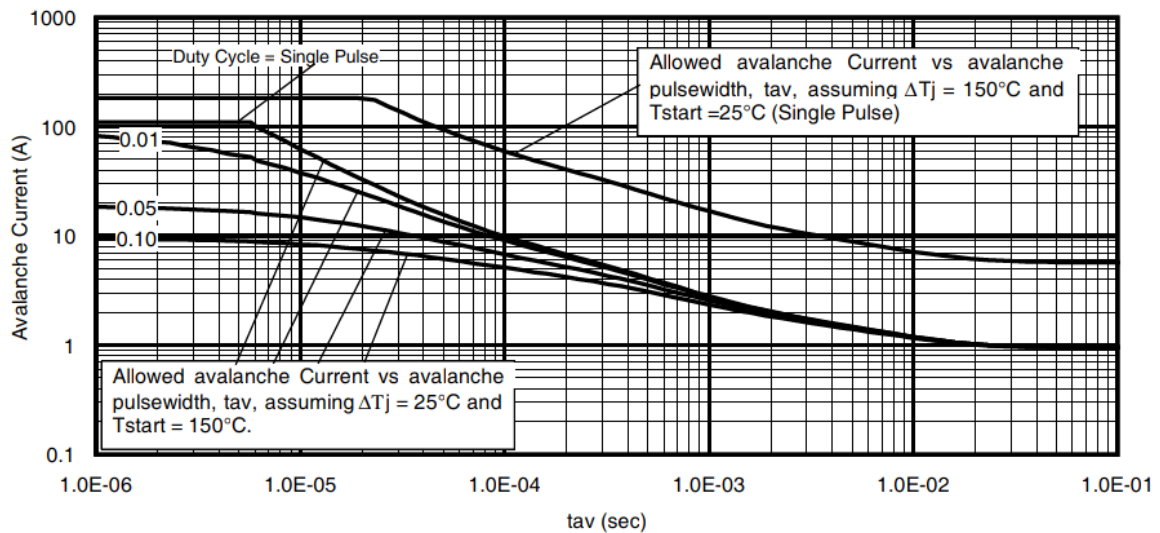


Fig 14. Avalanche Current vs. Pulse width

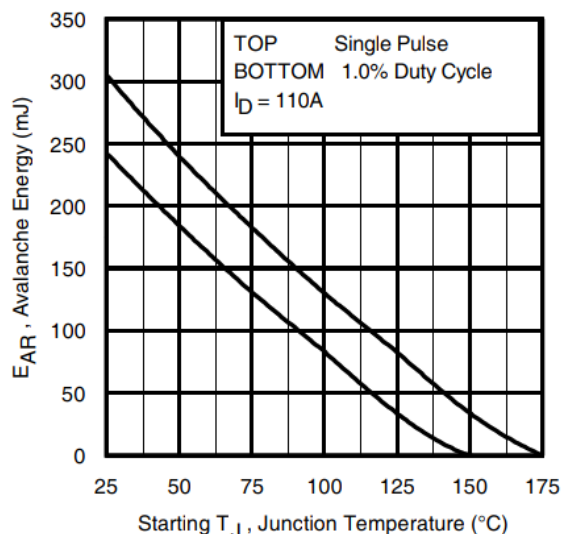


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 18a, 18b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 13, 14).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = \frac{1}{2} (1.3 \cdot BV \cdot I_{av}) = \frac{\Delta T}{Z_{thJC}}$$

$$I_{av} = \frac{2\Delta T}{[1.3 \cdot BV \cdot Z_{thJC}]}$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

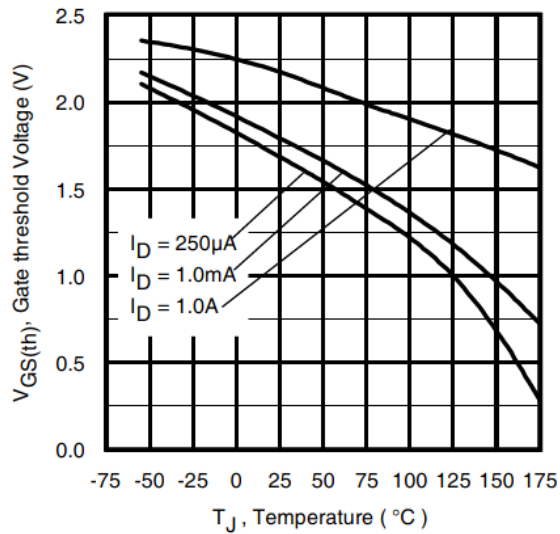
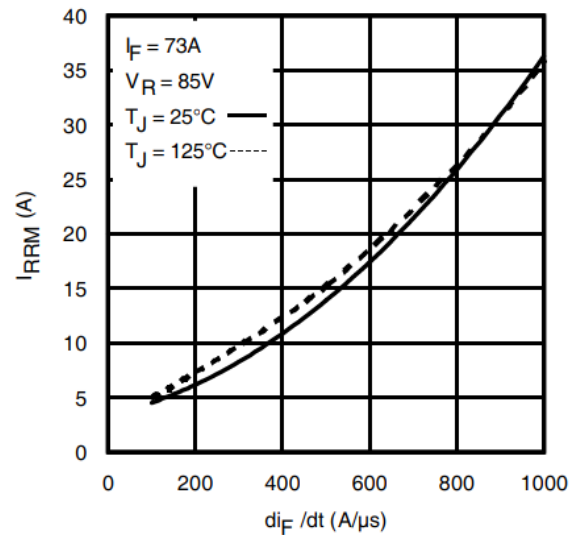
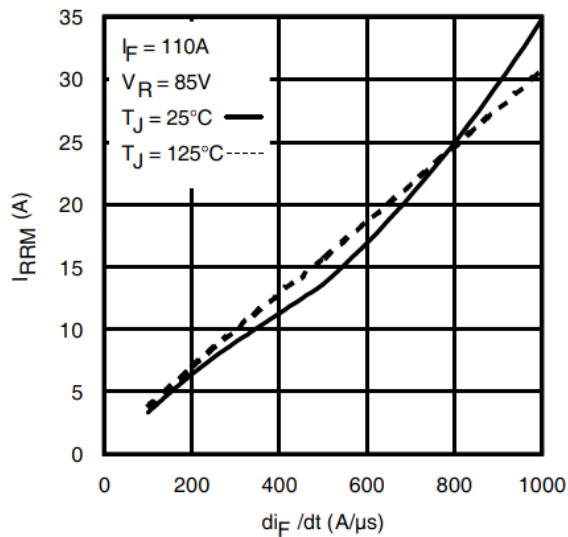
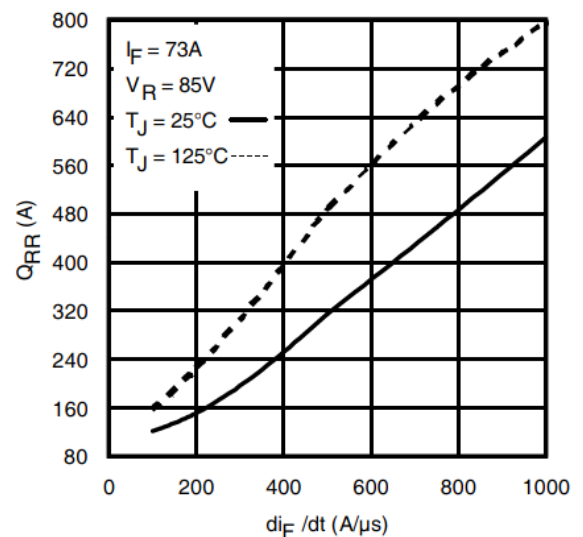
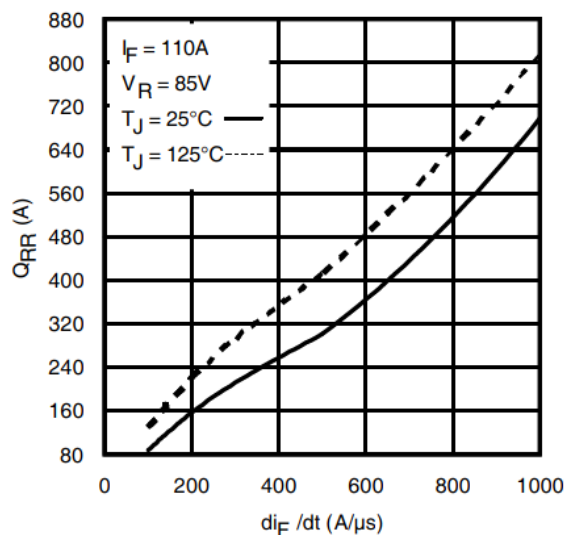


Fig. 16. Threshold Voltage vs. Temperature

Fig. 17 - Typical Recovery Current vs. di/dt Fig. 18 - Typical Recovery Current vs. di/dt Fig. 19 - Typical Stored Charge vs. di/dt Fig. 20 - Typical Stored Charge vs. di/dt

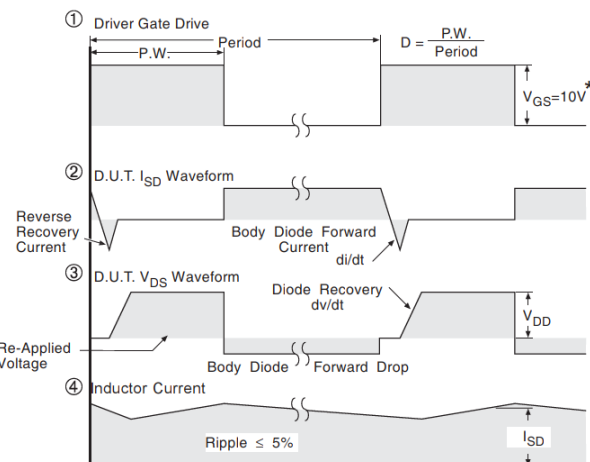


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

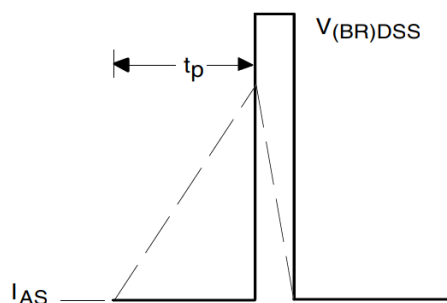


Fig 22b. Unclamped Inductive Waveforms

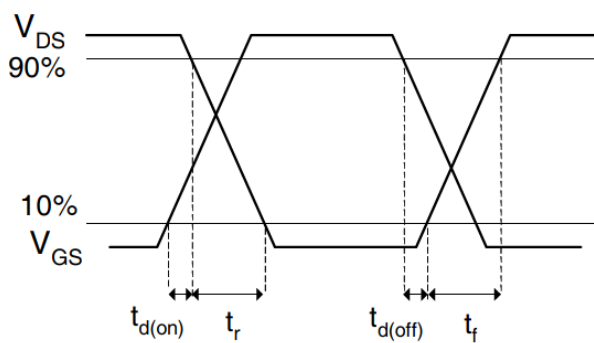


Fig 23b. Switching Time Waveforms

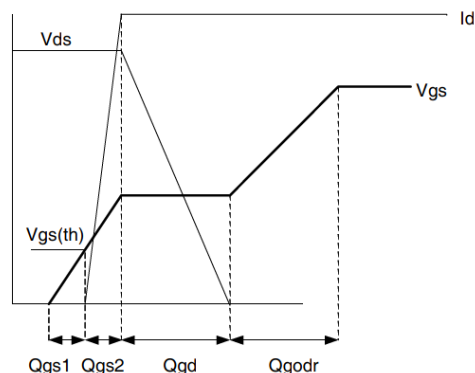
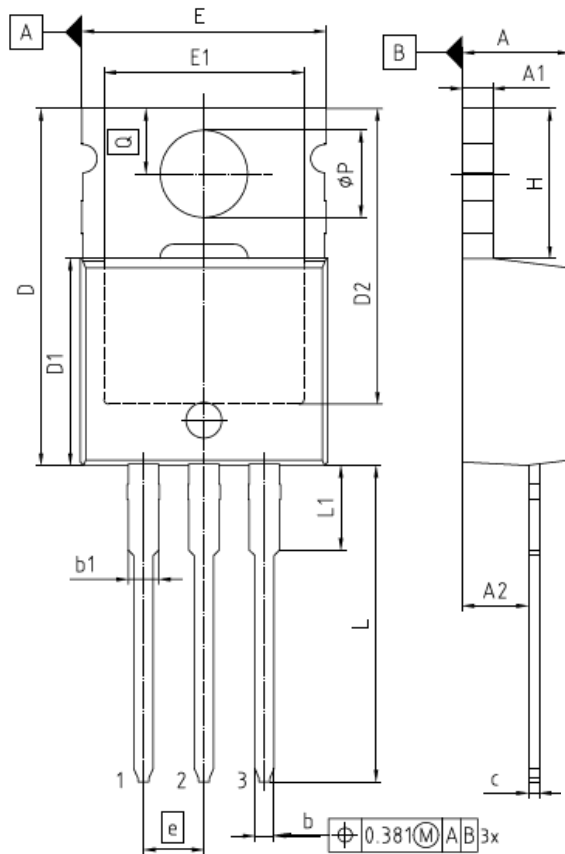
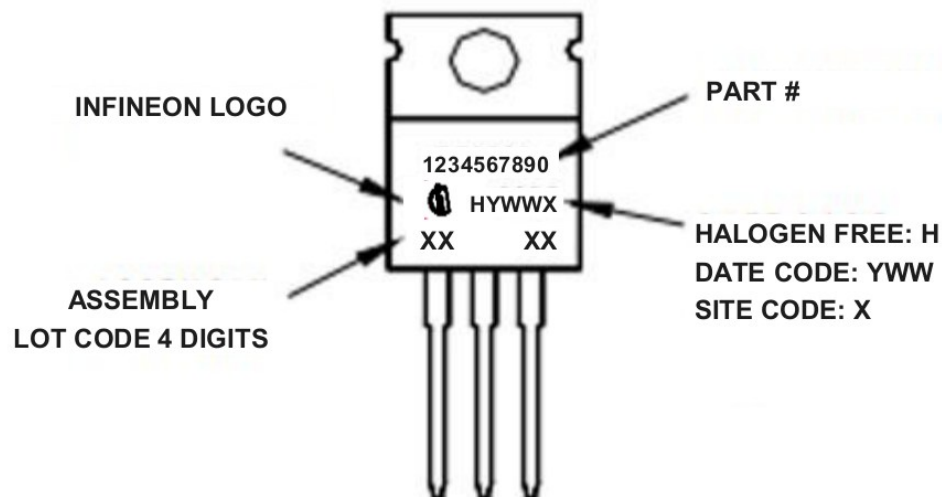


Fig 24b. Gate Charge Waveform

TO-220 Package Outline (Dimensions are shown in millimeters (inches))


NOTES:
 DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
 GATE BURRS ARE LESS THAN 0.5 mm

PACKAGE - GROUP NUMBER: PG-TO220-3-U05		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	3.56	4.83
A1	1.14	1.40
A2	2.03	2.92
b	0.38	1.01
b1	1.14	1.78
c	0.36	0.61
D	14.22	16.51
D1	8.38	9.20
D2	11.68	12.88
E	9.65	10.67
E1	6.86	8.89
e	2.54	
N	3	
H	5.84	6.86
L	12.70	14.73
L1	3.56	4.06
øP	3.54	4.08
Q	2.54	3.42

TO-220 Part Marking Information


TO-220 packages are not recommended for Surface Mount Application.

Revision History

Date	Rev.	Comments
2026-08-12	2.1	- Update datasheet to Infineon format - Updated Package Outline and Part marking –page 8 - Added disclaimer on last page.

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