

# IRHNM9A7024

PD-97899A

Radiation Hardened Power MOSFET Surface Mount (SMD-0.2) 60V, N-channel, R9 Technology

#### **Features**

- Single event effect (SEE) hardened
- Low R<sub>DS(on)</sub>
- Fast switching
- Low total gate charge
- · Simple drive requirements
- Hermetically sealed
- Ceramic package
- Surface mount
- Light weight
- ESD rating: class 1C per MIL-STD-750, Method 1020

### **Product Summary**

BV<sub>DSS</sub>: 60V

• I<sub>D</sub>: 25A\*

•  $R_{DS(on),max}$ : 30m $\Omega$ 

Q<sub>G, max</sub>: 31nC



### **Potential Applications**

- Isolated DC-DC Converter
- Motor Drives
- Solid state relays

#### **Product Validation**

Adhered to MIL-PRF-19500 qualification requirements for space applications

### Description

IR HiRel R9 technology provides superior power MOSFETs for space applications. These devices have improved immunity to Single Event Effect (SEE) and have been characterized for useful performance with Linear Energy Transfer (LET) up to 90 MeV·cm²/mg. Their combination of low R<sub>DS(on)</sub> and faster switching times reduces the power losses and increases power density in today's high speed switching applications such as DC-DC converters and motor controllers. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

### **Ordering Information**

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHNM9A7024	SMD-0.2	COTS	100krad(Si)
IRHNM9A3024	SMD-0.2	COTS	300krad(Si)
IRHNM9A7024SCS	SMD-0.2	S-Level	100krad(Si)
IRHNM9A3024SCS	SMD-0.2	S-Level	300krad(Si)

## **IRHNM9A7024**





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**Absolute Maximum Ratings** 

#### **Absolute Maximum Ratings** 1

**Absolute Maximum Ratings (Pre-Irradiation)** Table 2

Symbol	Parameter	Value	Unit
$I_{D1}$ @ $V_{GS}$ = 12V, $T_{C}$ = 25°C	Continuous Drain Current	25*	А
$I_{D2}$ @ $V_{GS}$ = 12V, $T_{C}$ = 100°C	Continuous Drain Current	20	Α
$I_{DM}$ @ $T_C = 25^{\circ}C$	Pulsed Drain Current <sup>1</sup>	100	Α
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	54	W
	Linear Derating Factor	0.43	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>2</sup>	520	mJ
I <sub>AR</sub>	Avalanche Current <sup>1</sup>	25	А
E <sub>AR</sub>	Repetitive Avalanche Energy <sup>1</sup>	5.4	mJ
dv/dt	Peak Diode Reverse Recovery <sup>3</sup>	8.6	V/ns
T <sub>J</sub> Operating Junction and Storage Temperature Range		-55 to +150	°C
Package Mounting Surface Tempe		300 (for 5 s)	
	Weight	0.25 (Typical)	g

<sup>\*</sup>Current is limited by package

<sup>&</sup>lt;sup>1</sup> Repetitive Rating; Pulse width limited by maximum junction temperature.

 $<sup>^2</sup>$  V<sub>DD</sub> = 60V, starting T<sub>J</sub> = 25°C, L = 2.6mH, Peak I<sub>L</sub> = 20A, V<sub>GS</sub> = 20V

 $<sup>^3</sup>$  I<sub>SD</sub>  $\leq$  25A, di/dt  $\leq$  1300A/ $\mu$ s, V<sub>DD</sub>  $\leq$  60V, T $_J$   $\leq$  150°C



#### **Device Characteristics**

### 2 Device Characteristics

### 2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage		_	_	V	$V_{GS} = 0V, I_D = 1.0 mA$
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient	_	0.06	_	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	_	_	30	mΩ	$V_{GS} = 12V$ , $I_{D2} = 20A^{1}$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	-	4.0	V	V = V L = CFO::A
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	_	-7.2	_	mV/°C	$V_{DS} = V_{GS}, I_{D} = 650 \mu A$
Gfs	Forward Transconductance	10	_	_	S	$V_{DS} = 15V$ , $I_{D2} = 20A^{1}$
	Zero Cata Valta da Busin Comunit	_	_	1.0		$V_{DS} = 48V, V_{GS} = 0V$
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	_	_	10	μΑ	$V_{DS} = 48V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
	Gate-to-Source Leakage Forward	_	_	100	0	V <sub>GS</sub> = 20V
$I_{GSS}$	Gate-to-Source Leakage Reverse	_	_	-100	nA	V <sub>GS</sub> = -20V
Q <sub>G</sub>	Total Gate Charge	_	_	31		I <sub>D1</sub> = 25A
Q <sub>GS</sub>	Gate-to-Source Charge	_	_	10	nC	V <sub>DS</sub> = 30V
$\overline{Q_{GD}}$	Gate-to-Drain ('Miller') Charge	_	_	6.4		$V_{GS} = 12V$
t <sub>d(on)</sub>	Turn-On Delay Time	_	_	11		I <sub>D1</sub> = 25A **
t <sub>r</sub>	Rise Time	_	_	20		$V_{DD} = 30V$
t <sub>d(off)</sub>	Turn-Off Delay Time	_	_	29	ns	$R_G = 7.5\Omega$
t <sub>f</sub>	Fall Time	_	_	12		$V_{GS} = 12V$
L <sub>s</sub> +L <sub>D</sub>	Total Inductance	_	6.8	_	nH	Measured from center of Drain pad to center of Source pad
C <sub>iss</sub>	Input Capacitance	_	1160	_		$V_{GS} = 0V$
C <sub>oss</sub>	Output Capacitance	_	440	_	рF	$V_{DS} = 25V$
C <sub>rss</sub>	Reverse Transfer Capacitance	_	2.6	_		f = 1.0MHz
$R_{G}$	Gate Resistance	_	1.5	_	Ω	f = 1.0MHz, open drain

<sup>\*\*</sup> Switching speed maximum limits are based on manufacturing test equipment and capability.

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 $<sup>^1</sup>$  Pulse width  $\leq$  300  $\mu s;$  Duty Cycle  $\leq$  2%



**Device Characteristics** 

## 2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Unit	<b>Test Conditions</b>	
Is	Continuous Source Current (Body Diode)	_	_	25	Α		
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>1</sup>	_	_	100	Α		
$V_{SD}$	Diode Forward Voltage	_	1	1.2	٧	$T_J = 25$ °C, $I_S = 25$ A, $V_{GS} = 0$ V <sup>2</sup>	
t <sub>rr</sub>	Reverse Recovery Time	_	75	150	ns	$T_J = 25$ °C, $I_F = 25$ A, $V_{DD} \le 25$ V	
Q <sub>rr</sub>	Reverse Recovery Charge	_	250	_	nC	di/dt = 100A/μs <sup>2</sup>	
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )					

### 2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Тур.	Max.	Unit
$R_{ heta JC}$	Junction-to-Case	_	_	2.3	°C/W

### 2.4 Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

#### 2.4.1 Electrical Characteristics - Post Total Dose Irradiation

Table 6 Electrical Characteristics @ T<sub>i</sub> = 25°C, Post Total Dose Irradiation <sup>3, 4</sup>

Cumbal	Paramatar.	Upto 300	Okrads (Si) <sup>5</sup>	11	T	
Symbol	Parameter	Min.	Max.	Unit	Test Conditions	
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	60	_	V	$V_{GS} = 0V, I_D = 1.0 mA$	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	V	$V_{DS} = V_{GS}, I_{D} = 650 \mu A$	
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	_	100	- Λ	V <sub>GS</sub> = 20V	
	Gate-to-Source Leakage Reverse	_	-100	nA	V <sub>GS</sub> = -20V	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	_	1.0	μΑ	$V_{DS} = 48V, V_{GS} = 0V$	
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) <sup>2</sup>	_	30	mΩ	$V_{GS} = 12V, I_{D2} = 20A$	
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance (SMD-0.2) <sup>2</sup>	_	30	mΩ	$V_{GS} = 12V, I_{D2} = 20A$	
$V_{SD}$	Diode Forward Voltage	_	1.2	V	$V_{GS} = 0V, I_F = 25A$	

<sup>&</sup>lt;sup>1</sup> Repetitive Rating; Pulse width limited by maximum junction temperature.

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 $<sup>^2</sup>$  Pulse width  $\leq$  300  $\mu s;$  Duty Cycle  $\leq$  2%

<sup>&</sup>lt;sup>3</sup> Total Dose Irradiation with V<sub>GS</sub> Bias. V<sub>GS</sub> = 12V applied and V<sub>DS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

<sup>&</sup>lt;sup>4</sup> Total Dose Irradiation with V<sub>DS</sub> Bias. V<sub>DS</sub> = 48V applied and V<sub>GS</sub> = 0 during irradiation per MlL-STD-750, Method 1019, condition A.

<sup>&</sup>lt;sup>5</sup> Part numbers IRHNM9A7024, IRHNM9A3024, IRHNM9A7024SCS and IRHNM9A3024SCS



**Device Characteristics** 

### 2.4.2 Single Event Effects – Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET	Energy	Range		V	<sub>DS</sub> (V)	
(MeV·cm²/mg)	(MeV)	(μm)	$V_{GS} = 0V$	V <sub>GS</sub> = -1V	V <sub>GS</sub> = -5V	V <sub>GS</sub> = -10V
38 ± 5%	355 ± 7.5%	43 ± 7.5%	60	60	60	60
60 ± 5%	753 ± 7.5%	60 ± 10%	60	60	60	60
90 ± 5%	1515 ± 7.5%	82 ± 7.5%	60	60	_	_

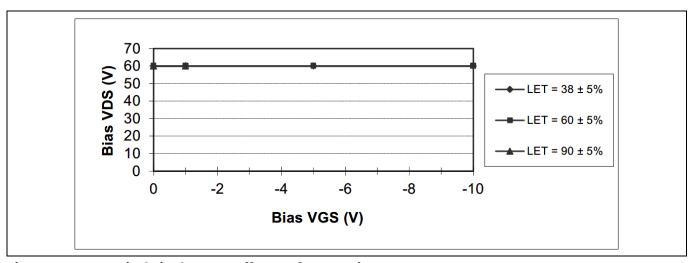


Figure 1 Typical Single Event Effect, Safe Operating Area



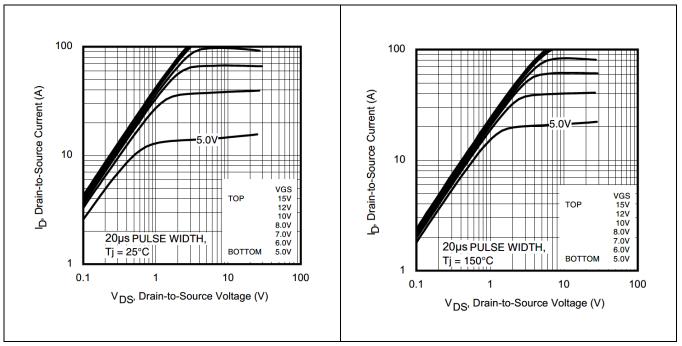


Figure 2 Typical Output Characteristics Figure 3 Typical Output Characteristics

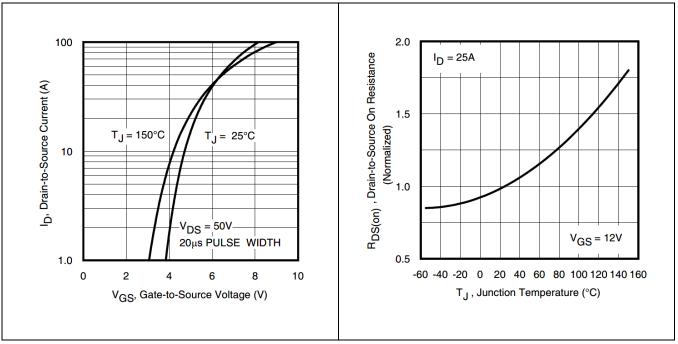


Figure 4 Typical Transfer Characteristics Figure 5 Normalized On-Resistance Vs.

Temperature



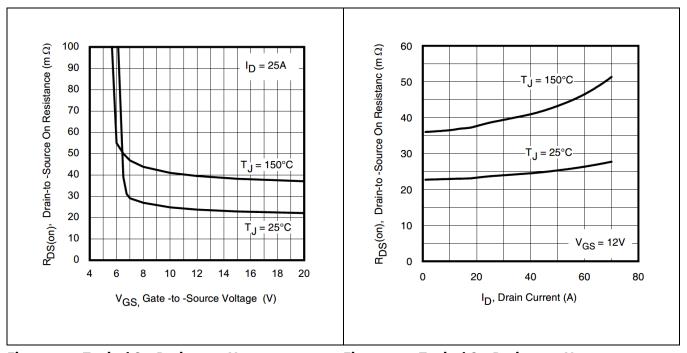


Figure 6 Typical On-Resistance Vs.
Gate Voltage

Figure 7 Typical On-Resistance Vs.

Drain Current

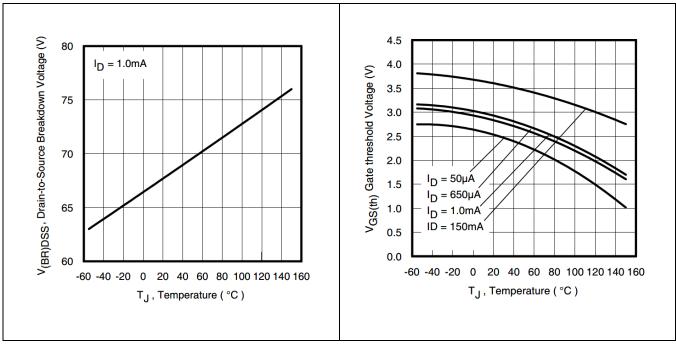


Figure 8 Typical Drain-to-Source Breakdown Voltage Vs. Temperature

Figure 9 Typical Threshold Voltage Vs.
Temperature



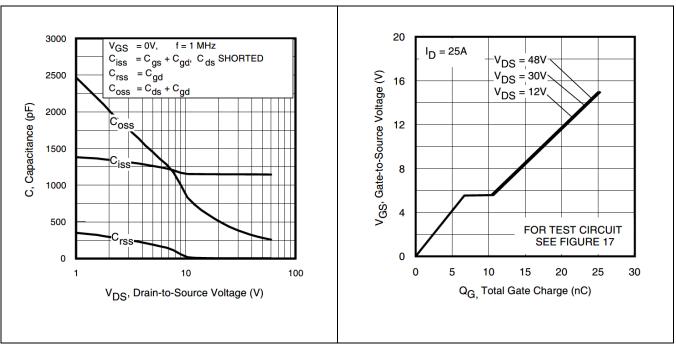


Figure 10 Typical Capacitance Vs.

Drain-to-Source Voltage

Figure 11 Typical Gate Charge Vs.

Gate-to-Source Voltage

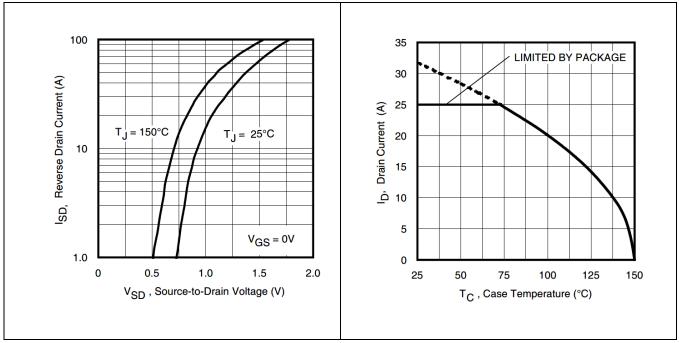


Figure 12 Typical Source-Drain Vs.
Diode Forward Voltage

Figure 13 Maximum Drain Current Vs. Case Temperature



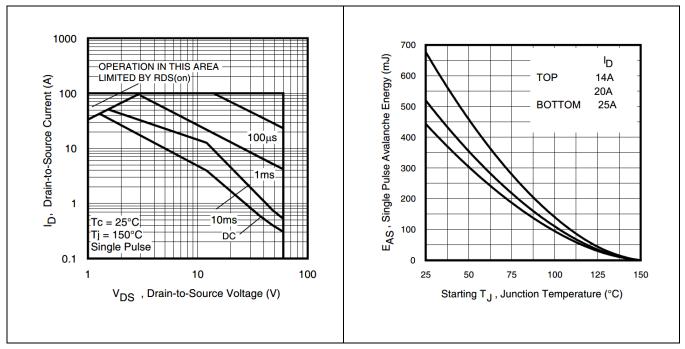


Figure 14 Maximum Safe Operating Area

Figure 15 Maximum Avalanche Energy Vs.

Drain Current

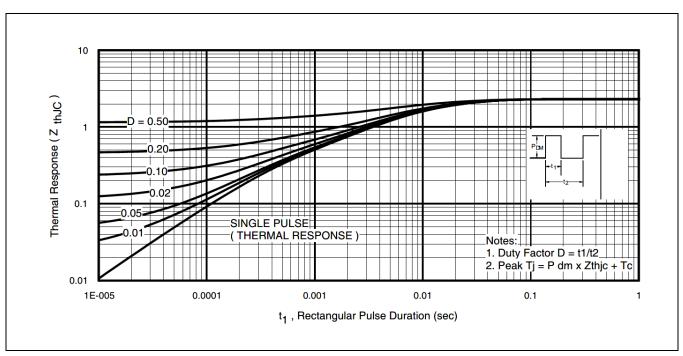


Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case



**Test Circuits (Pre-irradiation)** 

# 4 Test Circuits (Pre-irradiation)

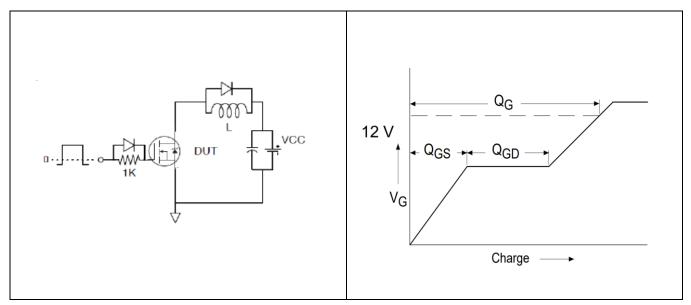


Figure 17 Gate Charge Test Circuit

Figure 18 Gate Charge Waveform

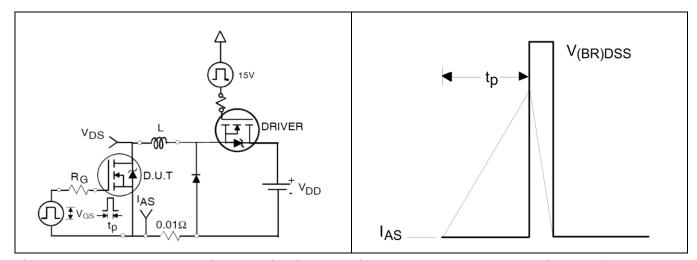


Figure 19 Unclamped Inductive Test Circuit

Figure 20 Unclamped Inductive Waveform

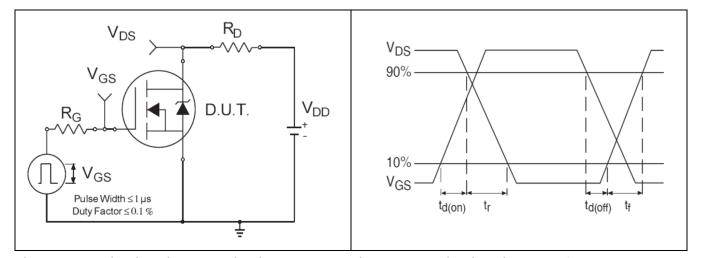


Figure 21 Switching Time Test Circuit

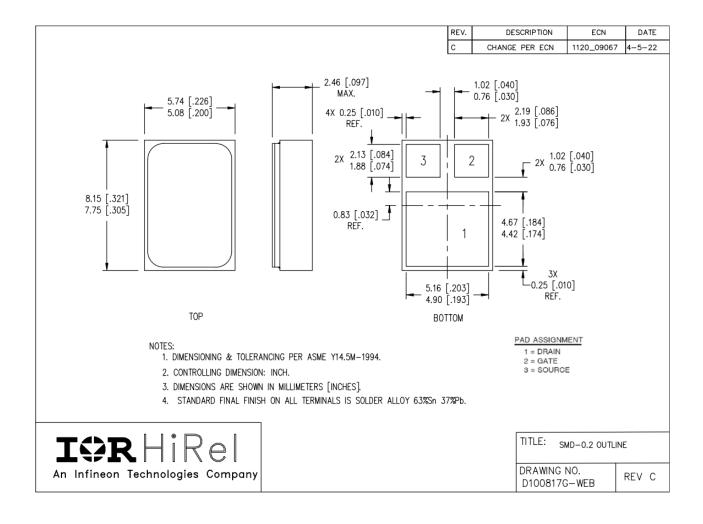
Figure 22 Switching Time Waveforms



**Package Outline** 

# 5 Package Outline

Note: For the most updated package outline, please see the website: **SMD-0.2** (Metal Lid)



## **IRHNM9A7024**

## Radiation Hardened Power MOSFET Surface-Mount (SMD-0.2)



**Revision history** 

# **Revision history**

Document version	Date of release	Description of changes
	10/23/2019	Preliminary datasheet with PPD number (PPD-97899)
Rev A	05/14/2025	Final datasheet with PD number

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