

IRHNJC67230 (JANSR2N7591U3C)

PD-98005

Radiation Hardened Power MOSFET Surface Mount (SMD-0.5 with Ceramic Lid) 200V, 16A, N-channel, R6 Technology

Features

- Single event effect (SEE) hardened
- Low $R_{DS(on)}$
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Ceramic package
- Light weight
- Surface mount
- ESD rating: Class 3A per MIL-STD-750, Method 1020

Product Summary

- BV_{DSS} : 200V
- I_D : 16A
- $R_{DS(on), max}$: 130m Ω
- $Q_{G, max}$: 50nC
- **REF:** MIL-PRF-19500/746



Potential Applications

- DC-DC converter
- Motor drives
- Electric propulsion

Product Validation

Qualified to JANS screening flow according to MIL-PRF-19500 for space applications

Description

IR HiRel R6 technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHNJC67230	SMD-0.5 with Ceramic Lid	COTS	100 krad (Si)
IRHNJC67230SCV	SMD-0.5 with Ceramic Lid	JANTXV equivalent	100 krad (Si)
IRHNJC67230SCS	SMD-0.5 with Ceramic Lid	S-Level	100 krad (Si)
JANSR2N7591U3C	SMD-0.5 with Ceramic Lid	JANS	100 krad (Si)
IRHNJC63230	SMD-0.5 with Ceramic Lid	COTS	300 krad (Si)
JANSF2N7591U3C	SMD-0.5 with Ceramic Lid	JANS	300 krad (Si)

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Absolute Maximum Ratings

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = 12V, T_C = 25^\circ C$	Continuous Drain Current	16	A
$I_{D2} @ V_{GS} = 12V, T_C = 100^\circ C$	Continuous Drain Current	10	A
$I_{DM} @ T_C = 25^\circ C$	Pulsed Drain Current ¹	64	A
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ²	60	mJ
I_{AR}	Avalanche Current ¹	16	A
E_{AR}	Repetitive Avalanche Energy ¹	7.5	mJ
dv/dt	Peak Diode Reverse Recovery ³	8.6	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (for 5s)	
	Weight	1.0 (Typical)	

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.² $V_{DD} = 25V$, starting $T_J = 25^\circ C$, $L = 0.47mH$, Peak $I_L = 16A$, $V_{GS} = 12V$ ³ $I_{SD} \leq 16A$, $di/dt \leq 570A/\mu s$, $V_{DD} \leq 200V$, $T_J \leq 150^\circ C$

Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.22	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.13	Ω	$V_{GS} = 12V, I_{D2} = 10A^1$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 1mA$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-10.25	—	mV/ $^\circ\text{C}$	
Gfs	Forward Transconductance	10	—	—	S	$V_{DS} = 15V, I_{D2} = 10A^1$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	μA	$V_{DS} = 160V, V_{GS} = 0V$
		—	—	25		$V_{DS} = 160V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20V$
Q_G	Total Gate Charge	—	—	50	nC	$I_{D1} = 16A$ $V_{DS} = 100V$ $V_{GS} = 12V$
Q_{GS}	Gate-to-Source Charge	—	—	15		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	20		
$t_{d(on)}$	Turn-On Delay Time	—	—	25	ns	$I_{D1} = 16A^{**}$ $V_{DD} = 100V$ $R_G = 7.5\Omega$ $V_{GS} = 12V$
t_r	Rise Time	—	—	30		
$t_{d(off)}$	Turn-Off Delay Time	—	—	60		
t_f	Fall Time	—	—	30		
$L_s + L_D$	Total Inductance	—	4.0	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	1450	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	210	—		
C_{rss}	Reverse Transfer Capacitance	—	3.8	—		
R_G	Gate Resistance	—	0.9	—	Ω	$f = 1.0MHz, \text{open drain}$

** Switching speed maximum limits are based on manufacturing test equipment and capability.

¹ Pulse width $\leq 300 \mu\text{s}$; Duty Cycle $\leq 2\%$

Radiation Hardened Power MOSFET Surface Mount (SMD-0.5 with Ceramic Lid)

Device Characteristics

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	16	A	
I_{SM}	Pulsed Source Current (Body Diode) ¹	—	—	64	A	
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$, $I_S = 16\text{A}$, $V_{GS} = 0\text{V}$ ²
t_{rr}	Reverse Recovery Time	—	—	350	ns	$T_J = 25^\circ\text{C}$, $I_F = 16\text{A}$, $V_{DD} \leq 25\text{V}$ $di/dt = 100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovery Charge	—	2.3	—	μC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	1.67	$^\circ\text{C}/\text{W}$

2.4 Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ $T_J = 25^\circ\text{C}$, Post Total Dose Irradiation^{3, 4}

Symbol	Parameter	Up to 300krad (Si) ⁵		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	—	V	$V_{GS} = 0\text{V}$, $I_D = 1.0\text{mA}$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	V	$V_{DS} = V_{GS}$, $I_D = 1.0\text{mA}$
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Leakage Reverse	—	-100		$V_{GS} = -20\text{V}$
I_{DSS}	Zero Gate Voltage Drain Current	—	10	μA	$V_{DS} = 160\text{V}$, $V_{GS} = 0\text{V}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) ²	—	0.134	Ω	$V_{GS} = 12\text{V}$, $I_{D2} = 10\text{A}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (SMD-0.5 with Ceramic Lid) ²	—	0.130	Ω	$V_{GS} = 12\text{V}$, $I_{D2} = 10\text{A}$
V_{SD}	Diode Forward Voltage	—	1.2	V	$V_{GS} = 0\text{V}$, $I_F = 16\text{A}$

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² Pulse width $\leq 300 \mu\text{s}$; Duty Cycle $\leq 2\%$

³ Total Dose Irradiation with V_{GS} Bias. $V_{GS} = 12\text{V}$ applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁴ Total Dose Irradiation with V_{DS} Bias. $V_{DS} = 160\text{V}$ applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁵ Part number(s): IRHNJC67230 (JANSR2N7591U3C) and IRHNJC63230 (JANSF2N7591U3C)

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Device Characteristics

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	V _{DS} (V)				
			V _{GS} = 0V	V _{GS} = -4V	V _{GS} = -5V	V _{GS} = -10V	V _{GS} = -15V
42 ± 5%	2450 ± 5%	205 ± 5%	200	200	200	200	190
61 ± 5%	825 ± 5%	66 ± 7.5%	200	200	200	200	190
90 ± 5%	1470 ± 5%	80 ± 5%	150	150	110	—	—

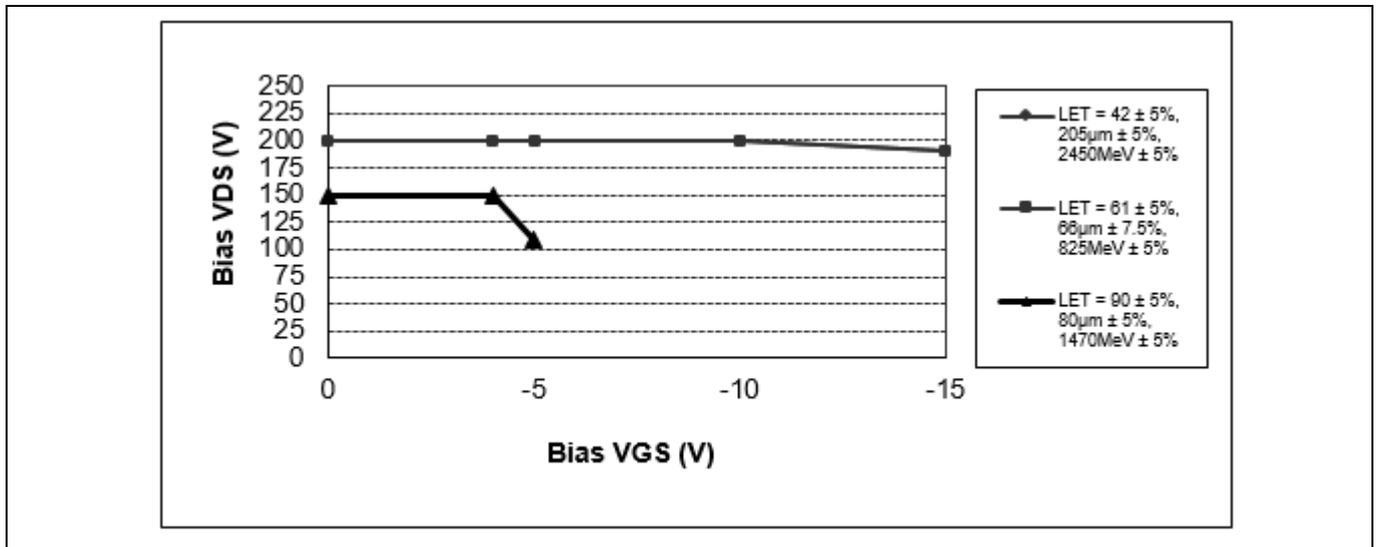


Figure 1 Typical Single Event Effect, Safe Operating Area

3 Electrical Characteristics Curves (Pre-irradiation)

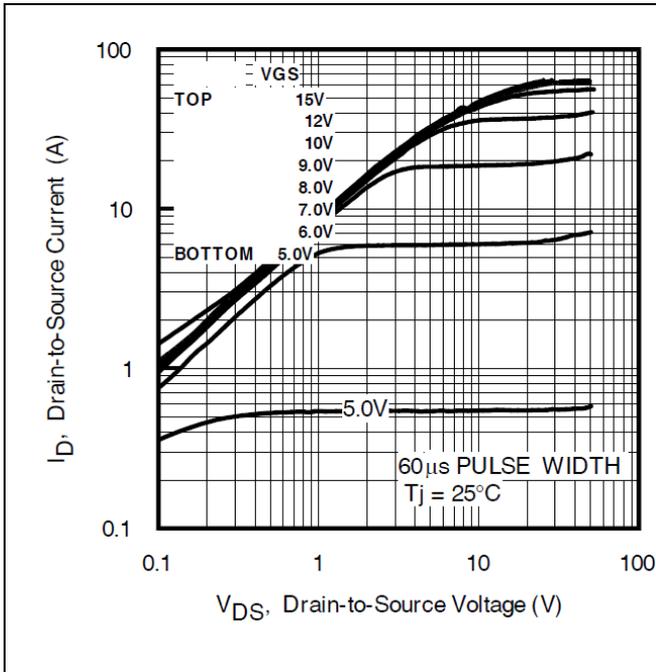


Figure 2 Typical Output Characteristics

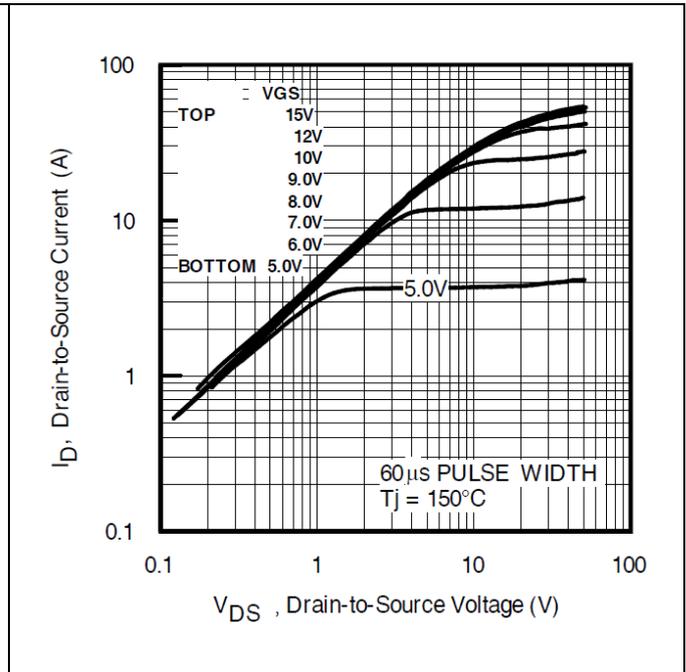


Figure 3 Typical Output Characteristics

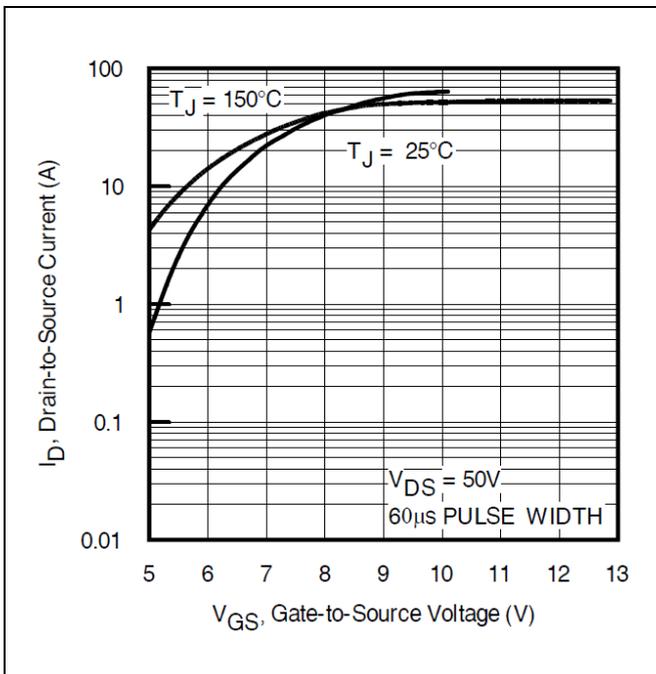


Figure 4 Typical Transfer Characteristics

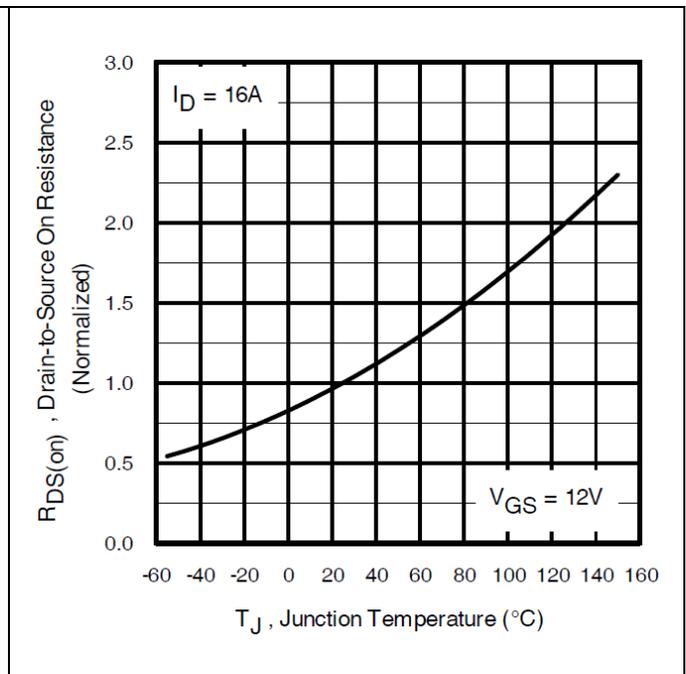


Figure 5 Normalized On-Resistance Vs. Temperature

IRHNJC67230 (JANSR2N7591U3C)

Radiation Hardened Power MOSFET Surface Mount (SMD-0.5 with Ceramic Lid)

Electrical Characteristics Curves (Pre-irradiation)

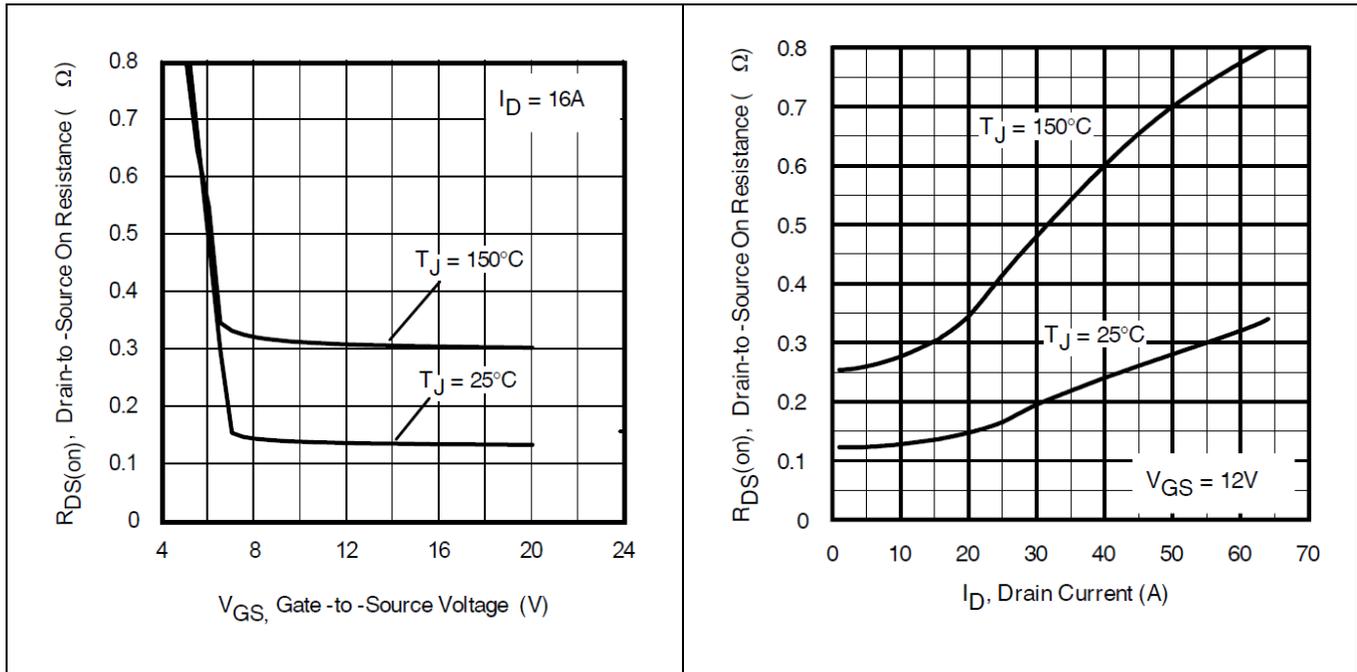


Figure 6 Typical On-Resistance Vs. Gate Voltage **Figure 7 Typical On-Resistance Vs. Drain Current**

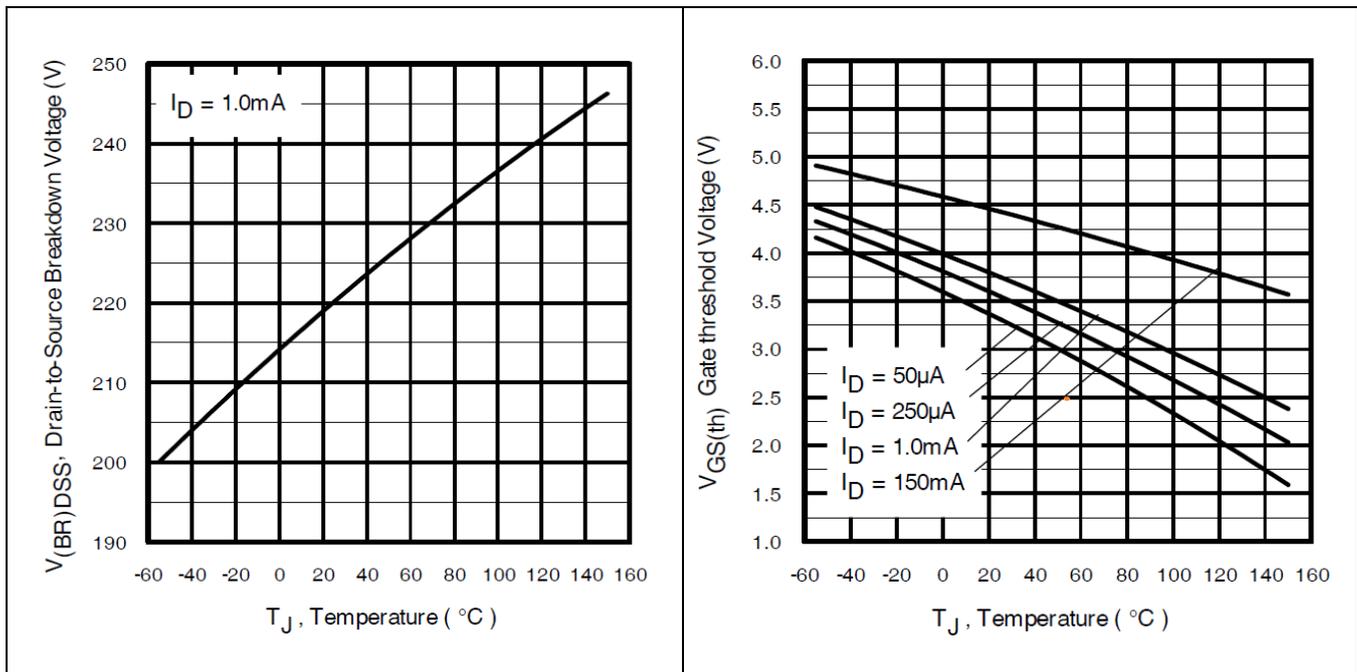


Figure 8 Typical Drain-to-Source Breakdown Voltage Vs. Temperature **Figure 9 Typical Threshold Voltage Vs. Temperature**

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Radiation Hardened Power MOSFET Surface Mount (SMD-0.5 with Ceramic Lid)

Electrical Characteristics Curves (Pre-irradiation)

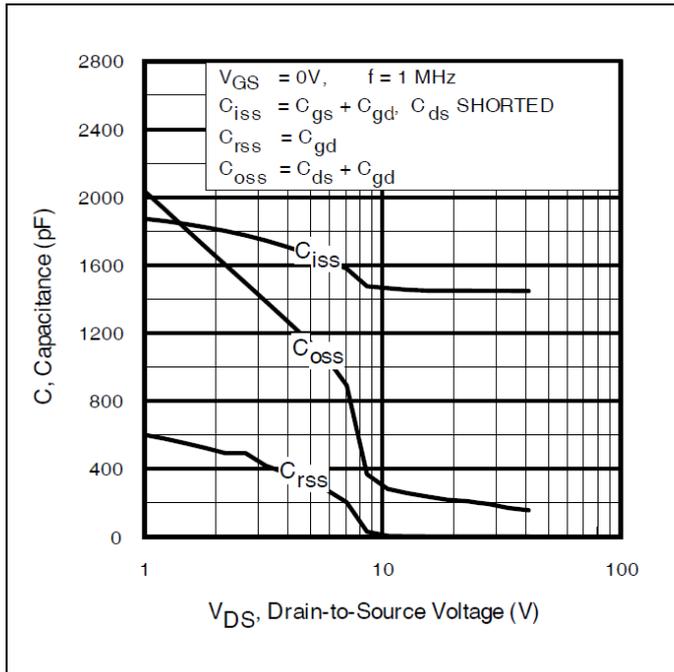


Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage

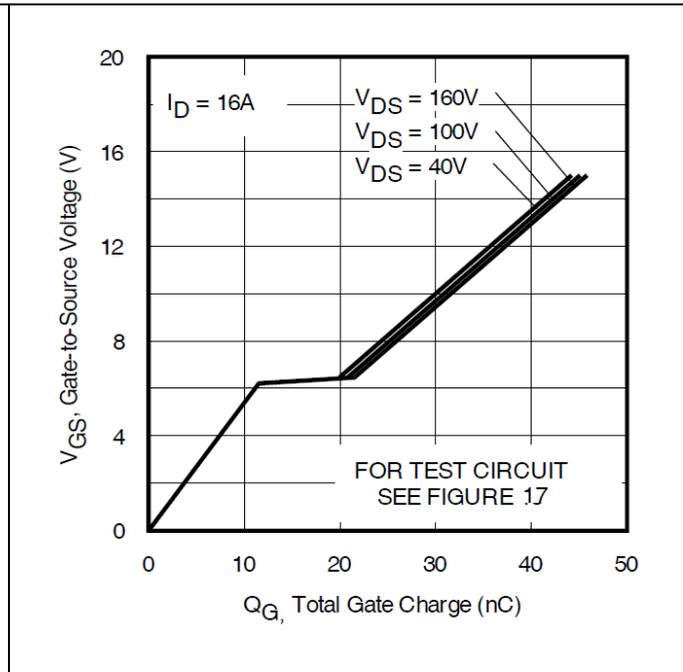


Figure 11 Gate-to-Source Voltage Vs. Typical Gate Charge

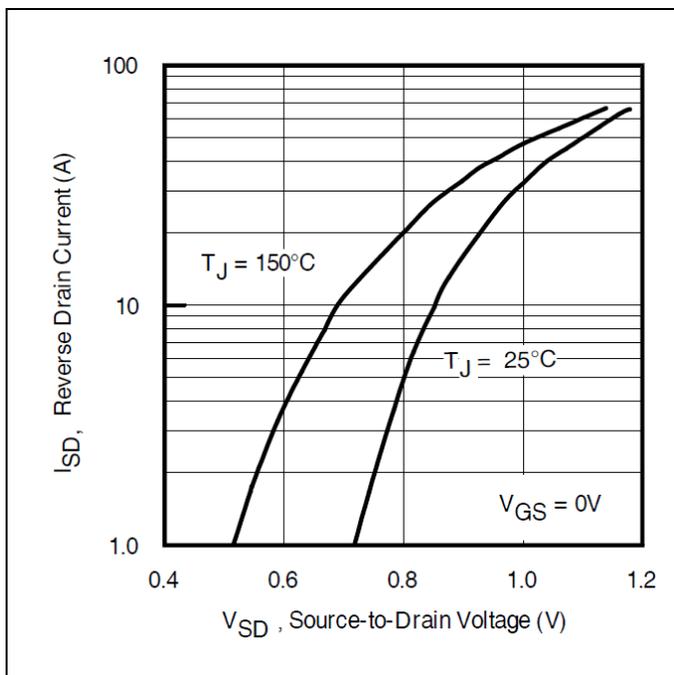


Figure 12 Typical Source-Drain Current Vs. Diode Forward Voltage

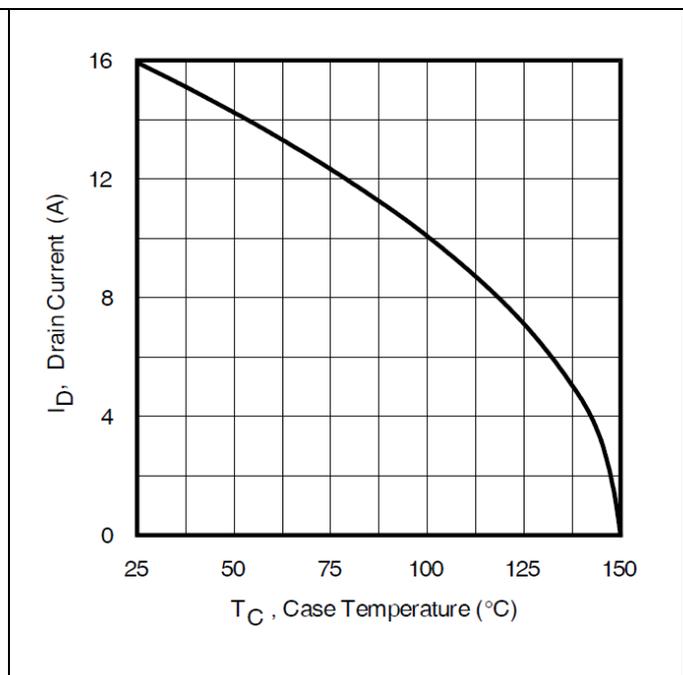


Figure 13 Maximum Drain Current Vs. Case Temperature

IRHNJC67230 (JANSR2N7591U3C)

Radiation Hardened Power MOSFET Surface Mount (SMD-0.5 with Ceramic Lid)

Electrical Characteristics Curves (Pre-irradiation)

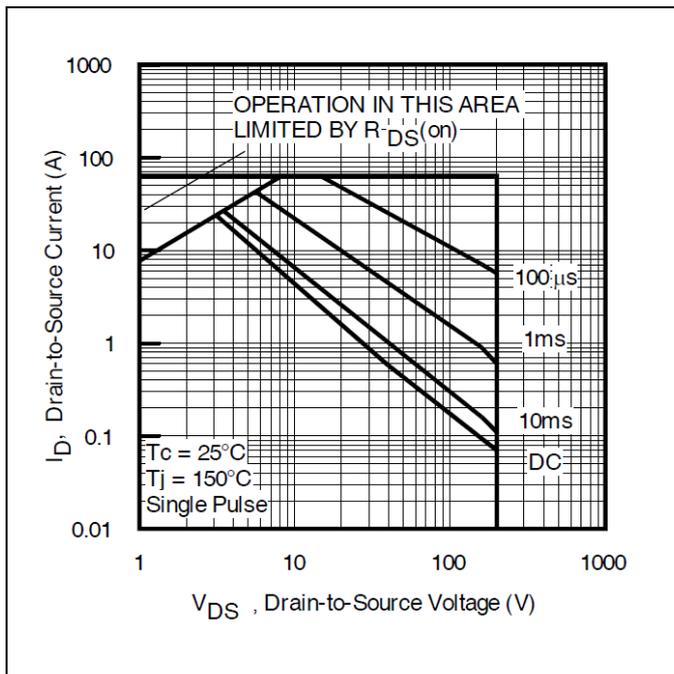


Figure 14 Maximum Safe Operating Area

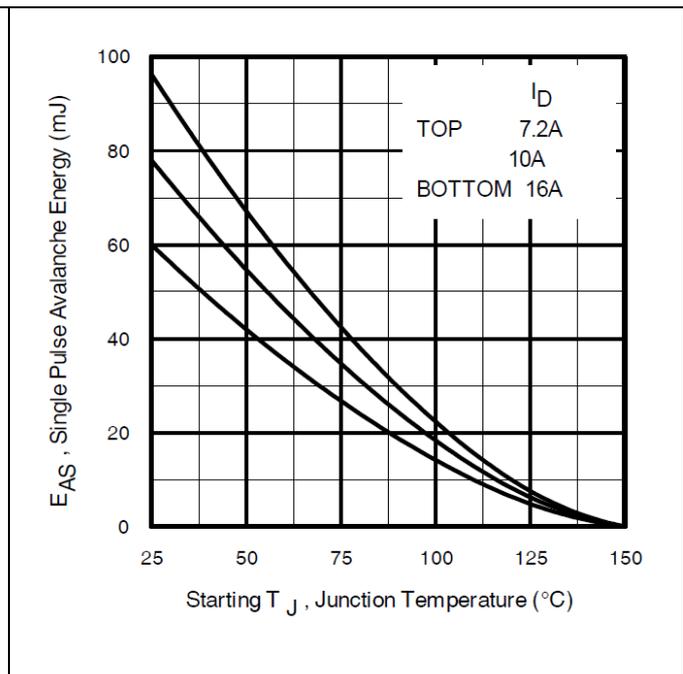


Figure 15 Maximum Avalanche Energy Vs. Junction Temperature

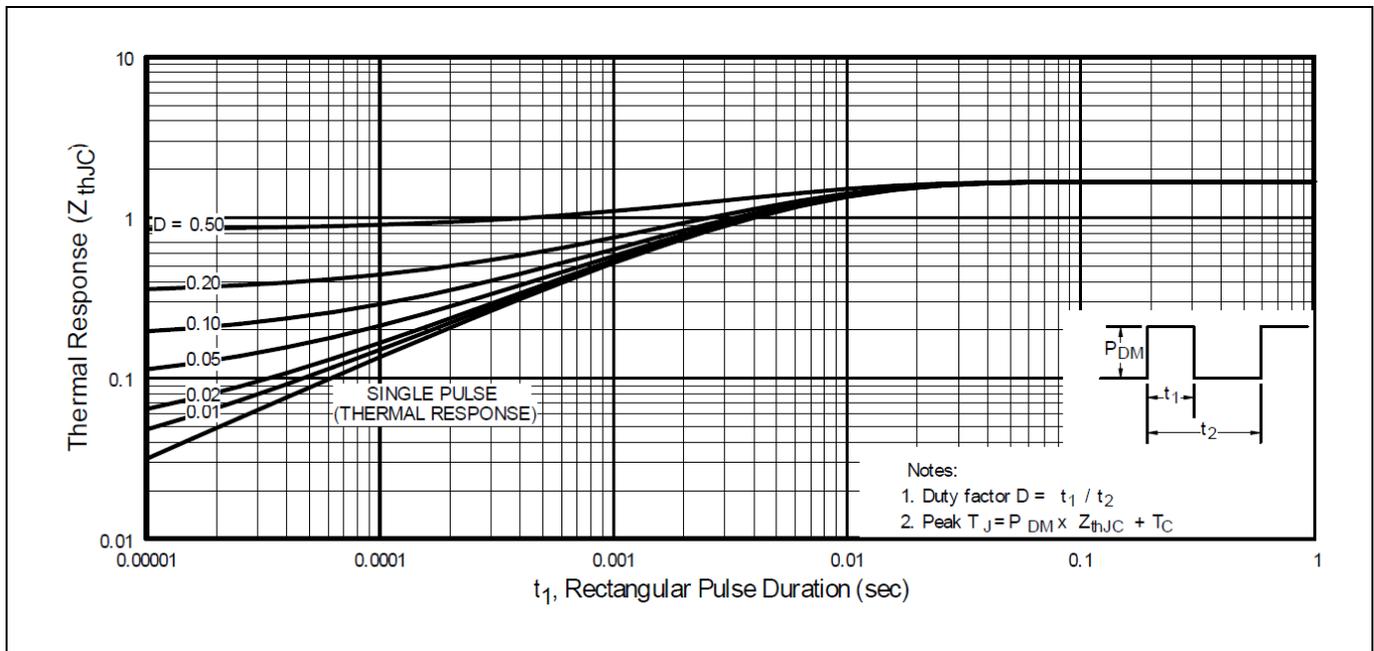


Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case

Test Circuits (Pre-irradiation)

4 Test Circuits (Pre-irradiation)

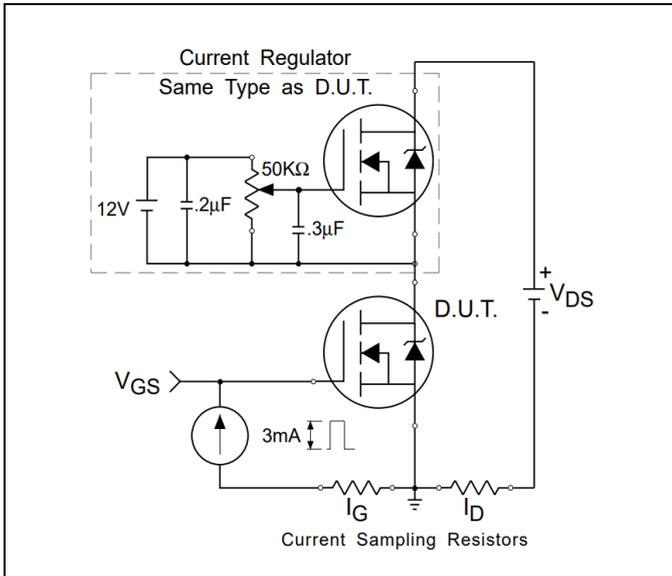


Figure 17 Gate Charge Test Circuit

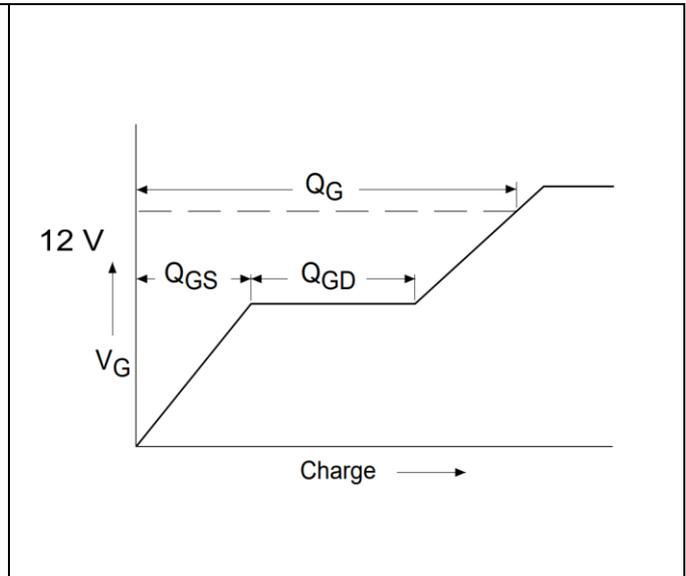


Figure 18 Gate Charge Waveform

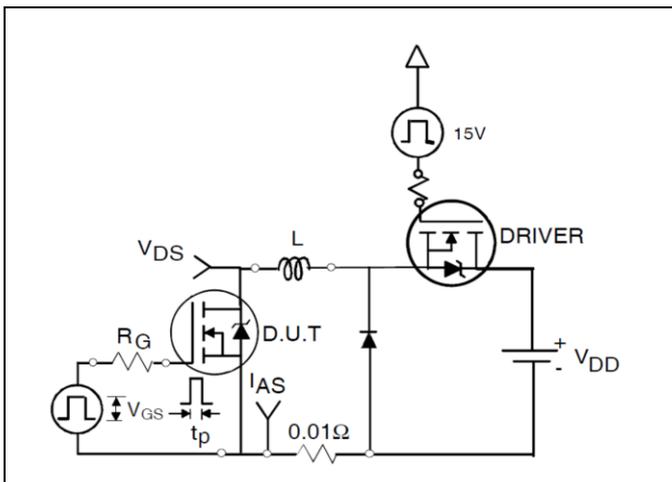


Figure 19 Unclamped Inductive Test Circuit

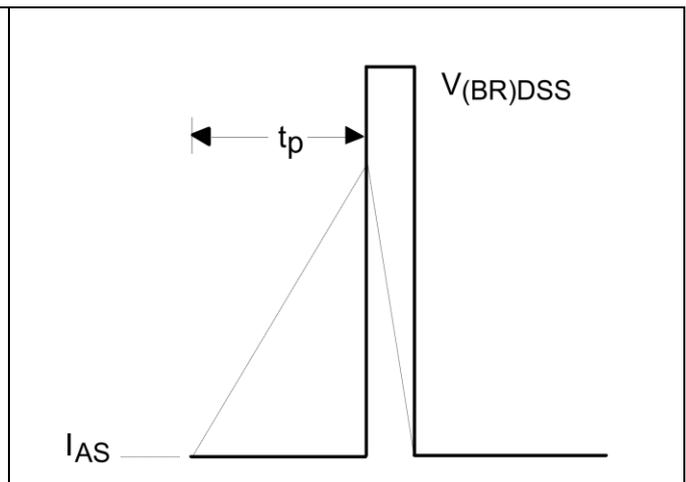


Figure 20 Unclamped Inductive Waveform

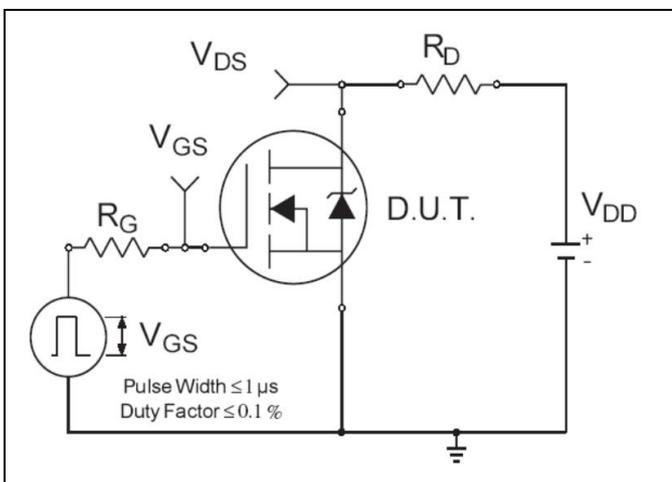


Figure 21 Switching Time Test Circuit

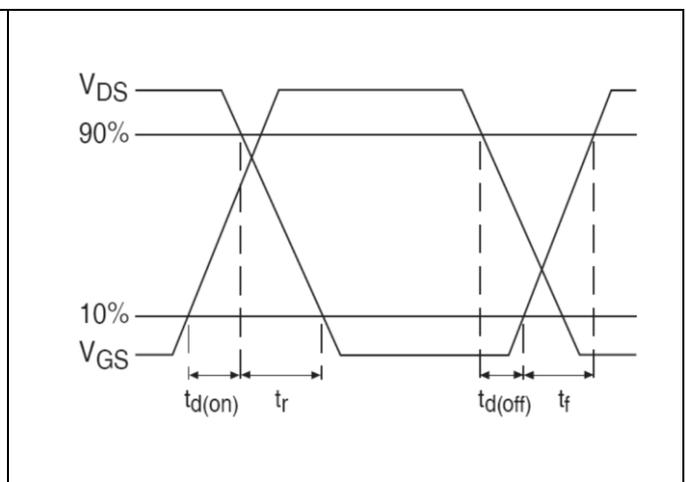


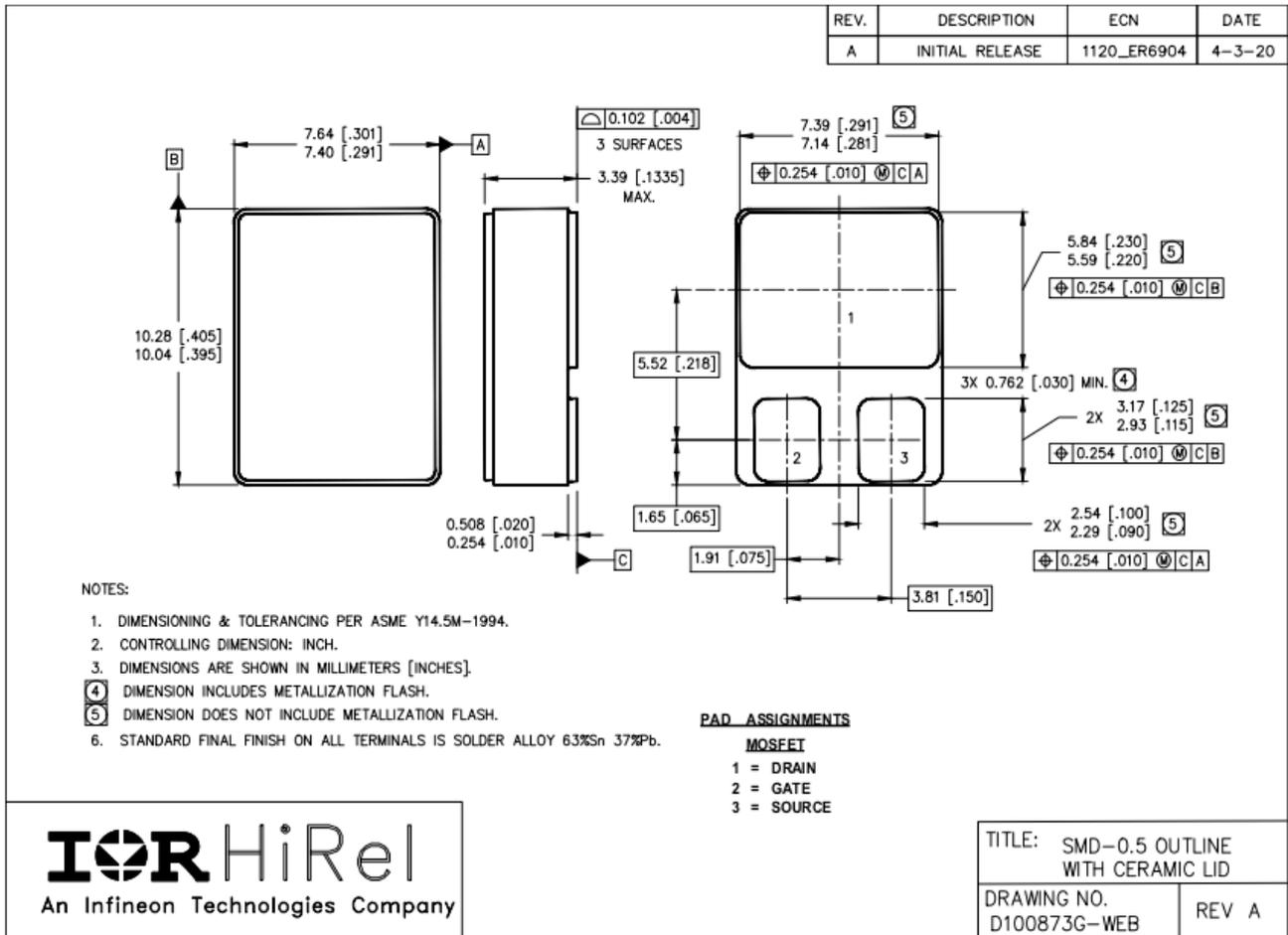
Figure 22 Switching Time Waveforms

Radiation Hardened Power MOSFET Surface Mount (SMD-0.5 with Ceramic Lid)

Package Outline

5 Package Outline

Note: For the most updated package outline, please see the website: [SMD-0.5 with Ceramic Lid](#)



IRHNJC67230 (JANSR2N7591U3C)

Radiation Hardened Power MOSFET Surface Mount (SMD-0.5 with Ceramic Lid)

Revision history

Revision history

Document version	Date of release	Description of changes
	11/14/2023	Final datasheet with PD number (PD-98005)

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